ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages

V_{DD}, OV_{DD} .... −0.3V to 2V

Analog Input Voltage (A_{IN}^+, A_{IN}^-,

PAR/$\overline{SER}$, SENSE) (Note 3) .... −0.3V to (V_{DD} + 0.2V)

Digital Input Voltage (ENC^+, ENC^-, $\overline{CS}$,

SDI, SCK) (Note 4) .... −0.3V to 3.9V

SDO (Note 4) .... −0.3V to 3.9V

Digital Output Voltage .... −0.3V to (OV_{DD} + 0.3V)

Operating Temperature Range

LTC2175C, 2174C, 2173C .... 0°C to 70°C

LTC2175I, 2174I, 2173I .... −40°C to 85°C

Storage Temperature Range .... −65°C to 150°C

PIN CONFIGURATIONS

TOP VIEW

Top pins (52–41): V_{DD}, V_{DD}, SENSE, GND, V_{REF}, PAR/$\overline{SER}$, SDO, GND, OUT1A$^+$, OUT1A$^-$, OUT1B$^+$, OUT1B$^-$

Left pins (1–14):
1 A_{IN1}^+
2 A_{IN1}^-
3 V_{CM12}
4 A_{IN2}^+
5 A_{IN2}^-
6 REFH
7 REFH
8 REFL
9 REFL
10 A_{IN3}^+
11 A_{IN3}^-
12 V_{CM34}
13 A_{IN4}^+
14 A_{IN4}^-

Right pins (40–27):
40 OUT2A$^+$
39 OUT2A$^-$
38 OUT2B$^+$
37 OUT2B$^-$
36 DCO$^+$
35 DCO$^-$
34 OV_{DD}
33 OGND
32 FR$^+$
31 FR$^-$
30 OUT3A$^+$
29 OUT3A$^-$
28 OUT3B$^+$
27 OUT3B$^-$

53 GND

Bottom pins (15–26): V_{DD}, V_{DD}, ENC^+, ENC^-, $\overline{CS}$, SCK, SDI, GND, OUT4B$^-$, OUT4B$^+$, OUT4A$^-$, OUT4A$^+$

UKG PACKAGE
52-LEAD (7mm × 8mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 28°C/W
EXPOSED PAD (PIN 53) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2175CUKG-14#PBF	LTC2175CUKG-14#TRPBF	LTC2175UKG-14	52-Lead (7mm × 8mm) Plastic QFN	0°C to 70°C
LTC2175IUKG-14#PBF	LTC2175IUKG-14#TRPBF	LTC2175UKG-14	52-Lead (7mm × 8mm) Plastic QFN	−40°C to 85°C
LTC2174CUKG-14#PBF	LTC2174CUKG-14#TRPBF	LTC2174UKG-14	52-Lead (7mm × 8mm) Plastic QFN	0°C to 70°C
LTC2174IUKG-14#PBF	LTC2174IUKG-14#TRPBF	LTC2174UKG-14	52-Lead (7mm × 8mm) Plastic QFN	−40°C to 85°C
LTC2173CUKG-14#PBF	LTC2173CUKG-14#TRPBF	LTC2173UKG-14	52-Lead (7mm × 8mm) Plastic QFN	0°C to 70°C
LTC2173IUKG-14#PBF	LTC2173IUKG-14#TRPBF	LTC2173UKG-14	52-Lead (7mm × 8mm) Plastic QFN	−40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

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CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		LTC2175-14 MIN	TYP	MAX	LTC2174-14 MIN	TYP	MAX	LTC2173-14 MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	14			14			14			Bits
Integral Linearity Error	Differential Analog Input (Note 6)	●	−4.1	±1.2	4.1	−3.25	±1	3.25	−2.75	±1	2.75	LSB
Differential Linearity Error	Differential Analog Input	●	−0.9	±0.3	0.9	−0.8	±0.3	0.8	−0.8	±0.3	0.8	LSB
Offset Error	(Note 7)	●	−12	±3	12	−12	±3	12	−12	±3	12	mV
Gain Error	Internal Reference External Reference	●	−2.6	−1.3 −1.3	0	−2.6	−1.3 −1.3	0	−2.6	−1.3 −1.3	0	%FS %FS
Offset Drift				±20			±20			±20		µV/°C
Full-Scale Drift	Internal Reference External Reference			±35 ±25			±35 ±25			±35 ±25		ppm/°C ppm/°C
Gain Matching	External Reference			±0.2			±0.2			±0.2		%FS
Offset Matching				±3			±3			±3		mV
Transition Noise	External Reference			1.2			1.2			1.2		LSB$_{RMS}$

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	1.7V < V_{DD} < 1.9V	●		1 to 2		V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^-$)/2	Differential Analog Input (Note 8)	●	V_{CM} − 100mV	V_{CM}	V_{CM} + 100mV	V
V_{SENSE}	External Voltage Reference Applied to SENSE	External Reference Mode	●	0.625	1.250	1.300	V
I_{INCM}	Analog Input Common Mode Current	Per Pin, 125Msps Per Pin, 105Msps Per Pin, 80Msps			155 130 100		µA µA µA
I_{IN1}	Analog Input Leakage Current No Encode	0 < A_{IN}^+, A_{IN}^- < V_{DD},	●	−1		1	µA
I_{IN2}	PAR/$\overline{SER}$ Input Leakage Current	0 < PAR/$\overline{SER}$ < V_{DD}	●	−3		3	µA
I_{IN3}	SENSE Input Leakage Current	0.625 < SENSE < 1.3V	●	−6		6	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Jitter				0.15		ps$_{RMS}$
CMRR	Analog Input Common Mode Rejection Ratio				80		dB
BW-3B	Full-Power Bandwidth	Figure 6 Test Circuit			800		MHz

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DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $A_{IN} = -1dBFS$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC2175-14 MIN	LTC2175-14 TYP	LTC2175-14 MAX	LTC2174-14 MIN	LTC2174-14 TYP	LTC2174-14 MAX	LTC2173-14 MIN	LTC2173-14 TYP	LTC2173-14 MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input 70MHz Input 140MHz Input	●	71.1	73.1 73 72.6		70.7	73 72.9 72.6		70.9	73 72.9 72.5		dBFS dBFS dBFS
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	5MHz Input 70MHz Input 140MHz Input	●	75	88 85 82		75	88 85 82		77	88 85 82		dBFS dBFS dBFS
	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input 70MHz Input 140MHz Input	●	84	90 90 90		84	90 90 90		85	90 90 90		dBFS dBFS dBFS
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input 70MHz Input 140MHz Input	●	69.6	73 72.6 72		70.2	73 72.6 72		70.4	72.9 72.6 72		dBFS dBFS dBFS
	Crosstalk, Near Channel	10MHz Input (Note 12)			-90			-90			-90		dBc
	Crosstalk, Far Channel	10MHz Input (Note 12)			-105			-105			-105		dBc

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $A_{IN} = -1dBFS$. (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	$I_{OUT} = 0$	$0.5 \cdot V_{DD} - 25mV$	$0.5 \cdot V_{DD}$	$0.5 \cdot V_{DD} + 25mV$	V
V_{CM} Output Temperature Drift			±25		ppm/°C
V_{CM} Output Resistance	$-600\mu A < I_{OUT} < 1mA$		4		Ω
V_{REF} Output Voltage	$I_{OUT} = 0$	1.225	1.250	1.275	V
V_{REF} Output Temperature Drift			±25		ppm/°C
V_{REF} Output Resistance	$-400\mu A < I_{OUT} < 1mA$		7		Ω
V_{REF} Line Regulation	$1.7V < V_{DD} < 1.9V$		0.6		mV/V

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DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC⁺, ENC⁻)							
Differential Encode Mode (ENC⁻ Not Tied to GND)							
V_{ID}	Differential Input Voltage	(Note 8)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 8)	●	1.1	1.2	1.6	V V
V_{IN}	Input Voltage Range	ENC⁺, ENC⁻ to GND	●	0.2		3.6	V
R_{IN}	Input Resistance	(See Figure 10)			10		kΩ
C_{IN}	Input Capacitance				3.5		pF
Single-Ended Encode Mode (ENC⁻ Tied to GND)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
V_{IN}	Input Voltage Range	ENC⁺ to GND	●	0		3.6	V
R_{IN}	Input Resistance	(See Figure 11)			30		kΩ
C_{IN}	Input Capacitance				3.5		pF
DIGITAL INPUTS (CS̄, SDI, SCK in Serial or Parallel Programming Mode. SDO in Parallel Programming Mode)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.3			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
I_{IN}	Input Current	V_{IN} = 0V to 3.6V	●	−10		10	μA
C_{IN}	Input Capacitance				3		pF
SDO OUTPUT (Serial Programming Mode. Open-Drain Output. Requires 2kΩ Pull-Up Resistor if SDO is Used)							
R_{OL}	Logic Low Output Resistance to GND	V_{DD} = 1.8V, SDO = 0V			200		Ω
I_{OH}	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	−10		10	μA
C_{OUT}	Output Capacitance				3		pF
DIGITAL DATA OUTPUTS							
V_{OD}	Differential Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	247 125	350 175	454 250	mV mV
V_{OS}	Common Mode Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	1.125 1.125	1.250 1.250	1.375 1.375	V V
R_{TERM}	On-Chip Termination Resistance	Termination Enabled, OV_{DD} = 1.8V			100		Ω

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POWER REQUIREMENTS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		LTC2175-14 MIN	TYP	MAX	LTC2174-14 MIN	TYP	MAX	LTC2173-14 MIN	TYP	MAX	UNITS
V_{DD}	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV_{DD}	Output Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{VDD}	Analog Supply Current	Sine Wave Input	●		283	305		224	243		184	200	mA
I_{OVDD}	Digital Supply Current	2-Lane Mode, 1.75mA Mode 2-Lane Mode, 3.5mA Mode	● ●		27 49	31 54		26 48	31 53		25 47	29 52	mA mA
P_{DISS}	Power Dissipation	2-Lane Mode, 1.75mA Mode 2-Lane Mode, 3.5mA Mode	● ●		558 598	605 646		450 490	493 533		376 416	412 454	mW mW
P_{SLEEP}	Sleep Mode Power				1			1			1		mW
P_{NAP}	Nap Mode Power				85			85			85		mW
$P_{DIFFCLK}$	Power Increase With Differential Encode Mode Enabled (No Increase for Sleep Mode)				20			20			20		mW

TIMING CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC2175-14 MIN	TYP	MAX	LTC2174-14 MIN	TYP	MAX	LTC2173-14 MIN	TYP	MAX	UNITS
f_S	Sampling Frequency	(Notes 10,11)	●	5		125	5		105	5		80	MHz
t_{ENCL}	ENC Low Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2	4 4	100 100	4.52 2	4.76 4.76	100 100	5.93 2	6.25 6.25	100 100	ns ns
t_{ENCH}	ENC High Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2	4 4	100 100	4.52 2	4.76 4.76	100 100	5.93 2	6.25 6.25	100 100	ns ns
t_{AP}	Sample-and-Hold Acquisition Delay Time				0			0			0		ns

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Data Outputs (R_{TERM} = 100Ω Differential, C_L = 2pF to GND on Each Output)							
t_{SER}	Serial Data Bit Period	2-Lanes, 16-Bit Serialization 2-Lanes, 14-Bit Serialization 2-Lanes, 12-Bit Serialization 1-Lane, 16-Bit Serialization 1-Lane, 14-Bit Serialization 1-Lane, 12-Bit Serialization			$1/(8 \cdot f_S)$ $1/(7 \cdot f_S)$ $1/(6 \cdot f_S)$ $1/(16 \cdot f_S)$ $1/(14 \cdot f_S)$ $1/(12 \cdot f_S)$		s s s s s s
t_{FRAME}	FR to DCO Delay	(Note 8)	●	$0.35 \cdot t_{SER}$	$0.5 \cdot t_{SER}$	$0.65 \cdot t_{SER}$	s
t_{DATA}	DATA to DCO Delay	(Note 8)	●	$0.35 \cdot t_{SER}$	$0.5 \cdot t_{SER}$	$0.65 \cdot t_{SER}$	s
t_{PD}	Propagation Delay	(Note 8)	●	$0.7n + 2 \cdot t_{SER}$	$1.1n + 2 \cdot t_{SER}$	$1.5n + 2 \cdot t_{SER}$	s
t_R	Output Rise Time	Data, DCO, FR, 20% to 80%			0.17		ns
t_F	Output Fall Time	Data, DCO, FR, 20% to 80%			0.17		ns
	DCO Cycle-Cycle Jitter	t_{SER} = 1ns			60		ps_{P-P}
	Pipeline Latency				6		Cycles

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TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SPI Port Timing (Note 8)							
t_{SCK}	SCK Period	Write Mode Readback Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	● ●	40 250			ns ns
t_S	$\overline{CS}$ to SCK Setup Time		●	5			ns
t_H	SCK to $\overline{CS}$ Setup Time		●	5			ns
t_{DS}	SDI Setup Time		●	5			ns
t_{DH}	SDI Hold Time		●	5			ns
t_{DO}	SCK Falling to SDO Valid	Readback Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	●			125	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND with GND and OGND shorted (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above V_{DD} they will not be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup.

Note 5: V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 125MHz (LTC2175), 105MHz (LTC2174), or 80MHz (LTC2173), 2-lane output mode, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, unless otherwise noted.

Note 6: Integral nonlinearity is defined as the deviation of a code from a best fit straight line to the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Offset error is the offset voltage measured from –0.5 LSB when the output code flickers between 00 0000 0000 0000 and 11 1111 1111 1111 in 2's complement output mode.

Note 8: Guaranteed by design, not subject to test.

Note 9: V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 125MHz (LTC2175), 105MHz (LTC2174), or 80MHz (LTC2173), 2-lane output mode, ENC^+ = single-ended 1.8V square wave, ENC^- = 0V, input range = $2V_{P-P}$ with differential drive, unless otherwise noted. The supply current and power dissipation specifications are totals for the entire chip, not per channel.

Note 10: Recommended operating conditions.

Note 11: The maximum sampling frequency depends on the speed grade of the part and also which serialization mode is used. The maximum serial data rate is 1000Mbps so t_{SER} must be greater than or equal to 1ns.

Note 12: Near-channel crosstalk refers to Ch. 1 to Ch.2, and Ch.3 to Ch.4. Far-channel crosstalk refers to Ch.1 to Ch.3, Ch.1 to Ch.4, Ch.2 to Ch.3, and Ch.2 to Ch.4.
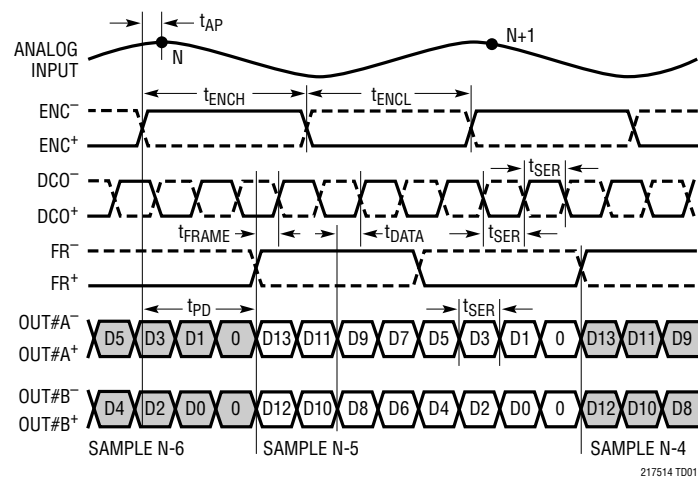
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TIMING DIAGRAMS

2-Lane Output Mode, 16-Bit Serialization*

*SEE THE DIGITAL OUTPUTS SECTION

217514 TD01

2-Lane Output Mode, 14-Bit Serialization

217514 TD02

NOTE THAT IN THIS MODE FR⁺/FR⁻ HAS TWO TIMES THE PERIOD OF ENC⁺/ENC⁻

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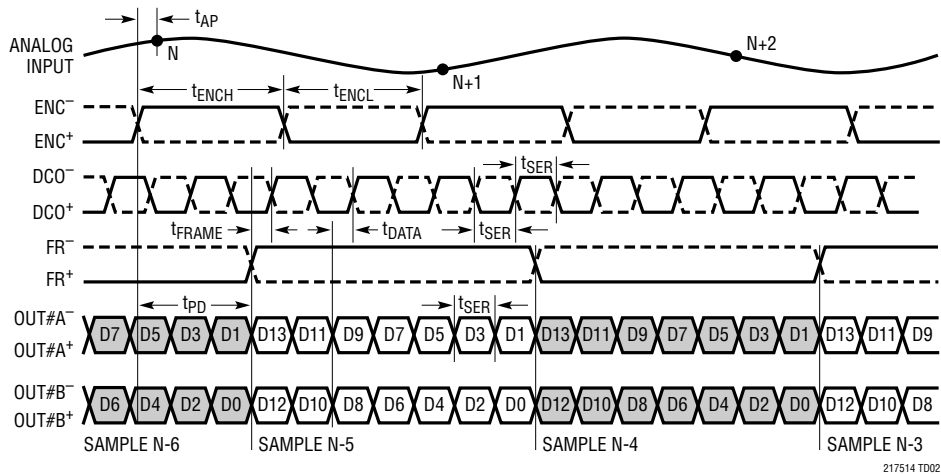
TIMING DIAGRAMS

2-Lane Output Mode, 12-Bit Serialization
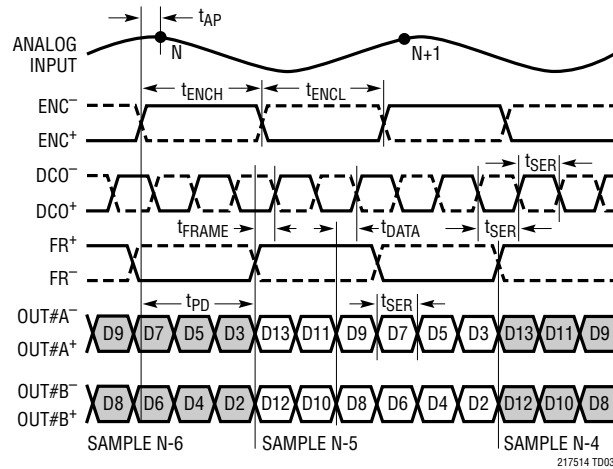
1-Lane Output Mode, 16-Bit Serialization
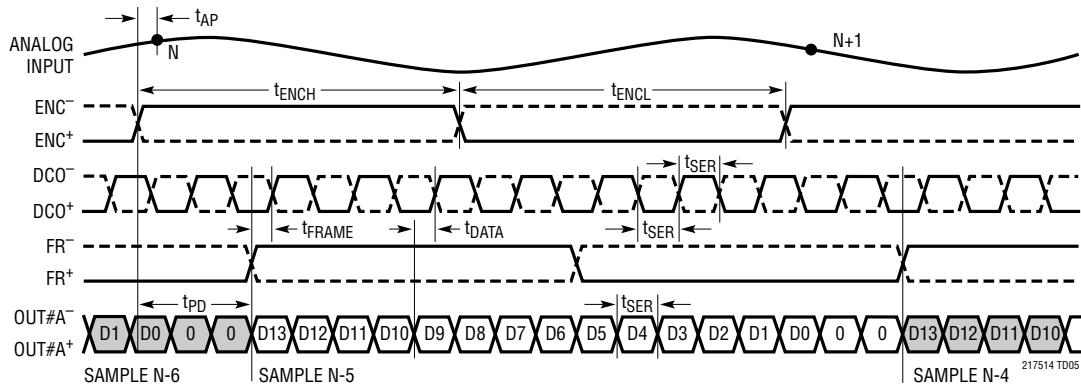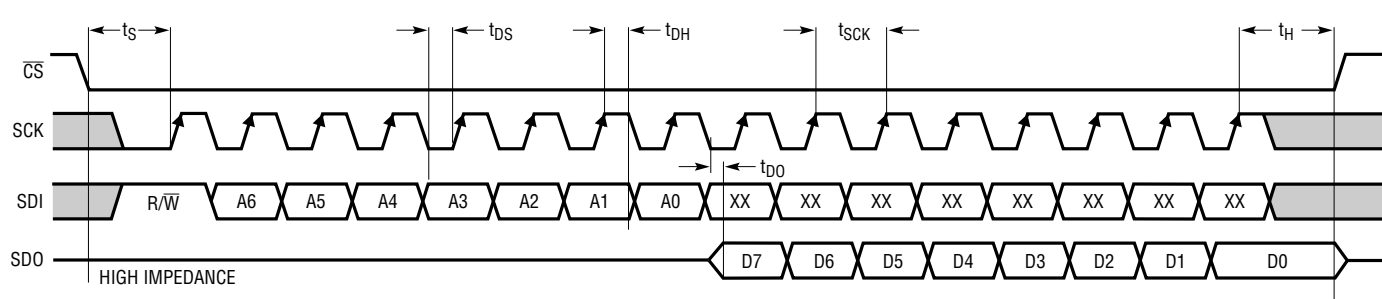

OUT#B⁺, OUT#B⁻ ARE DISABLED

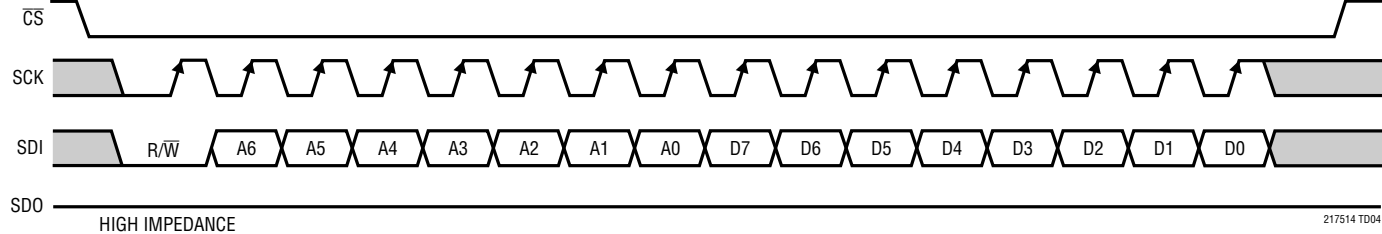# TIMING DIAGRAMS

One-Lane Output Mode, 14-Bit Serialization

OUT#B$^+$, OUT#B$^-$ ARE DISABLED

One-Lane Output Mode, 12-Bit Serialization

OUT#B$^+$, OUT#B$^-$ ARE DISABLED
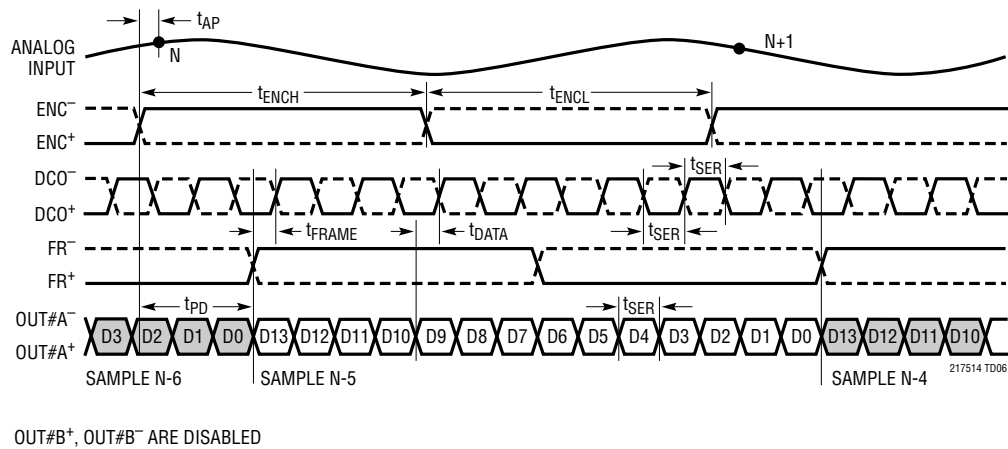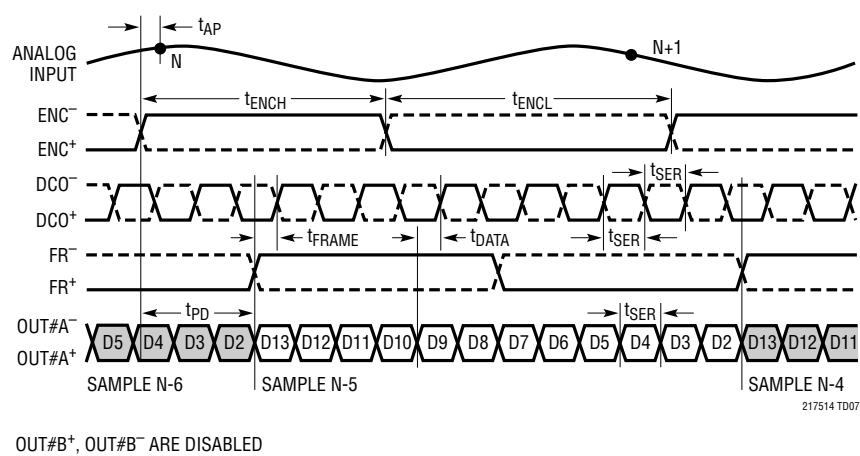
SPI Port Timing (Readback Mode)

SPI Port Timing (Write Mode)

217514 TD04

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TYPICAL PERFORMANCE CHARACTERISTICS

LTC2175-14: Integral Nonlinearity (INL)
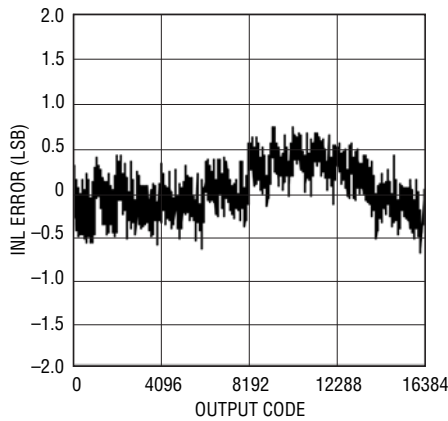
217514 G01

LTC2175-14: Differential Nonlinearity (DNL)
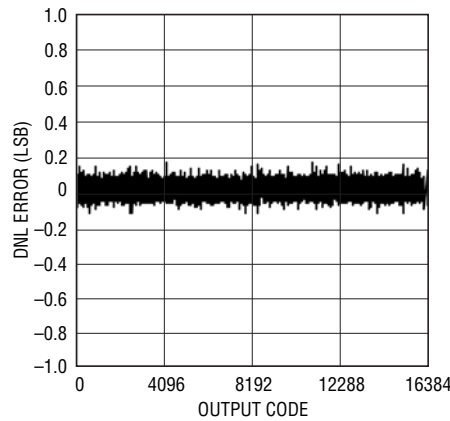
217514 G02

LTC2175-14: 8k Point FFT, f_IN = 5MHz −1dBFS, 125Msps
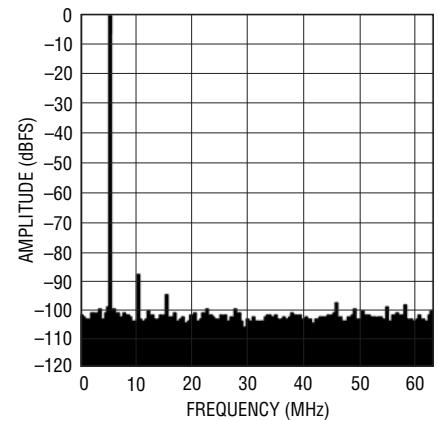
217514 G03

LTC2175-14: 8k Point FFT, f_IN = 30MHz −1dBFS, 125Msps
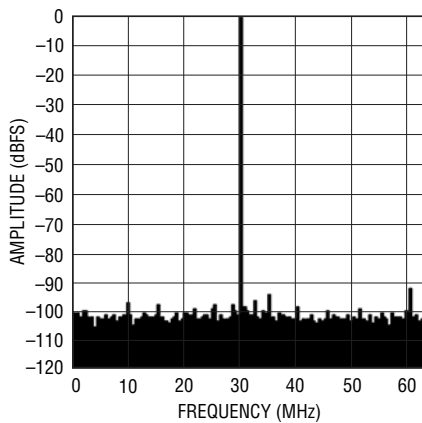
217514 G04

LTC2175-14: 8k Point FFT, f_IN = 70MHz −1dBFS, 125Msps
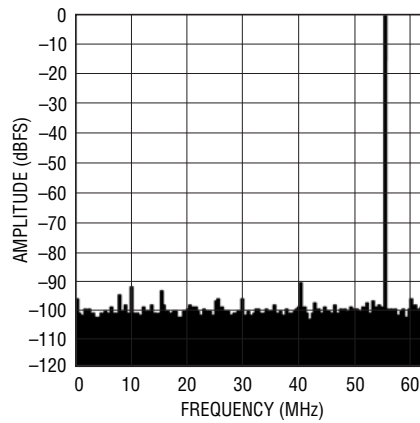
217514 G05

LTC2175-14: 8k Point FFT, f_IN = 140MHz −1dBFS, 125Msps
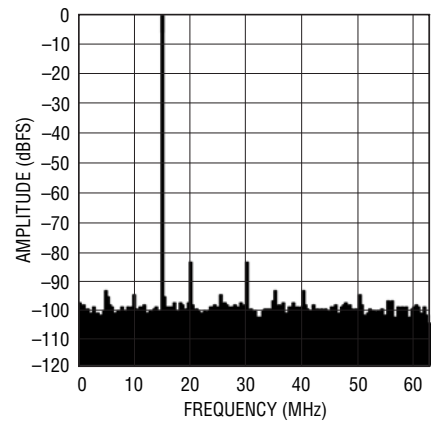
217514 G06

LTC2175-14: 8k Point 2-Tone FFT, f_IN = 70MHz, 75MHz, −1dBFS, 125Msps
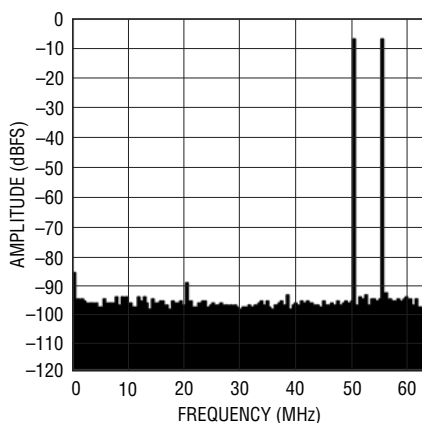
217514 G07

LTC2175-14: Shorted Input Histogram
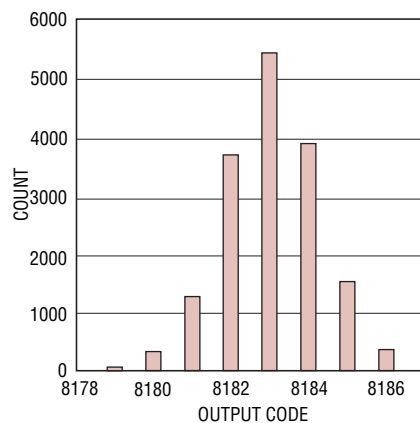
217514 G08

LTC2175-14: SNR vs Input Frequency, −1dB, 2V Range, 125Msps
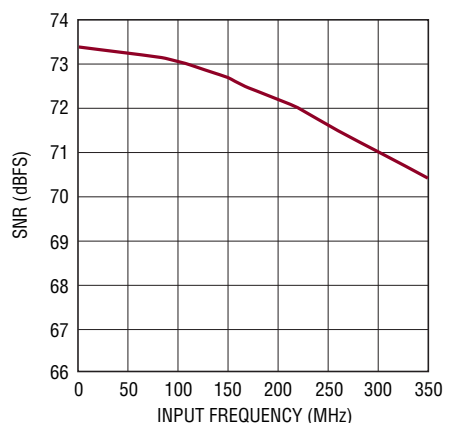
217514 G09

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TYPICAL PERFORMANCE CHARACTERISTICS

LTC2175-14: SFDR vs Input Frequency, −1dB, 2V Range, 125Msps
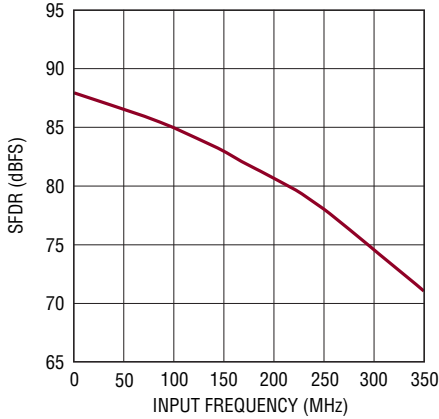
217514 G10

LTC2175-14: SFDR vs Input Level, f_IN = 70MHz, 2V Range, 125Msps
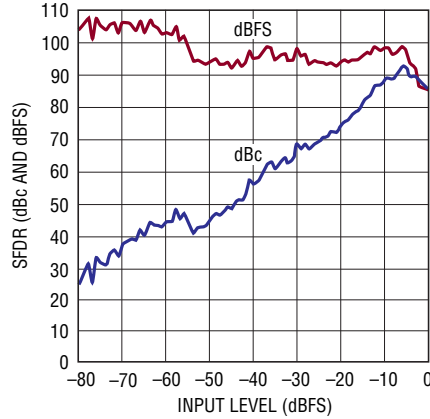
217514 G11

LTC2175-14: SNR vs Input Level, f_IN = 70MHz, 2V Range, 125Msps
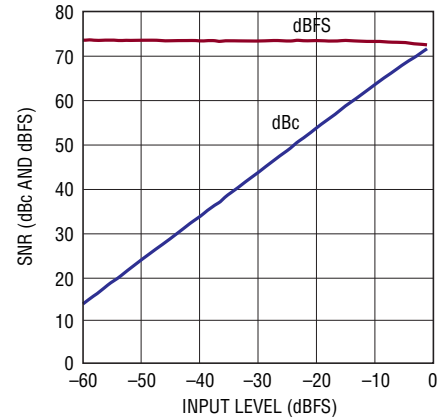
217514 G50

LTC2175-14: I_VDD vs Sample Rate, 5MHz Sine Wave Input, −1dB
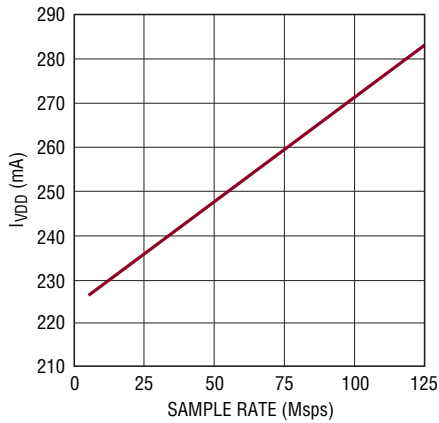
217514 G53

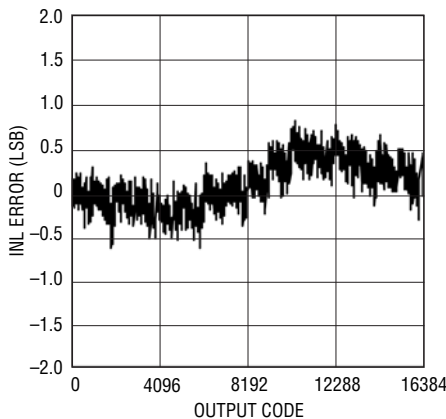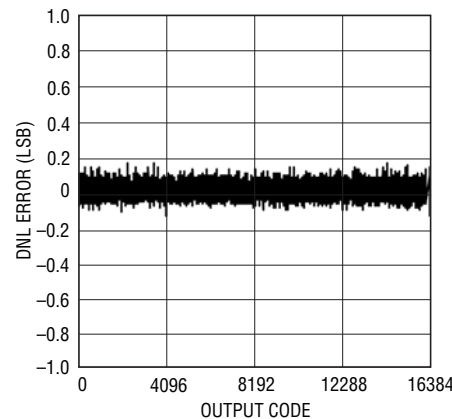**IO_VDD vs Sample Rate, 5MHz Sine Wave Input, −1dB**
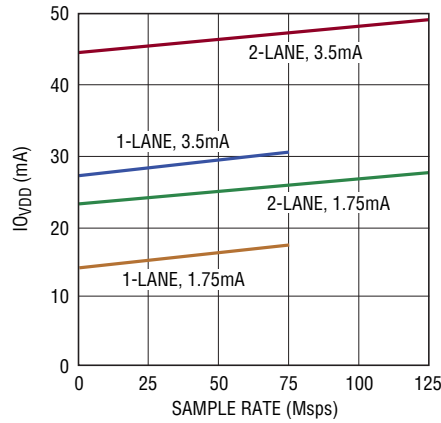
217514 G51

LTC2175-14: SNR vs SENSE, f_IN = 5MHz, −1dB
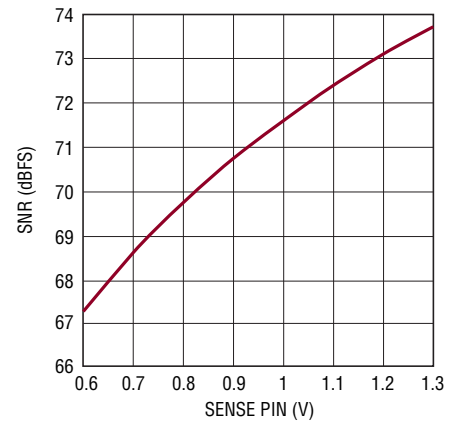
217514 G12

LTC2174-14: Integral Nonlinearity (INL)

217514 G14

LTC2174-14: Differential Nonlinearity (DNL)

217514 G15
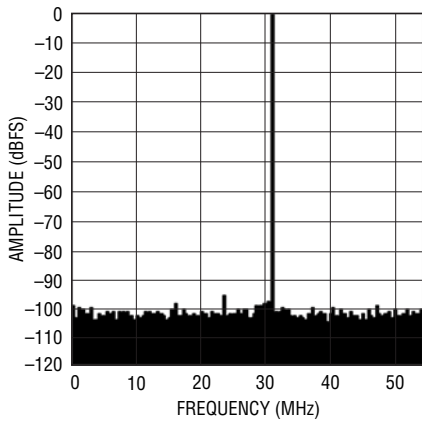
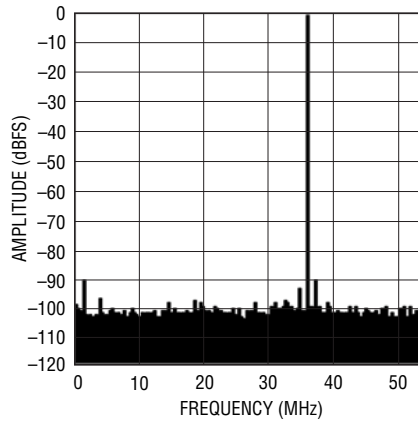**LTC2174-14: 8k Point FFT, f_IN = 5MHz −1dBFS, 105Msps**
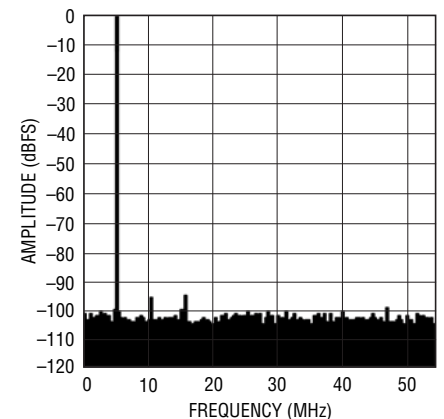
217514 G16

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TYPICAL PERFORMANCE CHARACTERISTICS

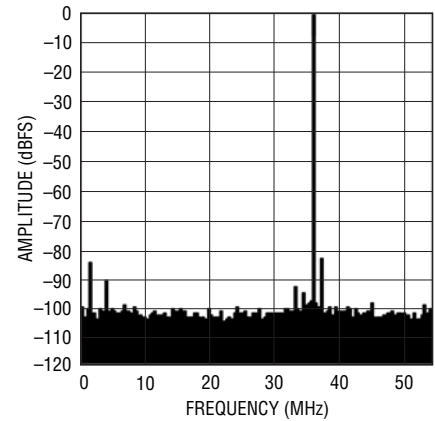**LTC2174-14: 8k Point FFT, f$_{IN}$ = 30MHz −1dBFS, 105Msps**

217514 G17

LTC2174-14: 8k Point FFT, f$_{IN}$ = 70MHz −1dBFS, 105Msps

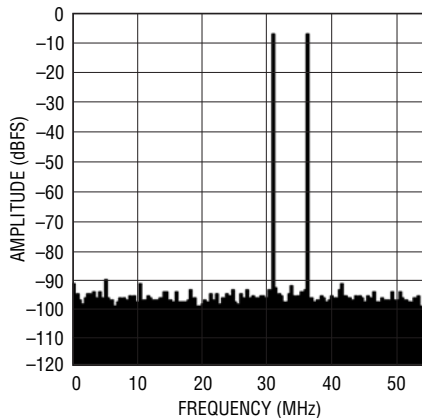
217514 G18

LTC2174-14: 8k Point FFT, f$_{IN}$ = 140MHz −1dBFS, 105Msps

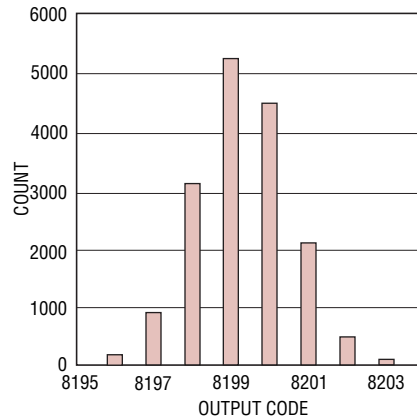
217514 G19

LTC2174-14: 8k Point 2-Tone FFT, f$_{IN}$ = 70MHz, 75MHz, −1dBFS, 105Msps
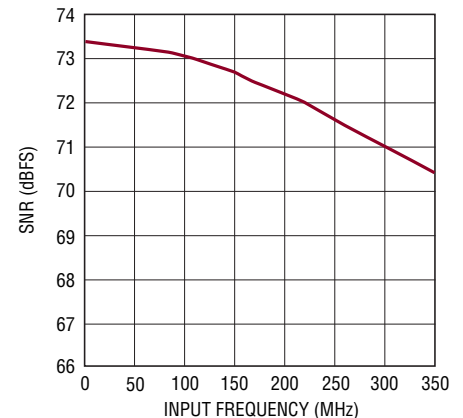

217514 G20

LTC2174-14: Shorted Input Histogram

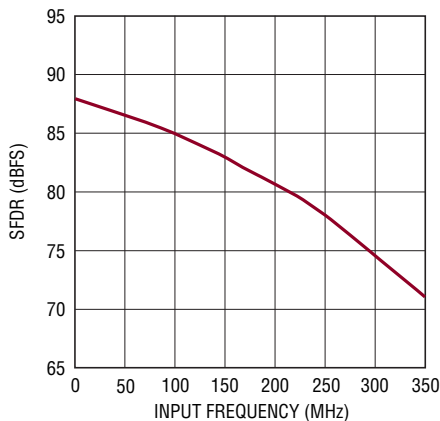217514 G21

LTC2174-14: SNR vs Input Frequency, −1dB, 2V Range, 105Msps
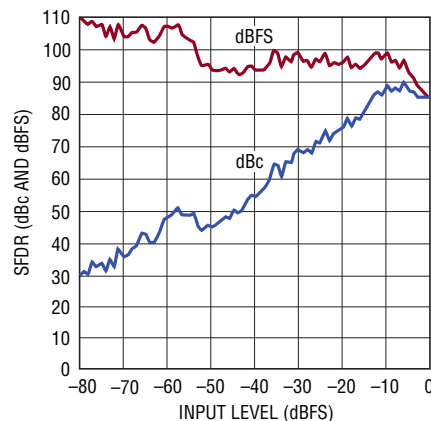

217514 G22

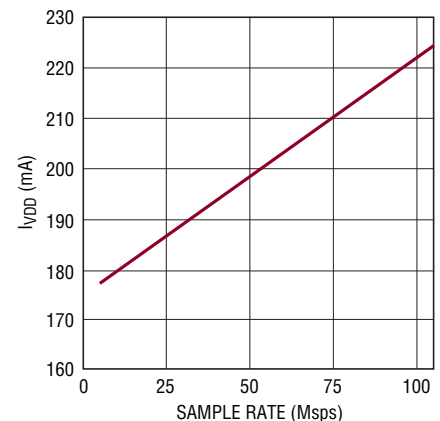**LTC2174-14: SFDR vs Input Frequency, −1dB, 2V Range, 105Msps**

217514 G23

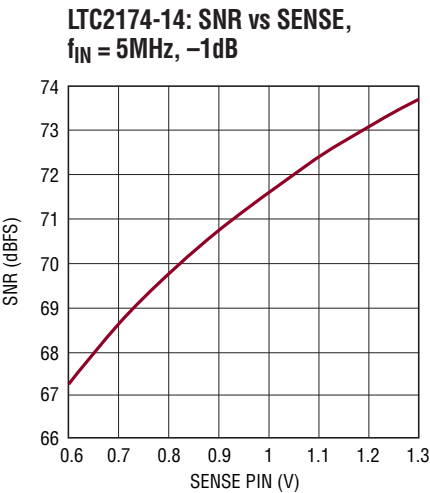**LTC2174-14: SFDR vs Input Level, f$_{IN}$ = 70MHz, 2V Range, 105Msps**

217514 G24

LTC2174-14: I$_{VDD}$ vs Sample Rate, 5MHz Sine Wave Input, −1dB

217514 G54
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TYPICAL PERFORMANCE CHARACTERISTICS

LTC2174-14: SNR vs SENSE,
f_{IN} = 5MHz, −1dB

217514 G25

LTC2173-14: Integral Nonlinearity
(INL)

217514 G26

LTC2173-14: Differential
Nonlinearity (DNL)

217514 G27

LTC2173-14: 8k Point FFT, f_{IN} = 5MHz
−1dBFS, 80Msps

217514 G28

LTC2173-14: 8k Point FFT, f_{IN} = 30MHz
−1dBFS, 80Msps

217514 G29

LTC2173-14: 8k Point FFT, f_{IN} = 70MHz
−1dBFS, 80Msps

217514 G30

LTC2173-14: 8k Point FFT, f_{IN} = 140MHz
−1dBFS, 80Msps

217514 G31

LTC2173-14: 8k Point 2-Tone FFT,
f_{IN} = 70MHz, 75MHz, −1dBFS,
80Msps

217514 G32

LTC2173-14: Shorted Input
Histogram

217514 G33
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TYPICAL PERFORMANCE CHARACTERISTICS

LTC2173-14: SNR vs Input Frequency, −1dB, 2V Range, 80Msps
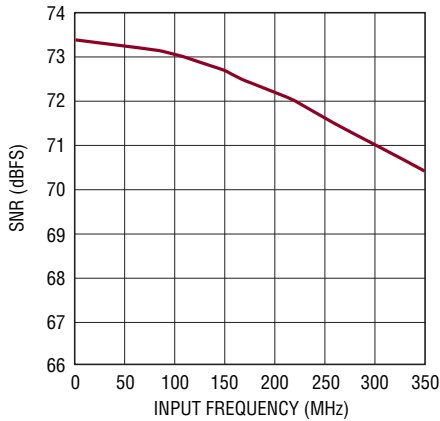
217514 G34

LTC2173-14: SFDR vs Input Frequency, −1dB, 2V Range, 80Msps
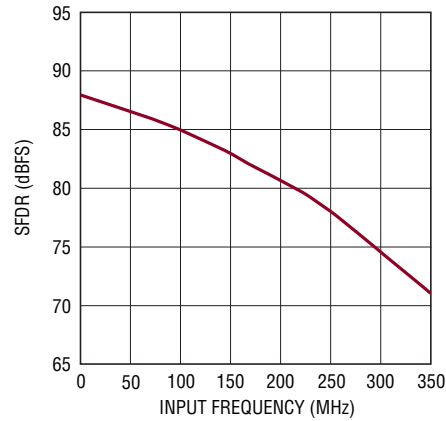
217514 G35

LTC2173-14: SFDR vs Input Level, f_{IN} = 70MHz, 2V Range, 80Msps

217514 G36

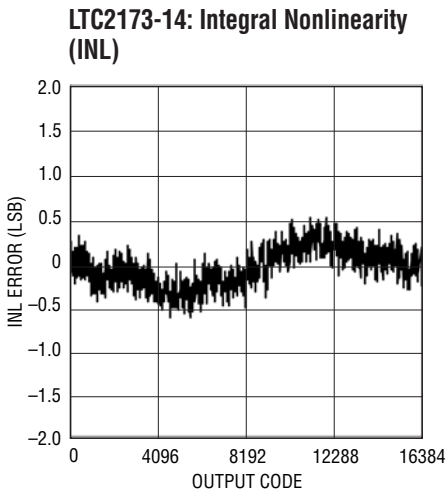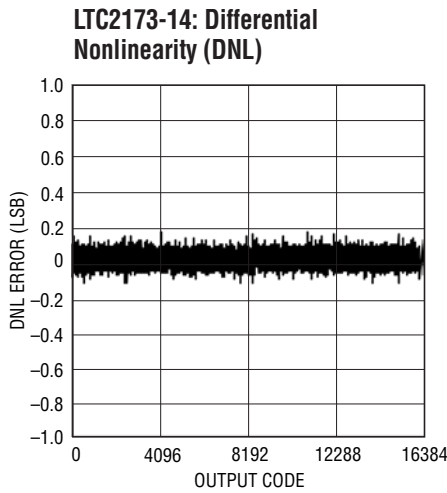**LTC2173-14: I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, −1dB**

217514 G55

LTC2173-14: SNR vs SENSE, f_{IN} = 5MHz, −1dB

217514 G37

DCO Cycle-Cycle Jitter vs Serial Data Rate

217514 G52

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PIN FUNCTIONS

A_{IN1}^+ **(Pin 1):** Channel 1 Positive Differential Analog Input.

A_{IN1}^- **(Pin 2):** Channel 1 Negative Differential Analog Input.

V_{CM12} **(Pin 3):** Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs of channels 1 and 2. Bypass to ground with a 0.1µF ceramic capacitor.

A_{IN2}^+ **(Pin 4):** Channel 2 Positive Differential Analog Input.

A_{IN2}^- **(Pin 5):** Channel 2 Negative Differential Analog Input.

REFH (Pins 6,7): ADC High Reference. Bypass to pins 8, 9 with a 2.2µF ceramic capacitor and to ground with a 0.1µF ceramic capacitor.

REFL (Pins 8,9): ADC Low Reference. Bypass to pins 6, 7 with a 2.2µF ceramic capacitor and to ground with a 0.1µF ceramic capacitor.

A_{IN3}^+ **(Pin 10):** Channel 3 Positive Differential Analog Input.

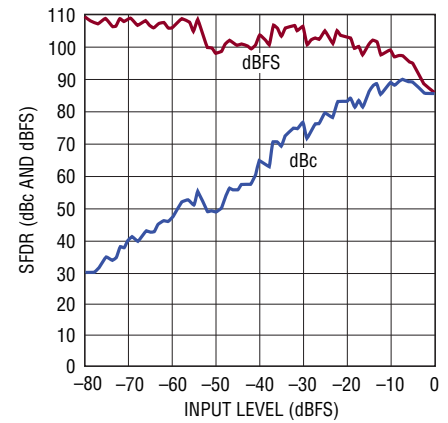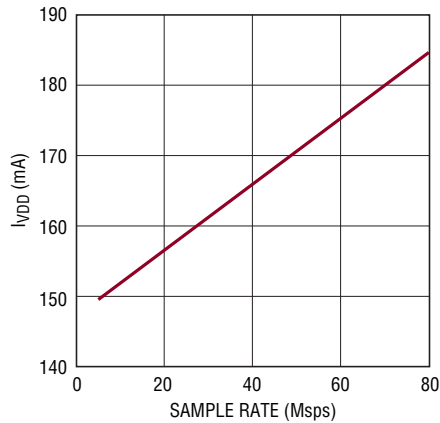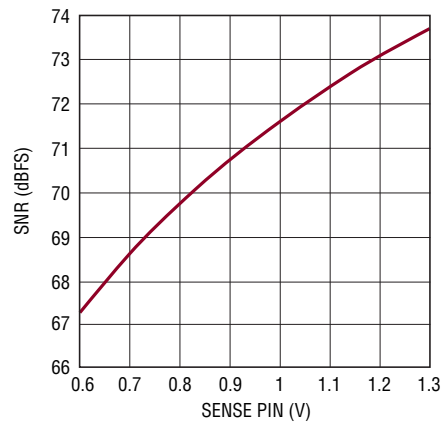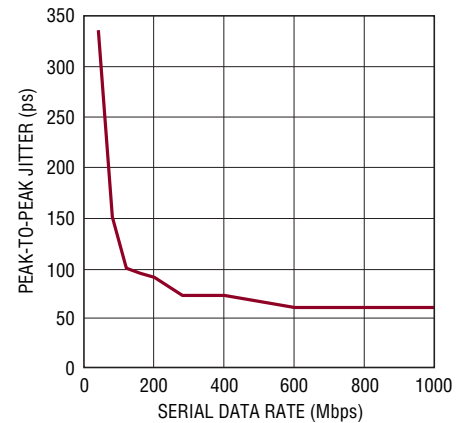A_{IN3}^- **(Pin 11):** Channel 3 Negative Differential Analog Input.

V_{CM34} **(Pin 12):** Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs of channels 3 and 4. Bypass to ground with a 0.1µF ceramic capacitor.

A_{IN4}^+ **(Pin 13):** Channel 4 Positive Differential Analog Input.

A_{IN4}^- **(Pin 14):** Channel 4 Negative Differential Analog Input.

V_{DD} **(Pins 15, 16, 51, 52):** 1.8V Analog Power Supply. Bypass to ground with 0.1µF ceramic capacitors. Adjacent pins can share a bypass capacitor.

ENC⁺ (Pin 17): Encode Input. Conversion starts on the rising edge.

ENC⁻ (Pin 18): Encode Complement Input. Conversion starts on the falling edge.

$\overline{CS}$ **(Pin 19):** In serial programming mode, (PAR/$\overline{SER}$ = 0V), $\overline{CS}$ is the serial interface chip select input. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), $\overline{CS}$ selects 2-lane or 1-lane output mode. $\overline{CS}$ can be driven with 1.8V to 3.3V logic.

SCK (Pin 20): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SCK is the serial interface clock input. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SCK selects 3.5mA or 1.75mA LVDS output currents. SCK can be driven with 1.8V to 3.3V logic.

SDI (Pin 21): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDI is the serial interface data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDI can be used to power down the part. SDI can be driven with 1.8V to 3.3V logic.

GND (Pins 22, 45, 49): ADC Power Ground.

OGND (Pin 33): Output Driver Ground. Must be shorted to the ground plane by a very low inductance path. Use multiple vias close to the pin.

OV_{DD} **(Pin 34):** Output Driver Supply. Bypass to ground with a 0.1µF ceramic capacitor.

SDO (Pin 46): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDO is the optional serial interface data output. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain NMOS output that requires an external 2k pull-up resistor to 1.8V – 3.3V. If read back from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDO is an input that enables internal 100Ω termination resistors on the digital outputs. When used as an input, SDO can be driven with 1.8V to 3.3V logic through a 1k series resistor.

PAR/$\overline{SER}$ (Pin 47): Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. $\overline{CS}$, SCK, SDI, SDO become a serial interface that control the A/D operating modes. Connect to V_{DD} to enable the parallel programming mode where $\overline{CS}$, SCK, SDI, SDO become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/$\overline{SER}$ should be connected directly to ground or the V_{DD} of the part and not be driven by a logic signal.

V_{REF} **(Pin 48):** Reference Voltage Output. Bypass to ground with a 1µF ceramic capacitor, nominally 1.25V.

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PIN FUNCTIONS

SENSE (Pin 50): Reference Programming Pin. Connecting SENSE to V_{DD} selects the internal reference and a ±1V input range. Connecting SENSE to ground selects the internal reference and a ±0.5V input range. An external reference between 0.625V and 1.3V applied to SENSE selects an input range of $\pm 0.8 \cdot V_{SENSE}$.

Exposed Pad (Pin 53): Ground. The Exposed Pad must be soldered to the PCB ground.

LVDS Outputs

All pins in this section are differential LVDS outputs. The output current level is programmable. There is an optional internal 100Ω termination resistor between the pins of each LVDS output pair.

OUT4B⁻/OUT4B⁺, OUT4A⁻/OUT4A⁺ (Pins 23/24, 25/26): Serial data outputs for Channel 4. In 1-lane output mode only OUT4A⁻/OUT4A⁺ are used.

OUT3B⁻/OUT3B⁺, OUT3A⁻/OUT3A⁺ (Pins 27/28, 29/30): Serial data outputs for Channel 3. In 1-lane output mode only OUT3A⁻/OUT3A⁺ are used.

FR⁻/FR⁺ (Pins 31/32): Frame Start Outputs.

DCO⁻/DCO⁺ (Pins 35/36): Data Clock Outputs.

OUT2B⁻/OUT2B⁺, OUT2A⁻/OUT2A⁺ (Pins 37/38, 39/40): Serial data outputs for Channel 2. In 1-lane output mode only OUT2A⁻/OUT2A⁺ are used.

OUT1B⁻/OUT1B⁺, OUT1A⁻/OUT1A⁺ (Pins 41/42, 43/44): Serial data outputs for Channel 1. In 1-lane output mode only OUT1A⁻/OUT1A⁺ are used.
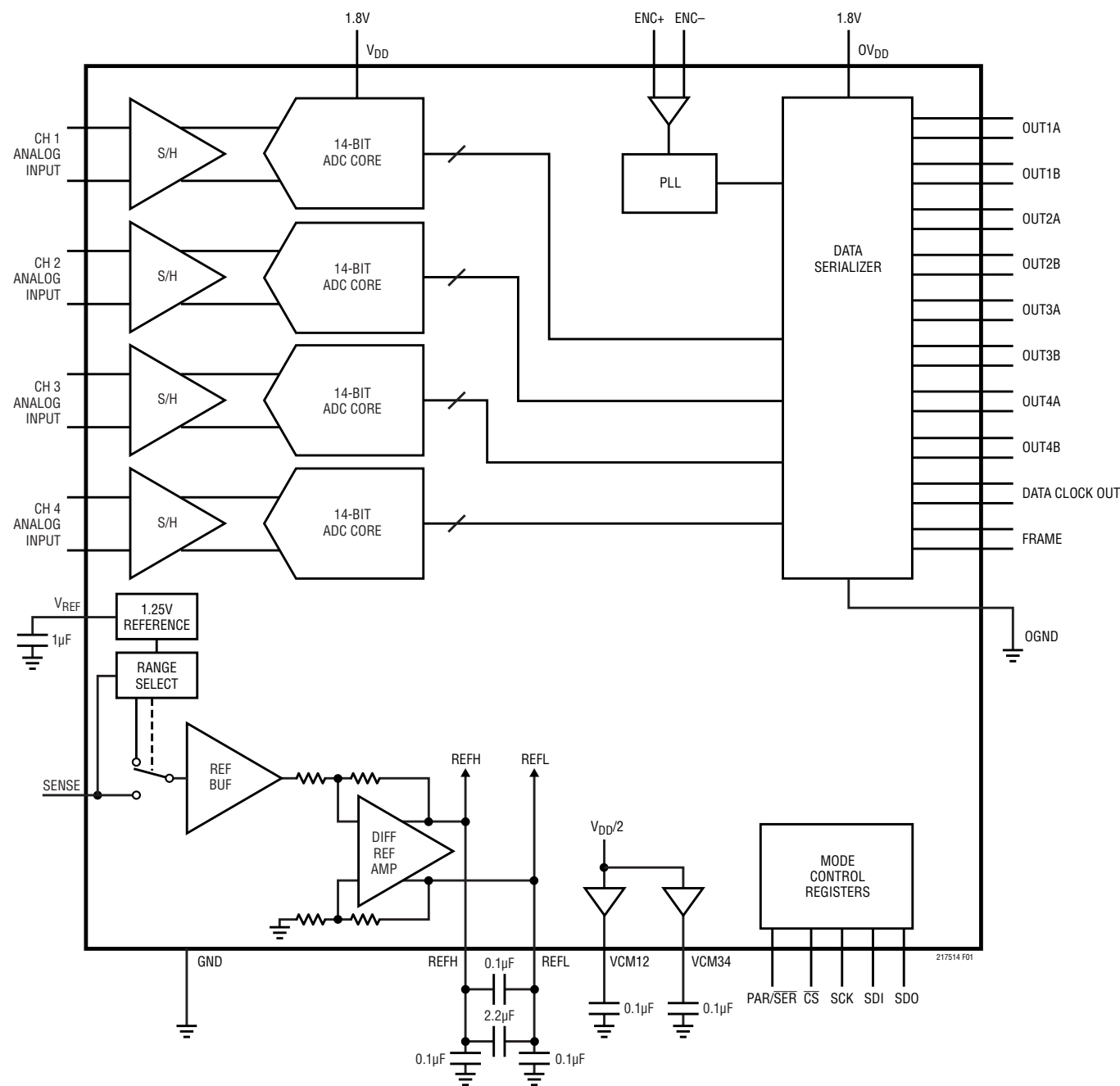
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FUNCTIONAL BLOCK DIAGRAM

Figure 1. Functional Block Diagram

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APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTC2175-14/LTC2174-14/LTC2173-14 are low power, 4-channel, 14-bit, 125Msps/105Msps/80Msps A/D converters that are powered by a single 1.8V supply. The analog inputs should be driven differentially. The encode input can be driven differentially for optimal jitter performance, or single-ended for lower power consumption. The digital outputs are serial LVDS to minimize the number of data lines. Each channel outputs two bits at a time (2-lane mode). At lower sampling rates there is a one bit per channel option (1-lane mode). Many additional features can be chosen by programming the mode control registers through a serial SPI port.

ANALOG INPUT

The analog inputs are differential CMOS sample-and-hold circuits (Figure 2). The inputs should be driven differentially around a common mode voltage set by the V_{CM12} or V_{CM34} output pins, which are nominally $V_{DD}/2$. For the 2V input range, the inputs should swing from $V_{CM} - 0.5V$ to $V_{CM} + 0.5V$. There should be 180° phase difference between the inputs.

The four channels are simultaneously sampled by a shared encode circuit (Figure 2).

INPUT DRIVE CIRCUITS

Input Filtering

If possible, there should be an RC low pass filter right at the analog inputs. This lowpass filter isolates the drive circuitry from the A/D sample-and-hold switching, and also limits wideband noise from the drive circuitry. Figure 3 shows an example of an input RC filter. The RC component values should be chosen based on the application's input frequency.

Transformer Coupled Circuits

Figure 3 shows the analog input being driven by an RF transformer with a center-tapped secondary. The center
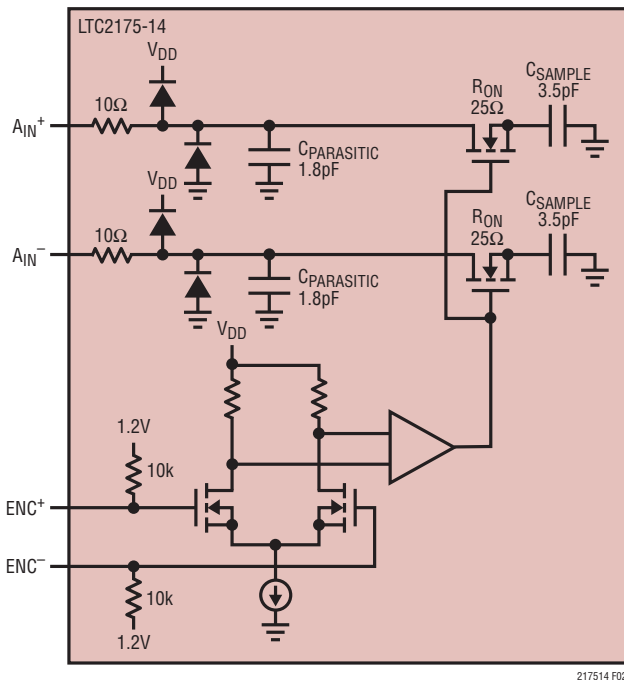

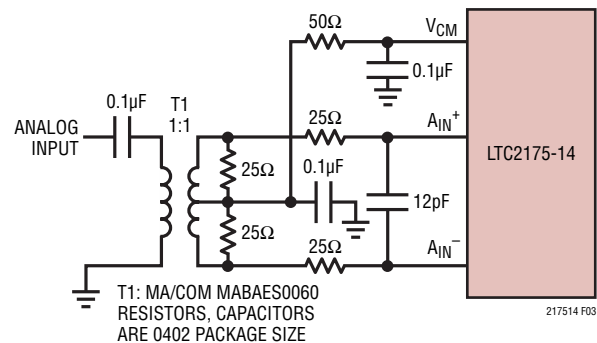**Figure 2. Equivalent Input Circuit. Only One of the Four Analog Channels is Shown.**

Figure 3. Analog Input Circuit Using a Transformer. Recommended for Input Frequencies from 5MHz to 70MHz.

APPLICATIONS INFORMATION

tap is biased with V_{CM}, setting the A/D input at its optimal DC level. At higher input frequencies a transmission line balun transformer (Figures 4 to 6) has better balance, resulting in lower A/D distortion.

Amplifier Circuits

Figure 7 shows the analog input being driven by a high speed differential amplifier. The output of the amplifier is AC-coupled to the A/D so the amplifier's output common mode voltage can be optimally set to minimize distortion.

At very high frequencies an RF gain block will often have lower distortion than a differential amplifier. If the gain block is single-ended, then a transformer circuit (Figures 4 to 6) should convert the signal to differential before driving the A/D.

Reference

The LTC2175-14/LTC2174-14/LTC2173-14 has an internal 1.25V voltage reference. For a 2V input range using the internal reference, connect SENSE to V_{DD}. For a 1V input range using the internal reference, connect SENSE to

T1: MA/COM MABA-007159-000000
T2: MA/COM MABAES0060
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE
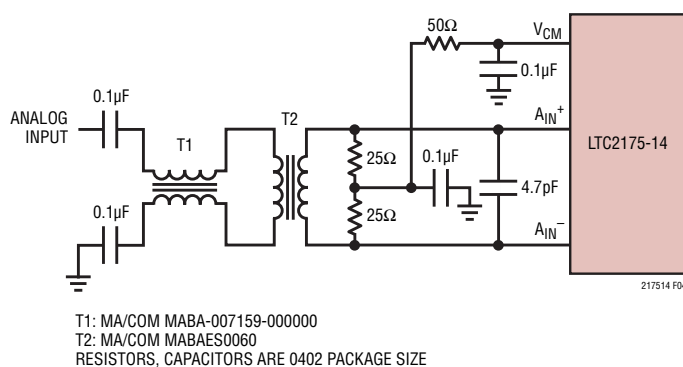
Figure 4. Recommended Front End Circuit for Input Frequencies from 70MHz to 170MHz

T1: MA/COM ETC1-1-13
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

Figure 6. Recommended Front End Circuit for Input Frequencies Above 300MHz

T1: MA/COM MABA-007159-000000
T2: COILCRAFT WBC1-1LB
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

Figure 5. Recommended Front End Circuit for Input Frequencies from 170MHz to 300MHz
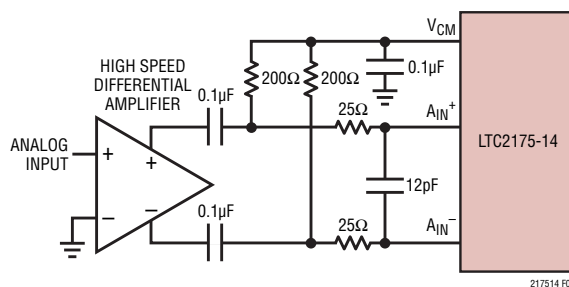
Figure 7. Front End Circuit Using a High Speed Differential Amplifier

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APPLICATIONS INFORMATION

ground. For a 2V input range with an external reference, apply a 1.25V reference voltage to SENSE (Figure 9).

The input range can be adjusted by applying a voltage to SENSE that is between 0.625V and 1.30V. The input range will then be $1.6 \cdot V_{SENSE}$.

The reference is shared by all four ADC channels, so it is not possible to independently adjust the input range of individual channels.

The V_{REF}, REFH and REFL pins should be bypassed as shown in Figure 8. The 0.1µF capacitor between REFH

and REFL should be as close to the pins as possible (not on the backside of the circuit board).

Encode Input

The signal quality of the encode inputs strongly affects the A/D noise performance. The encode inputs should be treated as analog signals—do not route them next to digital traces on the circuit board. There are two modes of operation for the encode inputs: the differential encode mode (Figure 10), and the single-ended encode mode (Figure 11).
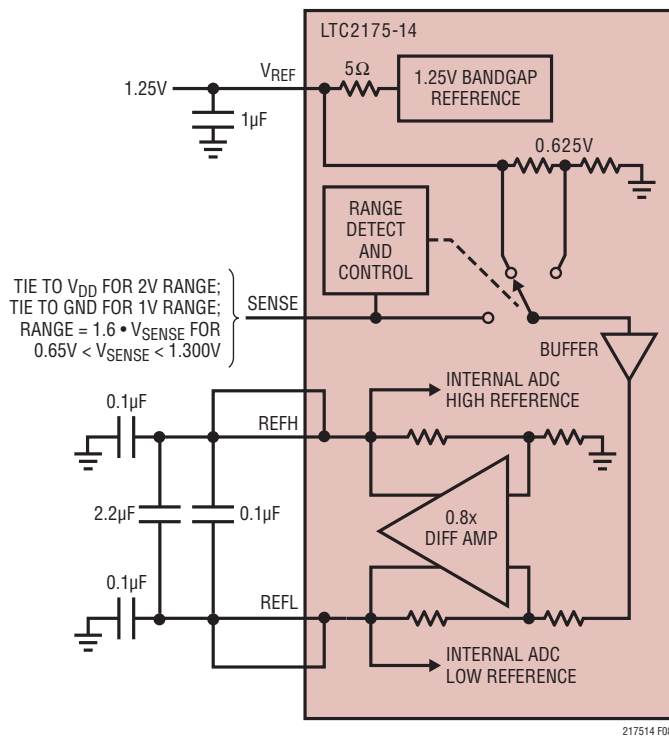
Figure 8. Reference Circuit

Figure 10. Equivalent Encode Input Circuit for Differential Encode Mode
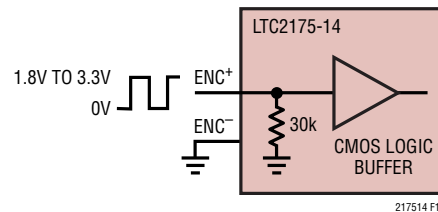
Figure 11. Equivalent Encode Input Circuit for Single-Ended Encode Mode

Figure 9. Using an External 1.25V Reference

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APPLICATIONS INFORMATION

The differential encode mode is recommended for sinu-soidal, PECL, or LVDS encode inputs (Figures 12 and 13). The encode inputs are internally biased to 1.2V through 10k equivalent resistance. The encode inputs can be taken above V_{DD} (up to 3.6V), and the common mode range is from 1.1V to 1.6V. In the differential encode mode, ENC$^-$ should stay at least 200mV above ground to avoid falsely triggering the single-ended encode mode. For good jitter performance ENC$^+$ should have fast rise and fall times.

The single-ended encode mode should be used with CMOS encode inputs. To select this mode, ENC$^-$ is connected to ground and ENC$^+$ is driven with a square wave encode input. ENC$^+$ can be taken above V_{DD} (up to 3.6V) so 1.8V to 3.3V CMOS logic levels can be used. The ENC$^+$ threshold

is 0.9V. For good jitter performance ENC$^+$ should have fast rise and fall times.

Clock PLL and Duty Cycle Stabilizer

The encode clock is multiplied by an internal phase-locked loop (PLL) to generate the serial digital output data. If the encode signal changes frequency or is turned off, the PLL requires 25µs to lock onto the input clock.

A clock duty cycle stabilizer circuit allows the duty cycle of the applied encode signal to vary from 30% to 70%. In the serial programming mode it is possible to disable the duty cycle stabilizer, but this is not recommended. In the parallel programming mode the duty cycle stabilizer is always enabled.

T1 = MA/COM ETC1-1-13
RESISTORS AND CAPACITORS
ARE 0402 PACKAGE SIZE
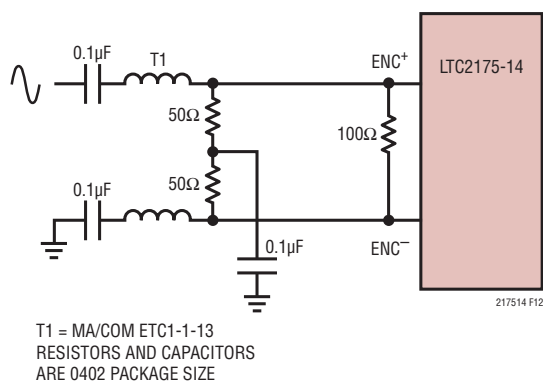
Figure 12. Sinusoidal Encode Drive

Figure 13. PECL or LVDS Encode Drive

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APPLICATIONS INFORMATION

DIGITAL OUTPUTS

The digital outputs of the LTC2175-14/LTC2174-14/ LTC2173-14 are serialized LVDS signals. Each channel outputs two bits at a time (2-lane mode). At lower sampling rates there is a one bit per channel option (1-lane mode). The data can be serialized with 16, 14, or 12-bit serialization (see timing diagrams for details). Note that with 12-bit serialization the two LSBs are not available— this mode is included for compatibility with the 12-bit versions of these parts.

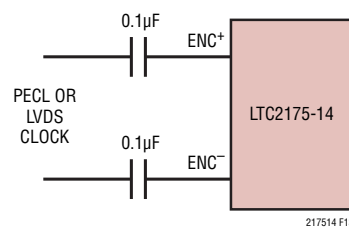The output data should be latched on the rising and falling edges of the data clock out (DCO). A data frame output (FR) can be used to determine when the data from a new conversion result begins. In the 2-lane, 14-bit serialization mode, the frequency of the FR output is halved.

The maximum serial data rate for the data outputs is 1Gbps, so the maximum sample rate of the ADC will depend on the serialization mode as well as the speed grade of the ADC (see Table 1). The minimum sample rate for all serialization modes is 5Msps.

By default the outputs are standard LVDS levels: 3.5mA output current and a 1.25V output common mode voltage. An external 100Ω differential termination resistor is required for each LVDS output pair. The termination resistors should be located as close as possible to the LVDS receiver.

The outputs are powered by OV_{DD} and OGND which are isolated from the A/D core power and ground.

Programmable LVDS Output Current

The default output driver current is 3.5mA. This current can be adjusted by control register A2 in the serial programming mode. Available current levels are 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA. In the parallel programming mode the SCK pin can select either 3.5mA or 1.75mA.

Optional LVDS Driver Internal Termination

In most cases using just an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by serially programming mode control register A2. The internal termination helps absorb any reflections caused by imperfect termination at the receiver. When the internal termination is enabled, the output driver current is doubled to maintain the same output voltage swing. In the parallel programming mode the SDO pin enables internal termination. Internal termination should only be used with 1.75mA, 2.1mA or 2.5mA LVDS output current modes.

Table 1. Maximum Sampling Frequency for All Serialization Modes. Note That These Limits Are for the LTC2175-14. The Sampling Frequency for the Slower Speed Grades Cannot Exceed 105MHz (LTC2174-14) or 80MHz (LTC2173-14).

SERIALIZATION MODE		MAXIMUM SAMPLING FREQUENCY, f_S (MHz)	DCO FREQUENCY	FR FREQUENCY	SERIAL DATA RATE
2-Lane	16-Bit Serialization	125	$4 \cdot f_S$	f_S	$8 \cdot f_S$
2-Lane	14-Bit Serialization	125	$3.5 \cdot f_S$	$0.5 \cdot f_S$	$7 \cdot f_S$
2-Lane	12-Bit Serialization	125	$3 \cdot f_S$	f_S	$6 \cdot f_S$
1-Lane	16-Bit Serialization	62.5	$8 \cdot f_S$	f_S	$16 \cdot f_S$
1-Lane	14-Bit Serialization	71.4	$7 \cdot f_S$	f_S	$14 \cdot f_S$
1-Lane	12-Bit Serialization	83.3	$6 \cdot f_S$	f_S	$12 \cdot f_S$

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DATA FORMAT

Table 2 shows the relationship between the analog input voltage and the digital data output bits. By default the output data format is offset binary. The 2's complement format can be selected by serially programming mode control register A1.

Table 2. Output Codes vs Input Voltage

$A_{IN}^+ - A_{IN}^-$ (2V RANGE)	D13-D0 (OFFSET BINARY)	D13-D0 (2's COMPLEMENT)
>1.000000V	11 1111 1111 1111	01 1111 1111 1111
+0.999878V	11 1111 1111 1111	01 1111 1111 1111
+0.999756V	11 1111 1111 1110	01 1111 1111 1110
+0.000122V	10 0000 0000 0001	00 0000 0000 0001
+0.000000V	10 0000 0000 0000	00 0000 0000 0000
−0.000122V	01 1111 1111 1111	11 1111 1111 1111
−0.000244V	01 1111 1111 1110	11 1111 1111 1110
−0.999878V	00 0000 0000 0001	10 0000 0000 0001
−1.000000V	00 0000 0000 0000	10 0000 0000 0000
<−1.000000V	00 0000 0000 0000	10 0000 0000 0000

Digital Output Randomizer

Interference from the A/D digital outputs is sometimes unavoidable. Digital interference may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can cause unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized which reduces the unwanted tone amplitude.

The digital output is *randomized* by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied —an exclusive-OR operation is applied between the LSB and all other bits. The FR and DCO outputs are not affected. The output randomizer is enabled by serially programming mode control register A1.

Digital Output Test Pattern

To allow in-circuit testing of the digital interface to the A/D, there is a test mode that forces the A/D data outputs (D13-D0) of all channels to known values. The digital output test patterns are enabled by serially programming mode control registers A3 and A4. When enabled, the test patterns override all other formatting modes: 2's complement and randomizer.

Output Disable

The digital outputs may be disabled by serially programming mode control register A2. The current drive for all digital outputs including DCO and FR are disabled to save power or enable in-circuit testing. When disabled the common mode of each output pair becomes high impedance, but the differential impedance may remain low.

Sleep and Nap Modes

The A/D may be placed in sleep or nap modes to conserve power. In sleep mode the entire chip is powered down, resulting in 1mW power consumption. Sleep mode is enabled by mode control register A1 (serial programming mode), or by SDI (parallel programming mode). The amount of time required to recover from sleep mode depends on the size of the bypass capacitors on V_{REF}, REFH, and REFL. For the suggested values in Figure 8, the A/D will stabilize after 2ms.

In nap mode any combination of A/D channels can be powered down while the internal reference circuits and the PLL stay active, allowing faster wakeup than from sleep

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mode. Recovering from nap mode requires at least 100 clock cycles. If the application demands very accurate DC settling then an additional 50µs should be allowed so the on-chip references can settle from the slight temperature shift caused by the change in supply current as the A/D leaves nap mode. Nap mode is enabled by mode control register A1 in the serial programming mode.

DEVICE PROGRAMMING MODES

The operating modes of the LTC2175-14/LTC2174-14/LTC2173-14 can be programmed by either a parallel interface or a simple serial interface. The serial interface has more flexibility and can program all available modes. The parallel interface is more limited and can only program some of the more commonly used modes.

Parallel Programming Mode

To use the parallel programming mode, PAR/$\overline{SER}$ should be tied to V_{DD}. The $\overline{CS}$, SCK, SDI and SDO pins are binary logic inputs that set certain operating modes. These pins can be tied to V_{DD} or ground, or driven by 1.8V, 2.5V, or 3.3V CMOS logic. When used as an input, SDO should be driven through a 1k series resistor. Table 3 shows the modes set by $\overline{CS}$, SCK, SDI and SDO.

Serial Programming Mode

To use the serial programming mode, PAR/$\overline{SER}$ should be tied to ground. The $\overline{CS}$, SCK, SDI and SDO pins become a serial interface that program the A/D mode control registers. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

Serial data transfer starts when $\overline{CS}$ is taken low. The data on the SDI pin is latched at the first 16 rising edges of SCK. Any SCK rising edges after the first 16 are ignored. The data transfer ends when $\overline{CS}$ is taken high again.

The first bit of the 16-bit input word is the R/$\overline{W}$ bit. The next seven bits are the address of the register (A6:A0). The final eight bits are the register data (D7:D0).

If the R/$\overline{W}$ bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0). If the R/$\overline{W}$ bit is high, data in the register set by the address bits (A6:A0) will be read back on the SDO pin (see the Timing Diagrams sections). During a read back command the register is not updated and data on SDI is ignored.

The SDO pin is an open-drain output that pulls to ground with a 200Ω impedance. If register data is read back through SDO, an external 2k pull-up resistor is required. If serial data is only written and read back is not needed,

Table 3. Parallel Programming Mode Control Bits (PAR/$\overline{SER}$ = V_{DD})

Pin	DESCRIPTION
$\overline{CS}$	**2-Lane / 1-Lane Selection Bit**
	0 = 2-Lane, 16-Bit Serialization Output Mode
	1 = 1-Lane, 14-Bit Serialization Output Mode
SCK	**LVDS Current Selection Bit**
	0 = 3.5mA LVDS Current Mode
	1 = 1.75mA LVDS Current Mode
SDI	**Power Down Control Bit**
	0 = Normal Operation
	1 = Sleep Mode
SDO	**Internal Termination Selection Bit**
	0 = Internal Termination Disabled
	1 = Internal Termination Enabled

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then SDO can be left floating and no pull-up resistor is needed. Table 4 shows a map of the mode control registers.

Software Reset

If serial programming is used, the mode control registers should be programmed as soon as possible after the power supplies turn on and are stable. The first serial command must be a software reset which will reset all register data bits to logic 0. To perform a software reset, bit D7 in the reset register is written with a logic 1. After the reset SPI write command is complete, bit D7 is automatically set back to zero.

GROUNDING AND BYPASSING

The LTC2175-14/LTC2174-14/LTC2173-14 requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane in the first layer beneath the ADC is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, OV_{DD}, V_{CM}, V_{REF}, REFH and REFL pins. Bypass capacitors must be located as close to the pins as possible. Of particular importance is the 0.1µF capacitor between REFH and REFL. This capacitor should be on the same side of the circuit board as the A/D, and as close to the device as possible (1.5mm or less). Size 0402 ceramic capacitors are recommended. The larger 2.2µF capacitor between REFH and REFL can be somewhat further away. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The analog inputs, encode signals, and digital outputs should not be routed next to each other. Ground fill and grounded vias should be used as barriers to isolate these signals from each other.

HEAT TRANSFER

Most of the heat generated by the LTC2175-14/LTC2174-14/LTC2173-14 is transferred from the die through the bottom-side Exposed Pad and package leads onto the printed circuit board. For good electrical and thermal performance, the Exposed Pad must be soldered to a large grounded pad on the PC board. This pad should be connected to the internal ground planes by an array of vias.

Table 4. Serial Programming Mode Register Map (PAR/$\overline{SER}$ = GND)

REGISTER A0: RESET REGISTER (ADDRESS 00h)

D7	D6	D5	D4	D3	D2	D1	D0
RESET	X	X	X	X	X	X	X

Bit 7	**RESET**	Software Reset Bit
	0 = Not Used	
	1 = Software Reset. All Mode Control Registers are Reset to 00h. The ADC is Momentarily Placed in SLEEP Mode.	
	This Bit is Automatically Set Back to Zero at the End of the SPI Write Command.	
	The Reset Register is Write Only.	
Bits 6-0	Unused, Don't Care Bits.	

REGISTER A1: FORMAT AND POWER-DOWN REGISTER (ADDRESS 01h)

D7	D6	D5	D4	D3	D2	D1	D0
DCSOFF	RAND	TWOSCOMP	SLEEP	NAP_4	NAP_3	NAP_2	NAP_1

Bit 7	**DCSOFF**	Clock Duty Cycle Stabilizer Bit
	0 = Clock Duty Cycle Stabilizer On	
	1 = Clock Duty Cycle Stabilizer Off. This is Not Recommended.	
Bit 6	**RAND**	Data Output Randomizer Mode Control Bit
	0 = Data Output Randomizer Mode Off	
	1 = Data Output Randomizer Mode On	

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Bit 5	**TWOSCOMP** Two's Complement Mode Control Bit
	0 = Offset Binary Data Format
	1 = Two's Complement Data Format

Bits 4-0	**SLEEP: NAP_4:NAP_1** Sleep/Nap Mode Control Bits
	00000 = Normal Operation
	0XXX1 = Channel 1 in Nap Mode
	0XX1X = Channel 2 in Nap Mode
	0X1XX = Channel 3 in Nap Mode
	01XXX = Channel 4 in Nap Mode
	1XXXX = Sleep Mode. All Channels are Disabled
	Note: Any Combination of Channels Can Be Placed in Nap Mode.

REGISTER A2: OUTPUT MODE REGISTER (ADDRESS 02h)

D7	D6	D5	D4	D3	D2	D1	D0
ILVDS2	ILVDS1	ILVDS0	TERMON	OUTOFF	OUTMODE2	OUTMODE1	OUTMODE0

Bits 7-5	**ILVDS2:ILVDS0** LVDS Output Current Bits
	000 = 3.5mA LVDS Output Driver Current
	001 = 4.0mA LVDS Output Driver Current
	010 = 4.5mA LVDS Output Driver Current
	011 = Not Used
	100 = 3.0mA LVDS Output Driver Current
	101 = 2.5mA LVDS Output Driver Current
	110 = 2.1mA LVDS Output Driver Current
	111 = 1.75mA LVDS Output Driver Current

Bit 4	**TERMON** LVDS Internal Termination Bit
	0 = Internal Termination Off
	1 = Internal Termination On. LVDS Output Driver Current is 2x the Current Set by ILVDS2:ILVDS0. Internal termination should only be used with 1.75mA, 2.1mA or 2.5mA LVDS output current modes.

Bit 3	**OUTOFF** Output Disable Bit
	0 = Digital Outputs are Enabled.
	1 = Digital Outputs are Disabled.

Bits 2-0	**OUTMODE2:OUTMODE0** Digital Output Mode Control Bits
	000 = 2-Lanes, 16-Bit Serialization
	001 = 2-Lanes, 14-Bit Serialization
	010 = 2-Lanes, 12-Bit Serialization
	011 = Not Used
	100 = Not Used
	101 = 1-Lane, 14-Bit Serialization
	110 = 1-Lane, 12-Bit Serialization
	111 = 1-Lane, 16-Bit Serialization

REGISTER A3: TEST PATTERN MSB REGISTER (ADDRESS 03h)

D7	D6	D5	D4	D3	D2	D1	D0
OUTTEST	X	TP13	TP12	TP11	TP10	TP9	TP8

Bit 7	**OUTTEST** Digital Output Test Pattern Control Bit
	0 = Digital Output Test Pattern Off
	1 = Digital Output Test Pattern On

| Bit 6 | Unused, Don't Care Bit. |

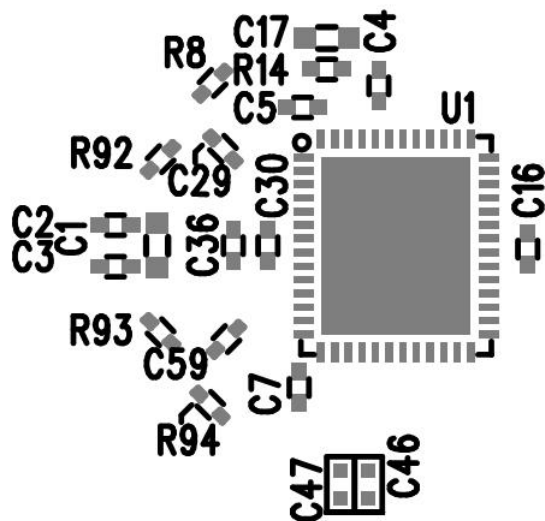| Bit 5-0 | **TP13:TP8** Test Pattern Data Bits (MSB) |
| | TP13:TP8 Set the Test Pattern for Data Bit 13(MSB) Through Data Bit 8. |

REGISTER A4: TEST PATTERN LSB REGISTER (ADDRESS 04h)

D7	D6	D5	D4	D3	D2	D1	D0
TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0

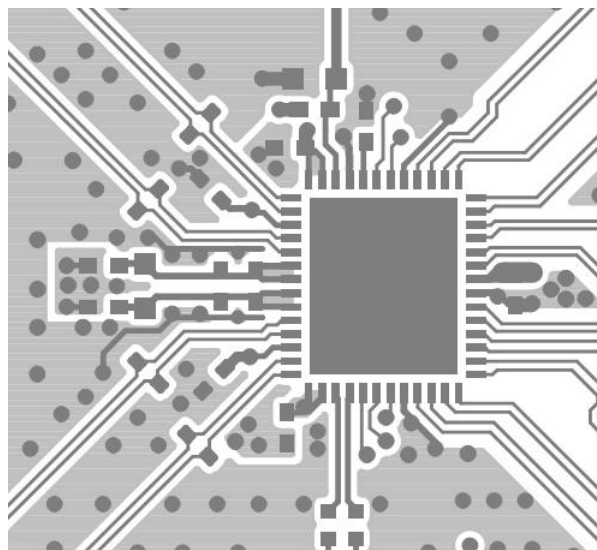| Bit 7-0 | **TP7:TP0** Test Pattern Data Bits (LSB) |
| | TP7:TP0 Set the Test Pattern for Data Bit 7 Through Data Bit 0(LSB). |

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TYPICAL APPLICATIONS

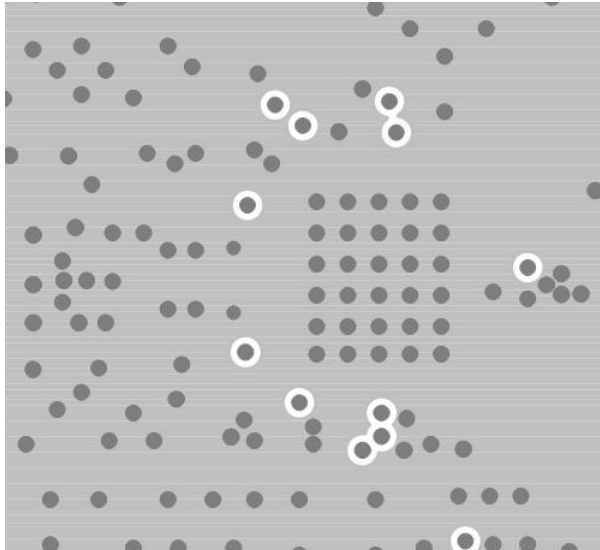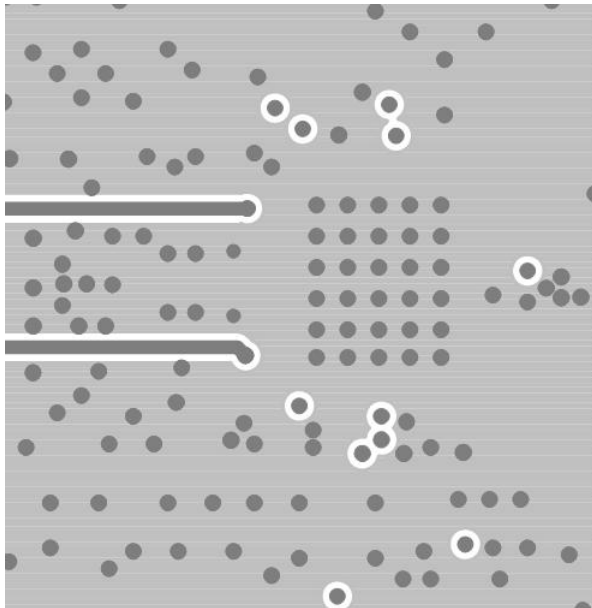**Silkscreen Top**

Top Side
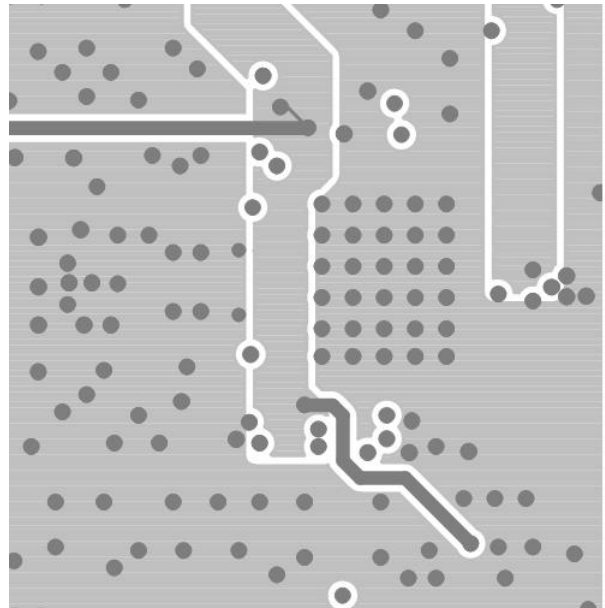
TYPICAL APPLICATIONS

Inner Layer 2 GND
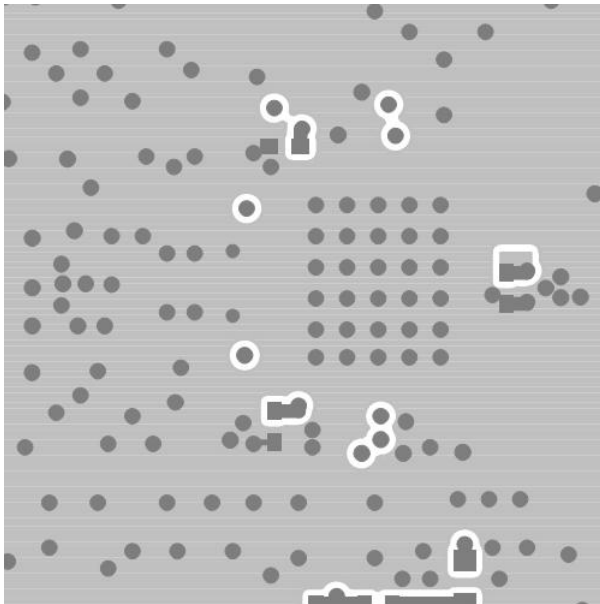

Inner Layer 3
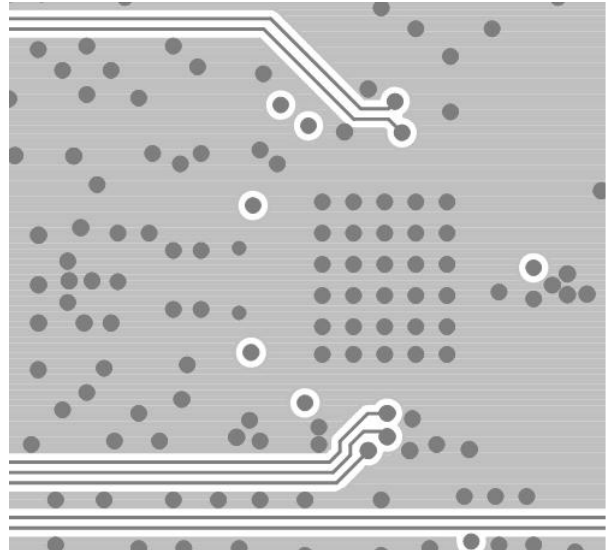
Inner Layer 4

Inner Layer 5 Power

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TYPICAL APPLICATIONS

Bottom Side

Silkscreen Bottom

C8

C9

C15
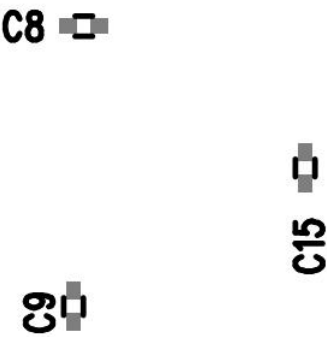
TYPICAL APPLICATIONS

LTC2175 Schematic

217514 TA02
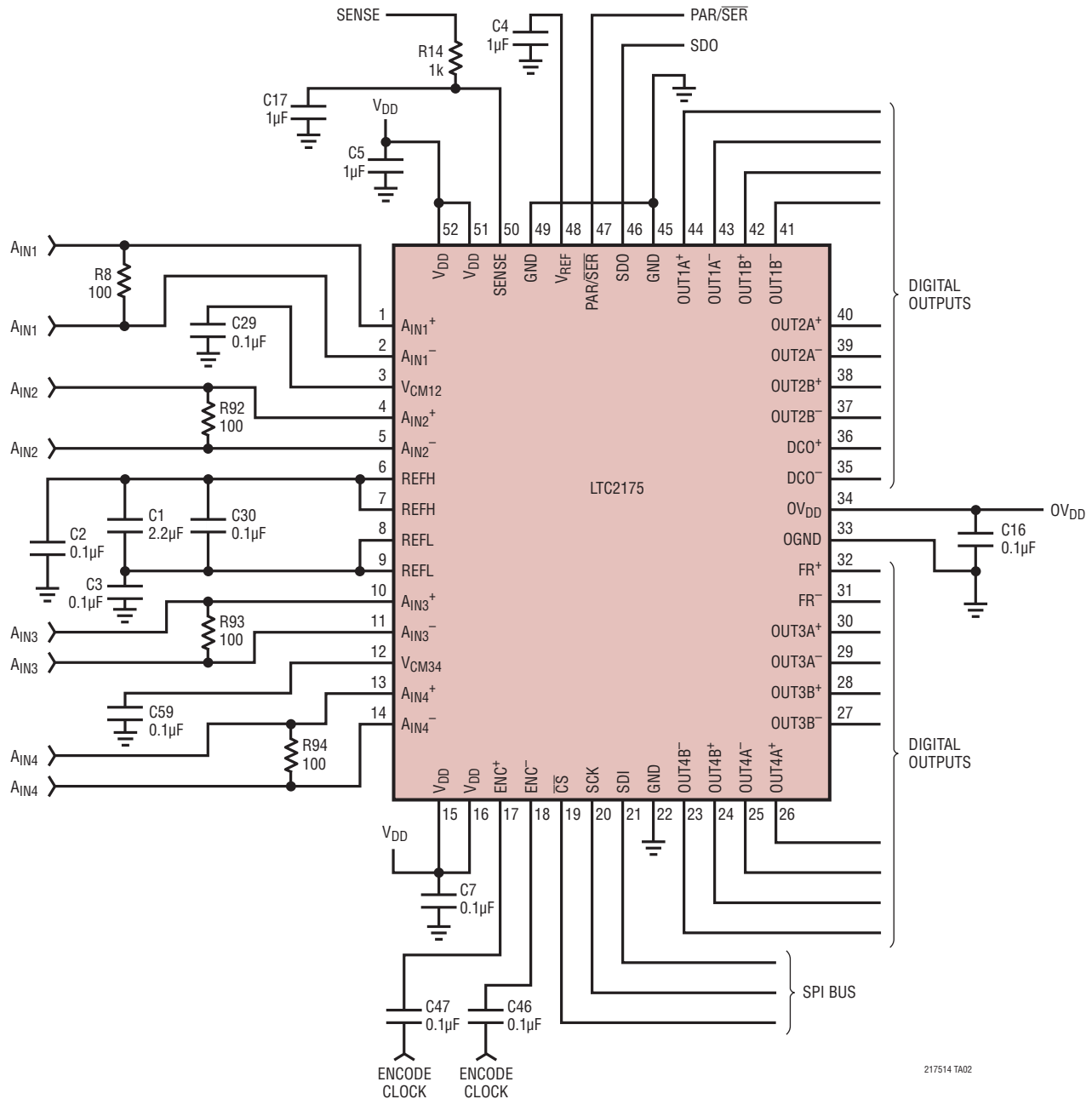
PACKAGE DESCRIPTION

UKG Package
52-Lead Plastic QFN (7mm × 8mm)
(Reference LTC DWG # 05-08-1729 Rev Ø)

7.50 ±0.05
6.10 ±0.05
5.50 REF
(2 SIDES)

0.70 ±0.05

6.45 ±0.05

6.50 REF
(2 SIDES)

7.10 ±0.05 8.50 ±0.05

5.41 ±0.05

← PACKAGE OUTLINE

0.25 ±0.05
0.50 BSC

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

7.00 ± 0.10
(2 SIDES)

0.75 ± 0.05
0.00 – 0.05

5.50 REF
(2 SIDES)

R = 0.115
TYP

51 52

0.40 ± 0.10

PIN 1 TOP MARK
(SEE NOTE 6)

1
2

PIN 1 NOTCH
R = 0.30 TYP OR
0.35 × 45°C
CHAMFER

8.00 ± 0.10
(2 SIDES)

6.50 REF
(2 SIDES)

6.45 ±0.10

5.41 ±0.10

R = 0.10
TYP

0.25 ± 0.05
0.50 BSC

(UKG52) QFN Ø Ø 0306

TOP VIEW

0.75 ± 0.05

0.200 REF
0.00 – 0.05

BOTTOM VIEW—EXPOSED PAD

SIDE VIEW

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS

4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/11	Corrected part numbers in Description.	1
		Revised Software Reset paragraph and Table 4 in Applications Information section.	26
		Added V_{DD} to LTC2175 Schematic in Typical Applications section.	31

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RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2170-14/LTC2171-14/ LTC2172-14	14-Bit, 25Msps/40Msps/65Msps 1.8V Quad ADCs, Ultralow Power	178mW/234mW/360mW, 73.4dB SNR, 85dB SFDR, Serial LVDS Outputs, 7mm × 8mm QFN-52
LTC2170-12/LTC2171-12/ LTC2172-12	12-Bit, 25Msps/40Msps/65Msps 1.8V Quad ADCs, Ultralow Power	178mW/234mW/360mW, 70.5dB SNR, 85dB SFDR, Serial LVDS Outputs, 7mm × 8mm QFN-52
LTC2173-12/LTC2174-12/ LTC2175-12	12-Bit, 80Msps/105Msps/125Msps 1.8V Quad ADCs, Ultralow Power	412mW/481mW/567mW, 70.5dB SNR, 85dB SFDR, Serial LVDS Outputs, 7mm × 8mm QFN-52
LTC2256-14/LTC2257-14/ LTC2258-14	14-Bit, 25Msps/40Msps/65Msps Msps1.8V ADCs, Ultralow Power	35mW/49mW/81mW, 74dB SNR, 88dB SFDR, DDR LVDS/DDR CMOS/CMOS Outputs, 6mm × 6mm QFN-36
LTC2259-14/LTC2260-14/ LTC2261-14	14-Bit, 80Msps/105Msps/125Msps 1.8V ADCs, Ultralow Power	89mW/106mW/127mW, 73.4dB SNR, 85dB SFDR, DDR LVDS/DDR CMOS/CMOS Outputs, 6mm × 6mm QFN-36
LTC2262-14	14-Bit, 150Msps 1.8V ADC, Ultralow Power	149mW, 72.8dB SNR, 88dB SFDR, DDR LVDS/DDR CMOS/CMOS Outputs, 6mm × 6mm QFN-36
LTC2263-14/LTC2264-14/ LTC2265-14	14-Bit, 25Msps/40Msps/65Msps 1.8V Dual ADCs, Ultralow Power	99mW/126mW/191mW, 73.4dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-36
LTC2263-12/LTC2264-12/ LTC2265-12	12-Bit, 25Msps/40Msps/65Msps 1.8V Dual ADCs, Ultralow Power	99mW/126mW/191mW, 70.5dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-36
LTC2266-14/LTC2267-14/ LTC2268-14	14-Bit, 80Msps/105Msps/125Msps 1.8V Dual ADCs, Ultralow Power	216mW/250mW/293mW, 73.4dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-36
LTC2266-12/LTC2267-12/ LTC2268-12	12-Bit, 80Msps/105Msps/125Msps 1.8V Dual ADCs, Ultralow Power	216mW/250mW/293mW, 70.5dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-36
RF Mixers/Demodulators		
LTC5517	40MHz to 900MHz Direct Conversion Quadrature Demodulator	High IIP3: 21dBm at 800MHz, Integrated LO Quadrature Generator
LTC5527	400MHz to 3.7GHz High Linearity Downconverting Mixer	24.5dBm IIP3 at 900MHz, 23.5dBm IIP3 at 3.5GHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LTC5557	400MHz to 3.8GHz High Linearity Downconverting Mixer	23.7dBm IIP3 at 2.6GHz, 23.5dBm IIP3 at 3.5GHz, NF = 13.2dB, 3.3V Supply Operation, Integrated Transformer
LTC5575	800MHz to 2.7GHz Direct Conversion Quadrature Demodulator	High IIP3: 28dBm at 900MHz, Integrated LO Quadrature Generator, Integrated RF and LO Transformer
Amplifiers/Filters		
LTC6412	800MHz, 31dB Range, Analog-Controlled Variable Gain Amplifier	Continuously Adjustable Gain Control, 35dBm OIP3 at 240MHz, 10dB Noise Figure, 4mm × 4mm QFN-24
LTC6420-20	1.8GHz Dual Low Noise, Low Distortion Differential ADC Drivers for 300MHz IF	Fixed Gain 10V/V, $1nV/\sqrt{Hz}$ Total Input Noise, 80mA Supply Current per Amplifier, 3mm × 4mm QFN-20
LTC6421-20	1.3GHz Dual Low Noise, Low Distortion Differential ADC Drivers	Fixed Gain 10V/V, $1nV/\sqrt{Hz}$ Total Input Noise, 40mA Supply Current per Amplifier, 3mm × 4mm QFN-20
LTC6605-7/ LTC6605-10/ LTC6605-14	Dual Matched 7MHz/10MHz/14MHz Filters with ADC Drivers	Dual Matched 2nd Order Lowpass Filters with Differential Drivers, Pin-Programmable Gain, 6mm × 3mm DFN-22
LTM9002	14-Bit Dual Channel IF/Baseband Receiver Subsystem	Integrated High Speed ADC, Passive Filters and Fixed Gain Differential Amplifiers

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