ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 10V
Digital Input Currents .... −100mA to 100mA
Digital Input Voltages .... −0.5V to 10V
Receiver Input Voltages .... ±14V
Receiver Output Voltages .... −0.5V to V_{DD} + 0.5V
Receiver Input Differential 10V

Short-Circuit Duration .... Indefinite
Operating Temperature Range
   LTC1518C/LTC1519C .... 0°C to 70°C
   LTC1518I/LTC1519I .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

```
B1    [1]        [16] VDD
A1    [2]        [15] B4
OUT 1 [3]        [14] A4
EN    [4]        [13] OUT 4
OUT 2 [5]        [12] EN
A2    [6]        [11] OUT 3
B2    [7]        [10] A3
GND   [8]        [9]  B3
```

S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 90°C/ W

ORDER PART NUMBER

LTC1518CS
LTC1518IS

TOP VIEW

```
B1    [1]        [16] VDD
A1    [2]        [15] B4
OUT 1 [3]        [14] A4
EN12  [4]        [13] OUT 4
OUT 2 [5]        [12] EN34
A2    [6]        [11] OUT 3
B2    [7]        [10] A3
GND   [8]        [9]  B3
```

S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 90°C/ W

ORDER PART NUMBER

LTC1519CS
LTC1519IS

Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V ±5% (Notes 2, 3) per receiver, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CM}	Input Common Mode Voltage	A, B Inputs	●	−7		12	V
V_{IH}	Input High Voltage	EN, $\overline{EN}$, EN12, EN34	●	2			V
V_{IL}	Input Low Voltage	EN, $\overline{EN}$, EN12, EN34	●			0.8	V
I_{IN1}	Input Current	EN, $\overline{EN}$, EN12, EN34	●	−1		1	µA
I_{IN2}	Input Current (A, B)	V_A, V_B = 12V	●			500	µA
		V_A, V_B = −7V	●	−500			µA
R_{IN}	Input Resistance	−7V ≤ V_{CM} ≤ 12V (Figure 5)	●	22			kΩ
C_{IN}	Input Capacitance	(Note 4)			3		pF
V_{OC}	Open-Circuit Input Voltage	V_{DD} = 5V (Note 4) (Figure 5)	●	3.2	3.3	3.4	V
$V_{ID(MIN)}$	Differential Input Threshold Voltage	−7V ≤ V_{CM} ≤ 12V	●	−0.3		0.3	V
dV_{ID}	Input Hysteresis	V_{CM} = 2.5V			25		mV
V_{OH}	Output High Voltage	I_{OUT} = −4mA, V_{ID} = 0.3V, V_{DD} = 5V	●	4.6			V
V_{OL}	Output Low Voltage	I_{OUT} = 4mA, V_{ID} = −0.3V, V_{DD} = 5V	●			0.4	V
I_{OZR}	Three-State Output Current	0V < V_{OUT} < 5V	●	−10		10	µA
I_{DD}	Total Supply Current All 4 Receivers	$|V_{ID}|$ > 0.3V, No Load, Device Enabled	●		12	20	mA
I_{OSR}	Short-Circuit Current	V_{OUT} = 0V, V_{OUT} = 5V (Note 7)	●	−50		50	mA

LINEAR TECHNOLOGY

DC ELECTRICAL CHARACTERISTICS
The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V ±5% (Notes 2, 3) per receiver, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Max V_{ID} for Fail-Safe Detection	$-7V \leq V_{CM} \leq 12V$			25		mV
	Min Time to Detect Fault Condition				2		µs
CMRR	Common Mode Rejection Ratio	V_{CM} = 2.5V, f = 26MHz (Note 4)			45		dB

SWITCHING TIME CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V ±5% (Notes 2, 3) V_{ID} = 1.5V, V_{CM} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}, t_{PHL}	Input-to-Output Propagation Delay	C_L = 15pF, 0°C ≤ T_A ≤ 70°C (Figure 1)	●	15	18.5	22	ns
		C_L = 15pF, −40°C ≤ T_A ≤ 85°C (Figure 1)	●	12		25	ns
t_r, t_f	Rise/Fall Times	C_L = 15pF			2.5		ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Skew	C_L = 15pF, Same Receiver (Note 5)			500		ps
t_{ZL}	Enable to Output Low	C_L = 15pF, 0°C ≤ T_A ≤ 70°C (Figure 2)	●		10	35	ns
		C_L = 15pF, −40°C ≤ T_A ≤ 85°C (Figure 2)			15		ns
t_{ZH}	Enable to Output High	C_L = 15pF, 0°C ≤ T_A ≤ 70°C (Figure 2)	●		10	35	ns
		C_L = 15pF, −40°C ≤ T_A ≤ 85°C (Figure 2)			15		ns
t_{LZ}	Disable from Output Low	C_L = 15pF, 0°C ≤ T_A ≤ 70°C (Figure 2)	●		20	35	ns
		C_L = 15pF, −40°C ≤ T_A ≤ 85°C (Figure 2)			25		ns
t_{HZ}	Disable from Output High	C_L = 15pF, 0°C ≤ T_A ≤ 70°C (Figure 2)	●		20	35	ns
		C_L = 15pF, −40°C ≤ T_A ≤ 85°C (Figure 2)			25		ns
t_{CH-CH}	Channel-to-Channel Skew	C_L = 15pF (Figure 3, Note 6)			500		ps
$t_{PKG-PKG}$	Package-to-Package Skew	C_L = 15pF, Same Temperature (Figure 4, Note 4)			1.5		ns
t_r, t_f Input	Maximum Input Rise or Fall Time	(Note 4)	●			2000	ns
	Minimum Input Pulse Width	0°C ≤ T_A ≤ 70°C (Note 4)	●		12	19.2	ns
		−40°C ≤ T_A ≤ 85°C (Note 4)	●		16	25	ns
$f_{IN(MAX)}$	Maximum Input Frequency	Square Wave, 0°C ≤ T_A ≤ 70°C (Note 4)	●	26	40		MHz
		Square Wave, −40°C ≤ T_A ≤ 85°C (Note 4)	●	20	30		MHz
	Maximum Data Rate	0°C ≤ T_A ≤ 70°C (Note 4)	●	52	80		Mbps
		−40°C ≤ T_A ≤ 85°C (Note 4)	●	40	65		Mbps
C_L	Load Capacitance	(Note 4)				500	pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into the device pins are positive; all currents out of the device pins are negative.

Note 3: All typicals are given for V_{DD} = 5V, T_A = 25°C.

Note 4: Guaranteed by design, but not tested.

**Note 5:** Worst-case $\lvert t_{PLH} - t_{PHL} \rvert$ skew for a single receiver in a package over the full operating temperature range.

Note 6: Maximum difference between any two t_{PLH} or t_{PHL} transitions in a single package over the full operating temperature range.

Note 7: Short-circuit current does not represent output drive capability. When the output detects a short-circuit condition, output drive current is significantly reduced until the short is removed.
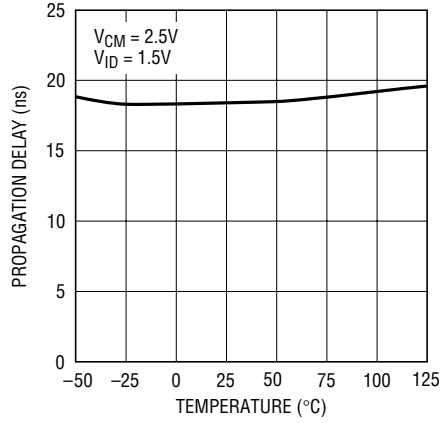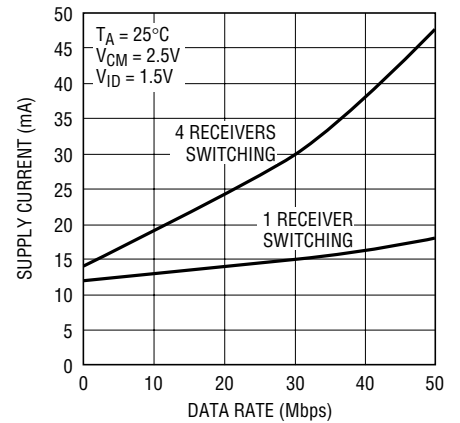
3

TYPICAL PERFORMANCE CHARACTERISTICS

CMRR vs Frequency

COMMON MODE REJECTION RATIO (dB) vs FREQUENCY (Hz)

$T_A = 25°C$
$V_{CM} = 2.5V$
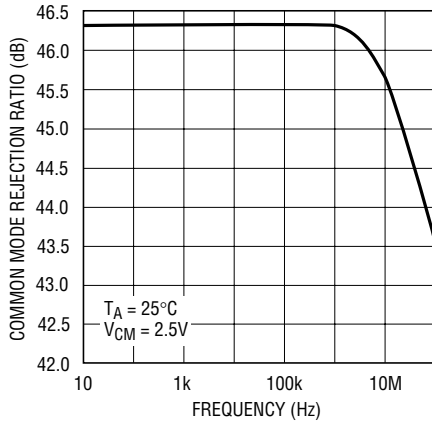
15189 G01

Propagation Delay (t_{PLH}/t_{PHL}) vs Temperature

PROPAGATION DELAY (ns) vs TEMPERATURE (°C)

$V_{CM} = 2.5V$
$V_{ID} = 1.5V$

15189 G02

Supply Current vs Data Rate

SUPPLY CURRENT (mA) vs DATA RATE (Mbps)

$T_A = 25°C$
$V_{CM} = 2.5V$
$V_{ID} = 1.5V$

4 RECEIVERS SWITCHING

1 RECEIVER SWITCHING

15189 G03

Supply Current vs Temperature and Data Rate

SUPPLY CURRENT (mA) vs DATA RATE (Mbps)

$V_{CM} = 2.5V$
$V_{ID} = 1.5V$
1 RECEIVER SWITCHING

100°C
25°C
0°C
−25°C
−50°C
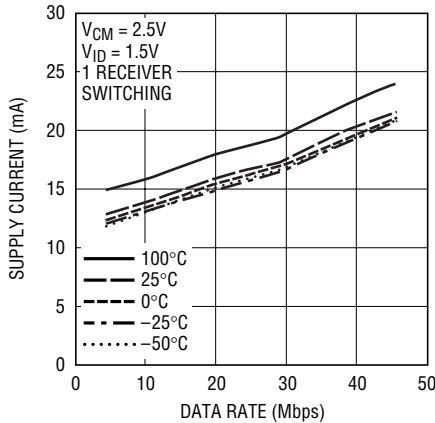
15189 G04

Propagation Delay vs Load Capacitance

PROPAGATION DELAY (ns) vs LOAD CAPACITANCE (pF)

$T_A = 25°C$
$V_{CM} = 2.5V$
$V_{ID} = 1.5V$
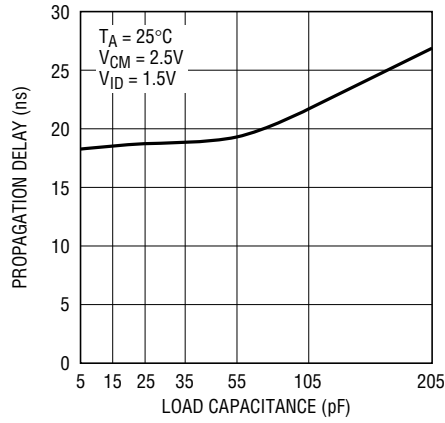
15189 G05

Propagation Delay vs Common Mode

PROPAGATION DELAY (ns) vs COMMON MODE (V)

$T_A = 25°C$
$V_{ID} = 1.5V$
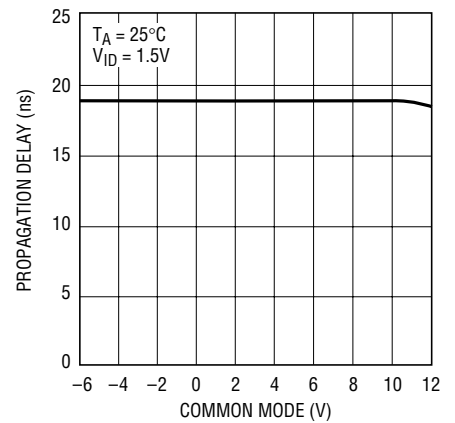
15189 G06

Propagation Delay vs Input Differential Voltage

PROPAGATION DELAY (ns) vs INPUT DIFFERENTIAL (V)

$T_A = 25°C$
$V_{CM} = 2.5V$
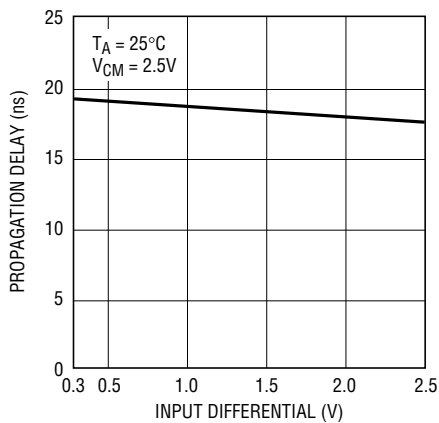
15189 G07

Maximum Data Rate vs Input Differential Voltage

DATA RATE (Mbps) vs INPUT DIFFERENTIAL (V)

$T_A = 25°C$
$V_{CM} = 2.5V$

15189 G08

4
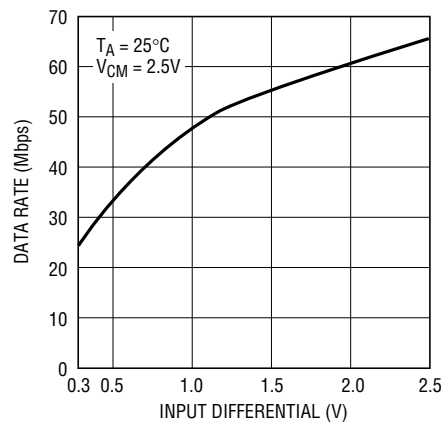
PIN FUNCTIONS

LTC1518

B1 (Pin 1): Receiver 1 Inverting Input.

A1 (Pin 2): Receiver 1 Noninverting Input.

OUT 1 (Pin 3): Receiver 1 Output.

EN (Pin 4): A high enables all outputs; a low on Pin 4 and a high on Pin 12 will put all outputs into a high impedance state. Do not float.

OUT 2 (Pin 5): Receiver 2 Output.

A2 (Pin 6): Receiver 2 Noninverting Input.

B2 (Pin 7): Receiver 2 Inverting Input.

GND (Pin 8): Ground Pin. A ground plane is recommended for all LTC1518 applications.

B3 (Pin 9): Receiver 3 Inverting Input.

A3 (Pin 10): Receiver 3 Noninverting Input.

OUT 3 (Pin 11): Receiver 3 Output.

$\overline{\text{EN}}$ (Pin 12): A low enables all outputs; a low on Pin 4 and a high on Pin 12 will put all outputs into a high impedance state. Do not float.

OUT 4 (Pin 13): Receiver 4 Output.

A4 (Pin 14): Receiver 4 Noninverting Input.

B4 (Pin 15): Receiver 4 Inverting Input.

V_{DD} (Pin 16): Power Supply Input. This pin should be decoupled with a 0.1µF ceramic capacitor as close as possible to the pin. Recommended: V_{DD} = 5V ±5%.

LTC1519

B1 (Pin 1): Receiver 1 Inverting Input.

A1 (Pin 2): Receiver 1 Noninverting Input.

OUT 1 (Pin 3): Receiver 1 Output.

EN12 (Pin 4): A high enables receivers 1 and 2; a low will put the outputs of receivers 1 and 2 into a high impedance state. Do not float.

OUT 2 (Pin 5): Receiver 2 Output.

A2 (Pin 6): Receiver 2 Noninverting Input.

B2 (Pin 7): Receiver 2 Inverting Input.

GND (Pin 8): Ground Pin. A ground plane is recommended for all LTC1519 applications.

B3 (Pin 9): Receiver 3 Inverting Input.

A3 (Pin 10): Receiver 3 Noninverting Input.

OUT 3 (Pin 11): Receiver 3 Output.

EN34 (Pin 12): A high enables receivers 3 and 4; a low will put the outputs of receivers 3 and 4 into a high impedance state. Do not float.

OUT 4 (Pin 13): Receiver 4 Output.

A4 (Pin 14): Receiver 4 Noninverting Input.

B4 (Pin 15): Receiver 4 Inverting Input.

V_{DD} (Pin 16): Power Supply Input. This pin should be decoupled with a 0.1µF ceramic capacitor as close as possible to the pin. Recommended: V_{DD} = 5V ±5%.

5

SWITCHING TIME WAVEFORMS $t_r = t_f \leq 3ns$ for all input and enable signals.
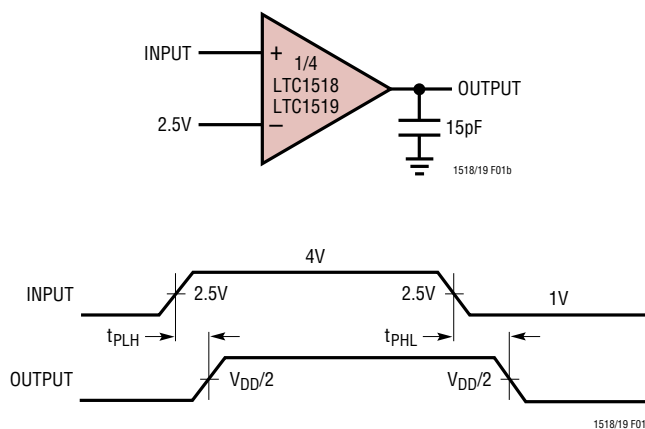

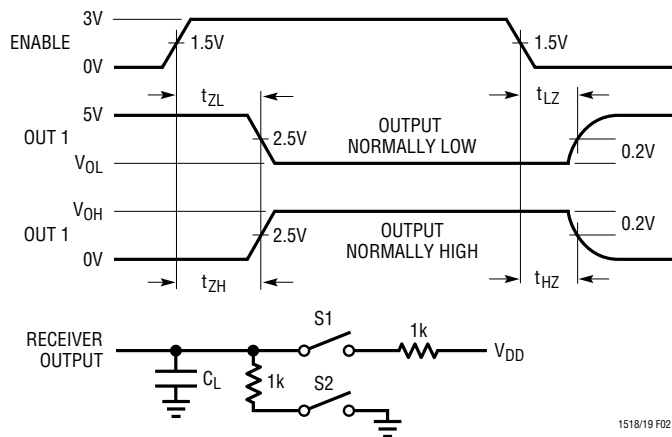Figure 1. Propagation Delay Test Circuit and Waveforms

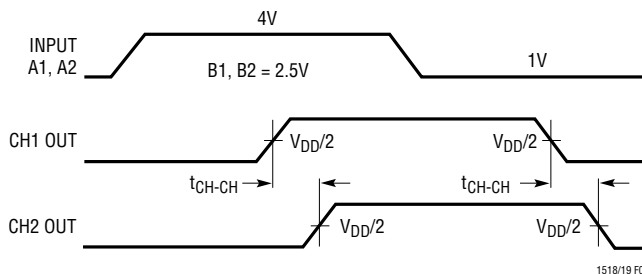Figure 2. Receiver Enable and Disable Timing Test Circuit and Waveforms

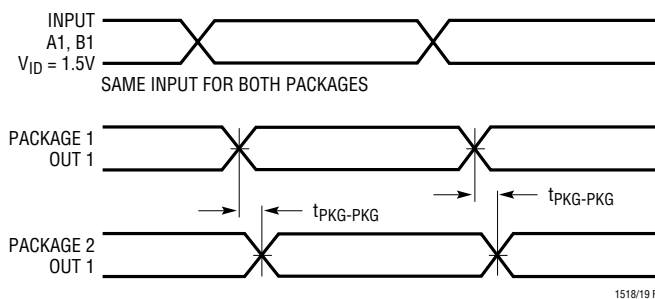Figure 3. Any Channel to Any Channel Skew, Same Package

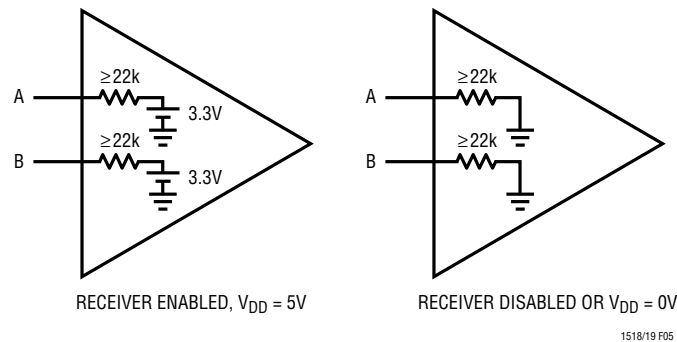Figure 4. Package-to-Package Propagation Delay Skew

EQUIVALENT INPUT NETWORKS

RECEIVER ENABLED, V_{DD} = 5V

RECEIVER DISABLED OR V_{DD} = 0V

1518/19 F05

Figure 5. Input Thevenin Equivalent

APPLICATIONS INFORMATION

Theory of Operation

Unlike typical line receivers whose propagation delay can vary by as much as 500% from package to package and show significant temperature drift, the LTC1518/LTC1519 employ a novel architecture that produces a tightly controlled and temperature compensated propagation delay. The differential timing skew is also minimized between rising and falling output edges, and the propagation delays of any two receivers within a package are very tightly matched.

The precision timing features of the LTC1518/LTC1519 reduce overall system timing constraints by providing a narrow ±3.5ns window during which valid data appears at the receiver output. This output timing window applies to all receivers in all packages over the commercial operating temperature range, thereby making the LTC1518/LTC1519 well suited for high speed data transmission.

In clocked data systems, the low skew minimizes duty cycle distortion of the clock signal. The LTC1518/LTC1519 can propagate signals at frequencies of 26MHz (52Mbps) with less than 5% duty cycle distortion. When a clock signal is used to retime parallel data, the maximum recommended data transmission rate is 25Mbps to avoid timing errors due to clock distortion.

Thermal shutdown and short-circuit protection prevent latchup damage to the LTC1518/LTC1519 during fault conditions.

Fail-Safe Features

The LTC1518/LTC1519 have a fail-safe feature that guarantees the output to be in a logic HIGH state when the inputs are either shorted or left open (note that when inputs are left open, any external large leakage current might override the fail-safe). The fail-safe feature detects shorted inputs over the entire common mode range. When a fault is detected, the output will typically go high in 2μs.

When some of the receivers within a package are not used, the open fail-safe feature will allow the user to let the receiver inputs float and maintain a high logic state at the output. Without the open fail-safe feature, any noise at the input would cause unwanted glitches at the output. When the inputs are left "open," one must make sure that there are no sources of leakage current connected to one or both of the inputs. This can happen if the device is being driven single-endedly and both the signal and the DC bias are disconnected. If the capacitor used to bypass the DC bias is left connected to the input of the device and is leaky (>1μA), the output of the device might not be the desired high logic state. Also keep in mind that the inputs are high impedance (≥22kΩ). When left open, noisy traces should be kept away from the receiver inputs to minimize capacitive coupling of undesired signals. Even with the open fail-safe feature, for maximum noise immunity, grounding the negative input of unused receivers is recommended.

APPLICATIONS INFORMATION

When the inputs are accidentally shorted (by cutting through a cable, for example), the short-circuit fail-safe feature will guarantee a high output logic level. Note also that if the line driver is removed and the termination resistors are left in place, the receiver will see this as a "short" and output a logic high.

Both of these fail-safe features will keep the receiver from outputting false data pulses under fault conditions.

Single-Ended Applications

Over short distances, the LTC1518/LTC1519 can be configured to receive single-ended data by tying one input to a fixed bias voltage and connecting the other input to the driver output. In such applications, standard high speed CMOS logic may be used as a driver for the LTC1518/LTC1519. With a 22k minimum input resistance, the receiver trip points may be easily adjusted to

accommodate different driver output swings by changing the resistor divider at the fixed input. Figure 6a shows a single-ended receiver configuration with the driver and receiver connected via PC traces. Note that at very high speeds, transmission line and driver ringing effects must be considered. Motorola's *MECL System Design Handbook* serves as an excellent reference for transmission line and termination effects. To mitigate transmission errors and duty cycle distortion due to driver ringing, a small output filter or a dampening resistor on the driver's V_{DD} may be needed as shown in Figure 6b. With an open circuit voltage of 3.3V at both inputs, the receivers can be used without an external bias applied to the fixed inputs. The fixed input should be bypassed with a 0.01µF ceramic capacitor. The positive input should be driven with a 5V CMOS part in order to minimize the skew caused by the 3.3V threshold. Figure 6c shows this configuration.
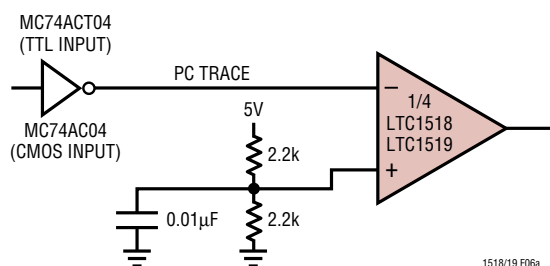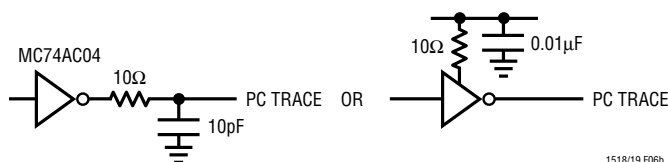

Figure 6a. Single-Ended Receiver

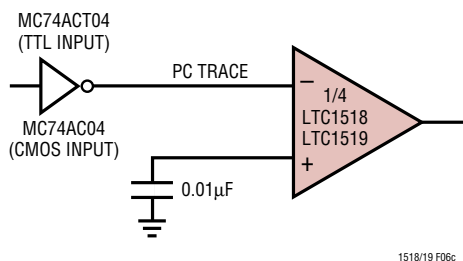Figure 6b. Techniques to Minimize Driver Ringing

Figure 6c. Self Biased Single Ended Receiver

8

APPLICATIONS INFORMATION

Note that due to the increased skew, this configuration might not operate at the highest data rates. To transmit single-ended data over short to medium distances, twisted pair is recommended with the unused wire grounded at both ends (Figure 7).

Differential Transmission

Data rates up to 52Mbps can be transmitted over 100 feet of high quality category 5 twisted pair. Figure 8 shows the LTC1518 receiving differential data from an LTC1685 transceiver. As in the single-ended configurations, care must be taken to properly terminate the differential data lines to avoid unwanted reflections, etc.
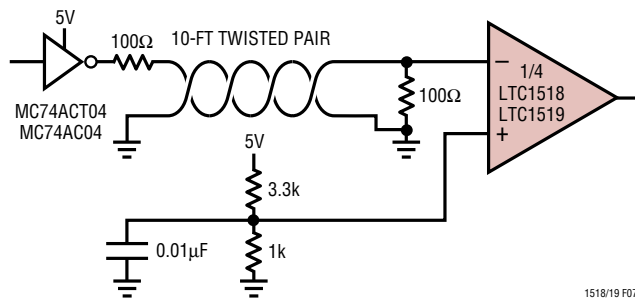

Figure 7. Medium Distance Single-Ended Transmission Using a CMOS Driver
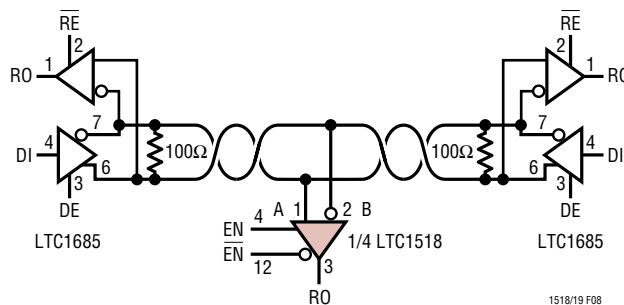

Figure 8. LTC1518 Connected to LTC1685 High Speed RS485 Transceiver

APPLICATIONS INFORMATION

Figure 9 shows a trace with 100ft category 5 UTP between an LTC1685 driver and an LTC1518 receiver. Notice that at the far end of the cable, the signal to the LTC1518 input has been reduced. Figure 10 shows a 52Mbps square wave.

Output Short-Circuit Protection

The LTC1518/LTC1519 employ voltage sensing short-circuit protection at the output terminals. For a given input differential, this circuitry determines what the correct output level should be. For example, if the input differential is $\geq 300mV$, it expects the output to be a logic high. If the output is subsequently shorted to a voltage below $V_{DD}/2$, this circuitry shuts off the output devices and turns on a smaller device in its place. A timeout period of about 50ns is used in order to maintain normal high frequency operation, even under heavy capacitive loads (>100mA transient current into the load).

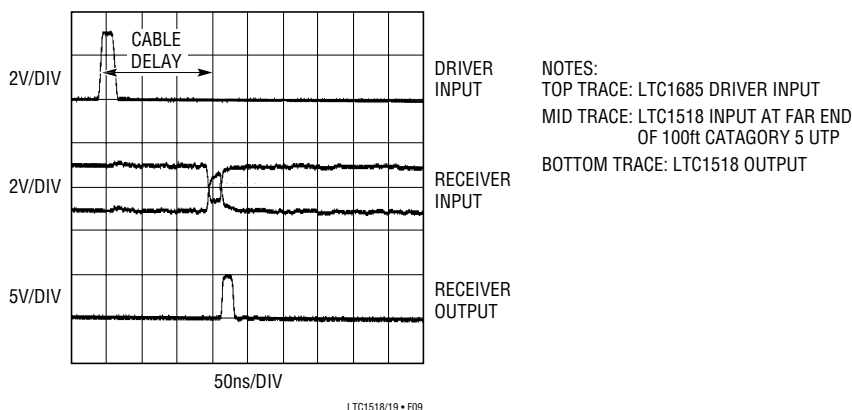**Figure 9. 20ns Pulse Propagating Down 100ft of Category 5 UTP**
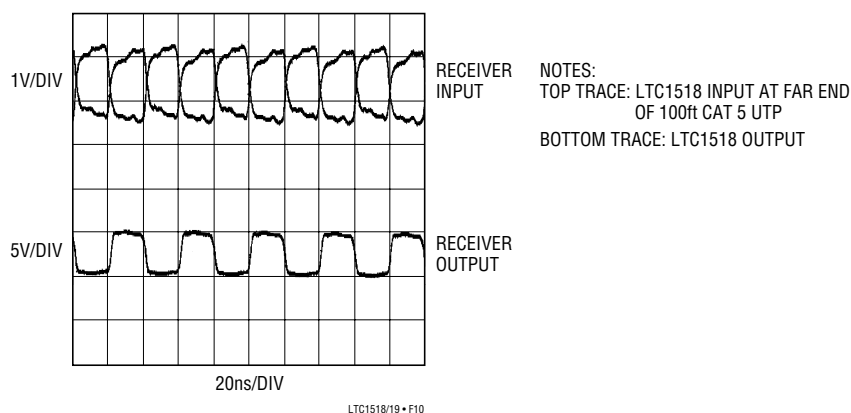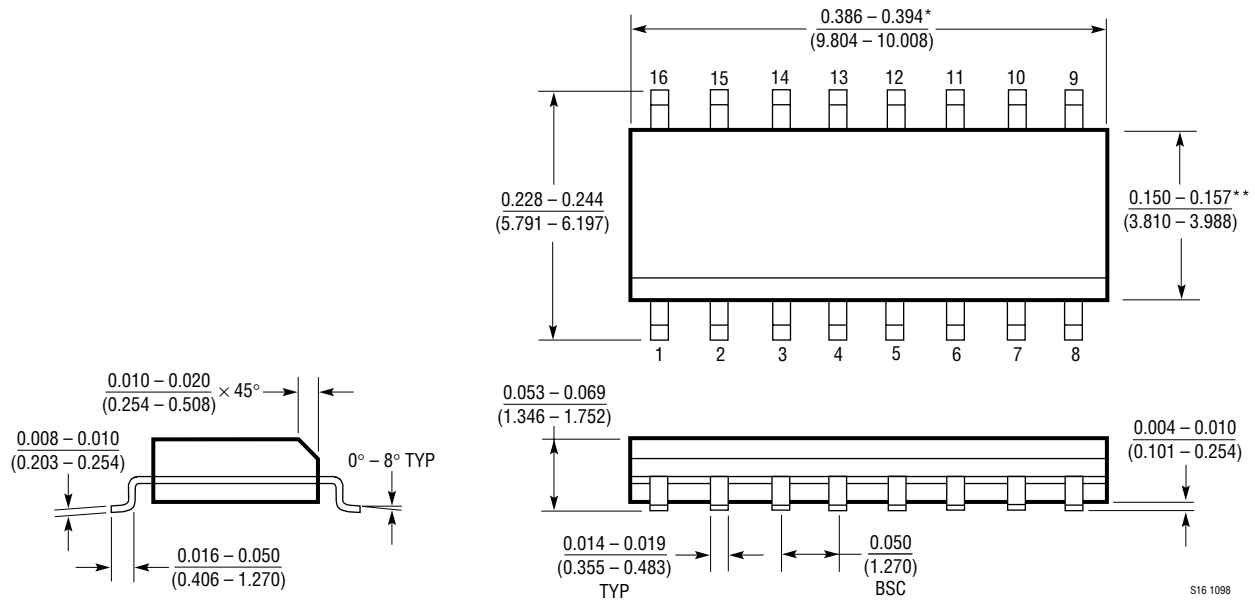

Figure 10. 52Mbps Pulse Train Over 100ft of Category 5 UTP

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PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

0.386 – 0.394*
(9.804 – 10.008)

16 15 14 13 12 11 10 9

0.228 – 0.244
(5.791 – 6.197)

0.150 – 0.157**
(3.810 – 3.988)

1   2   3   4   5   6   7   8

0.010 – 0.020
(0.254 – 0.508) × 45°

0.008 – 0.010
(0.203 – 0.254)

0° – 8° TYP

0.016 – 0.050
(0.406 – 1.270)

0.053 – 0.069
(1.346 – 1.752)

0.004 – 0.010
(0.101 – 0.254)

0.014 – 0.019
(0.355 – 0.483)
TYP

0.050
(1.270)
BSC

S16 1098

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

High Speed Receiver with Hot Swap Control

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC486/LTC487	Low Power Quad RS485 Drivers	10Mbps, −7V to 12V Common Mode Range
LTC488/LTC489	Low Power Quad RS485 Receivers	10Mbps, −7V to 12V Common Mode Range
LT®1016	UltraFast™ Precision Comparator	Single 5V Supply, 10ns Propagation Delay
LTC1520	High Speed, Precision Quad Differential Line Receiver	50Mbps, ±100mV Threshold, Rail-to-Rail Common Mode
LTC1685/LTC1686/ LTC1687	High Speed, Precision RS485 Transceivers	52Mbps, Pin Compatible with LTC485/490/491
LTC1688/LTC1689	High Speed, RS485 Quad Drivers	100Mbps, Pin Compatible with LTC486/LTC487

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