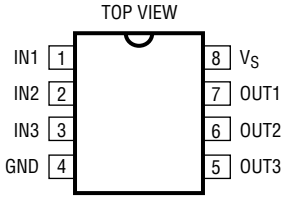
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 7V
Any Input Voltage ..... 7V to (GND – 0.3V)
Any Output Voltage ..... 20V to (GND – 0.3V)
Current (Any Pin) 50mA

Operating Temperature Range
LTC1163C/LTC1165C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

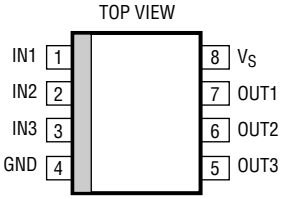
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1163CN8 LTC1165CN8



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 100°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1163CS8 LTC1165CS8
S8 PART MARKING
1163 1165

ELECTRICAL CHARACTERISTICS

V_S = 1.8V to 6V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1163C/LTC1165C MIN	TYP	MAX	UNITS
I_Q	Quiescent Current OFF	V_S = 1.8V, $V_{IN1} = V_{IN2} = V_{IN3} = V_{OFF}$ (Note 1,2)			0.01	1	µA
		V_S = 3.3V, $V_{IN1} = V_{IN2} = V_{IN3} = V_{OFF}$ (Note 1,2)			0.01	1	µA
		V_S = 5V, $V_{IN1} = V_{IN2} = V_{IN3} = V_{OFF}$ (Note 1,2)			0.01	1	µA
	Quiescent Current ON	V_S = 1.8V, $V_{IN} = V_{ON}$ (Note 2,3)			60	120	µA
		V_S = 3.3V, $V_{IN} = V_{ON}$ (Note 2,3)			95	200	µA
		V_S = 5V, $V_{IN} = V_{ON}$ (Note 2,3)			180	400	µA
V_{INH}	Input High Voltage	1.8V < V_S < 2.7V	●	80% × V_S			V
		2.7V < V_S < 6V	●	70% × V_S			V
V_{INL}	Input Low Voltage	1.8V < V_S < 6V	●			15% × V_S	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	●			±1	µA
C_{IN}	Input Capacitance				5		pF
$V_{GATE} – V_S$	Gate Voltage Above Supply	V_S = 1.8V, $V_{IN} = V_{ON}$ (Note 2)	●	3.5	4.1	6.0	V
		V_S = 2V, $V_{IN} = V_{ON}$ (Note 2)	●	4.0	4.6	7.0	V
		V_S = 2.2V, $V_{IN} = V_{ON}$ (Note 2)	●	4.5	5.2	8.0	V
		V_S = 3.3V, $V_{IN} = V_{ON}$ (Note 2)	●	6.0	8.0	9.5	V
		V_S = 5V, $V_{IN} = V_{ON}$ (Note 2)	●	5.0	9.0	13.0	V
t_{ON}	Turn-ON Time	V_S = 3.3V, C_{GATE} = 1000pF					
		Time for $V_{GATE} > V_S + 1V$		40	120	400	µs
		Time for $V_{GATE} > V_S + 2V$		60	180	600	µs
		V_S = 5V, C_{GATE} = 1000pF					
		Time for $V_{GATE} > V_S + 1V$		30	95	300	µs
		Time for $V_{GATE} > V_S + 2V$		40	130	400	µs

ELECTRICAL CHARACTERISTICS

V_S = 1.8V to 6V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1163C/LTC1165C MIN	TYP	MAX	UNITS
t_{OFF}	Turn-OFF Time	V_S = 3.3V, C_{GATE} = 1000pF Time for V_{GATE} < 0.5V	20	65	200	µs
		V_S = 5V, C_{GATE} = 1000pF Time for V_{GATE} < 0.5V	15	45	150	µs

The ● denotes specifications which apply over the full operating temperature range.

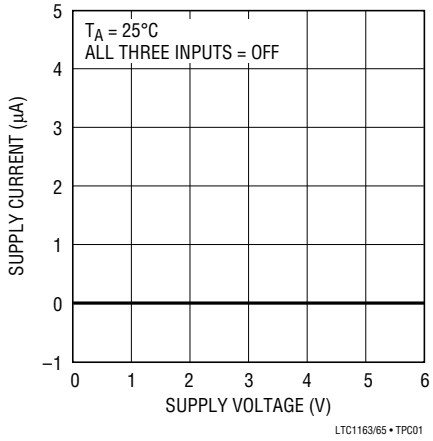
Note 1: Quiescent current OFF is for all channels in OFF condition.

Note 2: LTC1163: V_{OFF} = 0V, V_{ON} = V_S. LTC1165: V_{OFF} = V_S, V_{ON} = 0V

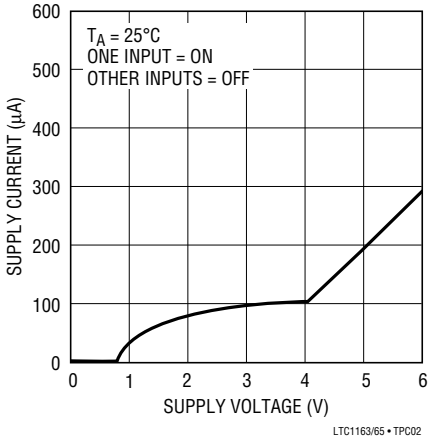
Note 3: Quiescent current ON is per driver and is measured independently.

TYPICAL PERFORMANCE CHARACTERISTICS

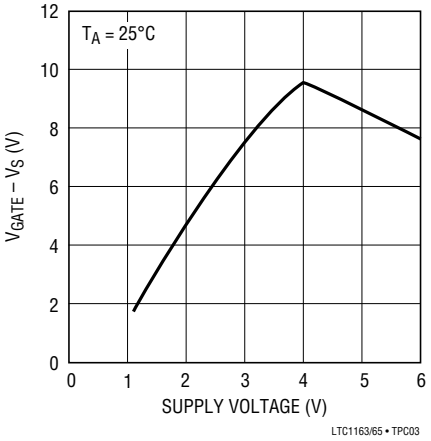
Standby Supply Current



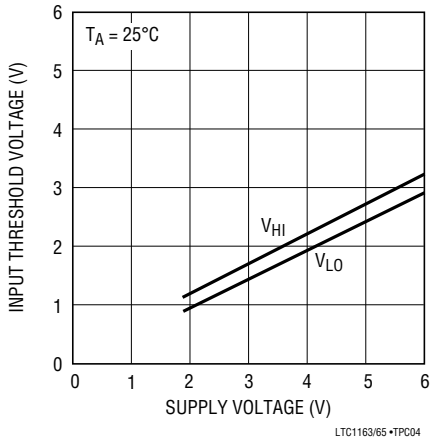
Supply Current per Driver ON



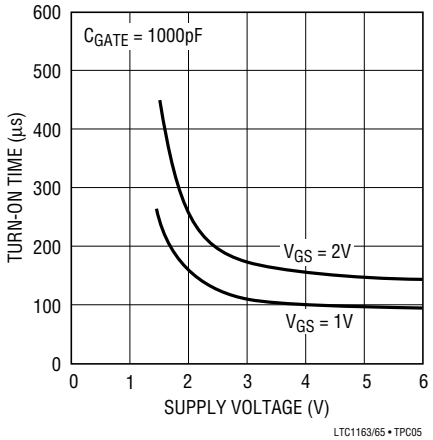
Gate Voltage Above Supply



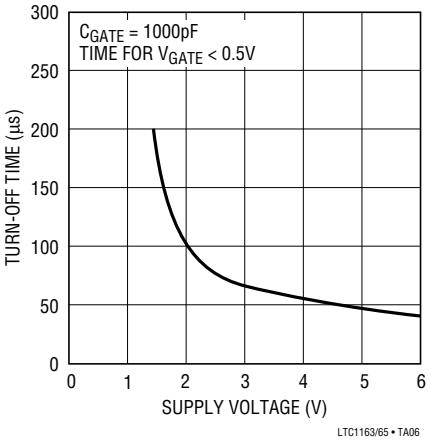
Input Threshold Voltage



Turn-ON Time

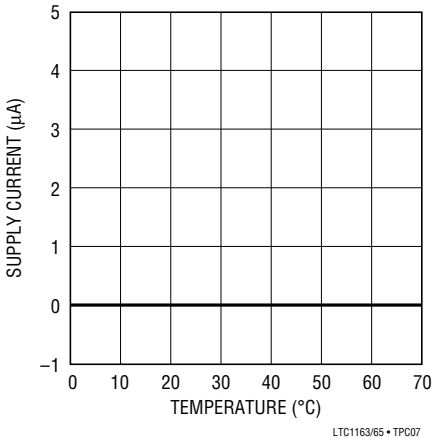


Turn-OFF Time

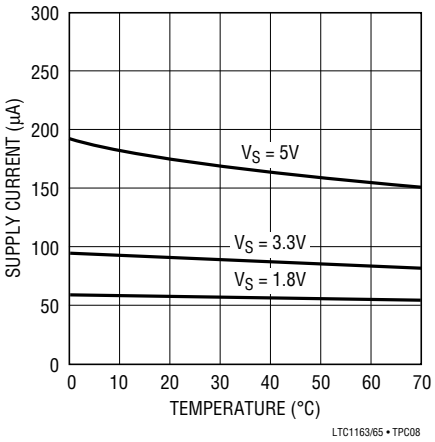


TYPICAL PERFORMANCE CHARACTERISTICS

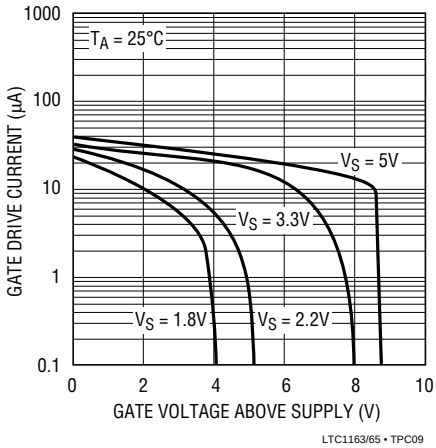
Standby Supply Current



Supply Current per Driver ON



MOSFET Gate Drive Current



PIN FUNCTIONS

Input Pins

The LTC1163 is noninverting; i.e., the MOSFET gate is driven above the supply when the input pin is held high. The LTC1165 is inverting and drives the MOSFET gate high when the input pin is held low. The inverting inputs of the LTC1165 allow P-channel switches to be replaced by lower resistance/cost N-channel switches while maintaining system drive polarity.

The LTC1163/LTC1165 logic inputs are high impedance CMOS gates with ESD protection diodes to ground and therefore should not be forced below ground. The inputs can however, be driven above the power supply rail as there are no clamping diodes connected between the input pins and supply pin. This facilitates operation in mixed 5V/3V systems.

Output Pins

The output pin is either driven to ground when the switch is turned OFF or driven above the supply rail when the switch is turned ON. The output is clamped to about 14V above ground by a built-in Zener clamp. This pin has a relatively high impedance when driven above the rail (the equivalent of a few hundred kΩ). Care should be taken to minimize any loading of this pin by parasitic resistance to ground or supply.

Supply Pin

A 150Ω resistor should be inserted in series with the ground pin or supply pin if negative supply voltage transients are anticipated. This will limit the current flowing from the power source into the LTC1163/LTC1165 to tens of milliamps during reverse battery conditions.

OPERATION

The LTC1163/LTC1165 are triple micropower MOSFET drivers designed for operation over the 1.8V to 6V supply range and include the following functional blocks:

3V Logic Compatible Inputs

The LTC1163/LTC1165 inputs have been designed to accommodate a wide range of 3V and 5V logic families. The input threshold voltage is set at roughly 50% of the supply voltage and approximately 200mV of input hysteresis is provided to ensure clean switching.

The input enables all of the following circuit blocks: the bias generator, the high frequency oscillator and gate charge pump. Therefore, when the input is turned off, the entire circuit powers down and the supply current drops below 1µA.

OPERATION

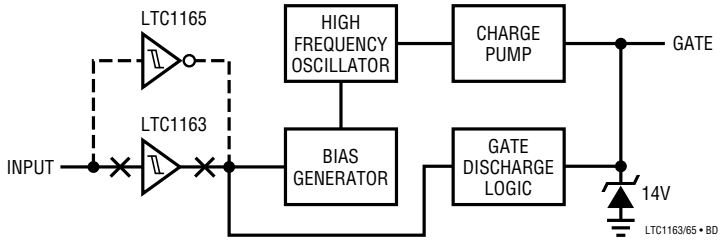
Gate Charge Pump

Gate drive for the power MOSFET is produced by an internal charge pump circuit which generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on chip and therefore no external components are required to generate gate drive.

Controlled Gate Rise and Fall Times

When the input is switched ON and OFF, the gate is charged by the internal charge pump and discharged in a controlled manner. The charge and discharge rates have been set to minimize RFI and EMI emissions.

BLOCK DIAGRAM (One Channel)



APPLICATIONS INFORMATION

Logic-Level MOSFET Switches

The LTC1163/LTC1165 are designed to operate with logic-level N-channel MOSFET switches. Although there is some variation among manufacturers, logic-level MOSFET switches are typically rated with V_{GS} = 4V with a maximum continuous V_{GS} rating of ±10V. $R_{DS(ON)}$ and maximum V_{DS} ratings are similar to standard MOSFETs and there is generally little price differential. Logic-level MOSFETs are frequently designated by an "L" and are usually available in surface mount packaging. Some logic-level MOSFETs are rated with V_{GS} up to ±15V and can be used in applications which require operation over the entire 1.8V to 6V range.

Powering Large Capacitive Loads

Electrical subsystems in portable battery-powered equipment are typically bypassed with large filter capacitors to reduce supply transients and supply induced glitching. If not properly powered however, these capacitors may themselves become the source of supply glitching.

For example, if a 100µF capacitor is powered through a switch with a slew rate of 0.1V/µs, the current during start-up is:

$$I_{START} = C(\Delta V/\Delta t)$$
$$= (100 \times 10^{-6})(1 \times 10^{5})$$
$$= 10A$$

Obviously, this is too much current for the regulator (or output capacitor) to supply and the output will glitch by as much as a few volts.

The startup current can be substantially reduced by limiting the slew rate at the gate of an N-channel as shown in Figure 1. The gate drive output of the LTC1163/LTC1165 is passed through a simple RC network, R1 and C1, which substantially slows the slew rate of the MOSFET gate to approximately 1.5×10^{-4}V/µs. Since the MOSFET is operating as a source follower, the slew rate at the source is essentially the same as that at the gate, reducing the startup current to approximately 15mA which is easily

APPLICATIONS INFORMATION

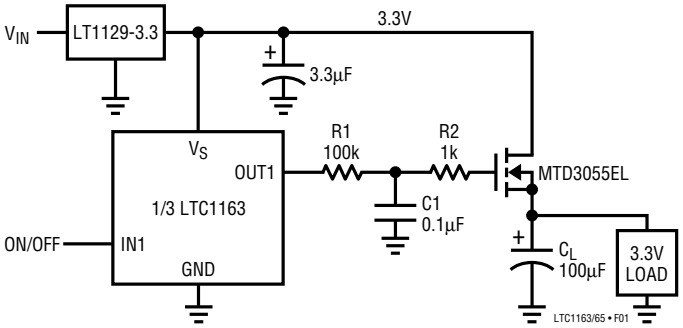


Figure 1. Powering a Large Capacitive Load

managed by the system regulator. R2 is required to eliminate the possibility of parasitic MOSFET oscillations during switch transitions. It is a good practice to isolate the gates of paralleled MOSFETs with 1k resistors to decrease the possibility of interaction between switches.

Mixed 5V/3V Systems

Because the input ESD protection diodes are referenced to ground instead of the supply pin, it is possible to drive the LTC1163/LTC1165 inputs from 5V CMOS or TTL logic even though the LTC1163/LTC1165 are powered from a 3.3V supply as shown in Figure 2. The input threshold voltage is approximately 50% of the supply voltage or 1.6V on a 3.3V supply which is compatible with 5V TTL and CMOS logic. (The LTC1163/LTC1165 cannot however, be driven by 3V logic when powered from a 5V supply because the threshold is approximately 2.5V.)

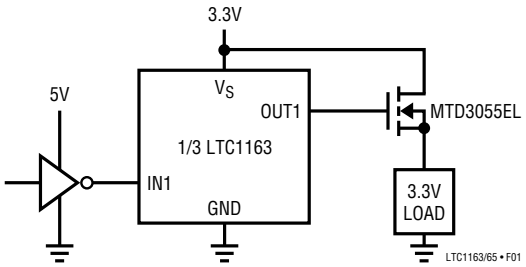


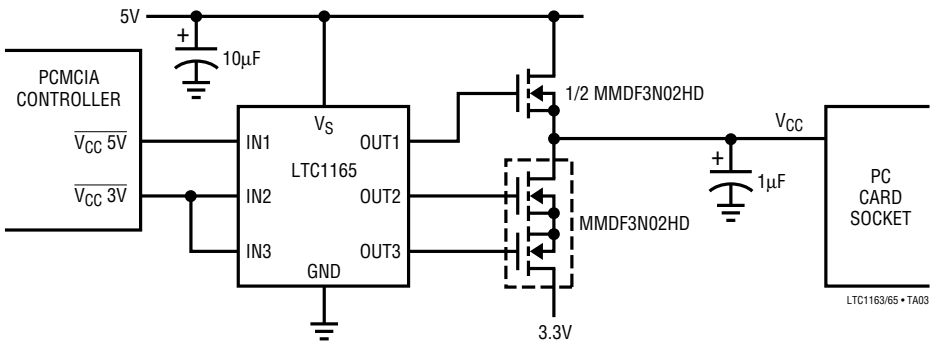
Figure 2. Direct Interface to 5V Logic

Reverse Battery Protection

The LTC1163/LTC1165 can be protected against reverse battery conditions by connecting a 150Ω resistor in series with the ground pin or supply pin. The resistor limits the supply current to less than 24mA with –3.6V applied. Because the LTC1163/LTC1165 draw very little current while in normal operation, the drop across the resistor is minimal. The 3.3V µP (or control logic) can be protected by adding 10k resistors in series with the input pins.

TYPICAL APPLICATIONS

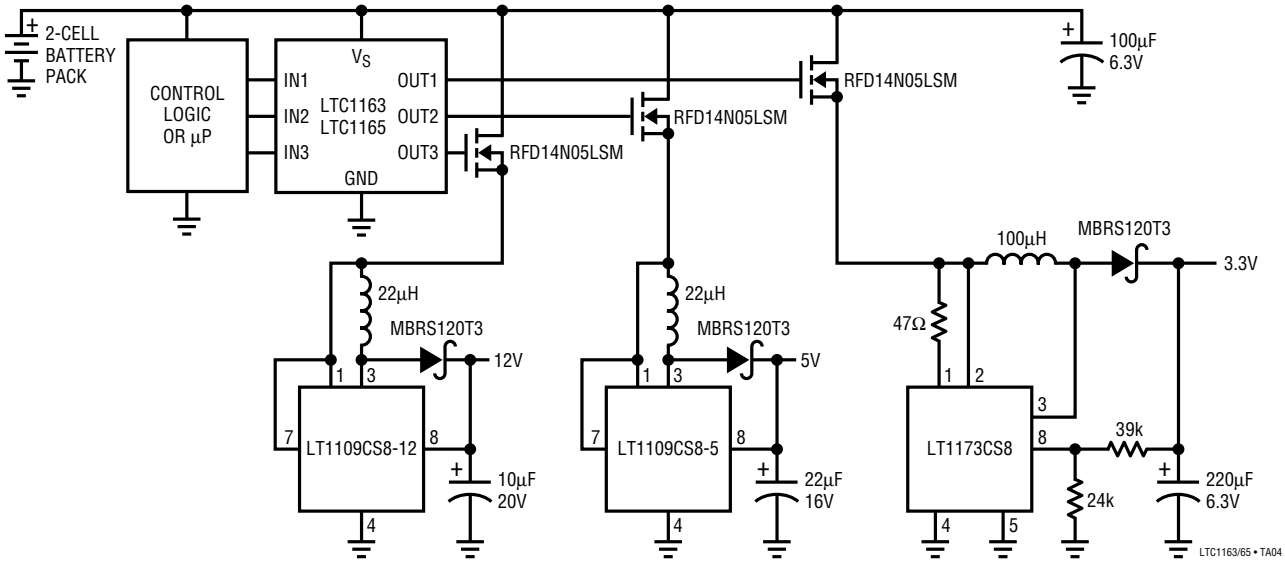
PCMCIA Card 3.3V/5V V_{CC} Switch



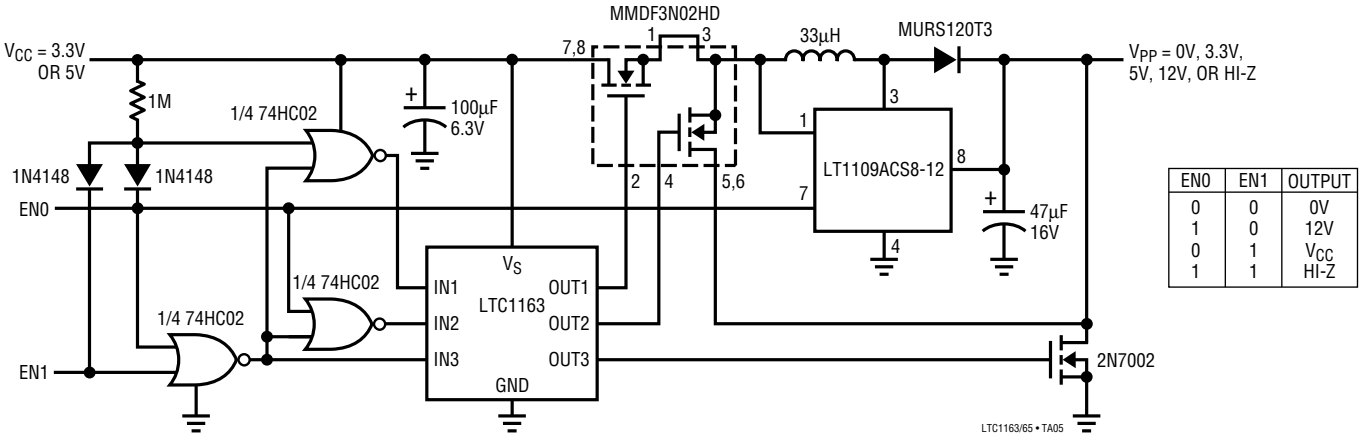
NOTE: USE LTC1163 WITH NONINVERTING PCMCIA CONTROLLERS

TYPICAL APPLICATIONS

2-Cell to 3.3V, 5V and 12V High-Side Switch/Converter with 0.01μA Standby Current

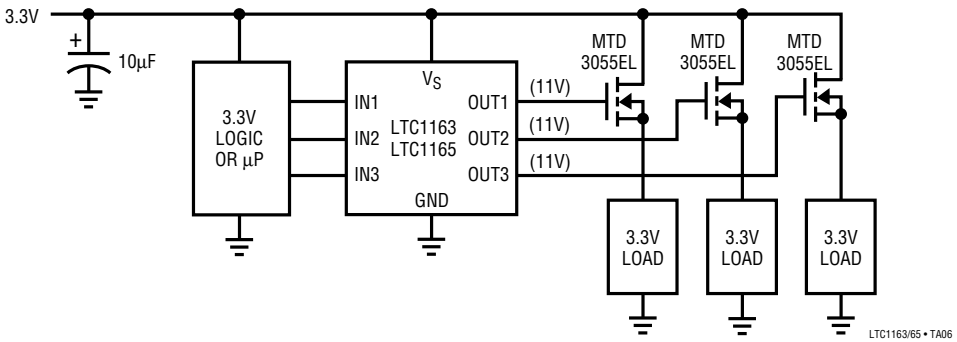


PCMCIA Card Socket V_{PP} Switch/Reglator



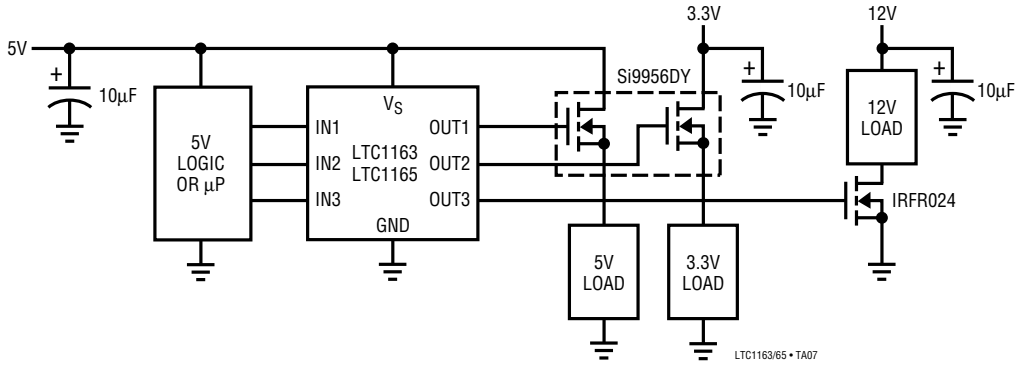
EN0	EN1	OUTPUT
0	0	0V
1	0	12V
0	1	V_{CC}
1	1	HI-Z

Ultra-Low Drop Triple 3.3V High-Side Switch

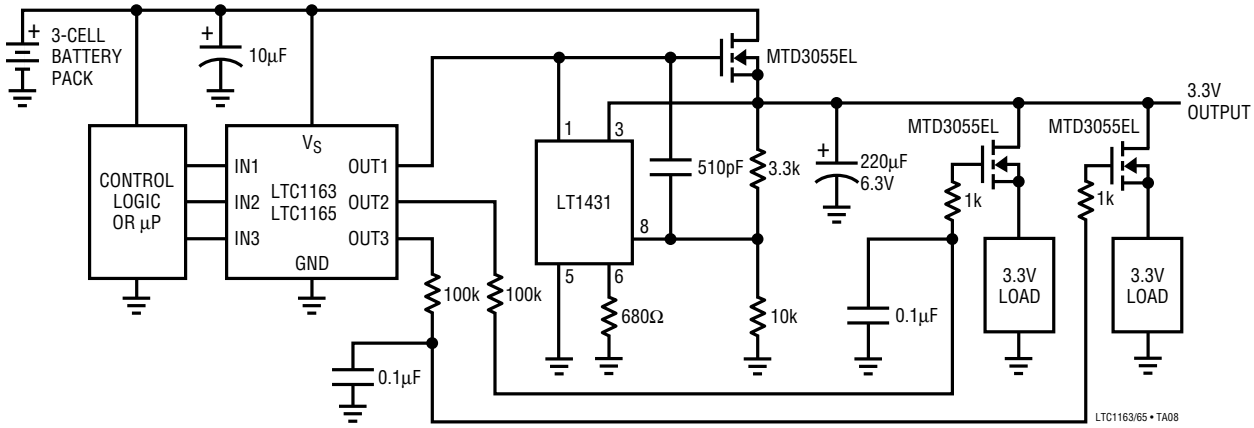


TYPICAL APPLICATIONS

Mixed Voltage High- and Low-Side Switches



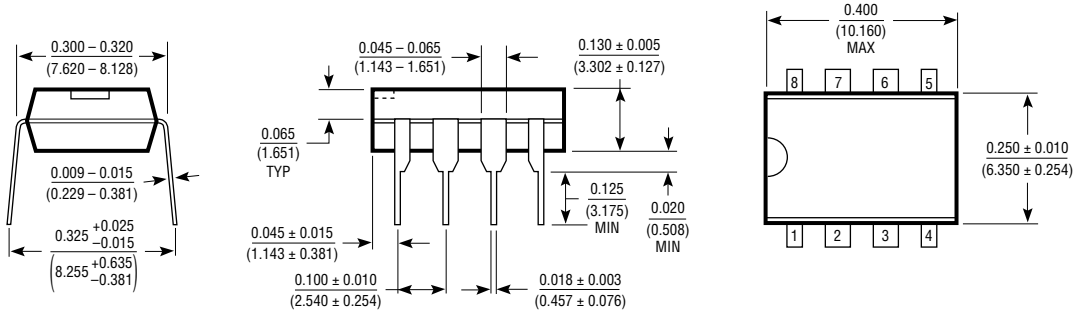
3-Cell to 3.3V Ultra-Low Drop Regulator with 2 Ramped Switches



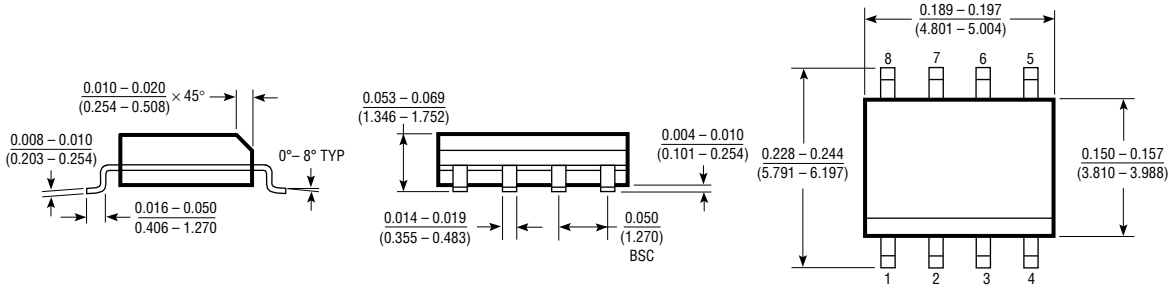
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package 8-Lead Plastic DIP



S8 Package 8-Lead Plastic SOIC



Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

LT/GP 1093 10K REV 0 • PRINTED IN USA