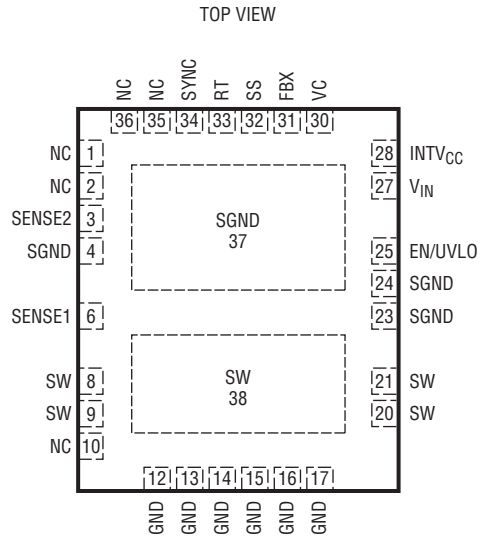
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UVLO (Note 5), SW 40V
$INTV_{CC}$ ..... V_{IN} + 0.3V, 8V
SYNC 8V
VC, SS.....3V
RT 1.5V
SENSE1, SGND ..... Internally Connected to GND
SENSE2.....±0.3V
FBX ..... –6V to 6V
Operating Junction Temperature Range
(Note 2)..... –40°C to 125°C
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UHE PACKAGE
36-LEAD (5mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 42°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 37) IS SGND, MUST BE SOLDERED TO SGND PLANE
EXPOSED PAD (PIN 38) IS SW, MUST BE SOLDERED TO SW PLANE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3957EUHE#PBF	LT3957EUHE#TRPBF	3957	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LT3957IUHE#PBF	LT3957IUHE#TRPBF	3957	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A \approx T_J = 25°C$. V_{IN} = 24V, EN/UVLO = 24V, SENSE2 = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Range			3		40	V
V_{IN} Shutdown I_Q	EN/UVLO = 0V EN/UVLO = 1.15V			0.1	1 6	µA µA
V_{IN} Operating I_Q	VC = 0.3V, R_T = 41.2k			1.7	2.3	mA
V_{IN} Operating I_Q with Internal LDO Disabled	VC = 0.3V, R_T = 41.2k, $INTV_{CC}$ = 5.5V			350	400	µA
SW Pin Current Limit		●	5	5.9	6.8	A
SW Pin On Voltage	I_{SW} = 3A			100		mV
SENSE2 Input Bias Current	Current Out of Pin			–65		µA
Error Amplifier						
FBX Regulation Voltage ($V_{FBX(REG)}$)	FBX > 0V (Note 3) FBX < 0V (Note 3)	● ●	1.569 –0.816	1.6 –0.800	1.631 –0.784	V V
FBX Overvoltage Lockout	FBX > 0V (Note 4) FBX < 0V (Note 4)		6 7	8 11	10 14	% %
FBX Pin Input Current	FBX = 1.6V (Note 3) FBX = –0.8V (Note 3)		 –10	70	100 10	nA nA
Transconductance g_m ($\Delta I_{VC}/\Delta FBX$)	(Note 3)			230		µS
VC Output Impedance	(Note 3)			5		MΩ
V_{FBX} Line Regulation ($\Delta V_{FBX}/[\Delta V_{IN} \bullet V_{FBX(REG)}]$)	FBX > 0V, 3V < V_{IN} < 40V (Notes 3, 6) FBX < 0V, 3V < V_{IN} < 40V (Notes 3, 6)			0.04 0.03	0.06 0.06	%/V %/V
VC Current Mode Gain ($\Delta V_{VC}/\Delta V_{SENSE}$)				10		V/V
VC Source Current	VC = 1.5V, FBX = 0V, Current Out of Pin			–15		µA
VC Sink Current	FBX = 1.7V FBX = –0.85V			12 11		µA µA
Oscillator						
Switching Frequency	R_T = 140k to SGND, FBX = 1.6V, V_C = 1.5V R_T = 41.2k to SGND, FBX = 1.6V, V_C = 1.5V R_T = 10.5k to SGND, FBX = 1.6V, V_C = 1.5V		80 270 850	100 300 1000	120 330 1200	kHz kHz kHz
RT Voltage	FBX = 1.6V			1.2		V
SW Minimum Off-Time				220	275	ns
SW Minimum On-Time				240	320	ns
SYNC Input Low					0.4	
SYNC Input High			1.5			
SS Pull-Up Current	SS = 0V, Current Out of Pin			–10		µA
Low Dropout Regulator						
$INTV_{CC}$ Regulation Voltage		●	5	5.2	5.45	V
$INTV_{CC}$ Undervoltage Lockout Threshold	Falling $INTV_{CC}$ UVLO Hysteresis		2.6	2.7 0.15	2.85	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A \approx T_J = 25°C$. $V_{IN} = 24V$, EN/UVLO = 24V, SENSE2 = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Current Limit	$V_{IN} = 40V$ $V_{IN} = 15V$		32	40 95	55	mA mA
$INTV_{CC}$ Load Regulation ($\Delta V_{INTVCC} / V_{INTVCC}$)	$0 < I_{INTVCC} < 20mA$, $V_{IN} = 8V$		–1	–0.5		%
$INTV_{CC}$ Line Regulation ($\Delta V_{INTVCC} / [\Delta V_{IN} \bullet V_{INTVCC}]$)	$6V < V_{IN} < 40V$			0.02	0.05	%/V
Dropout Voltage ($V_{IN} – V_{INTVCC}$)	$V_{IN} = 5V$, $I_{INTVCC} = 20mA$, VC = 0V			450		mV
$INTV_{CC}$ Current in Shutdown	EN/UVLO = 0V, $INTV_{CC} = 6V$			17		µA
$INTV_{CC}$ Voltage to Bypass Internal LDO					5.5	V
Logic Inputs						
EN/UVLO Threshold Voltage Falling	$V_{IN} = INTV_{CC} = 6V$	●	1.17	1.22	1.27	V
EN/UVLO Voltage Hysteresis				20		mV
EN/UVLO Input Low Voltage	I_{VIN} Drops Below 1µA				0.4	V
EN/UVLO Pin Bias Current Low	EN/UVLO = 1.15V		1.7	2	2.5	µA
EN/UVLO Pin Bias Current High	EN/UVLO = 1.33V			20	100	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3957E is guaranteed to meet performance specifications from the 0°C to 125°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3957I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: The LT3957 is tested in a feedback loop which servos V_{FBX} to the reference voltages (1.6V and –0.8V) with the VC pin forced to 1.3V.

Note 4: FBX overvoltage lockout is measured at $V_{FBX(OVERVOLTAGE)}$ relative to regulated $V_{FBX(REG)}$.

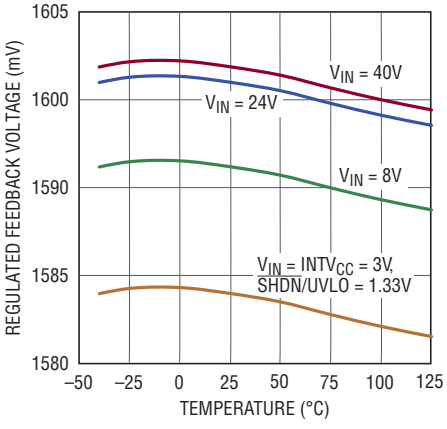
Note 5: For $3V \le V_{IN} < 6V$, the EN/UVLO pin must not exceed V_{IN}.

Note 6: EN/UVLO = 1.33V when $V_{IN} = 3V$.

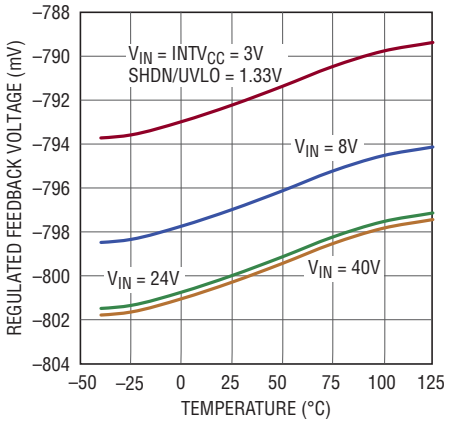
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A \approx T_J = 25°C$, unless otherwise noted.

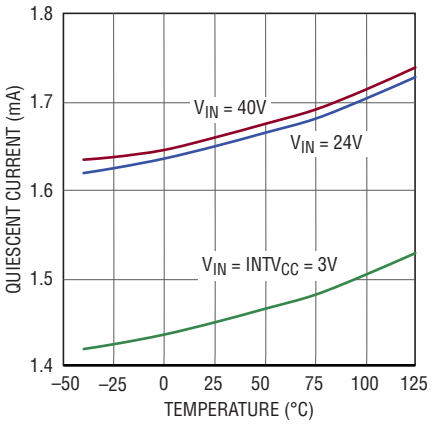
Positive Feedback Voltage vs Temperature, V_{IN}



Negative Feedback Voltage vs Temperature, V_{IN}

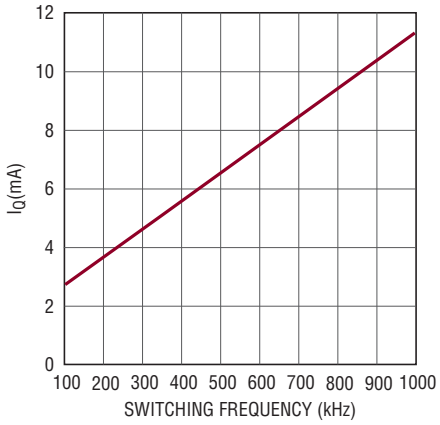


Quiescent Current vs Temperature, V_{IN}

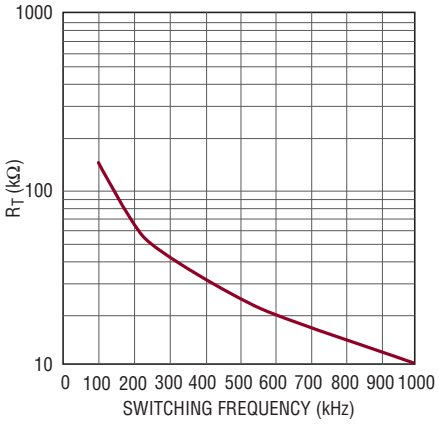


TYPICAL PERFORMANCE CHARACTERISTICS $T_A \approx T_J = 25°C$, unless otherwise noted.

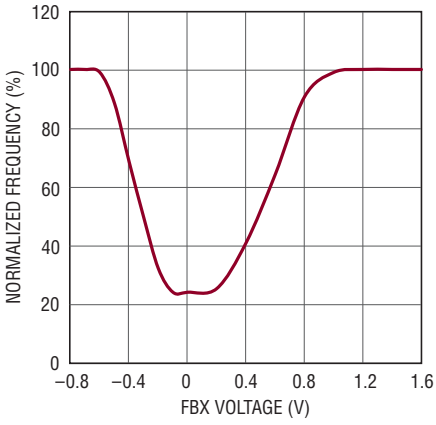
Dynamic Quiescent Current vs Switching Frequency



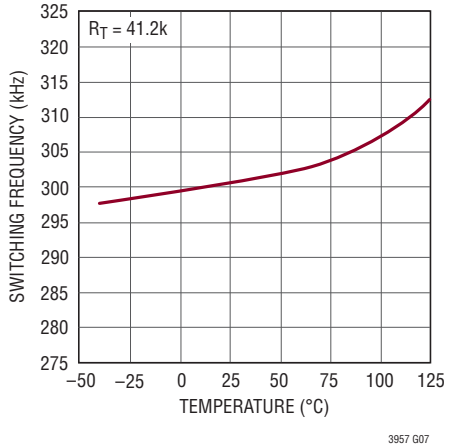
R_T vs Switching Frequency



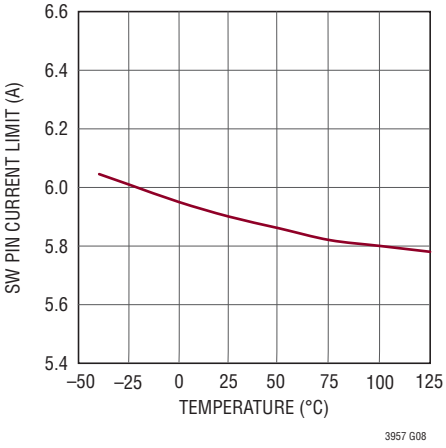
Normalized Switching Frequency vs FBX



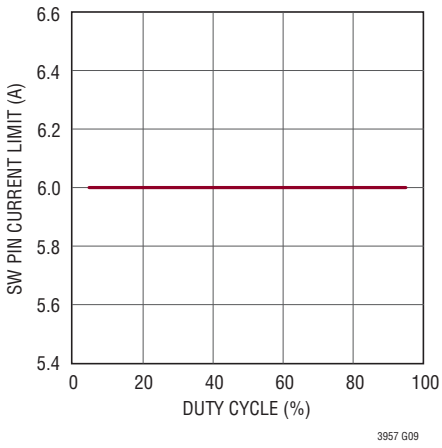
Switching Frequency vs Temperature



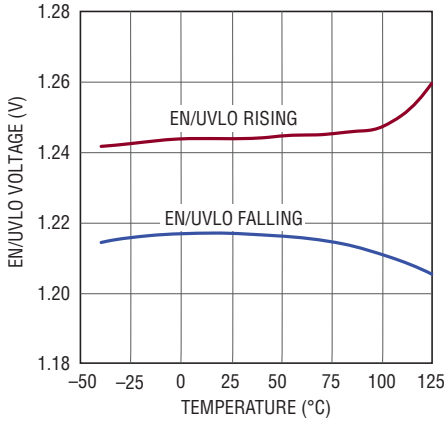
SW Pin Current Limit vs Temperature



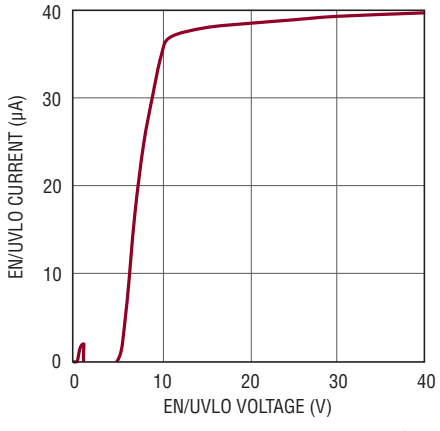
SW Pin Current Limit vs Duty Cycle



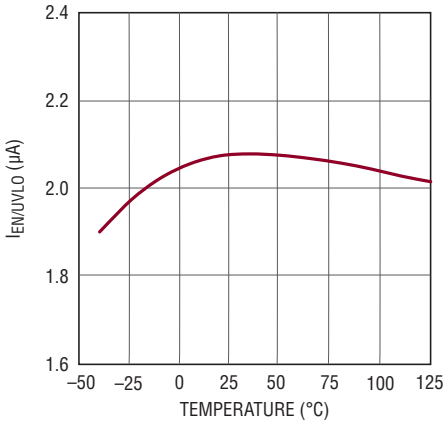
EN/UVLO Threshold vs Temperature



EN/UVLO Current vs Voltage



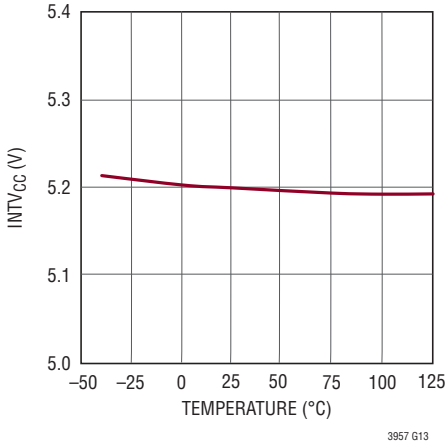
EN/UVLO Hysteresis Current vs Temperature



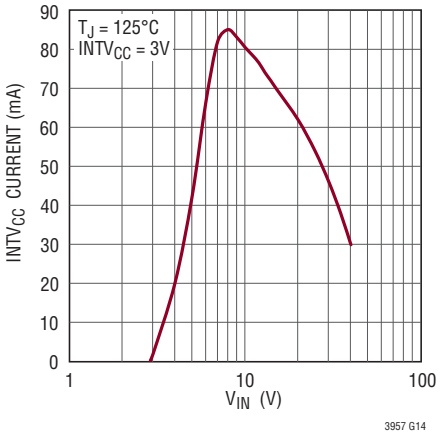
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A \approx T_J = 25°C$, unless otherwise noted.

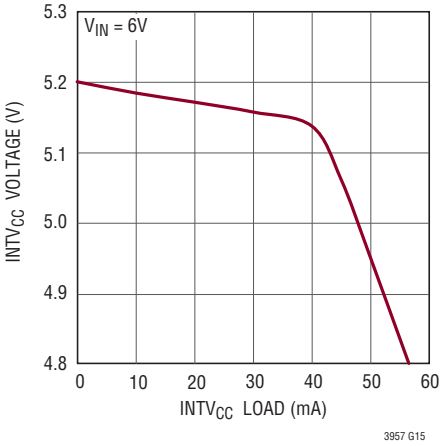
$INTV_{CC}$ vs Temperature



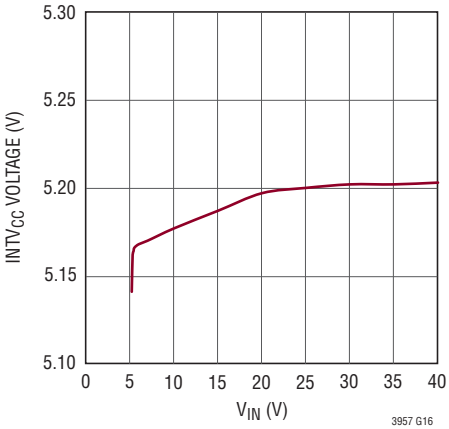
$INTV_{CC}$ Minimum Output Current Limit vs V_{IN}



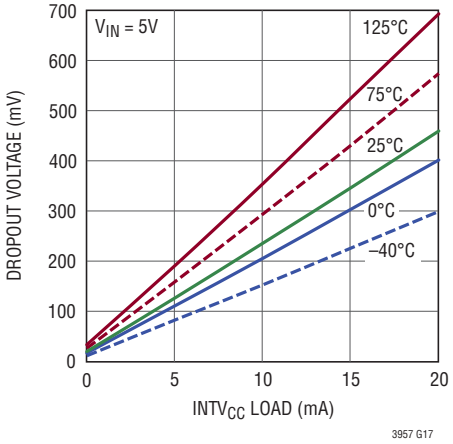
$INTV_{CC}$ Load Regulation



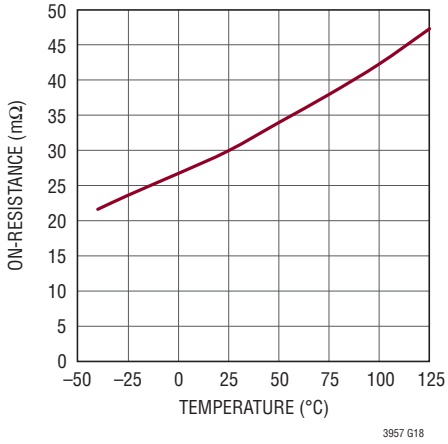
$INTV_{CC}$ Line Regulation



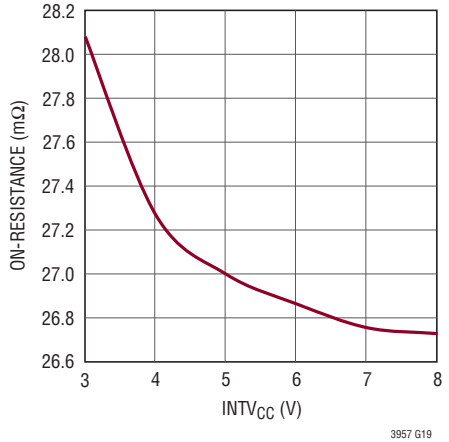
$INTV_{CC}$ Dropout Voltage vs Current, Temperature



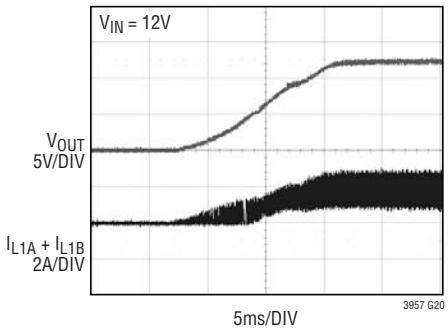
Internal Switch On-Resistance vs Temperature



Internal Switch On-Resistance vs $INTV_{CC}$

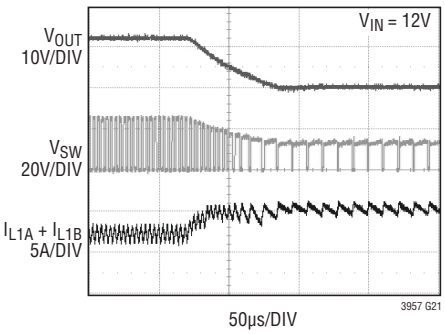


SEPIC Typical Start-Up Waveforms



SEE TYPICAL APPLICATION: 5V TO 16V INPUT, 12V OUTPUT SEPIC CONVERTER

SEPIC FBX Frequency Foldback Waveforms During Overcurrent



SEE TYPICAL APPLICATION: 5V TO 16V INPUT, 12V OUTPUT SEPIC CONVERTER

PIN FUNCTIONS

NC (Pins 1, 2, 10, 35, 36): No Internal Connection. Leave these pins open or connect them to the adjacent pins.

SENSE2 (Pin 3): The Current Sense Input for the Control Loop. Connect this pin to SENSE1 pin directly or through a low pass filter (connect this pin to SENSE1 pin through a resistor, and to SGND through a capacitor).

SGND (Pins 4, 23, 24, Exposed Pad Pin 37): Signal Ground. All small-signal components should connect to this ground. SGND is connected to GND inside the IC to ensure Kelvin connection for the internal switch current sensing. Do not connect SGND and GND externally.

SENSE1 (Pin 6): The Current Sense Output of the Internal N-channel MOSFET. Connect this pin to SENSE2 pin directly or through a low pass filter (connect this pin to SENSE1 pin through a resistor, then connect SENSE2 to SGND through a capacitor).

SW (Pins 8, 9, 20, 21, Exposed Pad Pin 38): Drain of Internal Power N-channel MOSFET.

GND (Pins 12, 13, 14, 15, 16, 17): Ground. These pins connect to the source terminal of internal power N-channel MOSFET through an internal sense resistor. GND is connected to SGND inside the IC to ensure Kelvin connection for the internal switch current sensing. Do not connect GND and SGND externally.

EN/UVLO (Pin 25): Shutdown and Undervoltage Detect Pin. An accurate 1.22V (nominal) falling threshold with externally programmable hysteresis detects when power is okay to enable switching. Rising hysteresis is generated by the external resistor divider and an accurate internal 2µA pull-down current. An undervoltage condition resets soft-start. Tie to 0.4V, or less, to disable the device and reduce V_{IN} quiescent current below 1µA.

V_{IN} (Pin 27): Input Supply Pin. The V_{IN} pin can be locally bypassed with a capacitor to GND (not SGND).

$INTV_{CC}$ (Pin 28): Regulated Supply for Internal Loads and Gate Driver. Supplied from V_{IN} and regulated to 5.2V (typical). $INTV_{CC}$ must be bypassed to SGND with a minimum of 4.7µF capacitor placed close to pin. $INTV_{CC}$ can be connected directly to V_{IN}, if V_{IN} is less than 8V. $INTV_{CC}$ can also be connected to a power supply whose voltage is higher than 5.5V, and lower than V_{IN}, provided that supply does not exceed 8V.

VC (Pin 30): Error Amplifier Compensation Pin. Used to stabilize the voltage loop with an external RC network. Place compensation components between the VC pin and SGND.

FBX (Pin 31): Positive and Negative Feedback Pin. Receives the feedback voltage from the external resistor divider between the output and SGND. Also modulates the switching frequency during start-up and fault conditions when FBX is close to SGND.

SS (Pin 32): Soft-Start Pin. This pin modulates compensation pin voltage (VC) clamp. The soft-start interval is set with an external capacitor between SS pin and SGND. The pin has a 10µA (typical) pull-up current source to an internal 2.5V rail. The soft-start pin is reset to SGND by an undervoltage condition at EN/UVLO, an $INTV_{CC}$ undervoltage or overvoltage condition or an internal thermal lockout.

RT (Pin 33): Switching Frequency Adjustment Pin. Set the frequency using a resistor to SGND. Do not leave this pin open.

SYNC (Pin 34): Frequency Synchronization Pin. Used to synchronize the switching frequency to an outside clock. If this feature is used, an R_T resistor should be chosen to program a switching frequency 20% slower than the SYNC pulse frequency. Tie the SYNC pin to SGND if this feature is not used. SYNC is bypassed when FBX is close to SGND.

BLOCK DIAGRAM

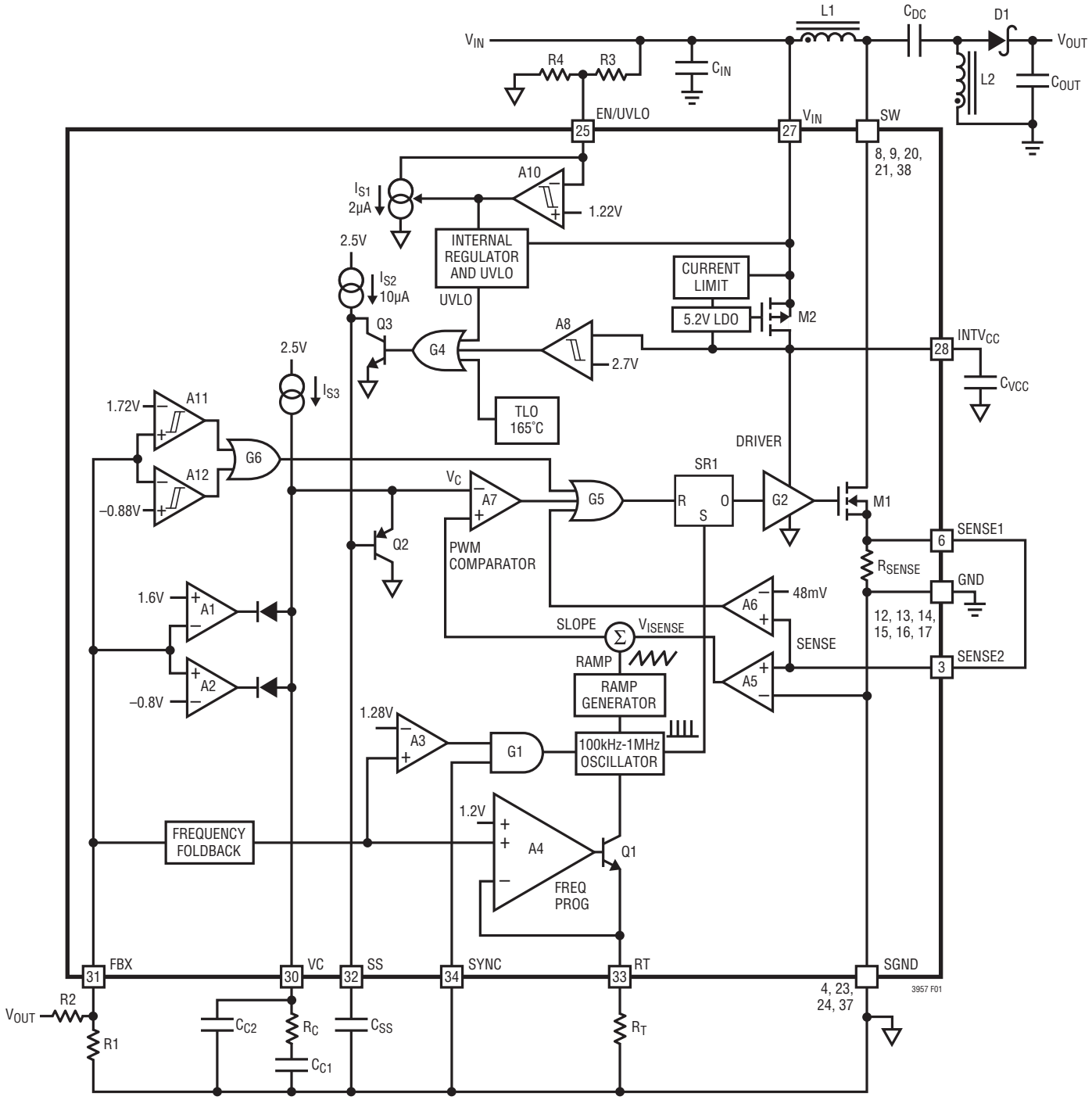


Figure 1. LT3957 Block Diagram Working as a SEPIC Converter

APPLICATIONS INFORMATION

Main Control Loop

The LT3957 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram in Figure 1.

The start of each oscillator cycle sets the SR latch (SR1) and turns on the internal power MOSFET switch M1 through driver G2. The switch current flows through the internal current sensing resistor R_{SENSE} and generates a voltage proportional to the switch current. This current sense voltage V_{ISENSE} (amplified by A5) is added to a stabilizing slope compensation ramp and the resulting sum (SLOPE) is fed into the positive terminal of the PWM comparator A7. When SLOPE exceeds the level at the negative input of A7 (VC pin), SR1 is reset, turning off the power switch. The level at the negative input of A7 is set by the error amplifier A1 (or A2) and is an amplified version of the difference between the feedback voltage (FBX pin) and the reference voltage (1.6V or –0.8V, depending on the configuration). In this manner, the error amplifier sets the correct peak switch current level to keep the output in regulation.

The LT3957 has a switch current limit function. The current sense voltage is input to the current limit comparator A6. If the SENSE2 pin voltage is higher than the sense current limit threshold $V_{SENSE(MAX)}$ (48mV, typical), A6 will reset SR1 and turn off M1 immediately.

The LT3957 is capable of generating either positive or negative output voltage with a single FBX pin. It can be configured as a boost, flyback or SEPIC converter to generate positive output voltage, or as an inverting converter to generate negative output voltage. When configured as a SEPIC converter, as shown in Figure 1, the FBX pin is pulled up to the internal bias voltage of 1.6V by a voltage divider (R1 and R2) connected from V_{OUT} to SGND. Comparator A2 becomes inactive and comparator A1 performs the inverting amplification from FBX to VC. When the LT3957 is in an inverting configuration, the FBX pin is pulled down to –0.8V by a voltage divider connected from V_{OUT} to SGND. Comparator A1 becomes inactive and comparator A2 performs the noninverting amplification from FBX to VC.

The LT3957 has overvoltage protection functions to protect the converter from excessive output voltage overshoot during start-up or recovery from a short-circuit condition. An overvoltage comparator A11 (with 20mV hysteresis) senses when the FBX pin voltage exceeds the positive regulated voltage (1.6V) by 8% and provides a reset pulse. Similarly, an overvoltage comparator A12 (with 10mV hysteresis) senses when the FBX pin voltage exceeds the negative regulated voltage (–0.8V) by 11% and provides a reset pulse. Both reset pulses are sent to the main RS latch (SR1) through G6 and G5. The power MOSFET switch M1 is actively held off for the duration of an output overvoltage condition.

Programming Turn-On and Turn-Off Thresholds with the EN/UVLO Pin

The EN/UVLO pin controls whether the LT3957 is enabled or is in shutdown state. A micropower 1.22V reference, a comparator A10 and a controllable current source I_{S1} allow the user to accurately program the supply voltage at which the IC turns on and off. The falling value can be accurately set by the resistor dividers R3 and R4. When EN/UVLO is above 0.4V, and below the 1.22V threshold, the small pull-down current source I_{S1} (typical 2µA) is active.

The purpose of this current is to allow the user to program the rising hysteresis. The Block Diagram of the comparator and the external resistors is shown in Figure 1. The typical falling threshold voltage and rising threshold voltage can be calculated by the following equations:

$$V_{VIN,FALLING} = 1.22 \bullet \frac{(R3+R4)}{R4}$$

$$V_{VIN,RISING} = 2\mu A \bullet R3 + V_{IN,FALLING}$$

For applications where the EN/UVLO pin is only used as a logic input, the EN/UVLO pin can be connected directly to the input voltage V_{IN} for always-on operation.

APPLICATIONS INFORMATION

$INTV_{CC}$ Regulator Bypassing and Operation

An internal, low dropout (LDO) voltage regulator produces the 5.2V $INTV_{CC}$ supply which powers the gate driver, as shown in Figure 1. The LT3957 contains an undervoltage lockout comparator A8 for the $INTV_{CC}$ supply. The $INTV_{CC}$ undervoltage (UV) threshold is 2.7V (typical), with 0.1V hysteresis, to ensure that the internal MOSFET has sufficient gate drive voltage before turning on. When $INTV_{CC}$ is below the UV threshold, the internal power switch will be turned off and the soft-start operation will be triggered. The logic circuitry within the LT3957 is also powered from the internal $INTV_{CC}$ supply.

The $INTV_{CC}$ regulator must be bypassed to SGND immediately adjacent to the IC pins with a minimum of 4.7µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

In an actual application, most of the IC supply current is used to drive the gate capacitance of the internal power MOSFET. The on-chip power dissipation can be significant when the internal power MOSFET is being driven at a high frequency and the V_{IN} voltage is high.

An effective approach to reduce the power consumption of the internal LDO for gate drive and to improve the efficiency is to tie the $INTV_{CC}$ pin to an external voltage source high enough to turn off the internal LDO regulator.

In SEPIC or flyback applications, the $INTV_{CC}$ pin can be connected to the output voltage V_{OUT} through a blocking diode, as shown in Figure 2, if V_{OUT} meets the following conditions:

1. $V_{OUT} < V_{IN}$ (pin voltage)
2. $V_{OUT} < 8V$

A resistor R_{VCC} can be connected, as shown in Figure 2, to limit the inrush current from V_{OUT}. Regardless of whether or not the $INTV_{CC}$ pin is connected to an external voltage source, it is always necessary to have the driver circuitry bypassed with a 4.7µF low ESR ceramic capacitor to ground immediately adjacent to the $INTV_{CC}$ and SGND pins.

If LT3957 operates at a low V_{IN} and high switching frequency, the voltage drop across the drain and the source of the LDO PMOS (M2 in Figure 1) could push $INTV_{CC}$ to be below the UV threshold. To prevent this from happening, the $INTV_{CC}$ pin can be shorted directly to the V_{IN} pin. V_{IN} must not exceed the $INTV_{CC}$ Absolute Maximum Rating (8V). In this condition, the internal LDO will be turned off and the gate driver will be powered directly from V_{IN}. It is recommended that $INTV_{CC}$ pin be shorted to the V_{IN} pin if V_{IN} is lower than 3.5V at 1MHz switching frequency, or V_{IN} is lower than 3.2V at 100kHz switching frequency. With the $INTV_{CC}$ pin shorted to V_{IN}, however, a small current (around 16µA) will load the $INTV_{CC}$ in shutdown mode.

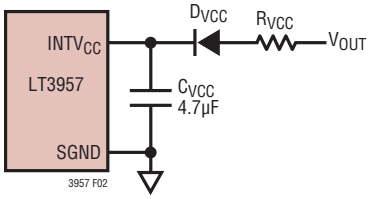


Figure 2. Connecting $INTV_{CC}$ to V_{OUT}

APPLICATIONS INFORMATION

Operating Frequency and Synchronization

The choice of operating frequency may be determined by on-chip power dissipation (a low switching frequency may be required to ensure IC junction temperature does not exceed 125°C), otherwise it is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing gate drive current and MOSFET and diode switching losses. However, lower frequency operation requires a physically larger inductor. Switching frequency also has implications for loop compensation. The LT3957 uses a constant-frequency architecture that can be programmed over a 100kHz to 1000kHz range with a single external resistor from the RT pin to SGND, as shown in Figure 1. A table for selecting the value of R_T for a given operating frequency is shown in Table 1.

Table 1. Timing Resistor (R_T) Value

SWITCHING FREQUENCY (kHz)	R_T (kΩ)
100	140
200	63.4
300	41.2
400	30.9
500	24.3
600	19.6
700	16.5
800	14
900	12.1
1000	10.5

The operating frequency of the LT3957 can be synchronized to an external clock source. By providing a digital clock signal into the SYNC pin, the LT3957 will operate at the SYNC clock frequency. The LT3957 detects the rising edge of each clock cycle. If this feature is used, an R_T resistor should be chosen to program a switching frequency 20% slower than SYNC pulse frequency. It is recommended that the SYNC pin has a minimum pulse width of 200ns. Tie the SYNC pin to SGND if this feature is not used.

Duty Cycle Consideration

Switching duty cycle is a key variable defining converter operation. As such, its limits must be considered. Minimum on-time is the smallest time duration that the LT3957 is capable of turning on the power MOSFET. This time is typically about 240ns (see Minimum On-Time in the Electrical Characteristics table). In each switching cycle, the LT3957 keeps the power switch off for at least 220ns (typical) (see Minimum Off-Time in the Electrical Characteristics table).

The minimum on-time, minimum off-time and the switching frequency define the minimum and maximum switching duty cycles a converter is able to generate:

Minimum duty cycle = minimum on-time • frequency

Maximum duty cycle = 1 – (minimum off-time • frequency)

Programming the Output Voltage

The output voltage V_{OUT} is set by a resistor divider, as shown in Figure 1. The positive and negative V_{OUT} are set by the following equations:

$$V_{OUT,POSITIVE} = 1.6V \bullet \left(1 + \frac{R2}{R1}\right)$$

$$V_{OUT,NEGATIVE} = -0.8V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistors R1 and R2 are typically chosen so that the error caused by the current flowing into the FBX pin during normal operation is less than 1% (this translates to a maximum value of R1 at about 158k).

APPLICATIONS INFORMATION

Soft-Start

The LT3957 contains several features to limit peak switch currents and output voltage (V_{OUT}) overshoot during start-up or recovery from a fault condition. The primary purpose of these features is to prevent damage to external components or the load.

High peak switch currents during start-up may occur in switching regulators. Since V_{OUT} is far from its final value, the feedback loop is saturated and the regulator tries to charge the output capacitor as quickly as possible, resulting in large peak currents. A large surge current may cause inductor saturation or power switch failure.

The LT3957 addresses this mechanism with the SS pin. As shown in Figure 1, the SS pin reduces the power MOSFET current by pulling down the VC pin through Q2. In this way the SS allows the output capacitor to charge gradually toward its final value while limiting the start-up peak currents. The typical start-up waveforms are shown in the Typical Performance Characteristics section. The inductor current I_L slewing rate is limited by the soft-start function.

Besides start-up (with EN/UVLO), soft-start can also be triggered by the following faults:

1. $INTV_{CC} < 2.85V$
2. Thermal lockout (TLO > 165°C)

Any of these three faults will cause the LT3957 to stop switching immediately. The SS pin will be discharged by Q3. When all faults are cleared and the SS pin has been discharged below 0.2V, a 10µA current source I_{S2} starts charging the SS pin, initiating a soft-start operation.

The soft-start interval is set by the soft-start capacitor selection according to the equation:

$$T_{SS} = C_{SS} \bullet \frac{1.25V}{10\mu A}$$

FBX Frequency Foldback

When V_{OUT} is very low during start-up, or an output short-circuit on a SEPIC, an inverting, or a flyback converter, the switching regulator must operate at low duty cycles to keep the power switch current below the current limit, since the inductor current decay rate is very low during switch off time. The minimum on-time limitation may prevent the switcher from attaining a sufficiently low duty cycle at the programmed switching frequency. So, the switch current may keep increasing through each switch cycle, exceeding the programmed current limit. To prevent the switch peak currents from exceeding the programmed value, the LT3957 contains a frequency foldback function to reduce the switching frequency when the FBX voltage is low (see the *Normalized Switching Frequency vs FBX* graph in the Typical Performance Characteristics section).

During frequency foldback, external clock synchronization is disabled to prevent interference with frequency reducing operation.

Loop Compensation

Loop compensation determines the stability and transient performance. The LT3957 uses current mode control to regulate the output which simplifies loop compensation. The optimum values depend on the converter topology, the component values and the operating conditions (including the input voltage, load current, etc.). To compensate the feedback loop of the LT3957, a series resistor-capacitor network is usually connected from the VC pin to SGND. Figure 1 shows the typical VC compensation network. For most applications, the capacitor should be in the range of 470pF to 22nF, and the resistor should be in the range of 5k to 50k. A small capacitor is often connected in parallel with the RC compensation network to attenuate the VC voltage ripple induced from the output voltage ripple through the internal error amplifier. The parallel capacitor usually ranges in value from 10pF to 100pF. A practical approach to design the compensation network is to start with one of the circuits in this data sheet that is similar to your application, and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. Application Note 76 is a good reference on loop compensation.

APPLICATIONS INFORMATION

The Internal Power Switch Current

For control and protection, the LT3957 measures the internal power MOSFET current by using a sense resistor (R_{SENSE}) between GND and the MOSFET source. Figure 3 shows a typical waveform of the internal switch current (I_{SW}).

Due to the current limit (minimum 5A) of the internal power switch, the LT3957 should be used in the applications that the switch peak current $I_{SW(PEAK)}$ during steady state normal operation is lower than 5A by a sufficient margin (10% or higher is recommended).

The LT3957 switching controller incorporates 100ns timing interval to blank the ringing on the current sense signal across R_{SENSE} immediately after M1 is turned on. This ringing is caused by the parasitic inductance and capacitance of the PCB trace, the sense resistor, the diode, and the MOSFET. The 100ns timing interval is adequate for most of the LT3957 applications. In the applications that have very large and long ringing on the current sense signal, a small RC filter can be added to filter out the excess ringing. Figure 4 shows the RC filter on the SENSE1 and SENSE2 pins. It is usually sufficient to choose 22Ω for R_{FLT} and 2.2nF to 10nF for C_{FLT}. Keep R_{FLT}'s resistance low. Remember that there is 65µA (typical) flowing out of the SENSE2 pin. Adding R_{FLT} will affect the internal power switch current limit threshold:

$$I_{SW\_ILIM} = \left(1 - \frac{65\mu A \bullet R_{FLT}}{48mV}\right) \bullet 5A$$

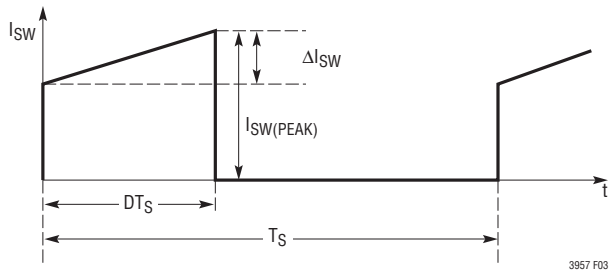


Figure 3. The Switch Current During a Switching Cycle

On-Chip Power Dissipation and Thermal Lockout (TLO)

The on-chip power dissipation of LT3957 can be estimated using the following equation:

$$P_{IC} \approx I^2_{SW} \bullet D \bullet R_{DS(ON)} + V^2_{PEAK} \bullet I_{SW} \bullet f \bullet 200pF/A + V_{IN} \bullet (1.6mA + f \bullet 10nC)$$

where $R_{DS(ON)}$ is the internal switch on-resistance which can be obtained from the Typical Performance Characteristics section. $V_{SW(PEAK)}$ is the peak switch off-state voltage. The maximum power dissipation $P_{IC(MAX)}$ can be obtained by comparing P_{IC} across all the V_{IN} range at the maximum output current . The highest junction temperature can be estimated using the following equation:

$$T_{J(MAX)} \approx T_A + P_{IC(MAX)} \bullet 42°C/W$$

It is recommended to measure the IC temperature in steady state to verify that the junction temperature limit is not exceeded. A low switching frequency may be required to ensure $T_{J(MAX)}$ does not exceed 125°C.

If LT3957 die temperature reaches thermal lockout threshold at 165°C (typical), the IC will initiate several protective actions. The power switch will be turned off. A soft-start operation will be triggered. The IC will be enabled again when the junction temperature has dropped by 5°C (nominal).

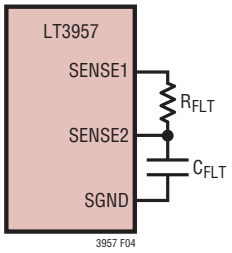


Figure 4. The RC Filter on SENSE1 Pin and SENSE2 Pin

APPLICATIONS INFORMATION

APPLICATION CIRCUITS

The LT3957 can be configured as different topologies. The first topology to be analyzed will be the boost converter, followed by the flyback, SEPIC and inverting converters.

Boost Converter: Switch Duty Cycle and Frequency

The LT3957 can be configured as a boost converter for the applications where the converter output voltage is higher than the input voltage. Remember that boost converters are not short-circuit protected. Under a shorted output condition, the inductor current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, please refer to the Applications Information section covering SEPIC converters.

The conversion ratio as a function of duty cycle is

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

in continuous conduction mode (CCM).

For a boost converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}) and the input voltage (V_{IN}). The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

Discontinuous conduction mode (DCM) provides higher conversion ratios at a given frequency at the cost of reduced efficiencies and higher switching currents.

Boost Converter: Maximum Output Current Capability and Inductor Selection

For the boost topology, the maximum average inductor current is:

$$I_{L(MAX)} = I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

Due to the current limit of its internal power switch, the LT3957 should be used in a boost converter whose maximum output current ($I_{O(MAX)}$) is less than the maximum output current capability by a sufficient margin (10% or higher is recommended):

$$I_{O(MAX)} < \frac{V_{IN(MIN)}}{V_{OUT}} \bullet \left(5A - 0.5 \bullet \Delta I_{SW}\right)$$

The inductor ripple current ΔI_{SW} has a direct effect on the choice of the inductor value and the converter's maximum output current capability. Choosing smaller values of ΔI_{SW} increases output current capability, but requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_{SW} provides fast transient response and allows the use of low inductances, but results in higher input current ripple and greater core losses, and reduces output current capability.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value of the boost converter can be determined using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f} \bullet D_{MAX}$$

The peak inductor current is the switch current limit (5.9A typical), and the RMS inductor current is approximately equal to $I_{L(MAX)}$. The user should choose the inductors having sufficient saturation and RMS current ratings.

Boost Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is desirable. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage plus any additional ringing across its anode-to-cathode during the on-time. The average forward current in normal operation is equal to the output current.

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than V_{OUT} by a safety margin (a 10V safety margin is usually sufficient).

APPLICATIONS INFORMATION

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

where V_D is diode's forward voltage drop, and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ to be used in this equation normally includes the $R_{\theta JC}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

Boost Converter: Output Capacitor Selection

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct output capacitors for a given output ripple voltage. The effect of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform for a typical boost converter is illustrated in Figure 5.

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step ΔV_{ESR} and the charging/discharging ΔV_{COUT}. For the purpose of simplicity, we will choose 2% for the maximum output ripple, to be divided equally between ΔV_{ESR} and ΔV_{COUT}. This percentage ripple will change, depending on the requirements of the application, and the following equations can easily be modified. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \le \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}}$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} \ge \frac{I_{O(MAX)}}{0.01 \bullet V_{OUT} \bullet f}$$

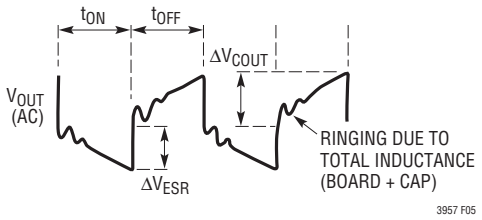


Figure 5. The Output Ripple Waveform of a Boost Converter

The output capacitor in a boost regulator experiences high RMS ripple currents, as shown in Figure 5. The RMS ripple current rating of the output capacitor can be determined using the following equation:

$$I_{RMS(COUT)} \ge I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

Multiple capacitors are often paralleled to meet ESR requirements. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the required RMS current rating. Additional ceramic capacitors in parallel are commonly used to reduce the effect of parasitic inductance in the output capacitor, which reduces high frequency switching noise on the converter output.

Boost Converter: Input Capacitor Selection

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input, and the input current waveform is continuous. The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 1µF to 100µF. A low ESR capacitor is recommended, although it is not as critical as for the output capacitor.

The RMS input capacitor ripple current for a boost converter is:

$$I_{RMS(CIN)} = 0.3 \bullet \Delta I_L$$

APPLICATIONS INFORMATION

FLYBACK CONVERTER APPLICATIONS

The LT3957 can be configured as a flyback converter for the applications where the converters have multiple outputs, high output voltages or isolated outputs. Due to the 40V rating of the internal power switch, LT3797 should be used in low input voltage flyback converters. Figure 6 shows a simplified flyback converter.

The flyback converter has a very low parts count for multiple outputs, and with prudent selection of turns ratio, can have high output/input voltage conversion ratios with a desirable duty cycle. However, it has low efficiency due to the high peak currents, high peak voltages and consequent power loss. The flyback converter is commonly used for an output power of less than 50W.

The flyback converter can be designed to operate either in continuous or discontinuous mode. Compared to continuous mode, discontinuous mode has the advantage of smaller transformer inductances and easy loop compensation, and the disadvantage of higher peak-to-average current and lower efficiency.

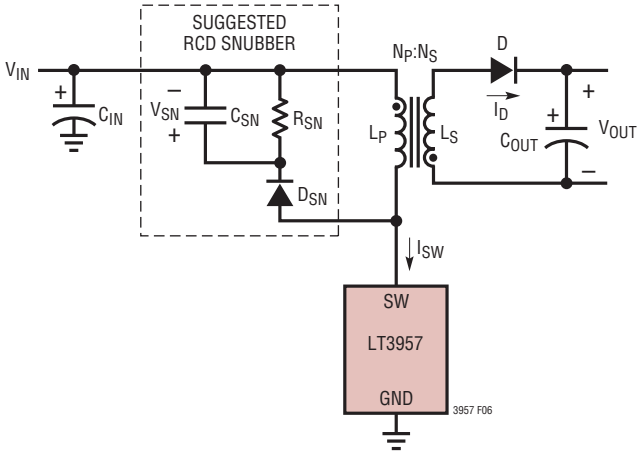


Figure 6. A Simplified Flyback Converter

Flyback Converter: Switch Duty Cycle and Turns Ratio

The flyback converter conversion ratio in the continuous mode operation is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \bullet \frac{D}{1-D}$$

where N_S/N_P is the second to primary turns ratio. D is duty cycle.

Figure 7 shows the waveforms of the flyback converter in discontinuous mode operation. During each switching period T_S, three subintervals occur: DT_S, $D2T_S$, $D3T_S$. During DT_S, M is on, and D is reverse-biased. During $D2T_S$, M is off, and L_S is conducting current. Both L_P and L_S currents are zero during $D3T_S$.

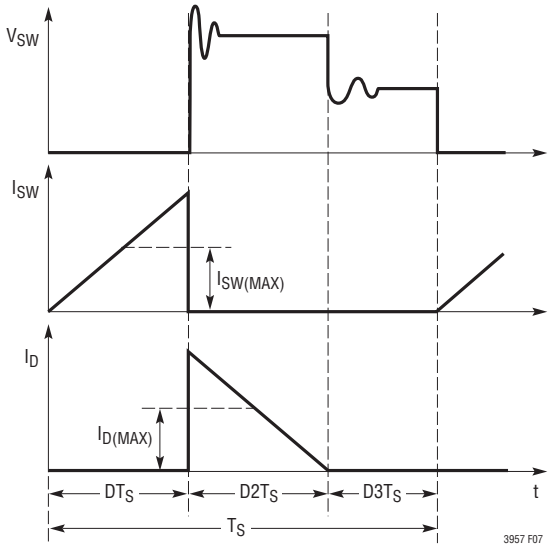


Figure 7. Waveforms of the Flyback Converter in Discontinuous Mode Operation

The flyback converter conversion ratio in the discontinuous mode operation is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \bullet \frac{D}{D2}$$

According to Figure 6, the peak SW voltage is:

$$V_{SW(PEAK)} = V_{IN(MAX)} + V_{SN}$$

where V_{SN} is the snubber capacitor voltage. A smaller V_{SN} results in a larger snubber loss. A reasonable V_{SN} is 1.5 to 2 times of the reflected output voltage:

$$V_{SN} = k \bullet \frac{V_{OUT} \bullet N_P}{N_S}$$

$$k = 1.5 \sim 2$$

APPLICATIONS INFORMATION

According to the Absolute Maximum Ratings table, the SW voltage Absolute Maximum value is 40V. Therefore, the maximum primary to secondary turns ratio (for both the continuous and the discontinuous operation) should be.

$$\frac{N_P}{N_S} \leq \frac{40V - V_{IN(MAX)}}{k \bullet V_{OUT}}$$

According to the preceding equations, the user has relative freedom in selecting the switch duty cycle or turns ratio to suit a given application. The selections of the duty cycle and the turns ratio are somewhat iterative processes, due to the number of variables involved. The user can choose either a duty cycle or a turns ratio as the start point. The following trade-offs should be considered when selecting the switch duty cycle or turns ratio, to optimize the converter performance. A higher duty cycle affects the flyback converter in the following aspects:

- Lower MOSFET RMS current $I_{SW(RMS)}$, but higher MOSFET V_{SW} peak voltage
- Lower diode peak reverse voltage, but higher diode RMS current $I_{D(RMS)}$
- Higher transformer turns ratio (N_P/N_S)

It is recommended to choose a duty cycle between 20% and 80%.

Flyback Converter: Maximum Output Current Capability and Transformer Design

The maximum output current capability and transformer design for continuous conduction mode (CCM) is chosen as presented here.

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum V_{IN}:

$$D_{MAX} = \frac{V_{OUT} \bullet \left(\frac{N_P}{N_S}\right)}{V_{OUT} \bullet \left(\frac{N_P}{N_S}\right) + V_{IN(MIN)}}$$

Due to the current limit of its internal power switch, the LT3957 should be used in a flyback converter whose maximum output current ($I_{O(MAX)}$) is less than the maximum output current capability by a sufficient margin (10% or higher is recommended):

$$I_{O(MAX)} < \frac{V_{IN(MIN)}}{V_{OUT}} \bullet D_{MAX} \bullet \left(5A - 0.5 \bullet \Delta I_{SW}\right)$$

The transformer ripple current ΔI_{SW} has a direct effect on the design/choice of the transformer and the converter's output current capability. Choosing smaller values of ΔI_{SW} increases the output current capability, but requires large primary and secondary inductances and reduce the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_{SW} allows the use of low primary and secondary inductances, but results in higher input current ripple, greater core losses, and reduces the output current capability.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the primary winding, the primary winding inductance can be calculated using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f} \bullet D_{MAX}$$

The primary winding peak current is the switch current limit (typical 5.9A). The primary and secondary maximum RMS currents are:

$$I_{LP(RMS)} \approx \frac{P_{OUT(MAX)}}{D_{MAX} \bullet V_{IN(MIN)} \bullet \eta}$$

$$I_{LS(RMS)} \approx \frac{I_{OUT(MAX)}}{1 - D_{MAX}}$$

where η is the converter efficiency.

Based on the preceding equations, the user should design/choose the transformer having sufficient saturation and RMS current ratings.

Flyback Converter: Snubber Design

Transformer leakage inductance (on either the primary or secondary) causes a voltage spike to occur after the MOSFET turn-off. This is increasingly prominent at higher load currents, where more stored energy must be dissipated.

APPLICATIONS INFORMATION

In some cases a snubber circuit will be required to avoid overvoltage breakdown at the MOSFET's drain node. There are different snubber circuits (such as RC snubber, RCD snubber, Zener clamp, etc.), and Application Note 19 is a good reference on snubber design. An RC snubber circuit can be connected between SW and GND to damp the ringing on SW pins. The snubber resistor values should be close to the impedance of the parasitic resonance. The snubber capacitor value should be larger than the circuit parasitic capacitance, but be small enough to keep the snubber resistor power dissipation low.

If the RC snubber is insufficient to prevent SW pins overvoltage, the RCD snubber can be used to limit the peak voltage on the SW pins, which is shown in Figure 6.

The snubber resistor value (R_{SN}) can be calculated by the following equation:

$$R_{SN} = 2 \bullet \frac{V^2_{SN} - V_{SN} \bullet V_{OUT} \bullet \frac{N_P}{N_S}}{I^2_{SW(PEAK)} \bullet L_{LK} \bullet f}$$

L_{LK} is the leakage inductance of the primary winding, which is usually specified in the transformer characteristics. L_{LK} can be obtained by measuring the primary inductance with the secondary windings shorted. The snubber capacitor value (C_{SN}) can be determined using the following equation:

$$C_{CN} = \frac{V_{SN}}{\Delta V_{SN} \bullet R_{SN} \bullet f}$$

where ΔV_{SN} is the voltage ripple across C_{SN}. A reasonable ΔV_{SN} is 5% to 10% of V_{SN}. The reverse voltage rating of D_{SN} should be higher than the sum of V_{SN} and $V_{IN(MAX)}$. A Zener clamp can also be connected between SW and GND to ensure SW voltage does not exceed 40V.

Flyback Converter: Output Diode Selection

The output diode in a flyback converter is subject to large RMS current and peak reverse voltage stresses. A fast switching diode with a low forward drop and a low reverse leakage is desired. Schottky diodes are recommended if the output voltage is below 100V.

Approximate the required peak repetitive reverse voltage rating V_{RRM} using:

$$V_{RRM} > \frac{N_S}{N_P} \bullet V_{IN(MAX)} + V_{OUT}$$

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ to be used in this equation normally includes the $R_{\theta JC}$ for the device, plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

Flyback Converter: Output Capacitor Selection

The output capacitor of the flyback converter has a similar operation condition as that of the boost converter. Refer to the Boost Converter: Output Capacitor Selection section for the calculation of C_{OUT} and ESR_{COUT}.

The RMS ripple current rating of the output capacitors in continuous operation can be determined using the following equation:

$$I_{RMS(COUT),CONTINUOUS} \approx I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1-D_{MAX}}}$$

Flyback Converter: Input Capacitor Selection

The input capacitor in a flyback converter is subject to a large RMS current due to the discontinuous primary current. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum RMS current. The RMS ripple current rating of the input capacitors in continuous operation can be determined using the following equation:

$$I_{RMS(CIN),CONTINUOUS} \approx \frac{P_{OUT(MAX)}}{V_{IN(MIN)} \bullet \eta} \bullet \sqrt{\frac{1-D_{MAX}}{D_{MAX}}}$$

APPLICATIONS INFORMATION

SEPIC CONVERTER APPLICATIONS

The LT3957 can be configured as a SEPIC (single-ended primary inductance converter), as shown in Figure 1. This topology allows for the input to be higher, equal, or lower than the desired output voltage. The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT}+V_D}{V_{IN}}=\frac{D}{1-D}$$

in continuous conduction mode (CCM).

In a SEPIC converter, no DC path exists between the input and output. This is an advantage over the boost converter for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

Compared to the flyback converter, the SEPIC converter has the advantage that both the power MOSFET and the output diode voltages are clamped by the capacitors (C_{IN}, C_{DC} and C_{OUT}), therefore, there is less voltage ringing across the power MOSFET and the output diodes. The SEPIC converter requires much smaller input capacitors than those of the flyback converter. This is due to the fact that, in the SEPIC converter, the current through inductor L1 (which is series with the input) is continuous.

SEPIC Converter: Switch Duty Cycle and Frequency

For a SEPIC converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}), the input voltage (V_{IN}) and the diode forward voltage (V_D).

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX}=\frac{V_{OUT}+V_D}{V_{IN(MIN)}+V_{OUT}+V_D}$$

SEPIC Converter: The Maximum Output Current Capability and Inductor Selection

As shown in Figure 1, the SEPIC converter contains two inductors: L1 and L2. L1 and L2 can be independent, but can also be wound on the same core, since identical voltages are applied to L1 and L2 throughout the switching cycle.

For the SEPIC topology, the current through L1 is the converter input current. Based on the fact that, ideally, the output power is equal to the input power, the maximum average inductor currents of L1 and L2 are:

$$I_{L1(MAX)}=I_{IN(MAX)}=I_{O(MAX)}\bullet\frac{D_{MAX}}{1-D_{MAX}}$$

$$I_{L2(MAX)}=I_{O(MAX)}$$

Due to the current limit of its internal power switch, the LT3957 should be used in a SEPIC converter whose maximum output current ($I_{O(MAX)}$) is less than the output current capability by a sufficient margin (10% or higher is recommended):

$$I_{O(MAX)}<(1-D_{MAX})\bullet(5A-0.5\bullet\Delta I_{SW})$$

The inductor ripple currents ΔI_{L1} and ΔI_{L2} are identical:

$$\Delta I_{L1}=\Delta I_{L2}=0.5\bullet\Delta I_{SW}$$

The inductor ripple current ΔI_{SW} has a direct effect on the choice of the inductor value and the converter's maximum output current capability. Choosing smaller values of ΔI_{SW} requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_{SW} allows the use of low inductances, but results in higher input current ripple and greater core losses and reduces output current capability.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value (L1 and L2 are independent) of the SEPIC converter can be determined using the following equation:

$$L1=L2=\frac{V_{IN(MIN)}}{0.5\bullet\Delta I_{SW}\bullet f}\bullet D_{MAX}$$

For most SEPIC applications, the equal inductor values will fall in the range of 1µH to 100µH.

APPLICATIONS INFORMATION

By making L1 = L2, and winding them on the same core, the value of inductance in the preceding equation is replaced by 2L, due to mutual inductance:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f} \bullet D_{MAX}$$

This maintains the same ripple current and energy storage in the inductors. The peak inductor currents are:

$$I_{L1(PEAK)} = I_{L1(MAX)} + 0.5 \bullet \Delta I_{L1}$$

$$I_{L2(PEAK)} = I_{L2(MAX)} + 0.5 \bullet \Delta I_{L2}$$

The maximum RMS inductor currents are approximately equal to the maximum average inductor currents.

Based on the preceding equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

SEPIC Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with a low forward drop and low reverse leakage is desirable. The average forward current in normal operation is equal to the output current.

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than $V_{OUT} + V_{IN(MAX)}$ by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

where V_D is diode's forward voltage drop, and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ used in this equation normally includes the $R_{\theta JC}$ for the device, plus the thermal resistance from the board, to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

SEPIC Converter: Output and Input Capacitor Selection

The selections of the output and input capacitors of the SEPIC converter are similar to those of the boost converter. Please refer to the Boost Converter: Output Capacitor Selection and Boost Converter: Input Capacitor Selection sections.

SEPIC Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 1) should be larger than the maximum input voltage:

$$V_{CDC} > V_{IN(MAX)}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{V_{OUT} + V_D}{V_{IN(MIN)}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

INVERTING CONVERTER APPLICATIONS

The LT3957 can be configured as a dual-inductor inverting topology, as shown in Figure 8. The V_{OUT} to V_{IN} ratio is:

$$\frac{V_{OUT} - V_D}{V_{IN}} = -\frac{D}{1-D}$$

in continuous conduction mode (CCM).

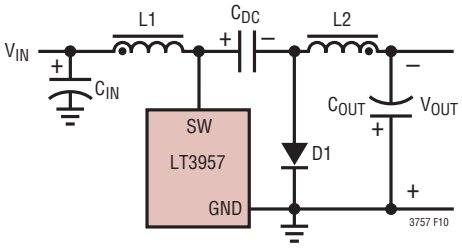


Figure 8. A Simplified Inverting Converter

APPLICATIONS INFORMATION

Inverting Converter: Switch Duty Cycle and Frequency

For an inverting converter operating in CCM, the duty cycle of the main switch can be calculated based on the negative output voltage (V_{OUT}) and the input voltage (V_{IN}).

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_D}{V_{OUT} - V_D - V_{IN(MIN)}}$$

Inverting Converter: Output Diode and Input Capacitor Selections

The selections of the inductor, output diode and input capacitor of an inverting converter are similar to those of the SEPIC converter. Please refer to the corresponding SEPIC converter sections.

Inverting Converter: Output Capacitor Selection

The inverting converter requires much smaller output capacitors than those of the boost, flyback and SEPIC converters for similar output ripples. This is due to the fact that, in the inverting converter, the inductor L2 is in series with the output, and the ripple current flowing through the output capacitors are continuous. The output ripple voltage is produced by the ripple current of L2 flowing through the ESR and bulk capacitance of the output capacitor:

$$\Delta V_{OUT(P-P)} = \Delta I_{L2} \bullet \left(ESR_{COUT} + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

After specifying the maximum output ripple, the user can select the output capacitors according to the preceding equation.

The ESR can be minimized by using high quality X5R or X7R dielectric ceramic capacitors. In many applications, ceramic capacitors are sufficient to limit the output voltage ripple.

The RMS ripple current rating of the output capacitor needs to be greater than:

$$I_{RMS(COUT)} > 0.3 \bullet \Delta I_{L2}$$

Inverting Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 10) should be larger than the maximum input voltage minus the output voltage (negative voltage):

$$V_{CDC} > V_{IN(MAX)} - V_{OUT}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

Board Layout

The high power and high speed operation of the LT3957 demands careful attention to board layout and component placement. Careful attention must be paid to the internal power dissipation of the LT3957 at high input voltages, high switching frequencies, and high internal power switch currents to ensure that a junction temperature of 125°C is not exceeded. This is especially important when operating at high ambient temperatures. Exposed pads on the bottom of the package are SGND and SW terminals of the IC, and must be soldered to a SGND ground plane and a SW plane respectively. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into the copper planes with as much as area as possible.

To prevent radiation and high frequency resonance problems, proper layout of the components connected to the IC is essential, especially the power paths with higher di/dt. The following high di/dt loops of different topologies should be kept as tight as possible to reduce inductive ringing:

- In boost configuration, the high di/dt loop contains the output capacitor, the internal power MOSFET and the Schottky diode.

APPLICATIONS INFORMATION

- In flyback configuration, the high di/dt primary loop contains the input capacitor, the primary winding, the internal power MOSFET. The high di/dt secondary loop contains the output capacitor, the secondary winding and the output diode.
- In SEPIC configuration, the high di/dt loop contains the internal power MOSFET, output capacitor, Schottky diode and the coupling capacitor.
- In inverting configuration, the high di/dt loop contains internal power MOSFET, Schottky diode and the coupling capacitor.

Check the stress on the internal power MOSFET by measuring the SW-to-GND voltage directly across the IC terminals. Make sure the inductive ringing does not exceed the maximum rating of the internal power MOSFET (40V).

The small-signal components should be placed away from high frequency switching nodes. For optimum load regulation and true remote sensing, the top of the output voltage sensing resistor divider should connect independently to the top of the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LT3957 in order to keep the high impedance FBX node short.

Figure 9 shows the suggested layout of the 4.5V to16V input, 24V output boost converter in the Typical Application section.

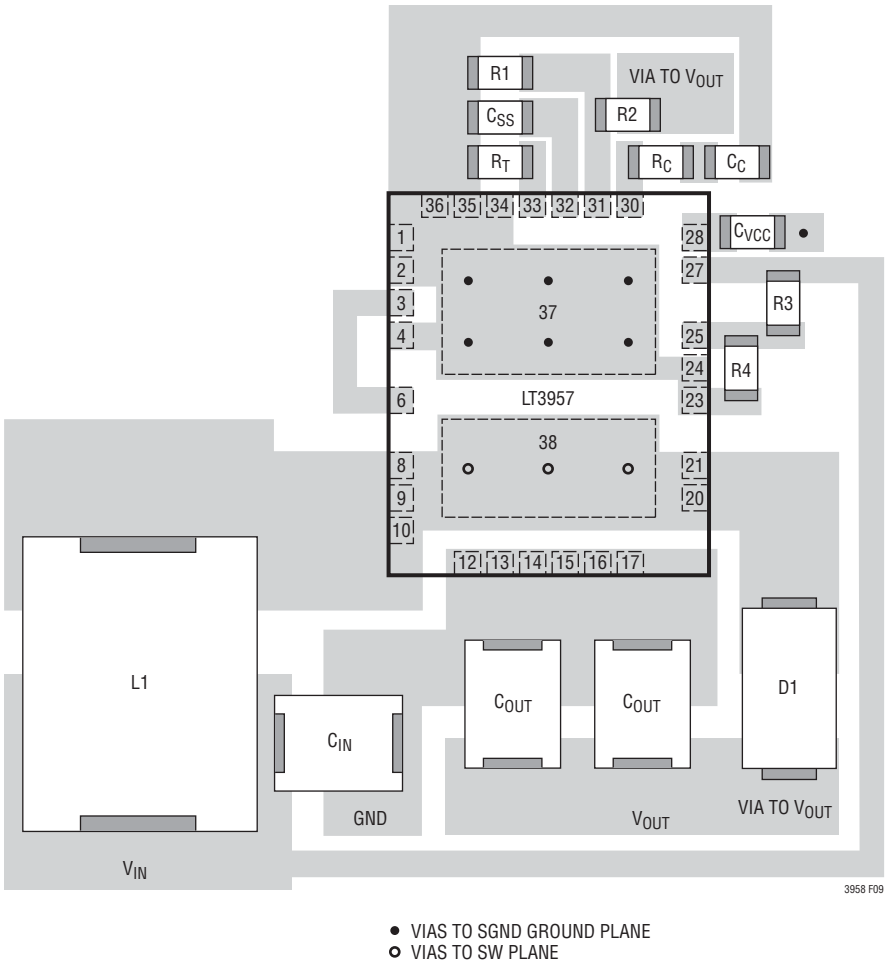


Figure 9. Suggested Layout of the 4.5V to 16V Input. 24V Output Boost Converter in the Typical Application Section

APPLICATIONS INFORMATION

Recommended Component Manufacturers

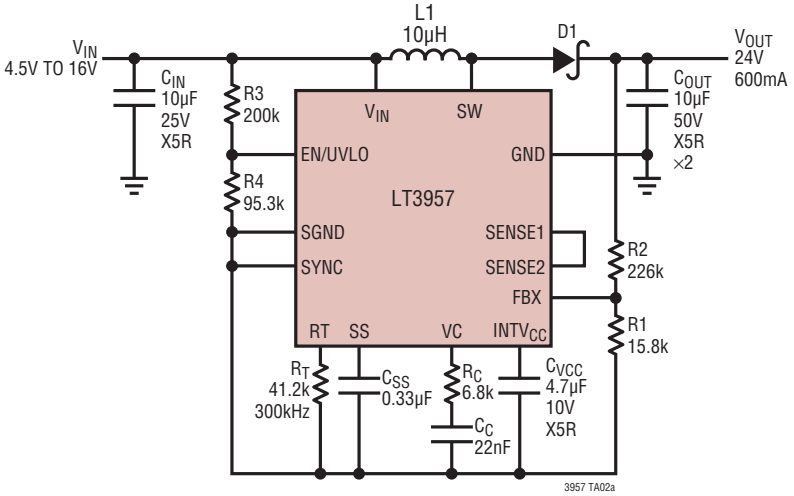
Some of the recommended component manufacturers are listed in Table 2.

Table 2. Recommended Component Manufacturers

VENDOR	COMPONENTS	WEB ADDRESS
AVX	Capacitors	avx.com
BH Electronics	Inductors, Transformers	bhelectronics.com
Coilcraft	Inductors	coilcraft.com
Cooper Bussmann	Inductors	bussmann.com
Diodes, Inc	Diodes	diodes.com
General Semiconductor	Diodes	generalsemiconductor.com
International Rectifier	Diodes	irf.com
Kemet	Tantalum Capacitors	kemet.com
Magnetics Inc	Toroid Cores	mag-inc.com
Microsemi	Diodes	microsemi.com
Murata-Erie	Inductors, Capacitors	murata.co.jp
Nichicon	Capacitors	nichicon.com
On Semiconductor	Diodes	onsemi.com
Panasonic	Capacitors	panasonic.com
Pulse	Inductors	pulseeng.com
Sanyo	Capacitors	sanyo.co.jp
Sumida	Inductors	sumida.com
Taiyo Yuden	Capacitors	t-yuden.com
TDK	Capacitors, Inductors	component.tdk.com
Thermalloy	Heat Sinks	aavidthermalloy.com
Tokin	Capacitors	nec-tokinamerica.com
Toko	Inductors	tokoam.com
United Chemi-Con	Capacitors	chemi-com.com
Vishay	Inductors	vishay.com
Würth Elektronik	Inductors	we-online.com
Vishay/Sprague	Capacitors	vishay.com
Zetex	Small-Signal Discretes	zetex.com

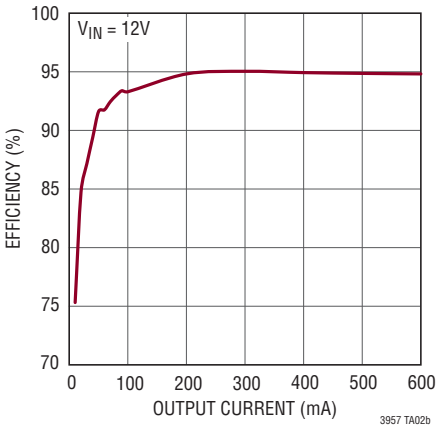
TYPICAL APPLICATIONS

4.5V to 16V Input, 24V Output Boost Converter



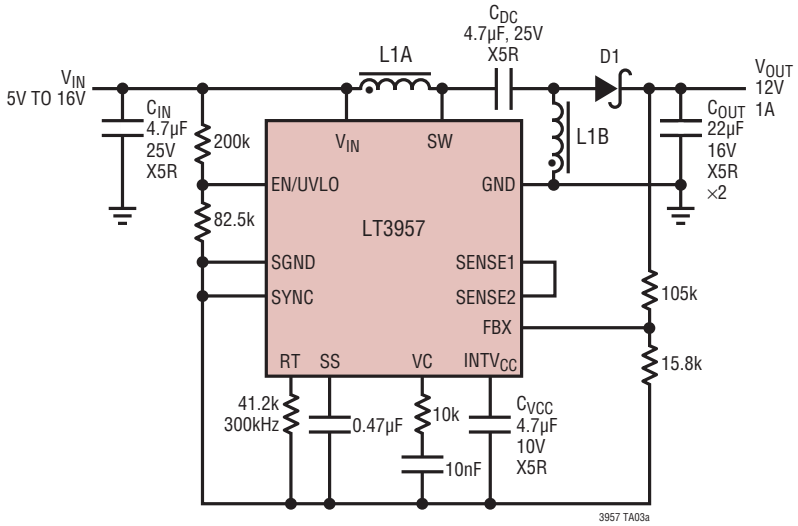
C_{IN}: MURATA GRM31ER61H106KA12
C_{OUT}: TAIYO YUDEN UMK325BJ106MM
D1: VISHAY SILICONIX 10BQ040
L1: VISHAY SILICONIX IHLP-5050CE-1

Efficiency vs Output Current



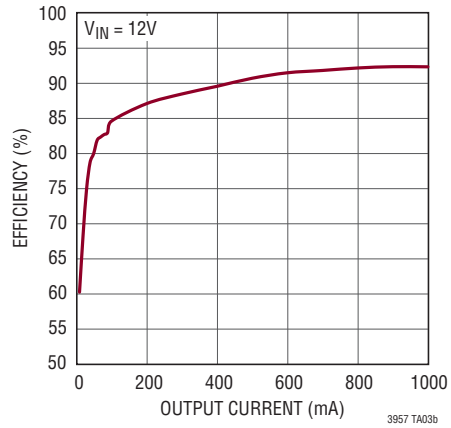
TYPICAL APPLICATIONS

5V to 16V Input, 12V Output SEPIC Converter

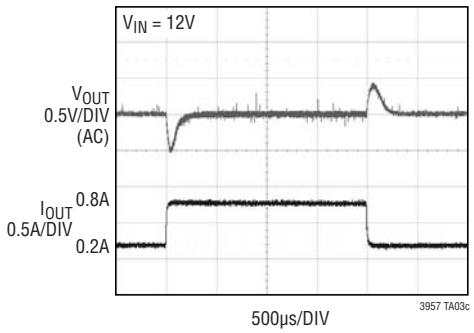


C_{IN}, C_{DC}: MURATA GRM21BR61E475KA12L
C_{OUT}: MURATA GRM32ER61C226KE20
D1: VISHAY SILICONIX 30BQ040
L1A, L1B: COILTRONICS DRQ127-100

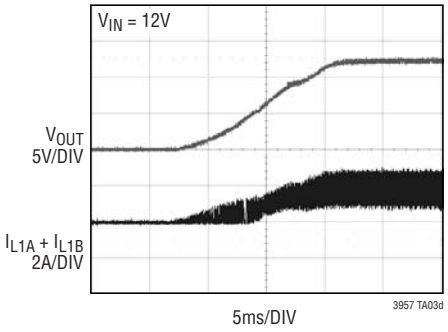
Efficiency vs Output Current



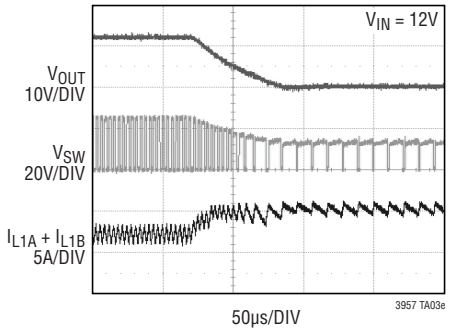
Load Step Waveforms



Start-Up Waveforms

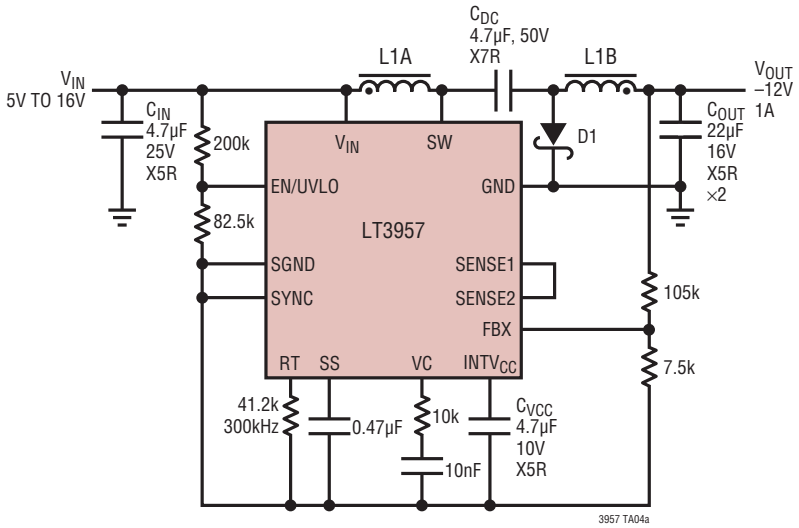


Frequency Foldback Waveforms When Output Short-Circuit



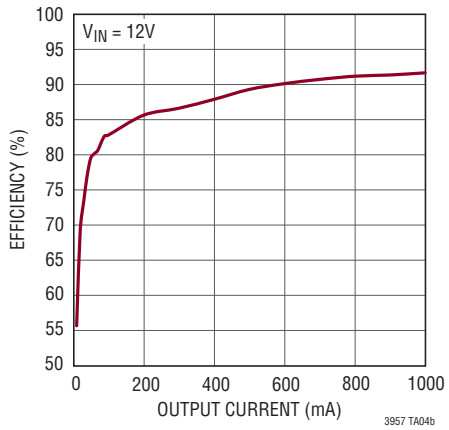
TYPICAL APPLICATIONS

5V to 16V Input, –12V Output Inverting Converter

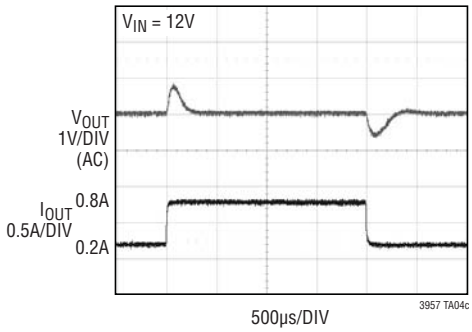


C_{IN}: MURATA GRM21BR61E475KA12L
C_{DC}: TAIYO YUDEN UMK316BJ475KL
C_{OUT}: MURATA GRM32ER61C226KE20
D1: VISHAY SILICONIX 30BQ040
L1A, L1B: COILTRONICS DRQ127-100

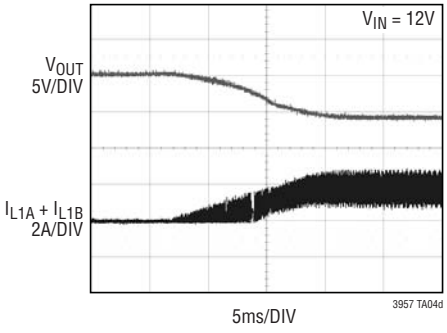
Efficiency vs Output Current



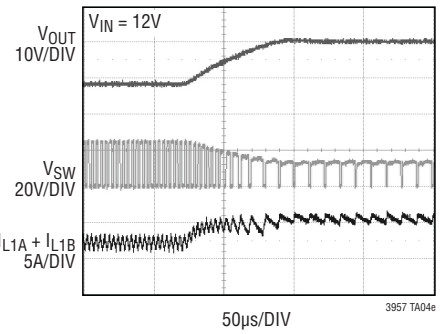
Load Step Waveforms



Start-Up Waveforms

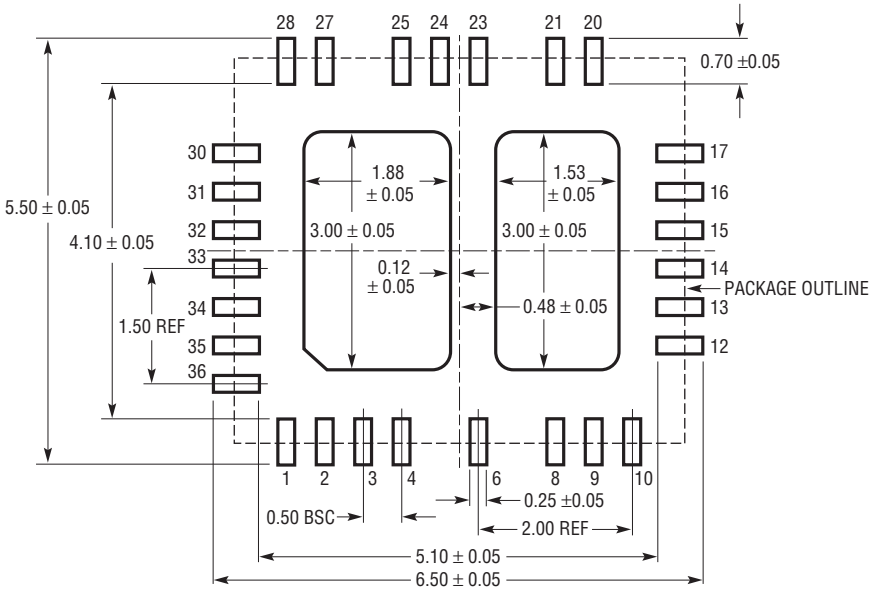


Frequency Foldback Waveforms When Output Short-Circuit

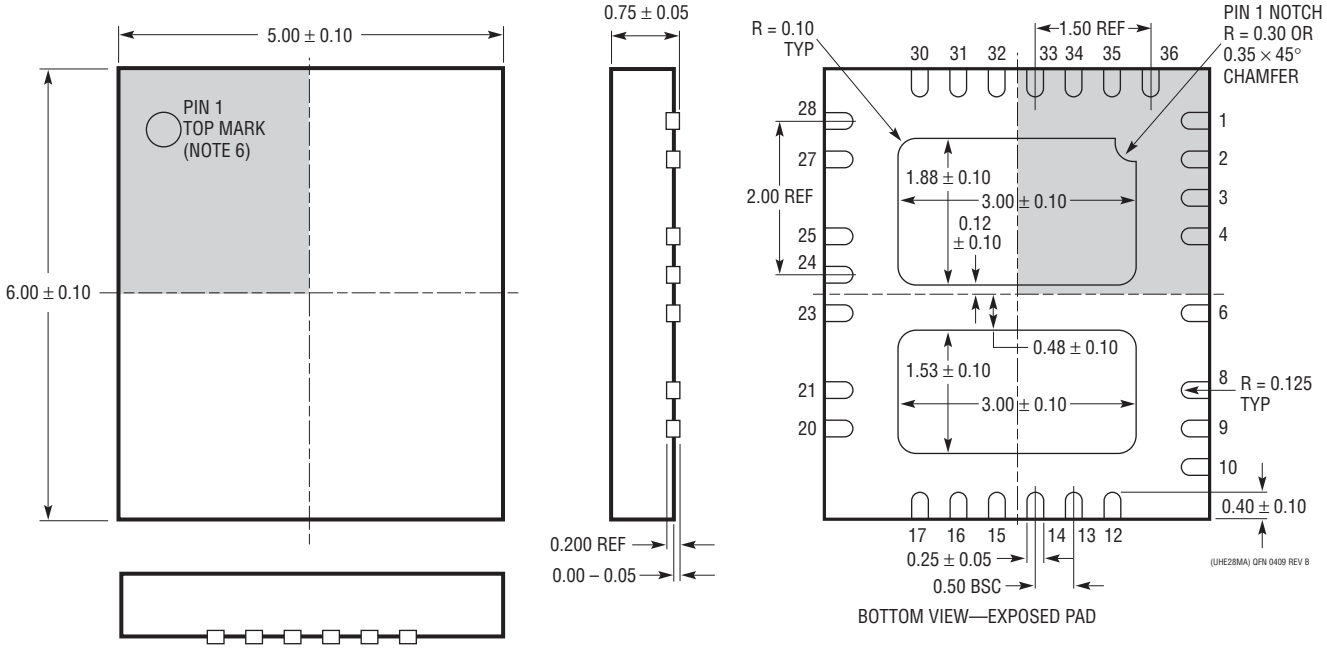


PACKAGE DESCRIPTION

UHE Package
Variation: UHE28MA
36-Lead Plastic QFN (5mm × 6mm)
(Reference LTC DWG # 05-08-1836 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

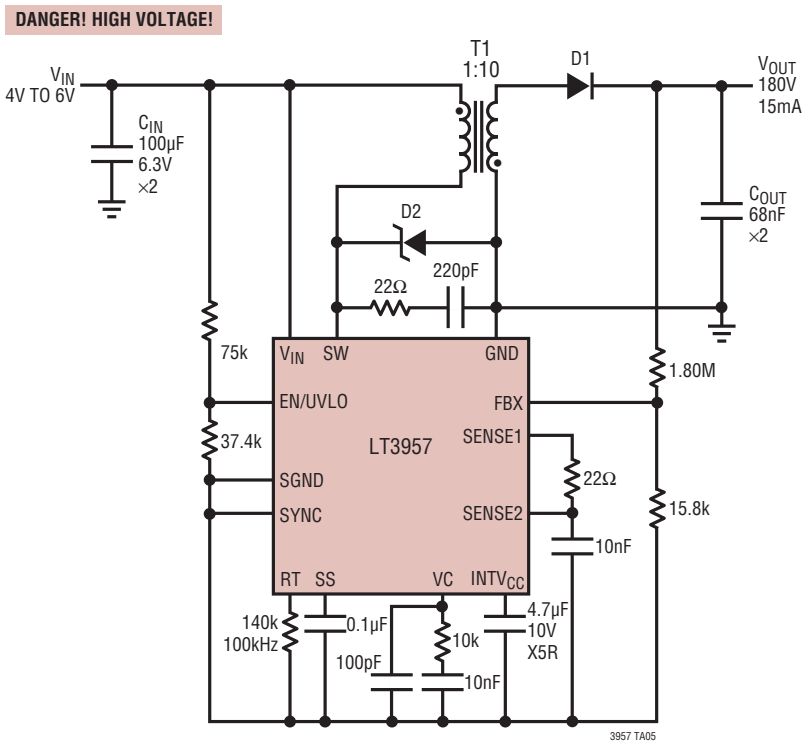


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATIONS

4V to 6V Input, 180V Output Flyback Converter



T1: TDK DCT15EFD-U44S003
C_{IN}: GRM31CR60J107ME39L
C_{OUT}: GRM43QR72J683KW01L
D1: VISHAY SILICONIX GSD2004S DUAL DIODE CONNECTED IN SERIES
D2: DIODES MMSZ5258B

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3958	High Input Voltage, Boost, Flyback, SEPIC and Inverting Converter with 3.5A/80V Switch	$5V \le V_{IN} < 80V$, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 5mm × 6mm QFN-36 Package
LT3580	Boost/Inverting DC/DC Converter with 2A Switch, Soft-Start and Synchronization	$2.5V \le V_{IN} \le 32V$, Current Mode Control, 200kHz to 2.5MHz, 3mm × 3mm DFN-8, MSOP-8E
LT3573	Isolated Flyback Converter with 1.25A/60V Integrated Switch	$3V \le V_{IN} \le 40V$, No Opto-Isolator or "Third Winding" Required, Up to 7W, MSOP-16E
LT3574	Isolated Flyback Converter with 0.65A/60V Integrated Switch	$3V \le V_{IN} \le 40V$, No Opto-Isolator or "Third Winding" Required, Up to 3W, MSOP-16
LT3757	Boost, Flyback, SEPIC and Inverting Controller	$2.9V \le V_{IN} \le 40V$, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 3mm × 3mm DFN-10 and MSOP-10E Package
LT3758	Boost, Flyback, SEPIC and Inverting Controller	$5.5V \le V_{IN} \le 100V$, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 3mm × 3mm DFN-10 and MSOP-10E Package
LTC1871/LTC1871-1/ LTC1871-7	Wide Input Range, No R_{SENSE}™ Low Quiescent Current Flyback, Boost and SEPIC Controller	Adjustable Switching Frequency, $2.5V \le V_{IN} \le 36V$, Burst Mode Operation at Light Load
LTC3803/LTC3803-3/ LTC3803-5	200kHz/300kHz Flyback DC/DC Controller	V_{IN} and V_{OUT} Limited Only by External Components, ThinSOT™ Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0610 • PRINTED IN USA