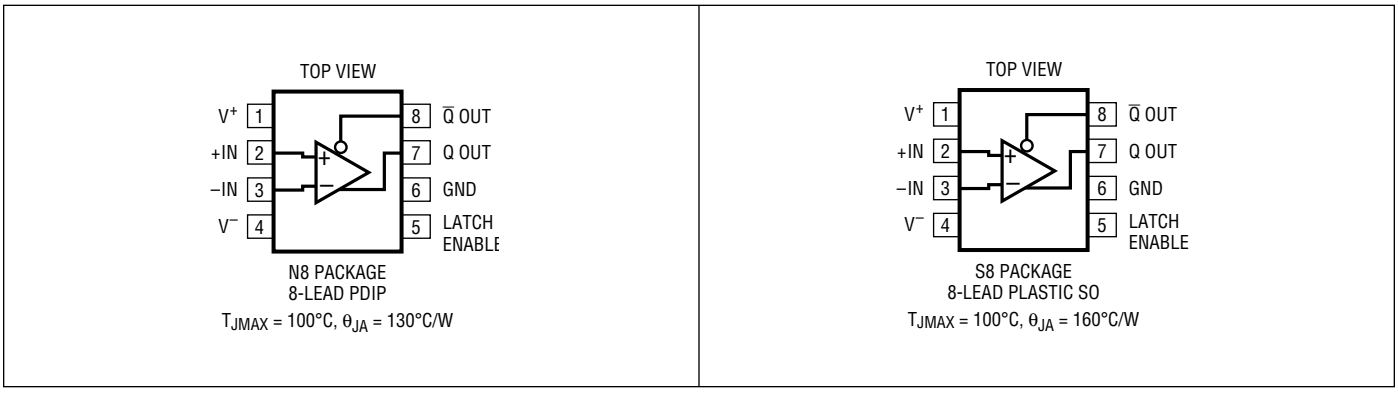
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+) to GND 7V
Negative Supply Voltage (V^-) ..... –7V to GND Voltage
Differential Input Voltage ..... ±15V
Inputs Voltage (Either Input) ..... (V^-) –0.3V to 15V
Latch Pin Voltage ..... Equal to Supplies
Output Current (Continuous) ..... ±20mA
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1116CN8#PBF	NA	1116	8-Lead PDIP	0°C to 70°C
LT1116CS8#PBF	LT1116CS8#TRPBF	1116	8-Lead Plastic SO	0°C to 70°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Parts ending with PBF are RoHS and WEEE compliant.
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = –5V, V_{OUT} (Q) = 1.4V, LATCH = 0V. Specifications for V_{OS}, I_B, CMRR, and Voltage Gain are valid for single supply operation, V^+ = 5V, V^- = 0V, unless noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$ (Note 2)	 ●		1.0	±3.0 3.5	mV mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift		●		5		µV/°C
I_{OS}	Input Offset Current	(Note 2)	●		0.5	2	µA
I_B	Input Bias Current, Sourcing	(Note 3)	●		10	20	µA
	Input Voltage Range	Arbitrary Supply Range Single 5V Supply	● ●	V^- 0		(V^+) –2.5 2.5	V V
CMRR	Common Mode Rejection Ratio	$-5V \le V_{CM} \le 2.5V$, $V_S = \pm 5V$ $0V \le V_{CM} \le 2.5V$	● ●	75 65	90 90		dB dB
PSRR	Power Supply Rejection Ratio	Positive Supply, $4.6V \le V^+ \le 5.4V$ Negative Supply, $-7 \le V^- \le -2V$	● ●	60 80	75 100		dB dB
A_V	Small Signal Voltage Gain	$1V \le V_{OUT} \le 2V$		1400	3000		V/V
I^+	Positive Supply Current		●		27	38	mA
I^-	Negative Supply Current		●		5	7	mA
V_{OH}	Output High Voltage	I_{SOURCE} = 1mA I_{SOURCE} = 10mA	● ●	2.7 2.4	3.4 3.0		V V
V_{OL}	Output Low Voltage	I_{SINK} = 4mA I_{SINK} = 10mA	●		0.3 0.4	0.5	V V
V_{IH}	+ Positive Latch Threshold		●	2.0			V
V_{IL}	– Latch Threshold		●			0.8	V
I_{IL}	Latch Input Current	V_{LATCH} = 0V	●		–20	–500	µA
t_{PD}	Propagation Delay	ΔV_{IN} = 100mV, OD = 5mV (Note 4)	 ●		12	16 18	ns ns
t_{PD}	Propagation Delay	ΔV_{IN} = 100mV, OD = 20mV (Note 4)	 ●		10	14 16	ns ns
Δt_{PD}	Differential Propagation Delay	ΔV_{IN} = 100mV, OD = 5mV (Note 4)				3	ns
t_{SU}	Latch Set-Up Time	(Note 5)			2		ns
t_H	Latch Hold Time	(Note 5)			2		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input offset voltage is defined as the average of two offset voltages measured by forcing first the Q output to 1.4V then forcing the $\overline{Q}$ output to 1.4V.

Note 3: Input bias current is defined as the average of the two input currents.

Note 4: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1116 is sample tested with a 1V step and 500mV overdrive. Correlation tests have shown that t_{PD} and Δt_{PD} can be guaranteed with this test if additional DC tests are performed to verify internal bias conditions are correct. For low overdrive conditions V_{OS} is added to the measured overdrive.

Note 5: Input latch set-up time, t_{SU}, is the interval in which the input signal must be stable prior to asserting the latch signal. The hold time, t_H, is the interval after the latch is asserted in which the input signal must be stable.

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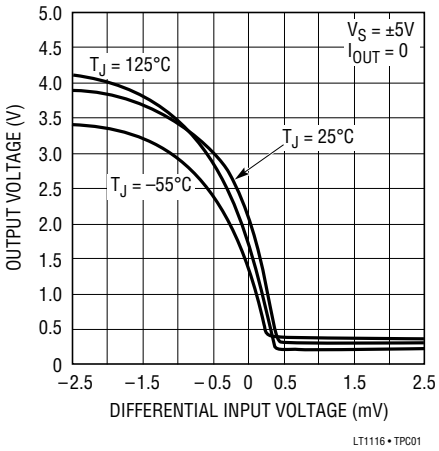
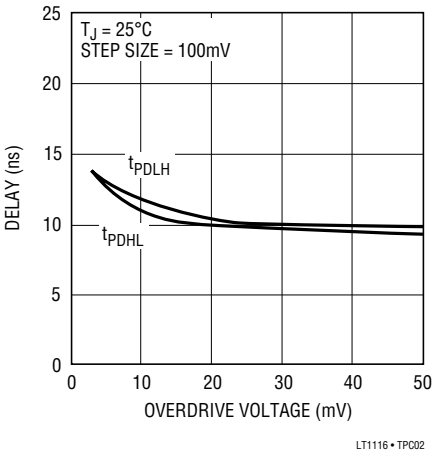
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Characteristics



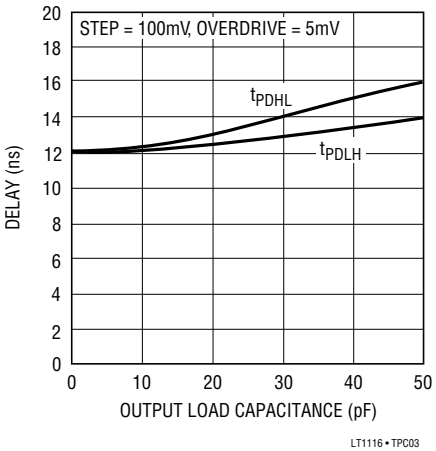
LT1116 • TPC01

Propagation Delay vs Overdrive



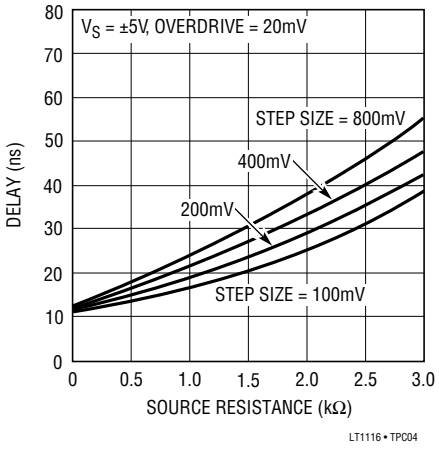
LT1116 • TPC02

Propagation Delay vs Load Capacitance



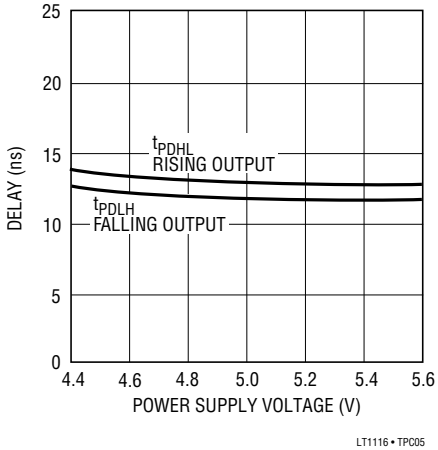
LT1116 • TPC03

Propagation Delay vs Source Resistance



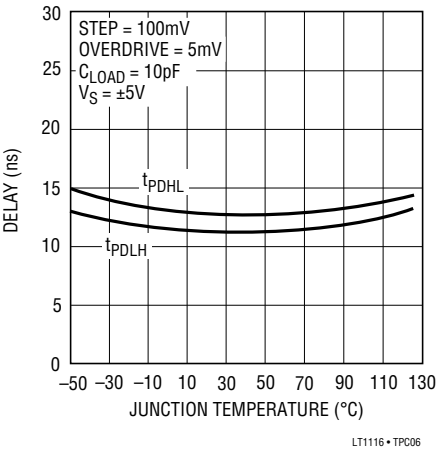
LT1116 • TPC04

Propagation Delay vs Positive Supply



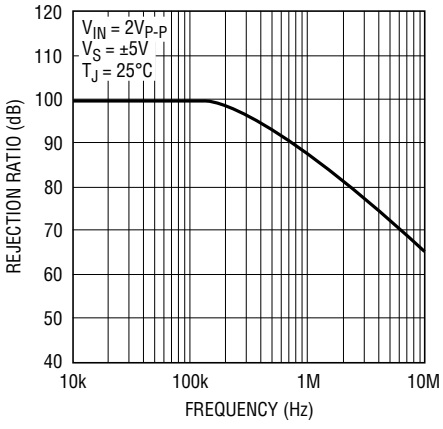
LT1116 • TPC05

Propagation Delay vs Temperature



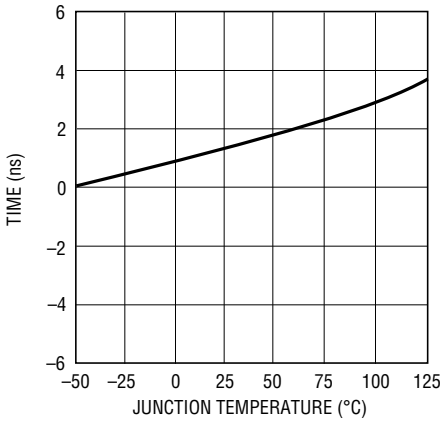
LT1116 • TPC06

Common Mode Rejection



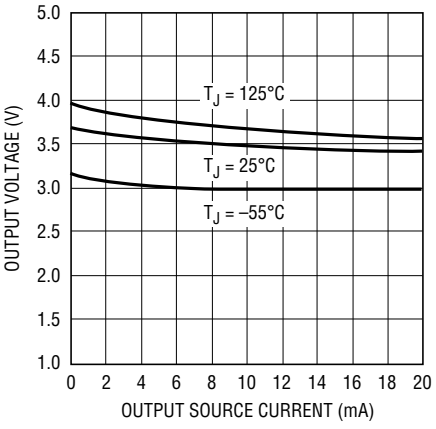
LT1116 • TPC07

Latch Set-Up Time



LT1116 • TPC08

Output High Voltage (V_{OH})



LT1116 • TPC09

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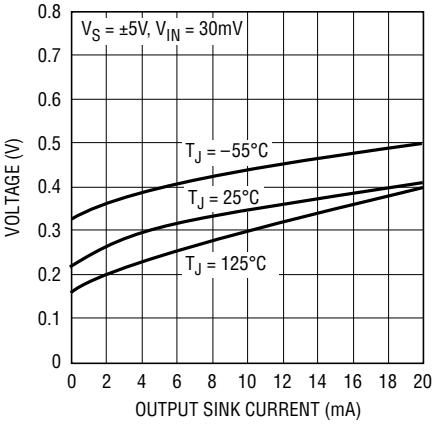
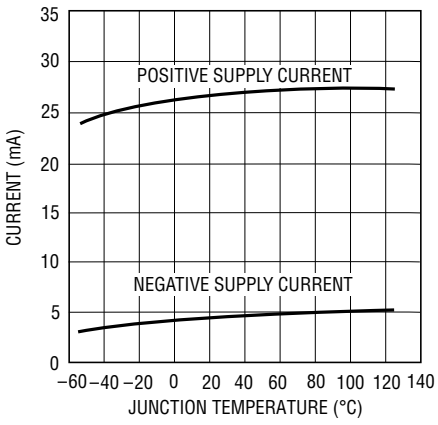
TYPICAL PERFORMANCE CHARACTERISTICS

Output Low Voltage (V_{OL})



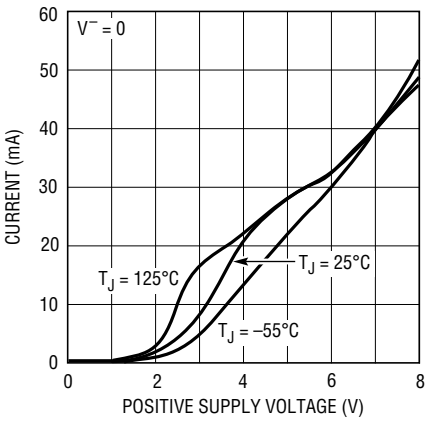
LT1116 • TPC10

Supply Current vs Temperature



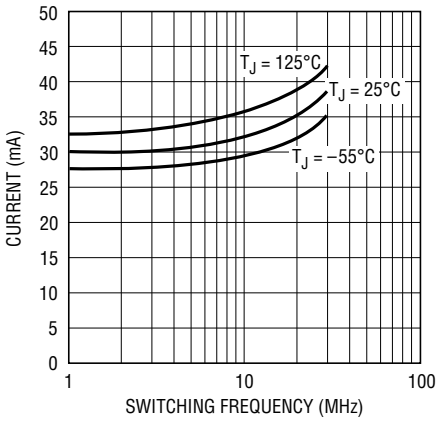
LT1116 • TPC11

Positive Supply Current



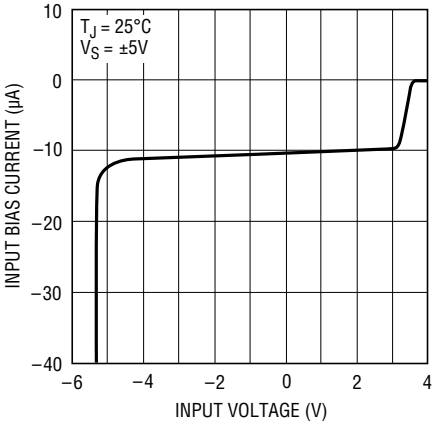
LT1116 • TPC12

Positive Supply Current



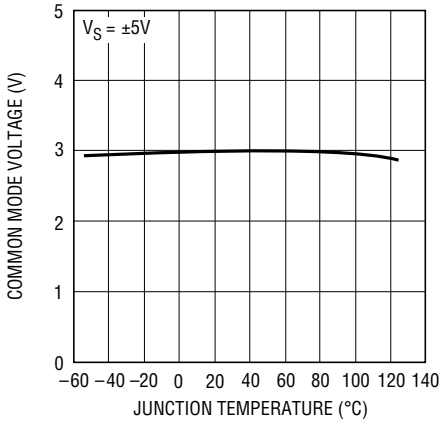
LT1116 • TPC13

Input Bias Current



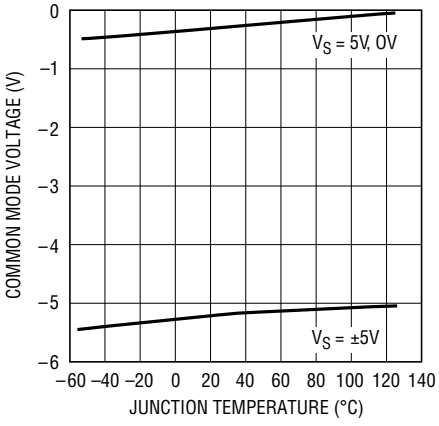
LT1116 • TPC14

Positive Common Mode Limit



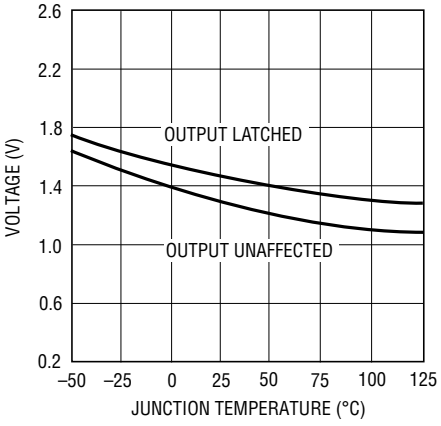
LT1116 • TPC15

Negative Common Mode Limit



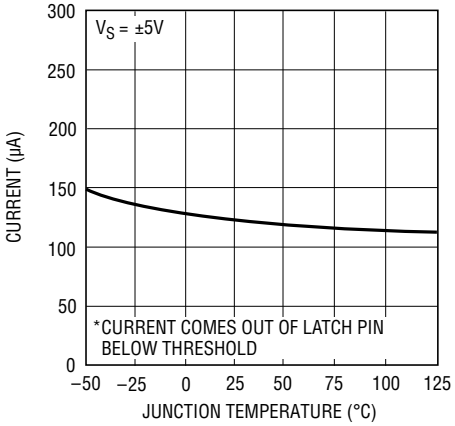
LT1116 • TPC16

Latch Pin Threshold



LT1116 • TPC17

Latch Pin Current*



LT1116 • TPC18

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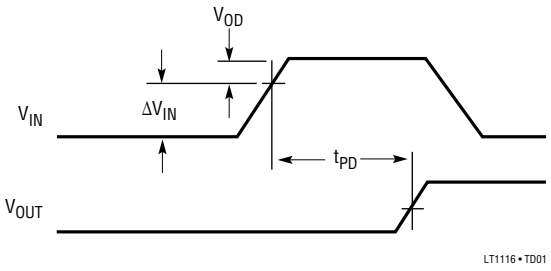
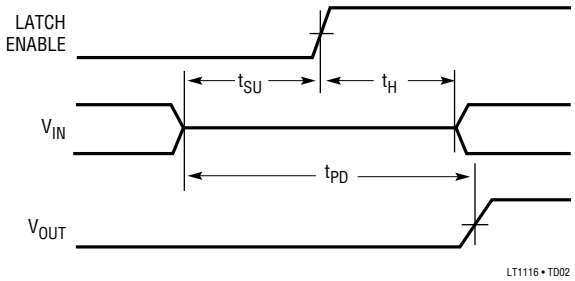
TIMING DIAGRAM





APPLICATIONS INFORMATION

Common Mode Considerations

The LT1116 is specified for a common mode range of 0V to 2.5V with a single 5V supply, and –5V to 2.5V with ±5V supplies. The common mode range is defined as the DC input for which the output responds correctly to small changes in the input differential. Input signals can exceed the positive common mode limit up to the 15V absolute maximum rating without damaging the comparator. There will, however, be an increase in propagation delay of up to 10ns when the input signal switches back into the common mode range. When input signals fall below the negative common mode limit, the internal PN diode formed with the substrate can turn on (resulting in significant charge flow throughout the die). A Schottky clamp diode, between the input and the negative rail, speeds up recovery from negative overdrive by preventing the substrate diode from turning on. The zero crossing detector in Figure 1 demonstrates the use of a fast clamp diode. Recovery, from 500mV overdrive below V^-, for this circuit is approximately 18ns.

Fast Zero Crossing Detector

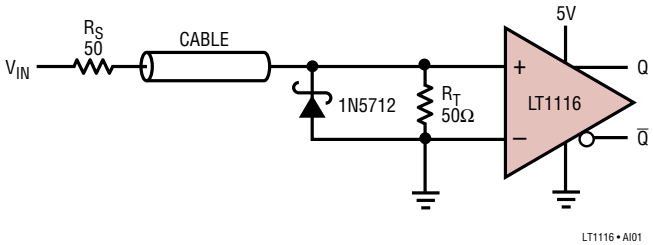


Figure 1. The Zero Crossing Detector Terminates the Transmission Line at Its 50Ω Characteristic Impedance. Negative Inputs Should Not Fall Below –2V to Keep the Signal Current Within the Clamp Diode's Maximum Forward Rating. Positive Inputs Should not Exceed the Device's Absolute Maximum Ratings nor the Power Rating on the Terminating Resistor

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APPLICATIONS INFORMATION

Input Characteristics

Each input to the LT1116 is buffered with a fast PNP follower—input bias current therefore does not vary significantly throughout the common mode range. When either input exceeds the positive common mode limit, the bias current drops to zero. Inputs that fall more than one diode and drop below V^- will forward bias the substrate or clamp diode, causing large input current to flow.

Single ended input resistance is about 5MΩ, and remains roughly constant over the input common mode range. The common mode resistance is about 2.5MΩ with zero differential input voltage, and does not change significantly with the absolute value of differential input.

Effective input capacitance, typically 5pF, is determined by measuring the resulting change in propagation delay for a 1kΩ change in source resistance.

Latch Pin Dynamics

The internal latch uses local regenerative feedback to shorten set-up and hold times. Driving the latch pin high retains the output state. The latch pin floats to a high state when disconnected, so it must be driven low for flow-through operation. The set-up time required to guarantee detecting a given transition of the inputs is 2ns. The inputs must also remain stable for a 2ns hold time after latch is asserted. New data will appear at the output approximately 10ns to 12ns after the latch goes low. The latch pin has no built-in hysteresis, and is designed to be driven from TTL or CMOS logic gates.

Additional Information

Linear Technology's Application Note 13 provides an extensive discussion of design techniques for high speed comparators.

Single Supply Crystal Oscillator 10MHz to 15MHz

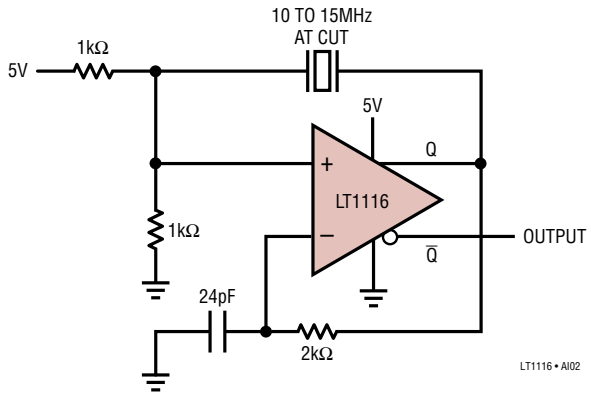

Figure 2. This Single Supply Crystal Oscillator Utilizes Crystals From 10MHz To 15MHz Without Component Changes

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APPLICATIONS INFORMATION

High Speed Adaptive Trigger Circuit

Line receivers often require an adaptive trigger to compensate for variations in signal amplitude and DC offsets. The circuit in Figure 3 triggers on 2mV to 200mV signals from 100Hz to 10MHz from a single 5V rail. The trigger level is the average of the input signal's positive and negative peaks stored on 0.005µF capacitors. Pairs of NPN and PNP transistors are used instead of diodes to temperature compensate the peak detector.

To achieve single supply operation, the input signal must be shifted into the pre-amplifier's common mode range. The input amplifier A1 adds a 1V level shift, while A2 provides a gain of 20 for high frequency signals. Capacitors C1 and C2 insure that low frequency signals see unity gain. Bandwidth limiting in A1 and A2 does not affect triggering because the adaptive trigger threshold varies ratiometrically to maintain circuit output.

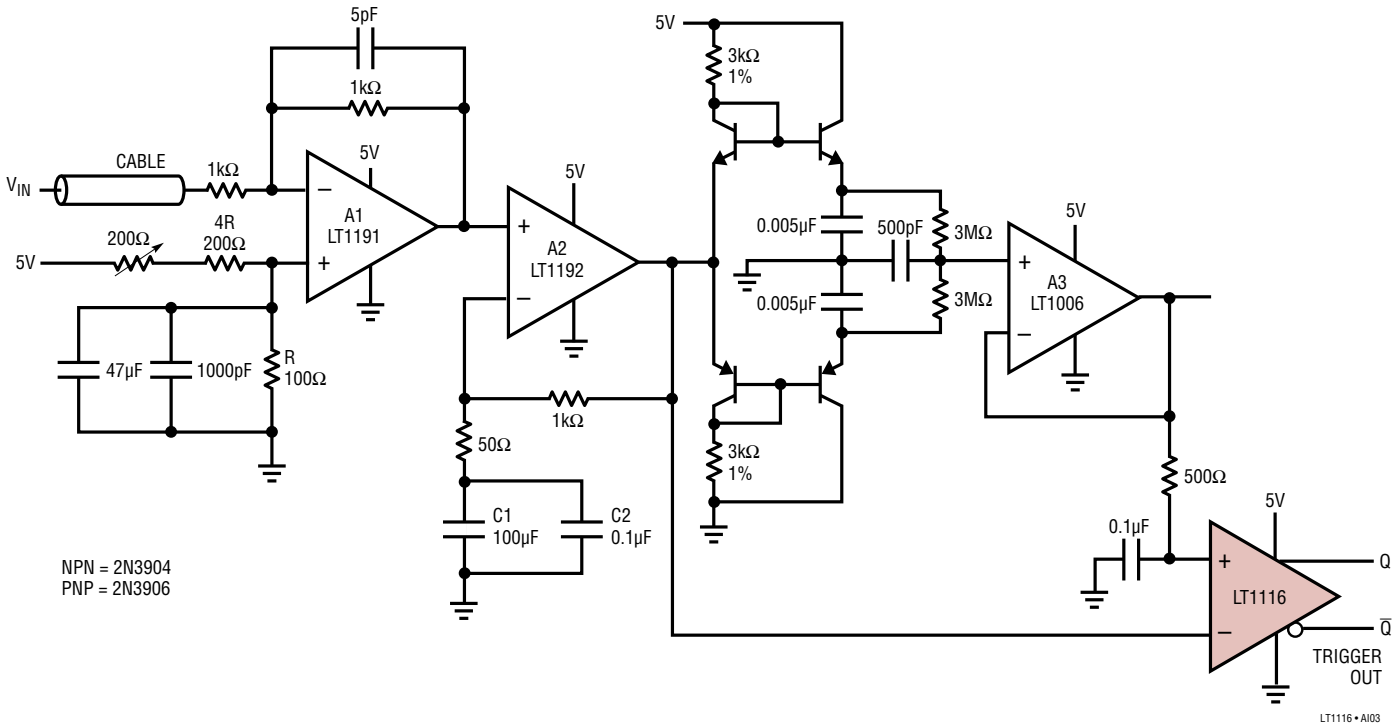

Figure 3. Fast Single Supply Adaptive Trigger

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REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	02/16	Addition of Web Links	2
		Reformat of Order Information	All
		Correction to Electrical Characteristics Conditions, V^- = –5V	3

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

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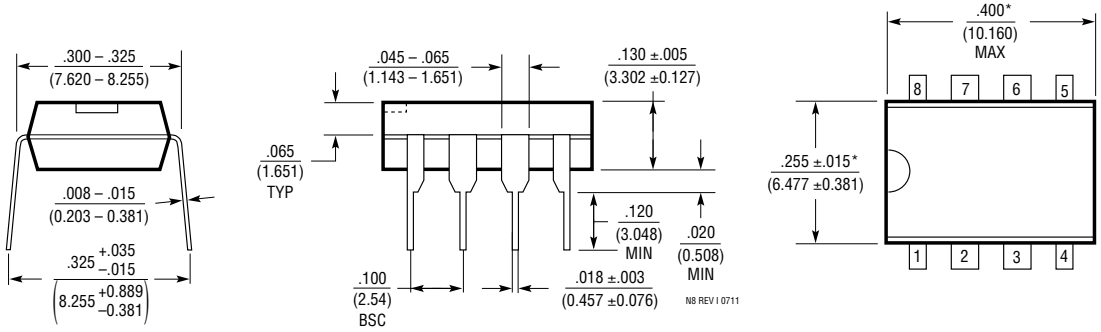
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT1116#packaging for the most recent package drawings.

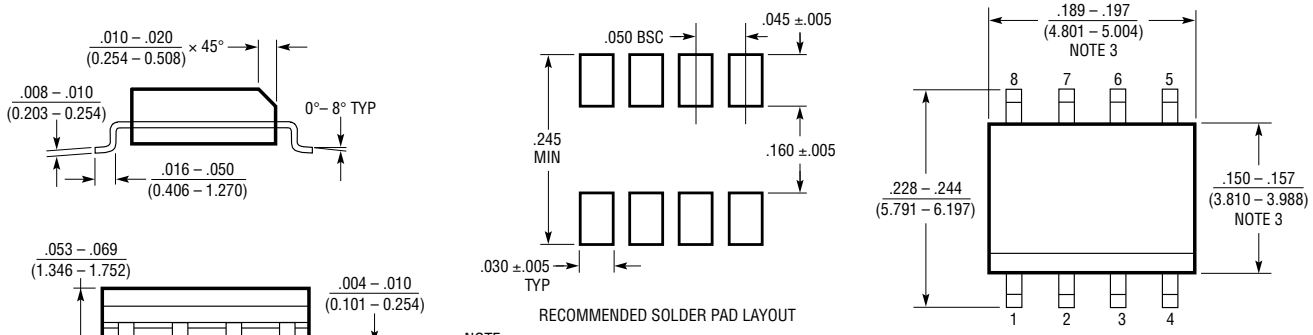
N Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1016	10ns Precision Comparator	Complementary Outputs with Latch, LT1116 Pinout
LT1394	7ns Single Supply Comparator	6mA, 100MHz Toggle Rate, LT1116 Pinout
LT1713/LT1714	7ns Single/Dual Comparator	Rail-to-Rail Input and Output, 2.7V to + 5.5V Operation
LT1715	4ns Dual Comparator	Independent Input/Output Supplies, 150MHz Toggle Rate
LT1719	4.5ns Single Supply Comparator	Independent Input/Output Supplies, 3V/5V
LT1720/LT1721	4.5ns Dual/Quad Comparator	4mA per Comparator, Input 100mV Below V –, 3V/5V
LTC6752	2.9ns 280MHz CMOS Output Comparator Family	5 Options Offer a Broad Range of Features

Linear Technology Corporation
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