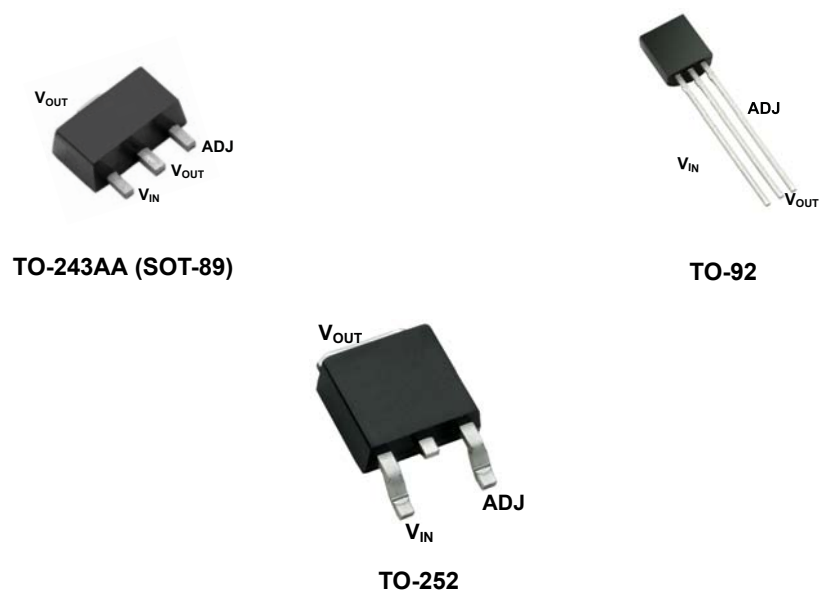


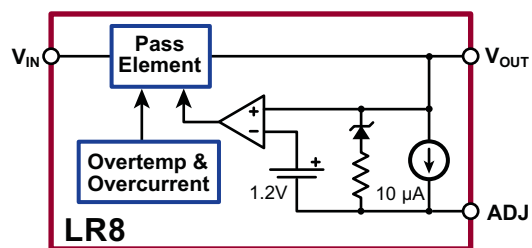
# LR8

## Package Type



See [Table 2-1](#) for pin information

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS<sup>†</sup>

$V_{IN}$ Input voltage (voltages ref to ADJ).....	-0.5 to +480V
Output voltage range.....	0.5 to +470V
Operating ambient temperature range.....	-40°C to +85°C
Operating junction temperature range .....	-40°C to +125°C
Storage temperature .....	-65°C to +150°C

**† Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS <sup>1</sup>

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input to output voltage difference	$V_{IN} - V_{OUT}$	12		450	V	
Overall output voltage regulation	$V_{OUT}$	1.14	1.20	1.26	V	$13.2V < V_{IN} < 400V$ , $R_1 = 2.4\text{ k}\Omega$ , $R_2 = 0$
		375	400	425	V	$R_1 = 2.4\text{ k}\Omega$ , $R_2 = 782\text{ k}\Omega$
Line regulation	$\Delta V_{OUT}$		0.003	0.01	%/V	$17V < V_{IN} < 400V$ , $V_{OUT} = 5V$ , $I_{OUT} = 0.5\text{mA}$
Load regulation			1.4	3.0	%	$V_{IN} = 17V$ , $V_{OUT} = 5V$ , $0.5\text{ mA} < I_{OUT} < 10\text{ mA}$
Temperature regulation		-1		+1	%	$V_{IN} = 17V$ , $V_{OUT} = 5V$ , $I_{OUT} = 10\text{ mA}$ , $-40^\circ\text{C} < T_A < 85^\circ\text{C}$
Output current limit	$I_{OUT}$	10		30	mA	$T_J < 85^\circ\text{C}$ , $V_{IN} - V_{OUT} = 12V$
				0.5	mA	$T_J > 125^\circ\text{C}$ , $V_{IN} - V_{OUT} = 450V$
Minimum output current	$I_{OUT}$		0.3	0.5	mA	Includes $R_1$ and load current
Adjust output current	$I_{ADJ}$	5.0	10	15	$\mu\text{A}$	
Minimum output load capacitance	$C_{LOAD}$	1.0			$\mu\text{F}$	
Ripple rejection ratio	$\Delta V_{OUT}/\Delta V_{IN}$	50	60		dB	120 Hz, $V_{OUT} = 5V$
Junction temperature limit	$T_{LIMIT}$	125			$^\circ\text{C}$	

<sup>1</sup> Test Conditions unless otherwise specified:  $-40^\circ\text{C} < T_A < 85^\circ\text{C}$ .

**TABLE 1-1: TYPICAL THERMAL RESISTANCE**

Package	$\theta_{ja}$
TO-252 (D-PAK)	$81^\circ\text{C/W}$
TO-92	$132^\circ\text{C/W}$
TO-243AA (SOT-89)	$133^\circ\text{C/W}$

**TABLE 1-2: THERMAL CHARACTERISTICS**

Package	Power Dissipation @ $T_A = 2.5^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$
TO-92	0.74W	125	170
TO-243AA (SOT-89)	1.6W	15	$78^1$
TO-252 (D-PAK)	2.5W	6.25	$50^1$

<sup>1</sup> Mounted on FR4 board, 25 mm x 2 mm x 1.57 mm

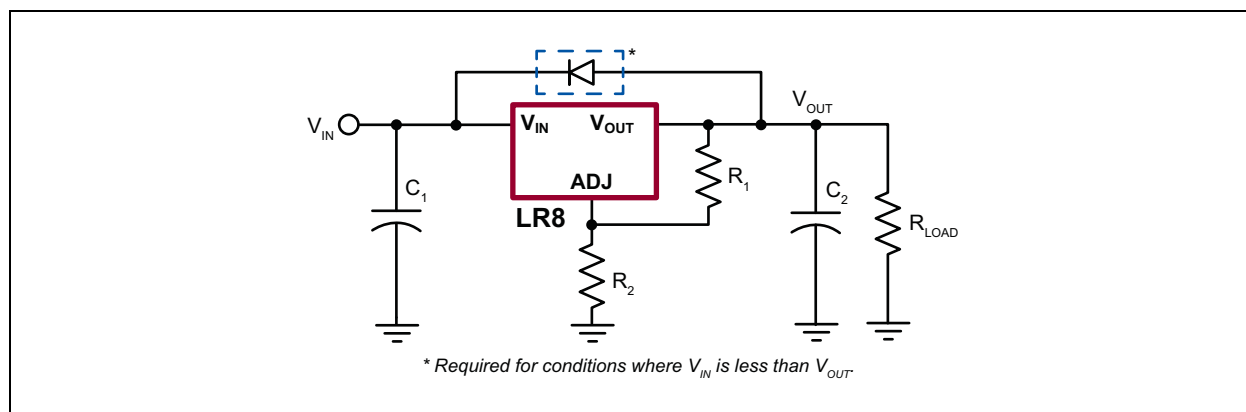
## 2.0 PIN DESCRIPTION

The locations of the pins are listed in [Package Type](#).

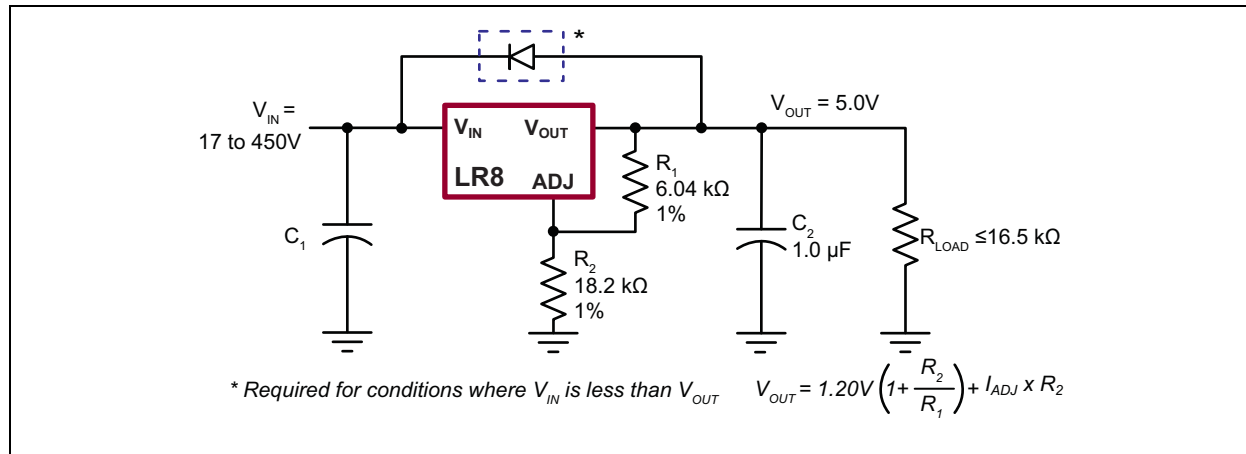
**TABLE 2-1: PIN DESCRIPTION**

Function	Description
V <sub>IN</sub>	Regulator input. 13.2-450V.
V <sub>OUT</sub>	Regulator output.
ADJ	Output voltage adjust.

## 3.0 TYPICAL APPLICATION CIRCUITS



**FIGURE 3-1:** Typical Application Circuit.



**FIGURE 3-2:** High-input Voltage, 5.0V Output Linear Regulator.

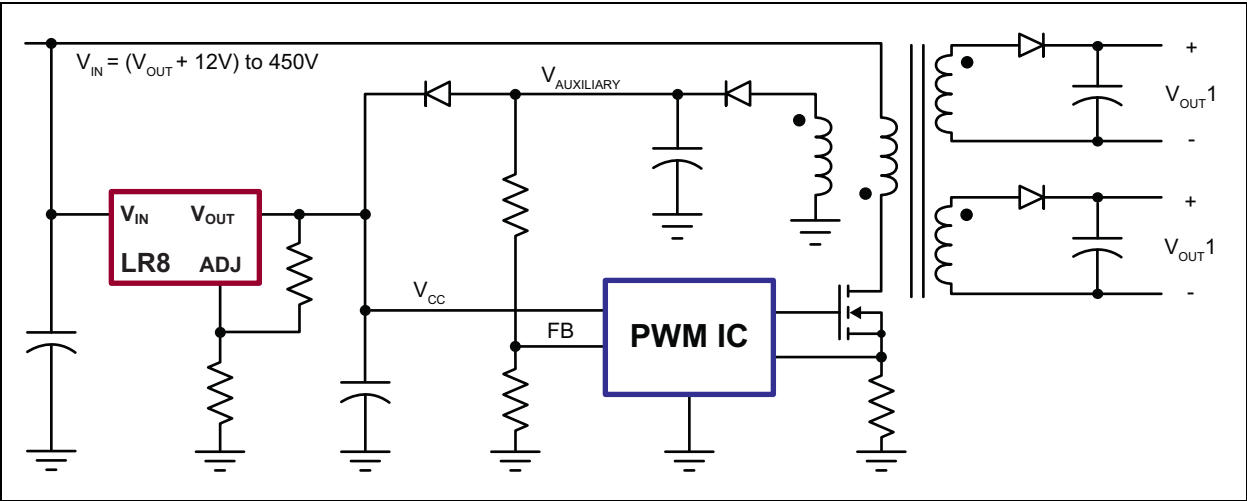


FIGURE 3-3: SMPS Start-Up Circuit.

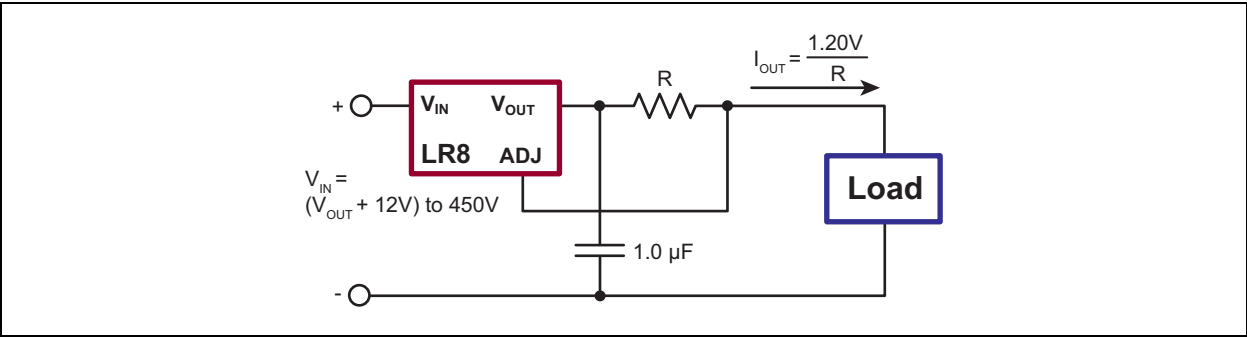
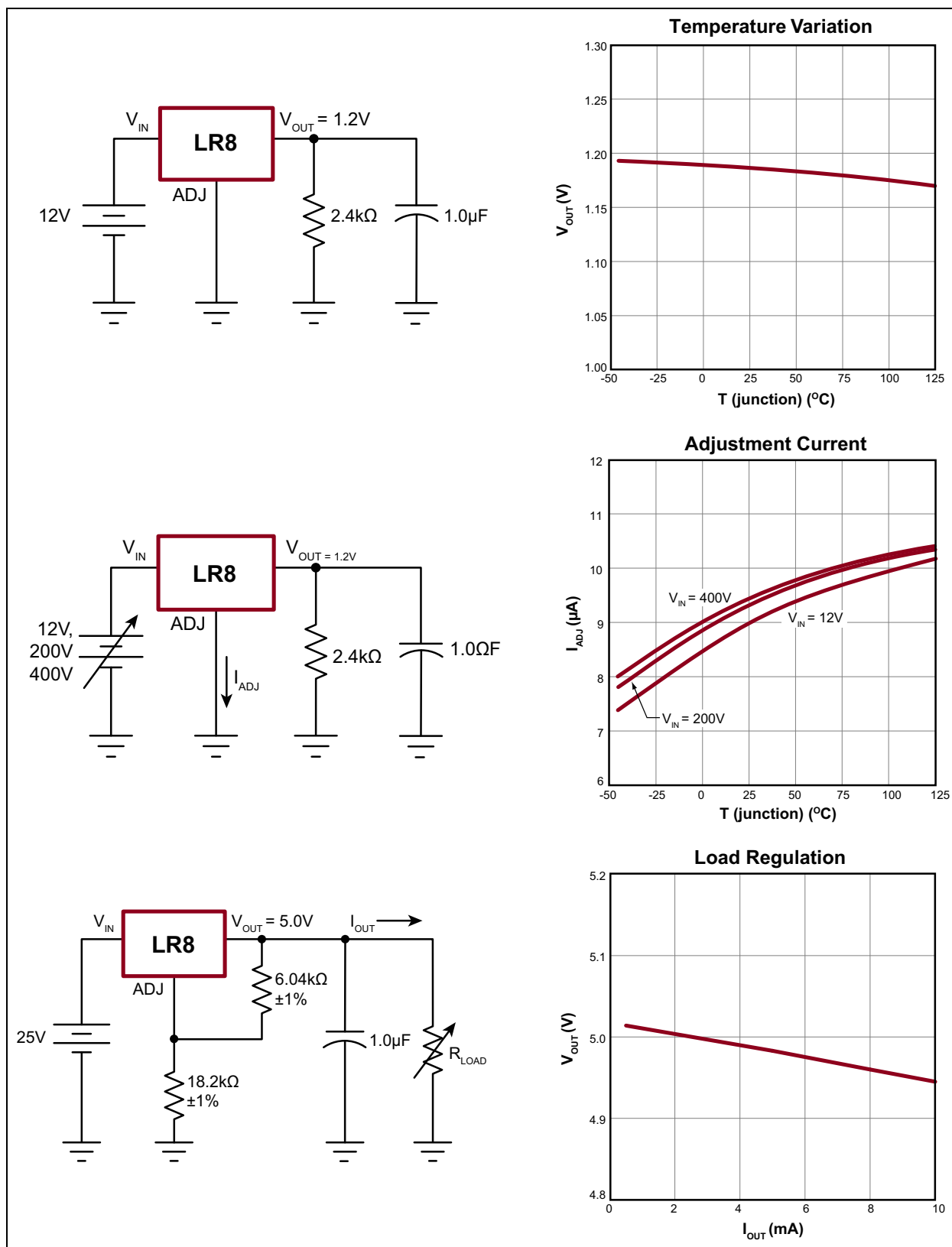
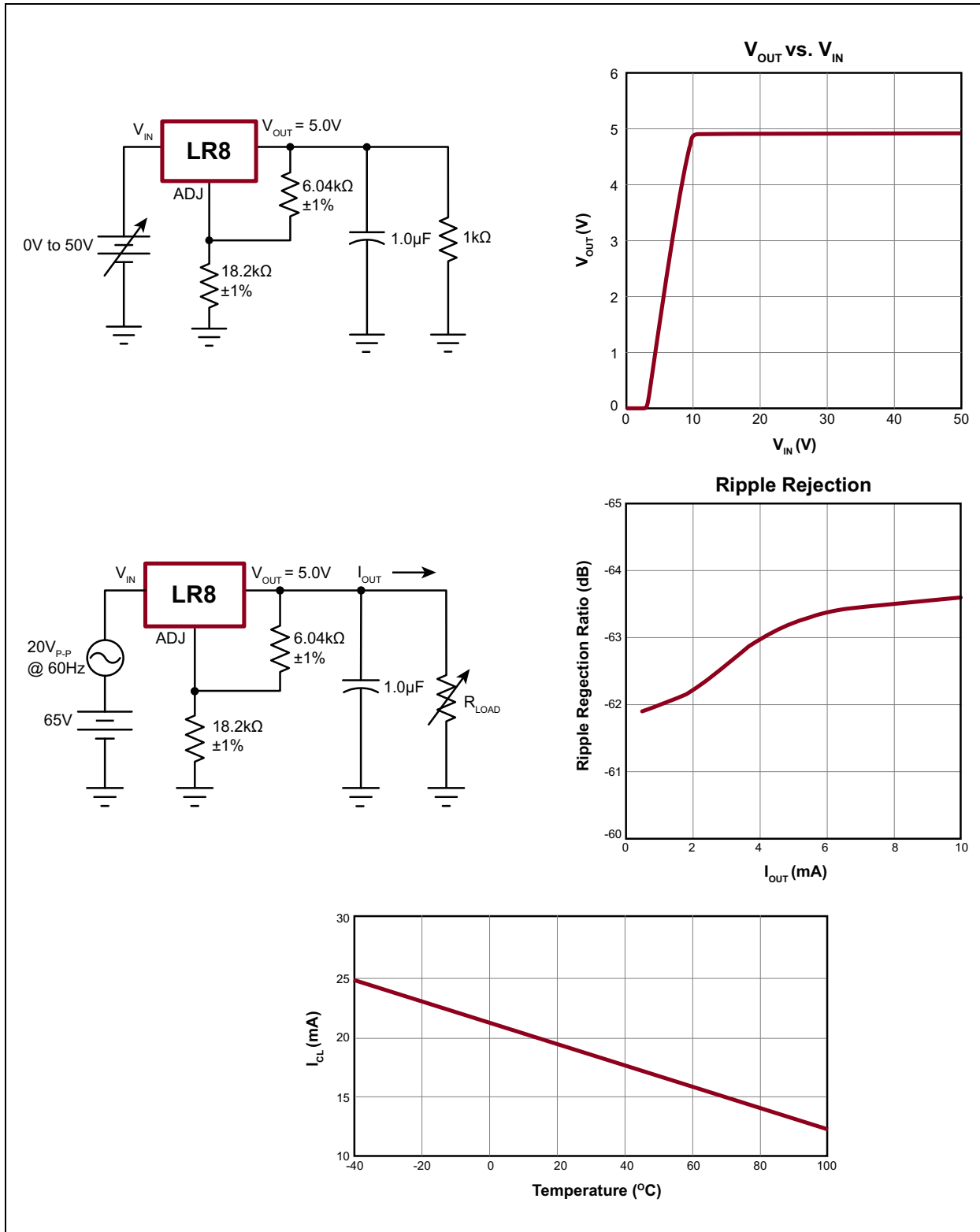


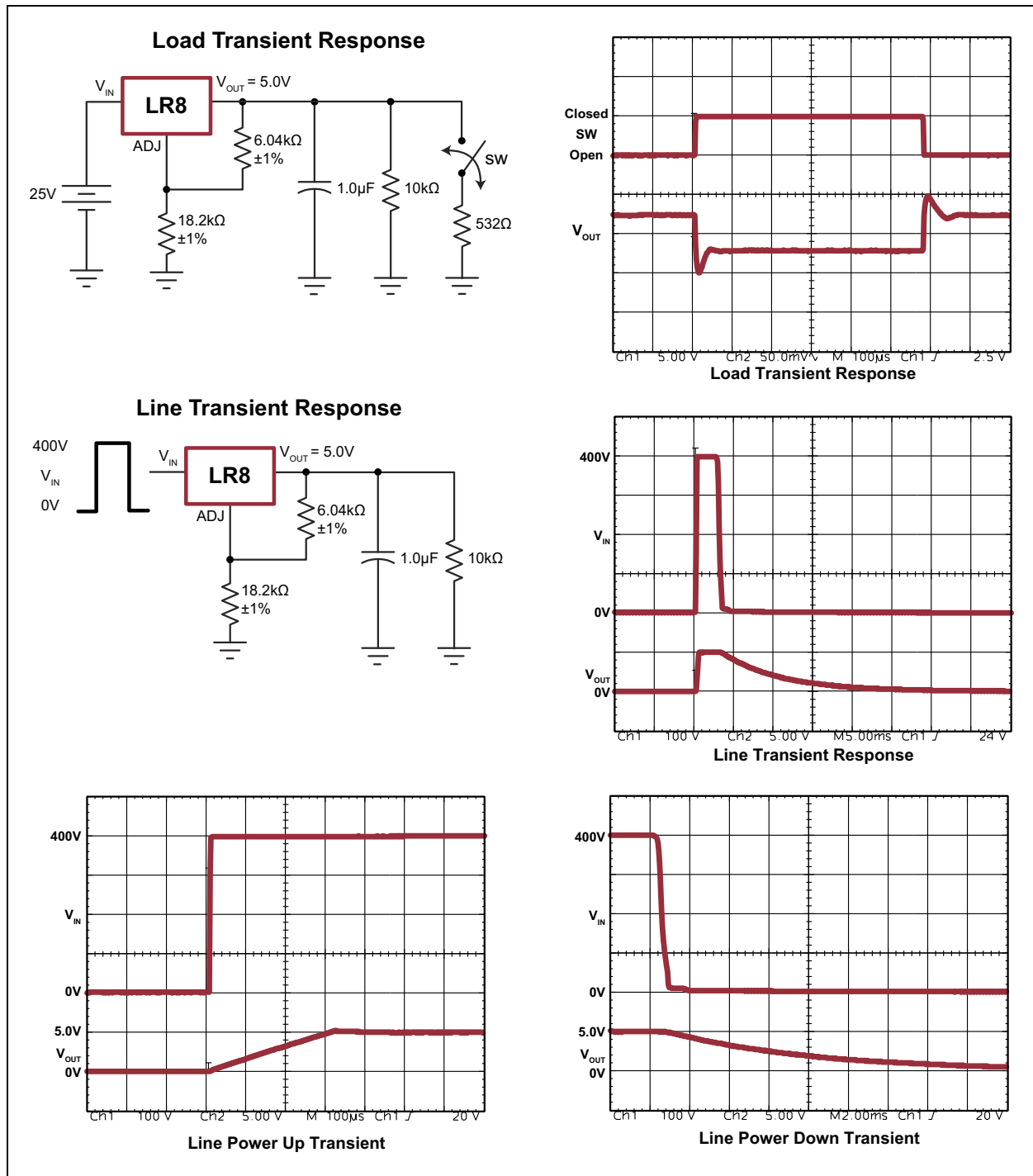
FIGURE 3-4: High-voltage, Adjustable, Constant-Current Source.



**FIGURE 3-5:** Typical Performance Curves 1 of 3.



**FIGURE 3-6:** Typical Performance Curves 2 of 3.

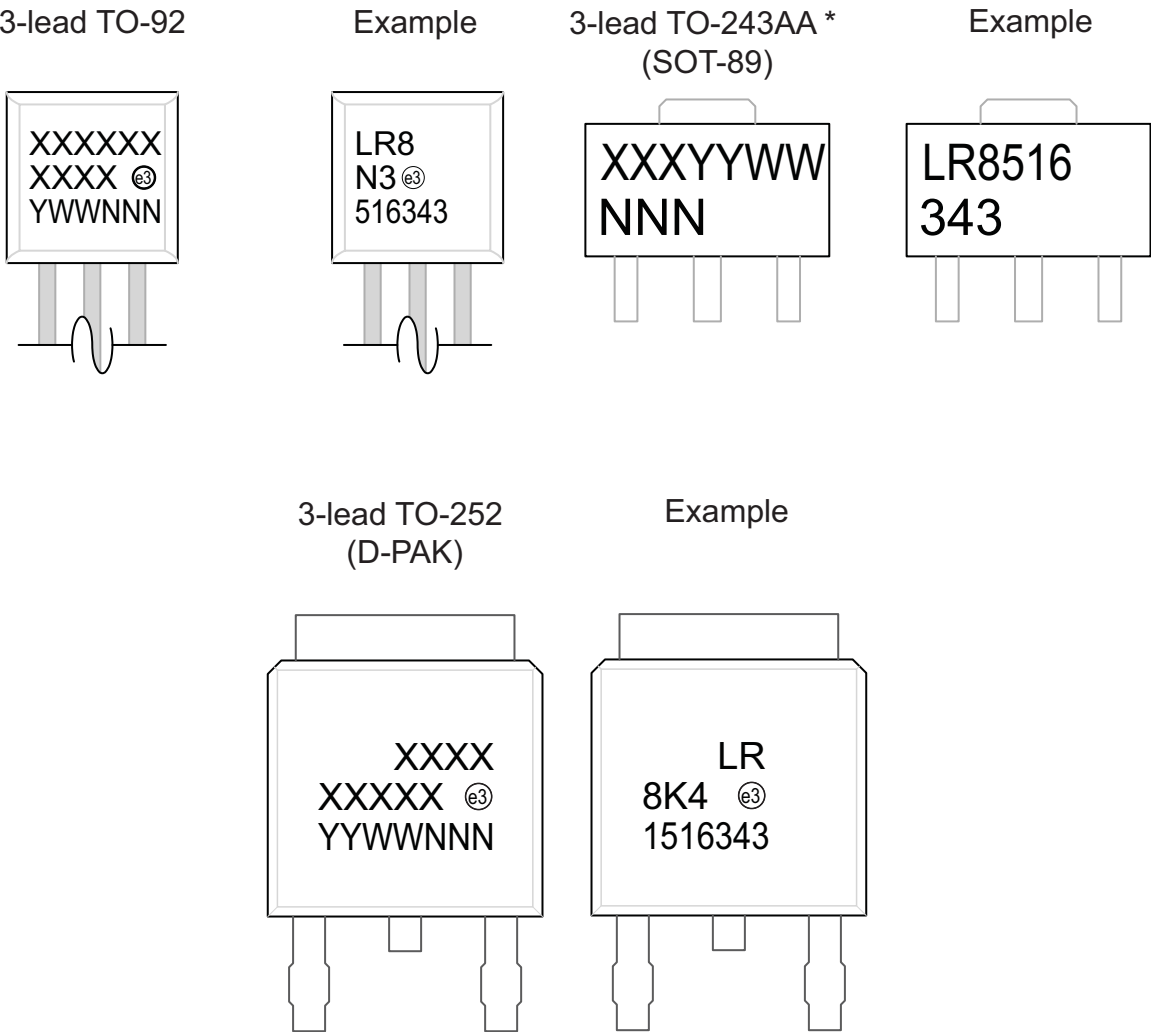


**FIGURE 3-7:** Typical Performance Curves 3 of 3.



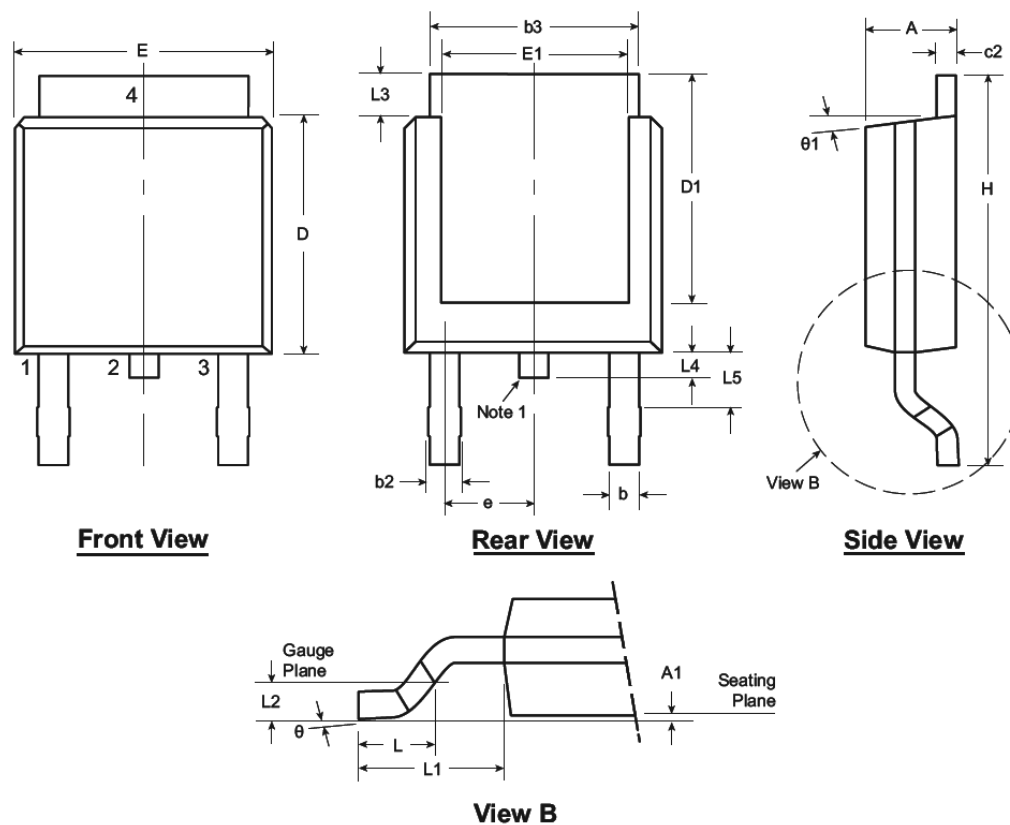
4.0 PACKAGING INFORMATION

4.1 Package Marking Information



<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

### 3-Lead TO-252 (D-PAK) Package Outline (K4)



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

**Note:**

1. Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

Symbol	A	A1	b	b2	b3	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1
Dimension (inches)	MIN	.086	.000*	.025	.030	.195	.018	.235	.205	.250	.170		.370	.055		.035	.025*	.035†	0°	0°
	NOM	-	-	-	-	-	.240	-	-	-			.060	.108 REF	.020 BSC	-	-	-	-	-
	MAX	.094	.005	.035	.045	.215	.035	.245	.217*	.265	.200*		.410	.070		.050	.040	.060	10°	15°

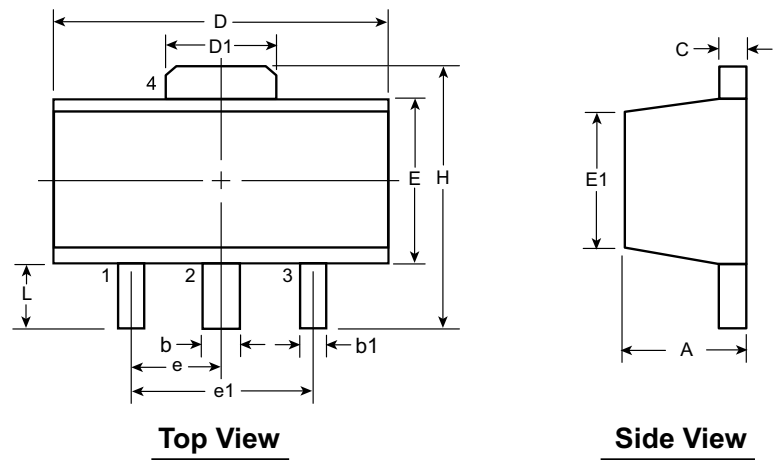
JEDEC Registration TO-252, Variation AA, Issue E, June 2004.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

3-Lead TO-243AA (SOT-89) Package Outline (N8)

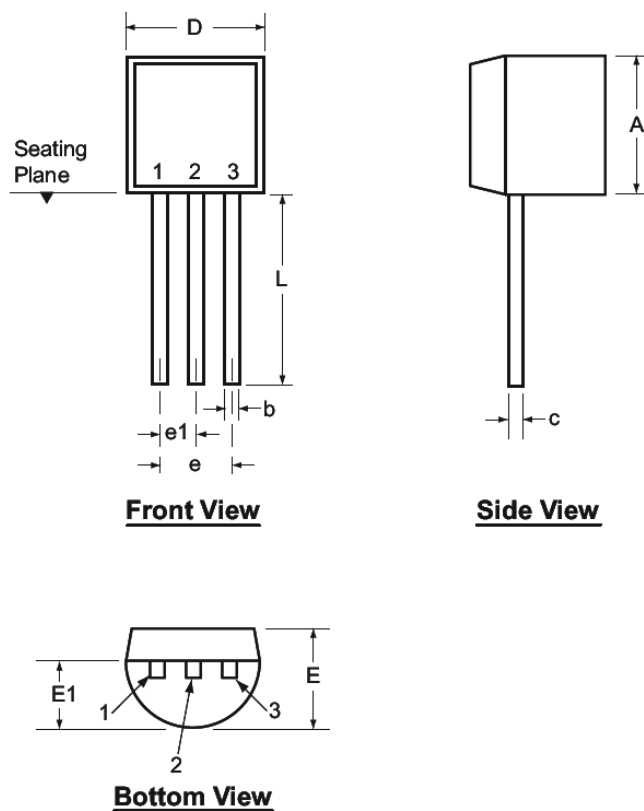


Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 <sup>†</sup>	1.50 BSC	3.00 BSC	3.94	0.73 <sup>†</sup>
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.  
<sup>†</sup> This dimension differs from the JEDEC drawing  
Drawings not to scale.

### 3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision B (November 2017)

The following is the list of modifications:

1. Updated [Figure 3-2](#).
2. Various typographical edits.

### Revision A (June 2015)

- Original Release of this Document.



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