## Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS and with all faults, and all risk associated with such information is entirely with Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# Contents

Acronyms in This Document ..... 9
1. Introduction ..... 10
1.1. Features ..... 11
1.1.1. Flexible Logic Architecture ..... 11
1.1.2. Ultra Low Power Devices ..... 11
1.1.3. Embedded and Distributed Memory ..... 11
1.1.4. On-Chip User Flash Memory ..... 11
1.1.5. Pre-Engineered Source Synchronous I/O ..... 11
1.1.6. High Performance, Flexible I/O Buffer ..... 11
1.1.7. Flexible On-Chip Clocking ..... 11
1.1.8. Non-volatile, Infinitely Reconfigurable ..... 11
1.1.9. TransFR™ Reconfiguration ..... 11
1.1.10. Enhanced System Level Support ..... 11
1.1.11. Broad Range of Package Options ..... 11
2. Architecture ..... 14
2.1. Architecture Overview ..... 14
2.2. PFU Blocks ..... 15
2.2.1. Slices ..... 16
2.2.2. Modes of Operation ..... 17
2.2.3. RAM Mode ..... 18
2.2.4. ROM Mode ..... 18
2.3. Routing ..... 18
2.4. Clock/Control Distribution Network ..... 18
2.4.1. sysCLOCK Phase Locked Loops (PLLs) ..... 20
2.5. sysMEM Embedded Block RAM Memory ..... 23
2.6. Programmable I/O Cells (PIC) ..... 27
2.7. PIO ..... 29
2.7.1. Input Register Block ..... 29
2.7.2. Output Register Block ..... 31
2.7.3. Tri-state Register Block ..... 32
2.8. Input Gearbox ..... 32
2.9. Output Gearbox ..... 34
2.10. DDR Memory Support ..... 36
2.11. DQS Read Write Block ..... 36
2.12. sysI/O Buffer ..... 36
2.12.1. Typical I/O Behavior During Power-up ..... 37
2.12.2. Supported Standards ..... 37
2.12.3. sysI/O Buffer Banks ..... 40
2.13. Hot Socketing ..... 41
2.14. On-chip Oscillator ..... 41
2.15. Embedded Hardened IP Functions and User Flash Memory ..... 42
2.15.1. Hardened $I^2C$ IP Core ..... 43
2.15.2. Hardened SPI IP Core ..... 44
2.15.3. Hardened Timer/Counter ..... 45
2.16. User Flash Memory (UFM) ..... 46
2.17. Standby Mode and Power Saving Options ..... 47
2.18. Power-On-Reset ..... 48
2.19. Configuration and Testing ..... 49
2.19.1. IEEE 1149.1-Compliant Boundary Scan Testability ..... 49
2.19.2. Device Configuration ..... 49
2.20. TraceID ..... 50
2.21. Density Shifting ..... 50

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

3. DC and Switching Characteristics....51
3.1. Absolute Maximum Ratings....51
3.2. Recommended Operating Conditions....51
3.3. Power Supply Ramp Rates....51
3.4. Power-On-Reset Voltage Levels....52
3.5. Programming/Erase Specifications....52
3.6. Hot Socketing Specifications....52
3.7. ESD Performance....52
3.8. DC Electrical Characteristics....53
3.9. Static Supply Current – ZE Devices....54
3.10. Static Power Consumption Contribution of Different Components – ZE Devices....54
3.11. Static Supply Current – HC/HE Devices....55
3.12. Programming and Erase Flash Supply Current – HC/HE Devices....56
3.13. Programming and Erase Flash Supply Current – ZE Devices....56
3.14. sysI/O Recommended Operating Conditions....57
3.15. sysI/O Single-Ended DC Electrical Characteristics....58
3.16. sysI/O Differential Electrical Characteristics....59
3.16.1. LVDS....59
3.16.2. LVDS Emulation....60
3.16.3. BLVDS....61
3.16.4. LVPECL....62
3.16.5. RSDS....63
3.17. Typical Building Block Function Performance – HC/HE Devices....64
3.17.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)....64
3.17.2. Register-to-Register Performance....64
3.18. Typical Building Block Function Performance – ZE Devices....65
3.18.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)....65
3.18.2. Register-to-Register Performance....65
3.19. Derating Logic Timing....65
3.20. Maximum sysI/O Buffer Performance....66
3.21. MachXO2 External Switching Characteristics – HC/HE Devices....67
3.22. MachXO2 External Switching Characteristics – ZE Devices....73
3.23. sysCLOCK PLL Timing....81
3.24. MachXO2 Oscillator Output Frequency....82
3.25. MachXO2 Standby Mode Timing – HC/HE Devices....82
3.26. MachXO2 Standby Mode Timing – ZE Devices....83
3.27. Flash Download Time....83
3.28. JTAG Port Timing Specifications....84
3.29. sysCONFIG Port Timing Specifications....85
3.30. $I^2C$ Port Timing Specifications....86
3.31. SPI Port Timing Specifications....86
3.32. Switching Test Conditions....86
4. Pinout Information....88
4.1. Signal Descriptions....88
4.2. Pinout Information Summary....90
4.3. For Further Information....95
4.4. Thermal Management....95
4.4.1. For Further Information....95
5. Ordering Information....96
5.1. MachXO2 Part Number Description....96
5.2. Ordering Information....97
5.2.1. Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging....97
5.2.2. High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging....99

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

5.2.3. High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging ..... 102
5.3. Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging ..... 103
5.3.1. High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging ..... 106
5.4. High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging ..... 109
5.5. R1 Device Specifications ..... 111
6. Supplemental Information ..... 112
Technical Support Assistance ..... 113
Revision History ..... 114

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# Figures

Figure 2.1. Top View of the MachXO2-1200 Device ....14
Figure 2.2. Top View of the MachXO2-4000 Device ....14
Figure 2.3. PFU Block Diagram ....15
Figure 2.4. Slice Diagram ....16
Figure 2.5. Primary Clocks for MachXO2 Devices ....19
Figure 2.6. Secondary High Fanout Nets for MachXO2 Devices ....20
Figure 2.7. PLL Diagram ....21
Figure 2.8. sysMEM Memory Primitives ....24
Figure 2.9. Memory Core Reset ....26
Figure 2.10. EBR Asynchronous Reset (Including GSR) Timing Diagram ....26
Figure 2.11. Group of Four Programmable I/O Cells ....28
Figure 2.12. MachXO2 Input Register Block Diagram (PIO on Left, Top and Bottom Edges) ....30
Figure 2.13. MachXO2 Input Register Block Diagram (PIO on Right Edge) ....30
Figure 2.14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges) ....31
Figure 2.15. MachXO2 Output Register Block Diagram (PIO on the Right Edges) ....32
Figure 2.16. Input Gearbox ....33
Figure 2.17. Output Gearbox ....35
Figure 2.18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks ....40
Figure 2.19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks ....40
Figure 2.20. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks ....42
Figure 2.21. $I^2C$ Core Block Diagram ....43
Figure 2.22. SPI Core Block Diagram ....44
Figure 2.23. Timer/Counter Block Diagram ....46
Figure 3.1. LVDS Using External Resistors (LVDS25E) ....60
Figure 3.2. BLVDS Multi-point Output Example ....61
Figure 3.3. Differential LVPECL ....62
Figure 3.4. RSDS (Reduced Swing Differential Standard) ....63
Figure 3.5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms ....78
Figure 3.6. Receiver RX.CLK.Centered Waveforms ....79
Figure 3.7. Transmitter TX.CLK.Aligned Waveforms ....79
Figure 3.8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms ....79
Figure 3.9. GDDR71 Video Timing Waveforms ....80
Figure 3.10. Receiver GDDR71_RX. Waveforms ....80
Figure 3.11. Transmitter GDDR71_TX. Waveforms ....80
Figure 3.12. JTAG Port Timing Waveforms ....84
Figure 3.13. Output Test Load, LVTTL and LVCMOS Standards ....86
Figure 5.1. MachXO2 Part Number Description ....96

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# Tables

Table 1.1. MachXO2 Family Selection Guide ..... 12
Table 2.1. Resources and Modes Available per Slice ..... 16
Table 2.2. Slice Signal Descriptions ..... 17
Table 2.3. Number of Slices Required For Implementing Distributed RAM ..... 18
Table 2.4. PLL Signal Descriptions ..... 22
Table 2.5. sysMEM Block Configurations ..... 23
Table 2.6. EBR Signal Descriptions ..... 24
Table 2.7. Programmable FIFO Flag Ranges ..... 25
Table 2.8. PIO Signal List ..... 29
Table 2.9. Input Gearbox Signal List ..... 32
Table 2.10. Output Gearbox Signal List ..... 34
Table 2.11. I/O Support Device by Device ..... 38
Table 2.12. Supported Input Standards ..... 38
Table 2.13. Supported Output Standards ..... 39
Table 2.14. Available MCLK Frequencies ..... 41
Table 2.15. Supported Input Standards ..... 43
Table 2.16. SPI Core Signal Description ..... 45
Table 2.17. Timer/Counter Signal Description ..... 46
Table 2.18. MachXO2 Power Saving Features Description ..... 47
Table 3.1. Absolute Maximum Ratings[1, 2, 3] ..... 51
Table 3.2. Recommended Operating Conditions[1] ..... 51
Table 3.3. Power Supply Ramp Rates ..... 51
Table 3.4. Power Supply Ramp Rates[1, 2, 3, 4, 5] ..... 52
Table 3.5. Programming/Erase Specifications ..... 52
Table 3.6. Hot Socketing Specifications[1, 2, 3] ..... 52
Table 3.7. DC Electrical Characteristics ..... 53
Table 3.8. Static Supply Current – ZE Devices[1, 2, 3, 6] ..... 54
Table 3.9. Static Power Consumption Contribution of Different Components – ZE Devices ..... 54
Table 3.10. Static Supply Current – HC/HE Devices[1, 2, 3, 6] ..... 55
Table 3.11. Programming and Erase Flash Supply Current – HC/HE Devices[1, 2, 3, 4] ..... 56
Table 3.12. Programming and Erase Flash Supply Current – ZE Devices[1, 2, 3, 4] ..... 56
Table 3.13. sysI/O Recommended Operating Conditions ..... 57
Table 3.14. sysI/O Single-Ended DC Electrical Characteristics[1, 2] ..... 58
Table 3.15. LVDS ..... 59
Table 3.16. LVDS25E DC Conditions ..... 60
Table 3.17. LVDS25E DC Conditions ..... 60
Table 3.18. BLVDS DC Conditions ..... 61
Table 3.19. LVPECL DC Conditions ..... 62
Table 3.20. RSDS DC Conditions ..... 63
Table 3.21. Pin-to-Pin Performance (LVCMOS25 12 mA Drive) ..... 64
Table 3.22. Register-to-Register Performance ..... 64
Table 3.23. Pin-to-Pin Performance (LVCMOS25 12 mA Drive) ..... 65
Table 3.24. Register-to-Register Performance ..... 65
Table 3.25. Maximum sysI/O Buffer Performance ..... 66
Table 3.26. MachXO2 External Switching Characteristics – HC/HE Devices[1, 2, 3, 4, 5, 6, 7] ..... 67
Table 3.27. MachXO2 External Switching Characteristics – ZE Devices[1, 2, 3, 4, 5, 6, 7] ..... 73
Table 3.28. sysCLOCK PLL Timing ..... 81
Table 3.29. MachXO2 Oscillator Output Frequency ..... 82
Table 3.30. MachXO2 Standby Mode Timing – HC/HE Devices ..... 82
Table 3.31. MachXO2 Standby Mode Timing – ZE Devices ..... 83
Table 3.32. Flash Download Time ..... 83
Table 3.33. JTAG Port Timing Specifications ..... 84

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

Table 3.34. sysCONFIG Port Timing Specifications ....85
Table 3.35. I²C Port Timing Specifications ....86
Table 3.36. SPI Port Timing Specifications ....86
Table 3.37. Test Fixture Required Components, Non-Terminated Interfaces ....87
Table 4.1. Signal Descriptions ....88
Table 4.2. MachXO2-256/MachXO2-640/MachXO2-640U Pin Summary ....90
Table 4.3. MachXO2-1200/MachXO2-1200U Pin Summary ....91
Table 4.4. MachXO2-2000/MachXO2-2000U Pin Summary ....92
Table 4.5. MachXO2-4000 Pin Summary ....93
Table 4.6. MachXO2-7000 Pin Summary ....94
Table 5.1. Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging ....97
Table 5.2. High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging ....99
Table 5.3. High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging 102
Table 5.4. Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging ....103
Table 5.5. High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging ....106
Table 5.6. High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging ....109
Table 5.7. R1 Device Specifications ....111

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---|---|
| BGA | Ball Grid Array |
| caBGA | ChipArray Ball Grill Array |
| CE | Clock Enable |
| CLK | System clock |
| CMOS | Complementary Metal Oxide Semiconductor |
| DDR | Double Data Rate |
| EBR | Embedded Block RAM |
| ECLK | Edge Clock |
| FCIN | Fast Carry In |
| FCO | Fast Carry Out |
| $I^2C$ | Inter-Integrated Circuit |
| IP | Intellectual Property |
| I/O | Input/Output |
| JTAG | Joint Test Action Group |
| LED | Light-emitting Diode |
| LSR | Local Set/Reset |
| LUT | Look-Up Table |
| LVCMOS | Low-Voltage CMOS |
| LVDS | Low-Voltage Differential Signaling |
| LVPECL | Low-Voltage Positive/Pseudo Emitter-Coupled Logic |
| LVTTL | Low Voltage Transistor to Transistor Logic |
| MIPI | Mobile Industry Processor Interface |
| MLVDS | Multipoint Low-Voltage Differential Signaling |
| PCI | Peripheral Component Interconnect |
| PCLK | Primary Clock |
| PDPR | Pseudo Dual Port RAM |
| PFU | Programmable Functional Unit |
| PIC | Programmable Interface Controllers |
| PIO | Programmed Input/Output |
| PLD | Programmable Logic Device |
| PLL | Phase Locked Loop |
| RAM | Random Access Memory |
| ROM | Read-only Memory |
| SDR | Single Data Rate |
| SHA | Secure Hash Algorithm |
| SPI | Serial Peripheral Interface |
| SPR | Single Port Random Access Memory |
| SRAM | Static Random Access Memory |
| TransFR™ | Transparent Field Reconfiguration |
| UFM | User Flash Memory |
| WLCSP | Wafer Level Chip Scale Package |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# 1. Introduction

The MachXO2™ family of ultra low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), preengineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, $I^2C$ controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65 nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/O and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in two versions – ultra low power (ZE) and high performance (HC and HE) devices. The ultra low power devices are offered in three speed grades –1, –2 and –3, with –3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: –4, –5 and –6, with –6 being the fastest. HC devices have an internal linear voltage regulator which supports external VCC supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external VCC supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 mm x 2.5 mm WLCSP to the 23 mm x 23 mm fpBGA. MachXO2 devices support density migration within the same package. Table 1.1 shows the LUT densities, package and I/O options, along with other key parameters.

The pre-engineered source synchronous logic implemented in the MachXO2 device family supports a broad range of interface standards, including LPDDR, DDR, DDR2 and 7:1 gearing for display I/O.

The MachXO2 devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pulldown and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO2 devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, keyboard scanner and similar state machines.

The MachXO2 devices also provide flexible, reliable and secure configuration from on-chip Flash memory. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the $I^2C$ port. Additionally, MachXO2 devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO2 family of devices. Popular logic synthesis tools provide synthesis library support for MachXO2. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO2 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO2 PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 1.1. Features

### 1.1.1. Flexible Logic Architecture

- Six devices with 256 to 6864 LUT4s and 18 to 334 I/O

### 1.1.2. Ultra Low Power Devices

- Advanced 65 nm low power process
- As low as 22 µW standby power
- Programmable low swing differential I/O
- Stand-by mode and other power saving options

### 1.1.3. Embedded and Distributed Memory

- Up to 240 kbits sysMEM™ Embedded Block RAM
- Up to 54 kbits Distributed RAM
- Dedicated FIFO control logic

### 1.1.4. On-Chip User Flash Memory

- Up to 256 kbits of User Flash Memory
- 100,000 write cycles
- Accessible through WISHBONE, SPI, $I^2C$ and JTAG interfaces
- Can be used as soft processor PROM or as Flash memory

### 1.1.5. Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/O
- Generic DDR, DDRX2, DDRX4
- Dedicated DDR/DDR2/LPDDR memory with DQS support

### 1.1.6. High Performance, Flexible I/O Buffer

- Programmable sysI/O™ buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTL
  - PCI
  - LVDS, Bus-LVDS, MLVDS, RSDS, LVPECL
  - SSTL 25/18
  - HSTL 18
  - MIPI D-PHY Emulated
  - Schmitt trigger inputs, up to 0.5 V hysteresis
  - I/O support hot socketing
  - On-chip differential termination
  - Programmable pull-up or pull-down mode

### 1.1.7. Flexible On-Chip Clocking

- Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
- Up to two analog PLLs per device with fractional-n frequency synthesis
  - Wide input frequency range (7 MHz to 400 MHz)

### 1.1.8. Non-volatile, Infinitely Reconfigurable

- Instant-on – powers up in microseconds
- Single-chip, secure solution
- Programmable through JTAG, SPI or $I^2C$
- Supports background programming of non-volatile memory
- Optional dual boot with external SPI memory

### 1.1.9. TransFR™ Reconfiguration

- In-field logic update while system operates

### 1.1.10. Enhanced System Level Support

- On-chip hardened functions: SPI, $I^2C$, timer/counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- One Time Programmable (OTP) mode
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

### 1.1.11. Broad Range of Package Options

- TQFP, WLCSP, ucBGA, csBGA, caBGA, ftBGA, fpBGA, QFN package options
- Small footprint package options
  - As small as 2.5 mm x 2.5 mm
- Density migration supported
- Advanced halogen-free packaging

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Table 1.1. MachXO2 Family Selection Guide**

| | | XO2-256 | XO2-640 | XO2-640U[1] | XO2-1200 | XO2-1200U[1] | XO2-2000 | XO2-2000U[1] | XO2-4000 | XO2-7000 |
|---|---|---|---|---|---|---|---|---|---|---|
| LUTs | | 256 | 640 | 640 | 1280 | 1280 | 2112 | 2112 | 4320 | 6864 |
| Distributed RAM (kbits) | | 2 | 5 | 5 | 10 | 10 | 16 | 16 | 34 | 34 |
| EBR SRAM (Kbits) | | 0 | 18 | 64 | 64 | 74 | 74 | 92 | 92 | 240 |
| Number of EBR SRAM Blocks (9 Kbits) | | 0 | 2 | 7 | 7 | 8 | 8 | 10 | 10 | 26 |
| UFM (kbits) | | 0 | 24 | 64 | 64 | 80 | 80 | 96 | 96 | 256 |
| Device Options: | HC[2] | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| | HE[3] | | | | | | Yes | Yes | Yes | Yes |
| | ZE[4] | Yes | Yes | | Yes | | Yes | | Yes | Yes |
| Number of PLLs | | 0 | 0 | 1 | 1 | 1 | 1 | 2 | 2 | 2 |
| Hardened Functions | $I^2C$ | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | SPI | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Timer/Counter | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **Packages** | | **I/O** | | | | | | | | |
| 25-ball WLCSP[5] (2.5 mm x 2.5 mm, 0.4 mm) | | | | | 18 | | | | | |
| 32 QFN[6] (5 mm x 5 mm, 0.5 mm) | | 21 | | | 21 | | | | | |
| 36-ball WLCSP[5] (2.5 mm x 2.5 mm, 0.4 mm) | | | | | 28 | | | | | |
| 48 QFN[8, 9] (7 mm x 7 mm, 0.5 mm) | | 40 | 40 | | | | | | | |
| 49-ball WLCSP[5] (3.2 mm x 3.2 mm, 0.4 mm) | | | | | | | 38 | | | |
| 64-ball ucBGA (4 mm x 4 mm, 0.4 mm) | | 44 | | | | | | | | |
| 81-ball WLCSP[5] (3.8 mm x 3.8 mm, 0.4 mm) | | | | | | | | | 63 | |
| 84 QFN[7] (7 mm x 7 mm, 0.5 mm) | | | | | | | | | 68 | |
| 100-pin TQFP (14 mm x 14 mm) | | 55 | 78 | | 79 | | 79 | | | |
| 132-ball csBGA (8 mm x 8 mm, 0.5 mm) | | 55 | 79 | | 104 | | 104 | | 104 | |
| 144-pin TQFP (20 mm x 20 mm) | | | | 107 | 107 | | 111 | | 114 | 114 |
| 184-ball csBGA[7] (8 mm x 8 mm, 0.5 mm) | | | | | | | | | 150 | |
| 256-ball caBGA (14 mm x 14 mm, 0.8 mm) | | | | | | | 206 | | 206 | 206 |
| 256-ball ftBGA (17 mm x 17 mm, 1.0 mm) | | | | | | 206 | 206 | | 206 | 206 |
| 332-ball caBGA (17 mm x 17 mm, 0.8 mm) | | | | | | | | | 274 | 278 |
| 484-ball ftBGA (23 mm x 23 mm, 1.0 mm) | | | | | | | | 278 | 278 | 334 |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Notes:**

1. Ultra high I/O device.
2. High performance with regulator – VCC = 2.5 V, 3.3 V
3. High performance without regulator – VCC = 1.2 V
4. Low power without regulator – VCC = 1.2 V
5. WLCSP package only available for ZE devices.
6. 32 QFN package only available for HC and ZE devices.
7. 184 csBGA package only available for HE devices.
8. 48-pin QFN information is 'Advanced'.
9. 48 QFN package only available for HC devices.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

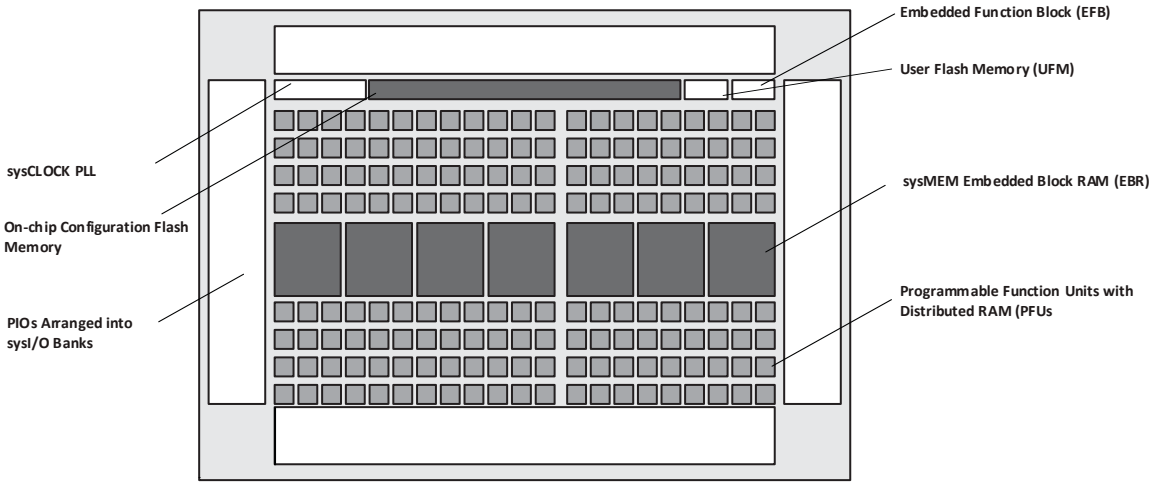


Downloaded from Arrow.com.

# 2. Architecture

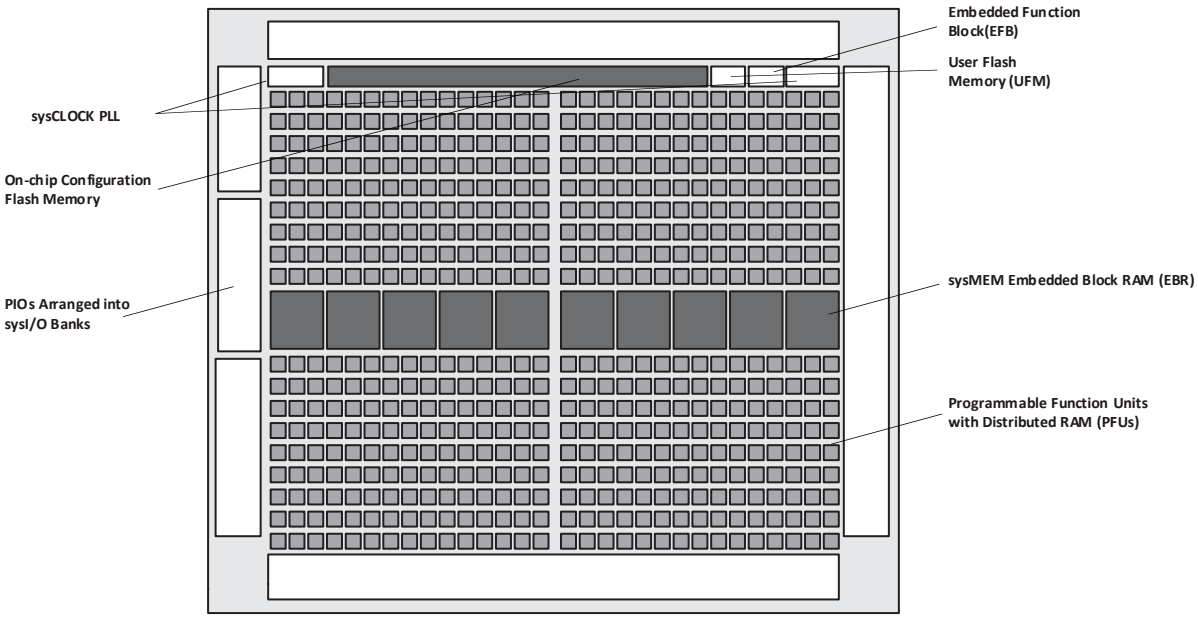
## 2.1. Architecture Overview

The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2.1 and Figure 2.2 show the block diagrams of the various family members.




Note: MachXO2-256, and MachXO2-640/U are similar to MachXO2-1200. MachXO2-256 has a lower LUT count and no PLL or EBR blocks. MachXO2-640 has no PLL, a lower LUT count and two EBR blocks. MachXO2-640U has a lower LUT count, one PLL and seven EBR blocks.

**Figure 2.1. Top View of the MachXO2-1200 Device**




Note: MachXO2-1200U, MachXO2-2000/U and MachXO2-7000 are similar to MachXO2-4000. MachXO2-1200U and MachXO2-2000 have a lower LUT count, one PLL, and eight EBR blocks. MachXO2-2000U has a lower LUT count, two PLLs, and 10 EBR blocks. MachXO2-7000 has a higher LUT count, two PLLs, and 26 EBR blocks.

**Figure 2.2. Top View of the MachXO2-4000 Device**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysI/O buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO2 family, the number of sysI/O banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found in MachXO2-640/U and larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO2 registers in PFU and sysI/O can be configured to be SET or RESET. After power-up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO2 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks on MachXO2- 640U, MachXO2-1200/U and larger devices. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO2 devices provide commonly used hardened functions such as SPI controller, $I^2C$ controller and timer/ counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, $I^2C$ and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO2 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

## 2.2. PFU Blocks

The core of the MachXO2 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2.3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

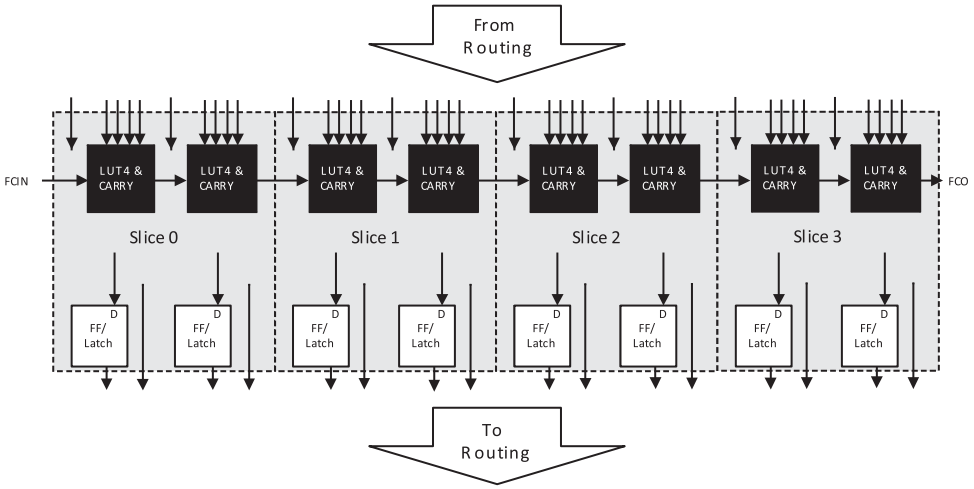



**Figure 2.3. PFU Block Diagram**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

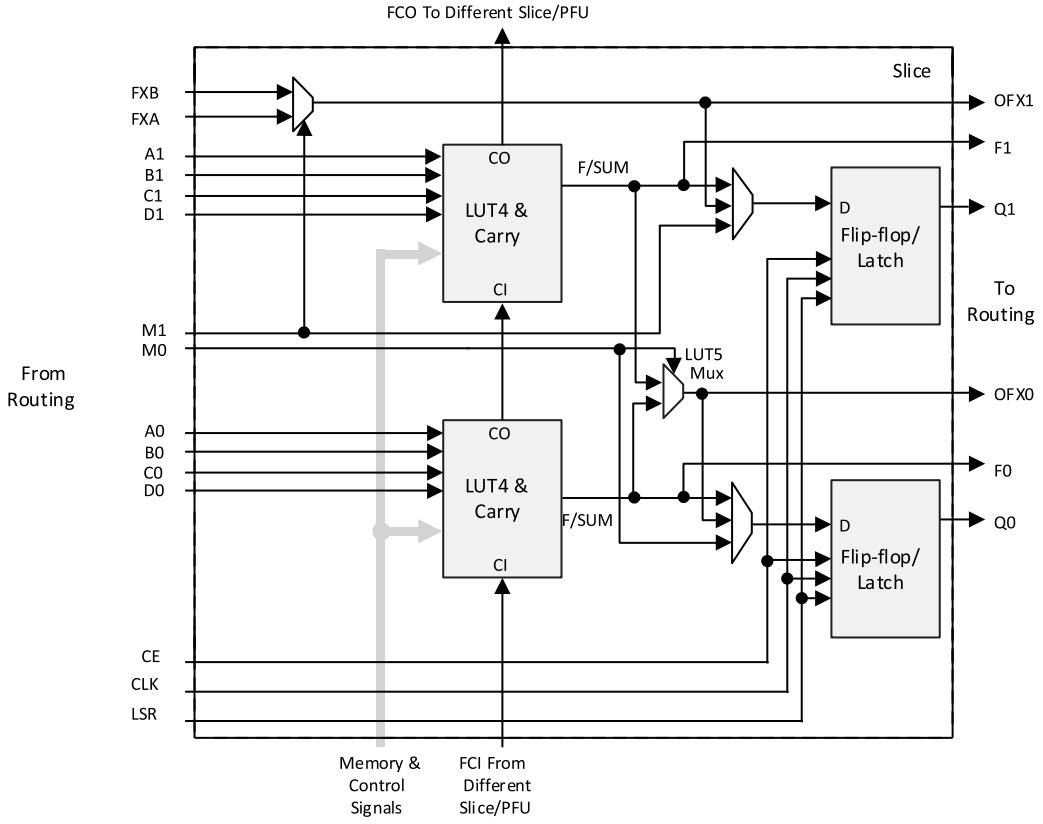
### 2.2.1. Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2.1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chipselect and wider RAM/ROM functions.

**Table 2.1. Resources and Modes Available per Slice**

| Slice | PFU Block | |
|---|---|---|
| | Resources | Modes |
| Slice 0 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM |
| Slice 3 | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |

Figure 2.4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/ negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2.2 lists the signals associated with Slices 0-3.




For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

**Figure 2.4. Slice Diagram**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Table 2.2. Slice Signal Descriptions**

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0/M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCIN | Fast Carry In[1] |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register Outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the Slice |
| Output | Inter-PFU signal | FCO | Fast Carry Out[1] |

**Notes:**

1. See Figure 2.3. for connection details.
2. Requires two PFUs.

## 2.2.2. Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

### Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

### Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
- A greater-than-or-equal-to B
- A not-equal-to B
- A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### 2.2.3. RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals. MachXO2 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO2 devices, see Memory Usage Guide for MachXO2 Devices (FPGA-TN-02159).

**Table 2.3. Number of Slices Required For Implementing Distributed RAM**

| | SPR 16x4 | PDPR 16x4 |
|---|---|---|
| Number of Slices | 3 | 3 |

**Note:** SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

### 2.2.4. ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, refer to Memory Usage Guide for MachXO2 Devices (FPGA-TN-02159).

## 2.3. Routing

There are many resources provided in the MachXO2 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## 2.4. Clock/Control Distribution Network

Each MachXO2 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO2 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO2-640U, MachXO2-1200/U and higher density devices have two edge clocks each on the top and bottom edges. Lower density devices have no edge clocks. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO2 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

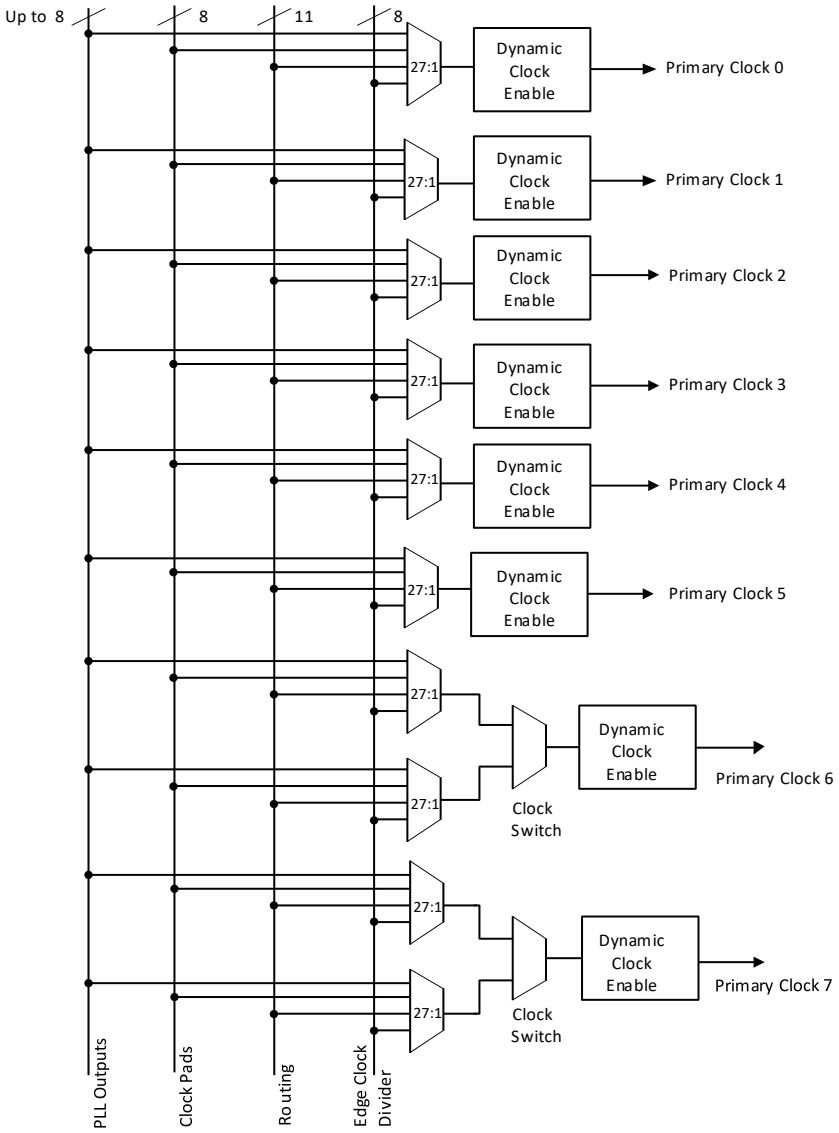
The maximum frequency for the primary clock network is shown in the MachXO2 External Switching Characteristics table.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

The primary clock signals for the MachXO2-256 and MachXO2-640 are generated from eight 17:1 muxes The available clock sources include eight I/O sources and 9 routing inputs. Primary clock signals for the MachXO2-640U, MachXO2-1200/U and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.




Primary clocks for MachXO2-640U, MachXO2-1200/U and larger devices.

Note: MachXO2-640 and smaller devices do not have inputs from the Edge Clock Divider or PLL and fewer routing inputs. These devices have 17:1 muxes instead of 27:1 muxes.

**Figure 2.5. Primary Clocks for MachXO2 Devices**

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2.6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in Table 3.26.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

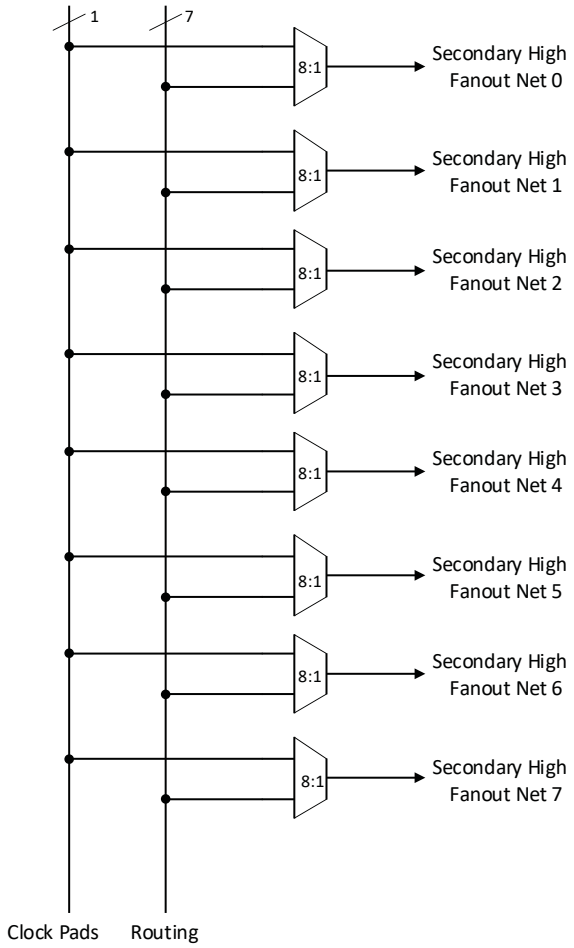



**Figure 2.6. Secondary High Fanout Nets for MachXO2 Devices**

### 2.4.1. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The MachXO2-640U, MachXO2-1200/U and larger devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO2 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, see MachXO2 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02157).

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO2 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2.7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

The MachXO2 also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO2 PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the tLOCK parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see MachXO2 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02157).

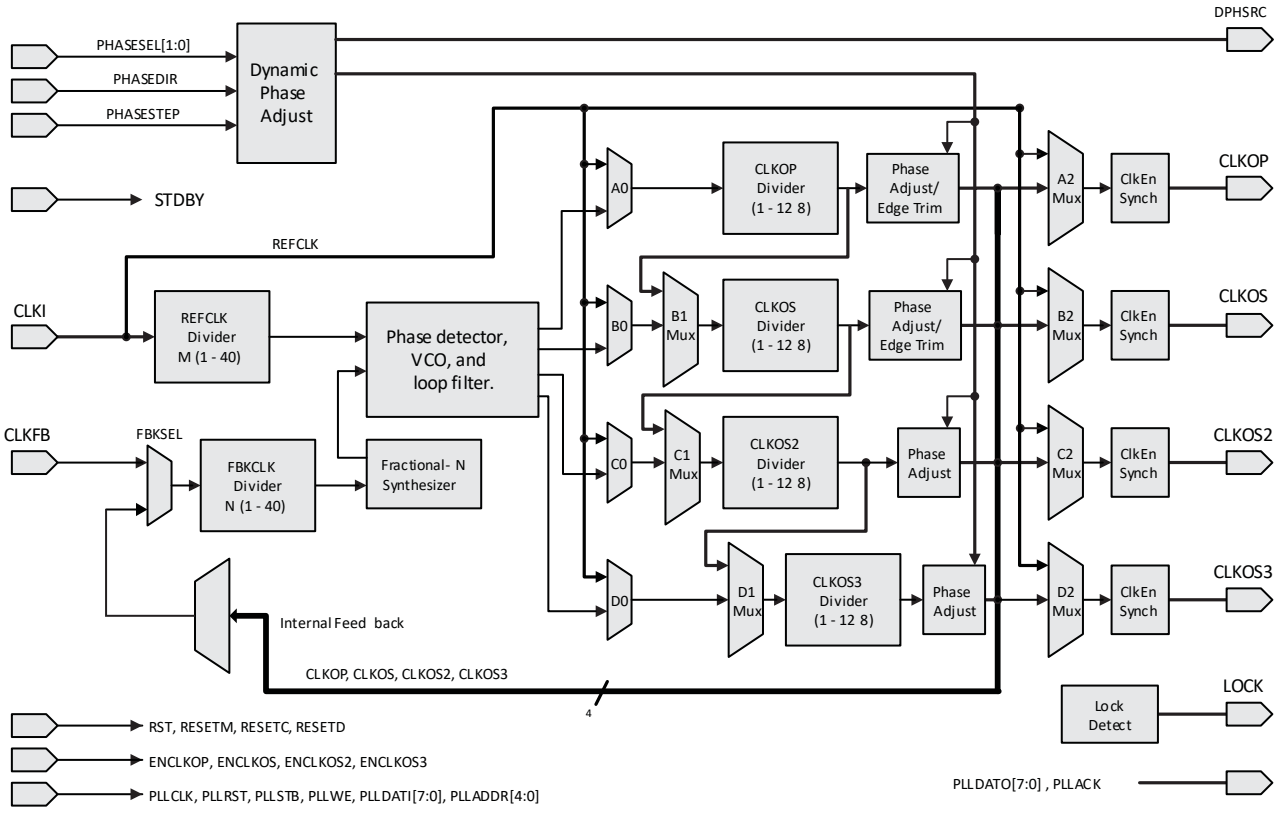



**Figure 2.7. PLL Diagram**

Table 2.4 provides signal descriptions of the PLL block.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Table 2.4. PLL Signal Descriptions**

| Port Name | I/O | Description |
|---|---|---|
| CLKI | I | Input clock to PLL |
| CLKFB | I | Feedback clock |
| PHASESEL[1:0] | I | Select which output is affected by Dynamic Phase adjustment ports |
| PHASEDIR | I | Dynamic Phase adjustment direction |
| PHASESTEP | I | Dynamic Phase step – toggle shifts VCO phase adjust by one step. |
| CLKOP | O | Primary PLL output clock (with phase shift adjustment) |
| CLKOS | O | Secondary PLL output clock (with phase shift adjust) |
| CLKOS2 | O | Secondary PLL output clock2 (with phase shift adjust) |
| CLKOS3 | O | Secondary PLL output clock3 (with phase shift adjust) |
| LOCK | O | PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals. |
| DPHSRC | O | Dynamic Phase source – ports or WISHBONE is active |
| STDBY | I | Standby signal to power down the PLL |
| RST | I | PLL reset without resetting the M-divider. Active high reset. |
| RESETM | I | PLL reset - includes resetting the M-divider. Active high reset. |
| RESETC | I | Reset for CLKOS2 output divider only. Active high reset. |
| RESETD | I | Reset for CLKOS3 output divider only. Active high reset. |
| ENCLKOP | I | Enable PLL output CLKOP |
| ENCLKOS | I | Enable PLL output CLKOS when port is active |
| ENCLKOS2 | I | Enable PLL output CLKOS2 when port is active |
| ENCLKOS3 | I | Enable PLL output CLKOS3 when port is active |
| PLLCLK | I | PLL data bus clock input signal |
| PLLRST | I | PLL data bus reset. This resets only the data bus not any register values. |
| PLLSTB | I | PLL data bus strobe signal |
| PLLWE | I | PLL data bus write enable signal |
| PLLADDR [4:0] | I | PLL data bus address |
| PLLDATI [7:0] | I | PLL data bus data input |
| PLLDATO [7:0] | O | PLL data bus data output |
| PLLACK | O | PLL data bus acknowledge signal |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 2.5. sysMEM Embedded Block RAM Memory

The MachXO2-640/U and larger devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2.5.

**Table 2.5. sysMEM Block Configurations**

| Memory Mode | Configurations |
|---|---|
| Single Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9 |
| True Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9 |
| Pseudo Dual Port | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |
| FIFO | 8,192 x 1<br>4,096 x 2<br>2,048 x 4<br>1,024 x 9<br>512 x 18 |

### Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

### RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO2 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

### Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

### Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2.8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

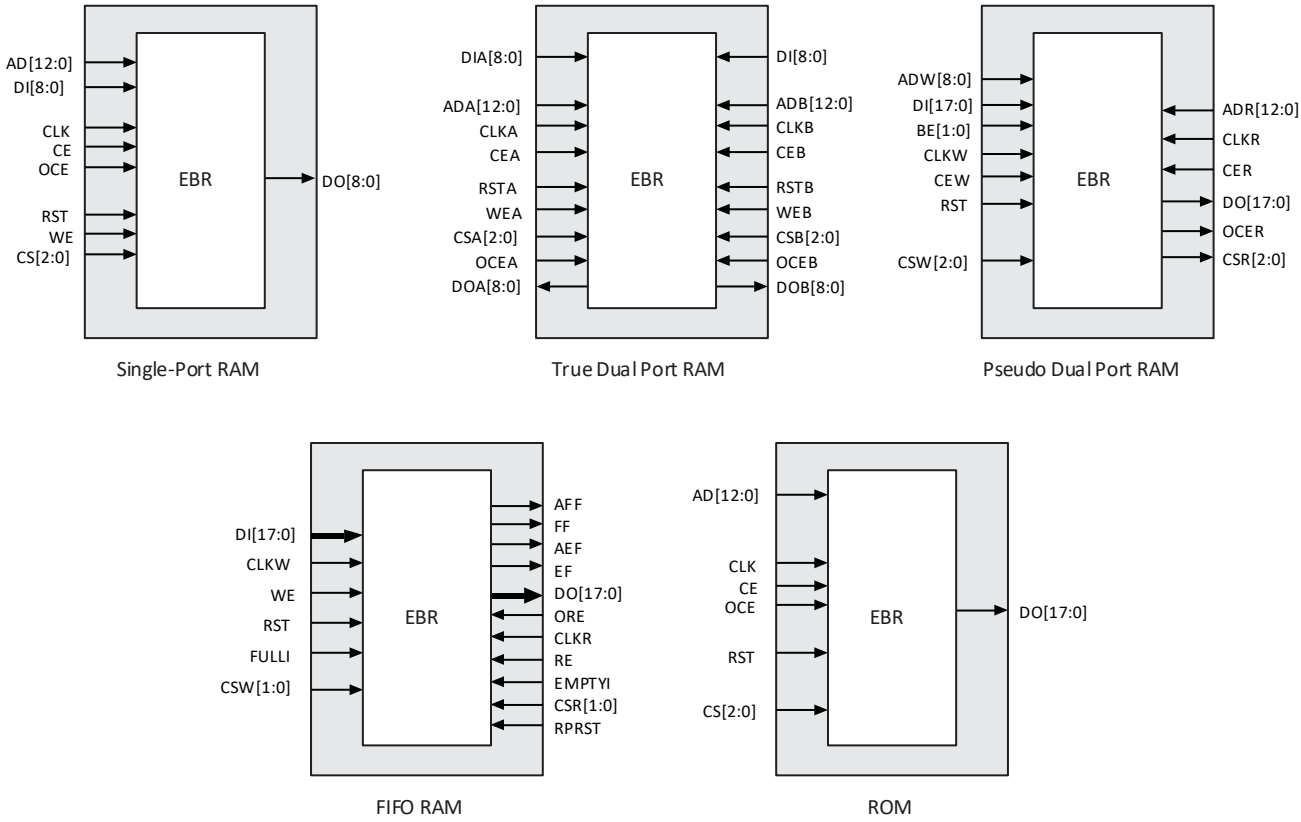



**Figure 2.8. sysMEM Memory Primitives**

**Table 2.6. EBR Signal Descriptions**

| Port Name | Description | Active State |
|---|---|---|
| CLK | Clock | Rising Clock Edge |
| CE | Clock Enable | Active High |
| OCE1 | Output Clock Enable | Active High |
| RST | Reset | Active High |
| BE1 | Byte Enable | Active High |
| WE | Write Enable | Active High |
| AD | Address Bus | — |
| DI | Data In | — |
| DO | Data Out | — |
| CS | Chip Select | Active High |
| AFF | FIFO RAM Almost Full Flag | — |
| FF | FIFO RAM Full Flag | — |
| AEF | FIFO RAM Almost Empty Flag | — |
| EF | FIFO RAM Empty Flag | — |
| RPRST | FIFO RAM Read Pointer Reset | — |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Notes:**

1. Optional signals.
2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

### FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2.7 shows the range of programming values for these flags.

**Table 2.7. Programmable FIFO Flag Ranges**

| Flag Name | Programming Range |
|---|---|
| Full (FF) | 1 to max (up to 2N-1) |
| Almost Full (AF) | 1 to Full-1 |
| Almost Empty (AE) | 1 to Full-1 |
| Empty (EF) | 0 |

**Note:** N = Address bit width

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

### Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2.9.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

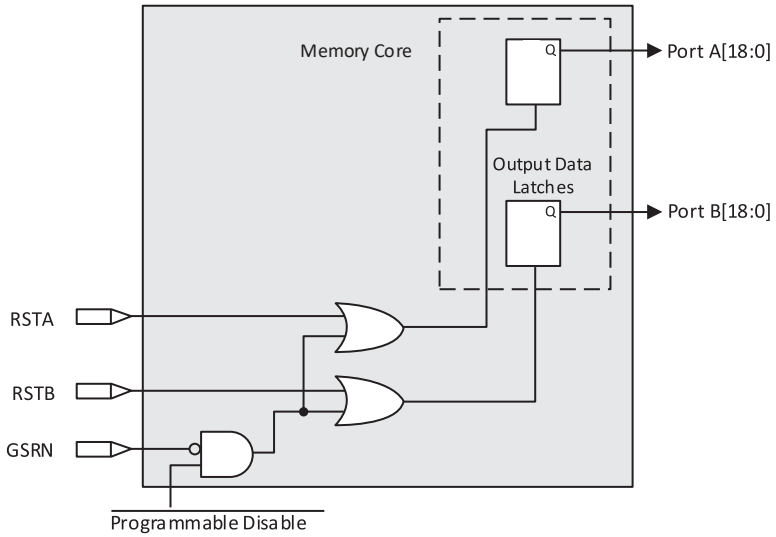



**Figure 2.9. Memory Core Reset**

For further information on the sysMEM EBR block, refer to Memory Usage Guide for MachXO2 Devices (FPGA-TN-02159).

### EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2.10. The GSR input to the EBR is always asynchronous.

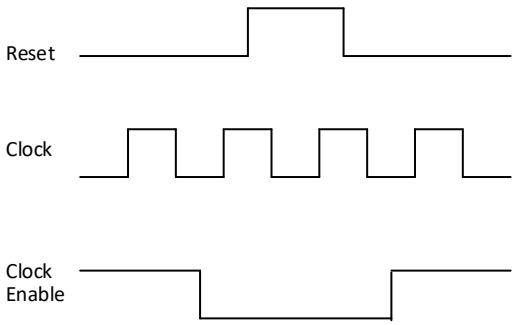



**Figure 2.10. EBR Asynchronous Reset (Including GSR) Timing Diagram**

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/O becoming active.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2.10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to Memory Usage Guide for MachXO2 Devices (FPGA-TN-02159).

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

## 2.6. Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysI/O buffers and pads. On the MachXO2 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

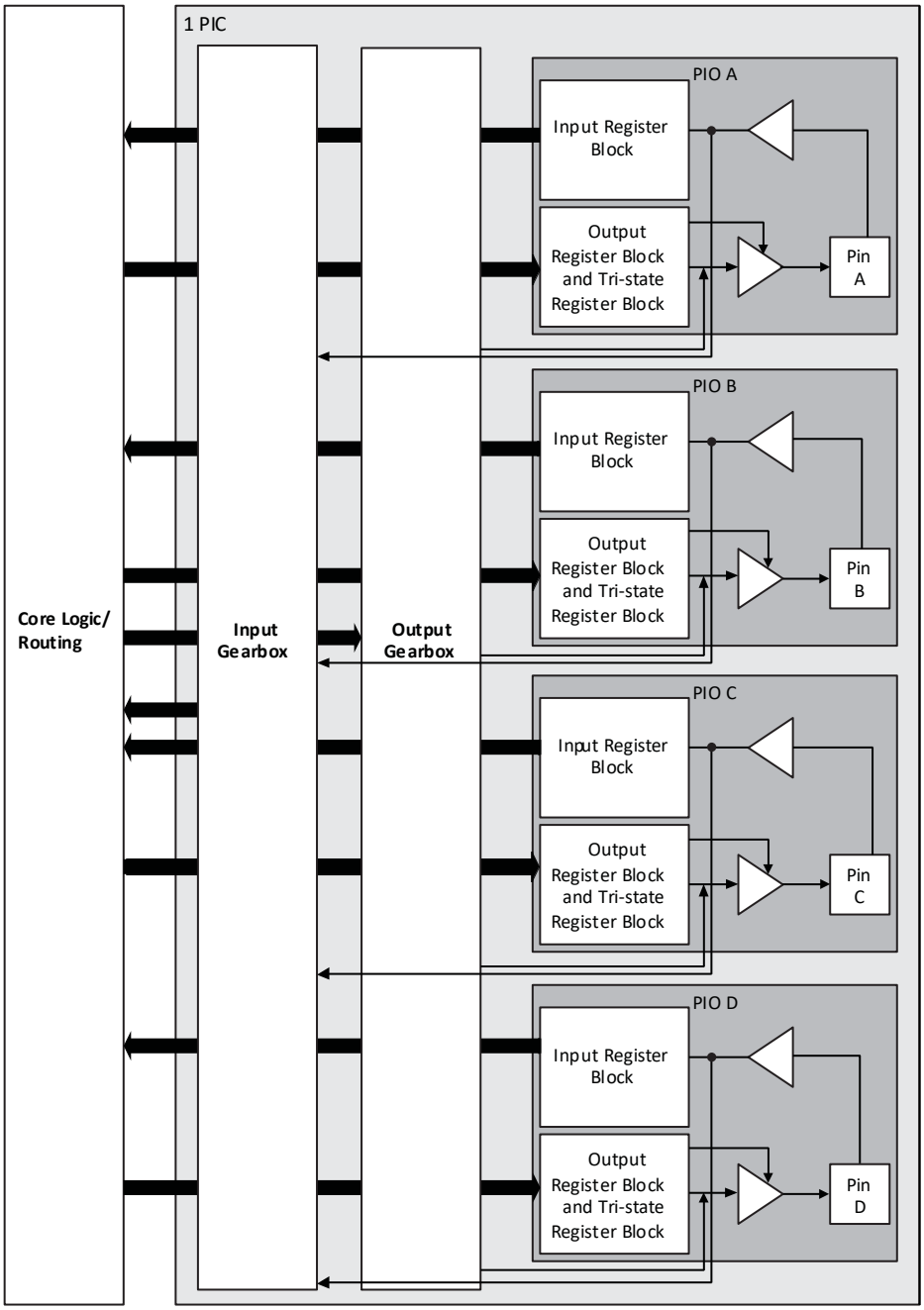
On all the MachXO2 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

The MachXO2-640U, MachXO2-1200/U and higher density devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these higher density devices have on-chip differential termination and also provide PCI support.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.




Notes:
1. Input gearbox is available only in PIC on the bottom edge of MachXO2-640U, MachXO2-1200/U and larger devices.
2. Output gearbox is available only in PIC on the top edge of MachXO2-640U, MachXO2-1200/U and larger devices.

**Figure 2.11. Group of Four Programmable I/O Cells**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 2.7. PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

**Table 2.8. PIO Signal List**

| Pin Name | I/O Type | Description |
|---|---|---|
| CE | Input | Clock Enable |
| D | Input | Pin input from sysI/O buffer |
| INDD | Output | Register bypassed input |
| INCK | Output | Clock input |
| Q0 | Output | DDR positive edge input |
| Q1 | Output | Registered input/DDR negative edge input |
| D0 | Input | Output signal from the core (SDR and DDR) |
| D1 | Input | Output signal from the core (DDR) |
| TD | Input | Tri-state signal from the core |
| Q | Output | Data output signals to sysI/O Buffer |
| TQ | Output | Tri-state output signals to sysI/O Buffer |
| DQSR90 | Input | DQS shift 90-degree read clock |
| DQSW90 | Input | DQS shift 90-degree write clock |
| DDRCLKPOL | Input | DDR input register polarity control signal from DQS |
| SCLK | Input | System clock for input and output/tri-state blocks |
| RST | Input | Local set reset signal |

**Note:** Available in PIO on right edge only.

### 2.7.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition to this functionality, the input register blocks for the PIOs on the right edge include built-in logic to interface to DDR memory.

Figure 2.12 shows the input register block for the PIOs located on the left, top and bottom edges. Figure 2.13 shows the input register block for the PIOs on the right edge.

#### Left, Top, Bottom Edges

Input signals are fed from the sysI/O buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/O on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

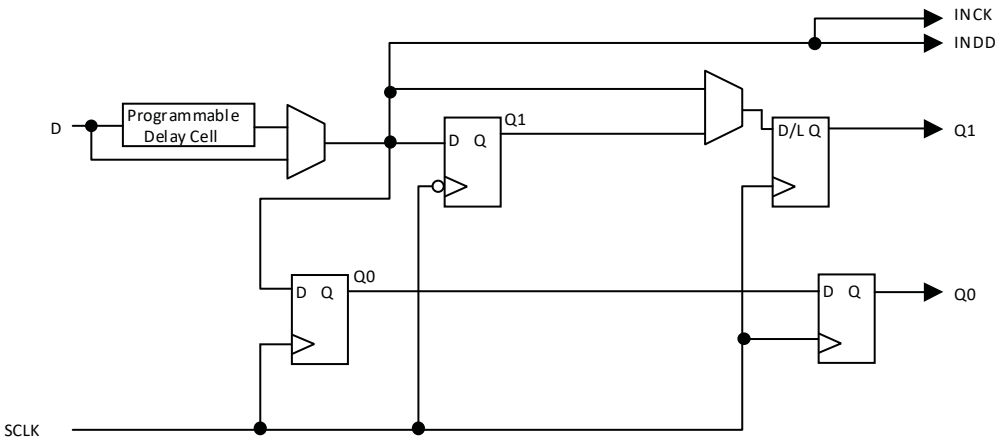



**Figure 2.12. MachXO2 Input Register Block Diagram (PIO on Left, Top and Bottom Edges)**

### Right Edge

The input register block on the right edge is a superset of the same block on the top, bottom, and left edges. In addition to the modes described above, the input register block on the right edge also supports DDR memory mode.

In DDR memory mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (DQSR90) in the DDR Memory mode creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the DQS domain. The DQSR90 and DDRCLKPOL signals are generated in the DQS read-write block.

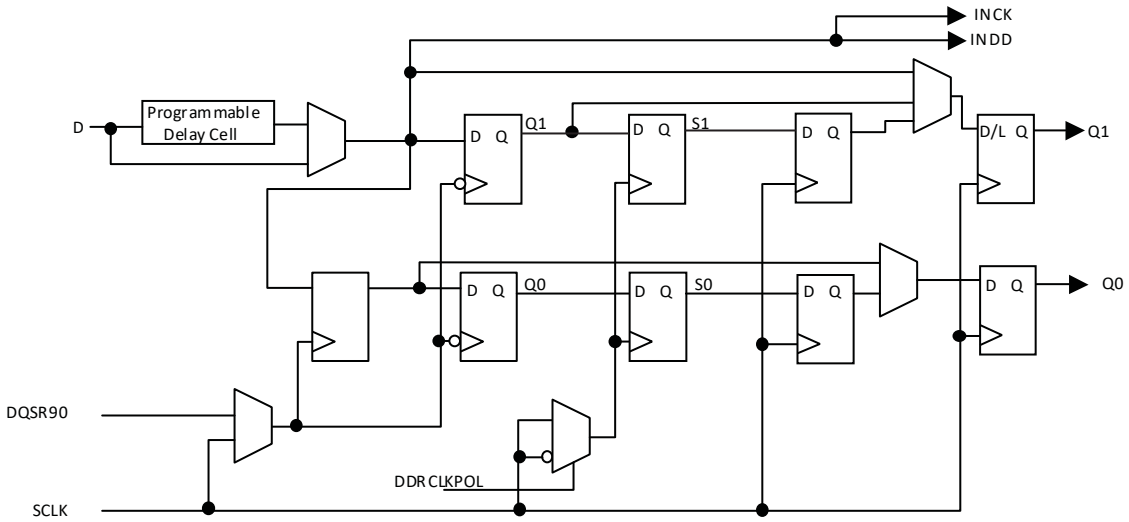



**Figure 2.13. MachXO2 Input Register Block Diagram (PIO on Right Edge)**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 2.7.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers.

**Left, Top, Bottom Edges**

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2.14 shows the output register block on the left, top and bottom edges.

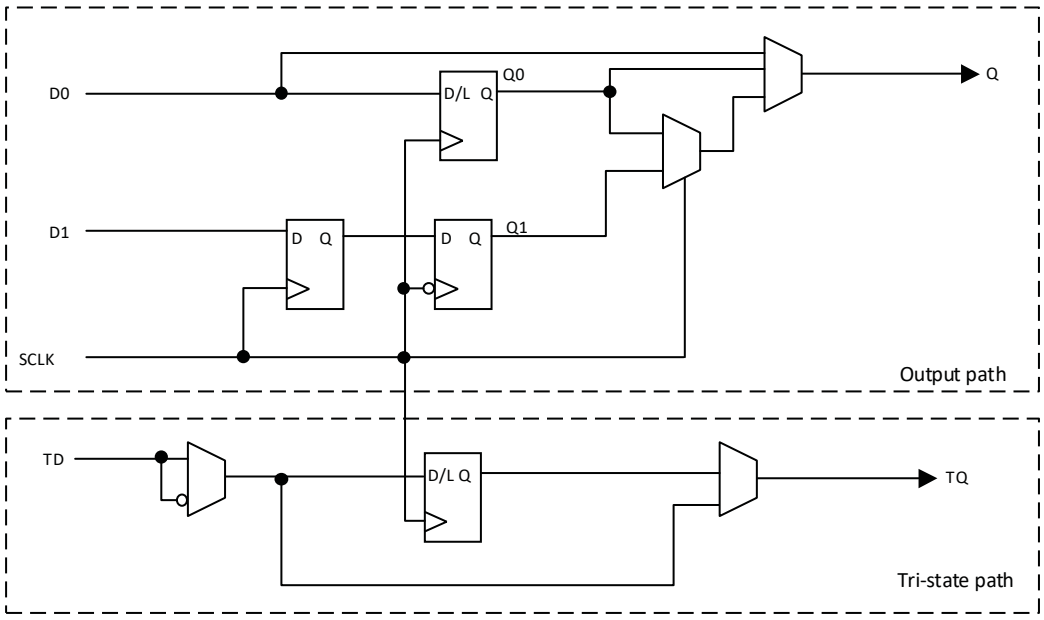



**Figure 2.14. MachXO2 Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)**

**Right Edge**

The output register block on the right edge is a superset of the output register on left, top and bottom edges of the device. In addition to supporting SDR and Generic DDR modes, the output register blocks for PIOs on the right edge include additional logic to support DDR-memory interfaces. Operation of this block is similar to that of the output register block on other edges.

In DDR memory mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the DQSW90 signal is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2.15 shows the output register block on the right edge.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

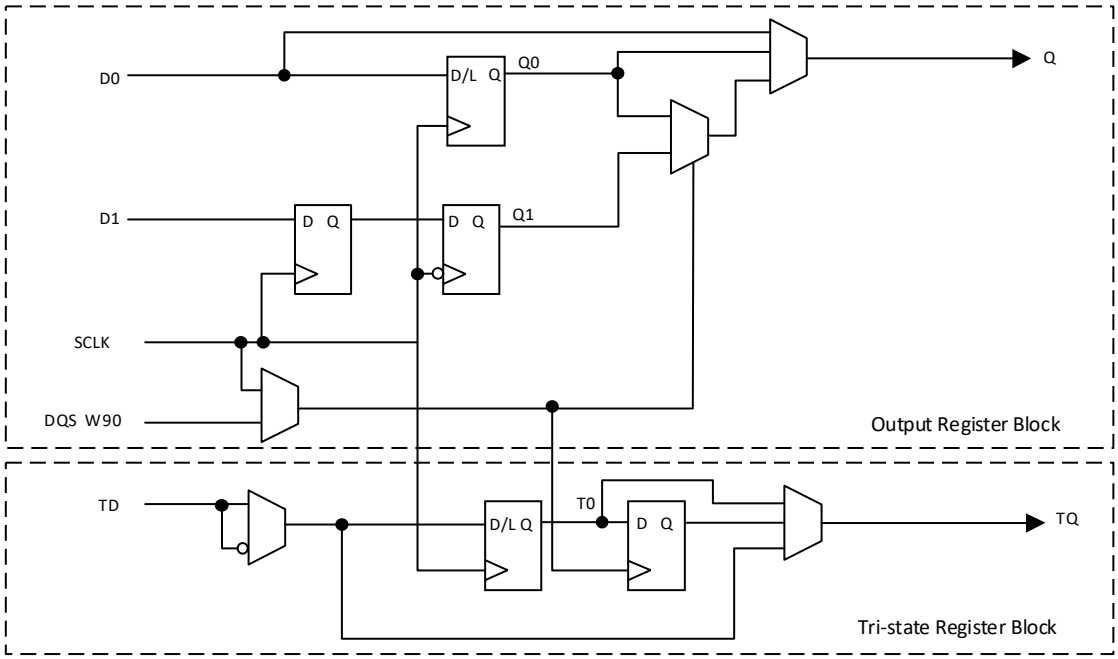



**Figure 2.15. MachXO2 Output Register Block Diagram (PIO on the Right Edges)**

### 2.7.3. Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

The tri-state register blocks on the right edge contain an additional register for DDR memory operation. In DDR memory mode, the register TS input is fed into another register that is clocked using the DQSW90 signal. The output of this register is used as a tri-state control.

## 2.8. Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2.9 shows the gearbox signals.

**Table 2.9. Input Gearbox Signal List**

| Name | I/O Type | Description |
|---|---|---|
| D | Input | High-speed data input after programmable delay in PIO A input register block |
| ALIGNWD | Input | Data alignment signal from device core |
| SCLK | Input | Slow-speed system clock |
| ECLK[1:0] | Input | High-speed edge clock |
| RST | Input | Reset |
| Q[7:0] | Output | Low-speed data to device core:<br>Video RX(1:7): Q[6:0]<br>GDDRX4(1:8): Q[7:0]<br>GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7<br>GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3 |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2.16 shows a block diagram of the input gearbox.

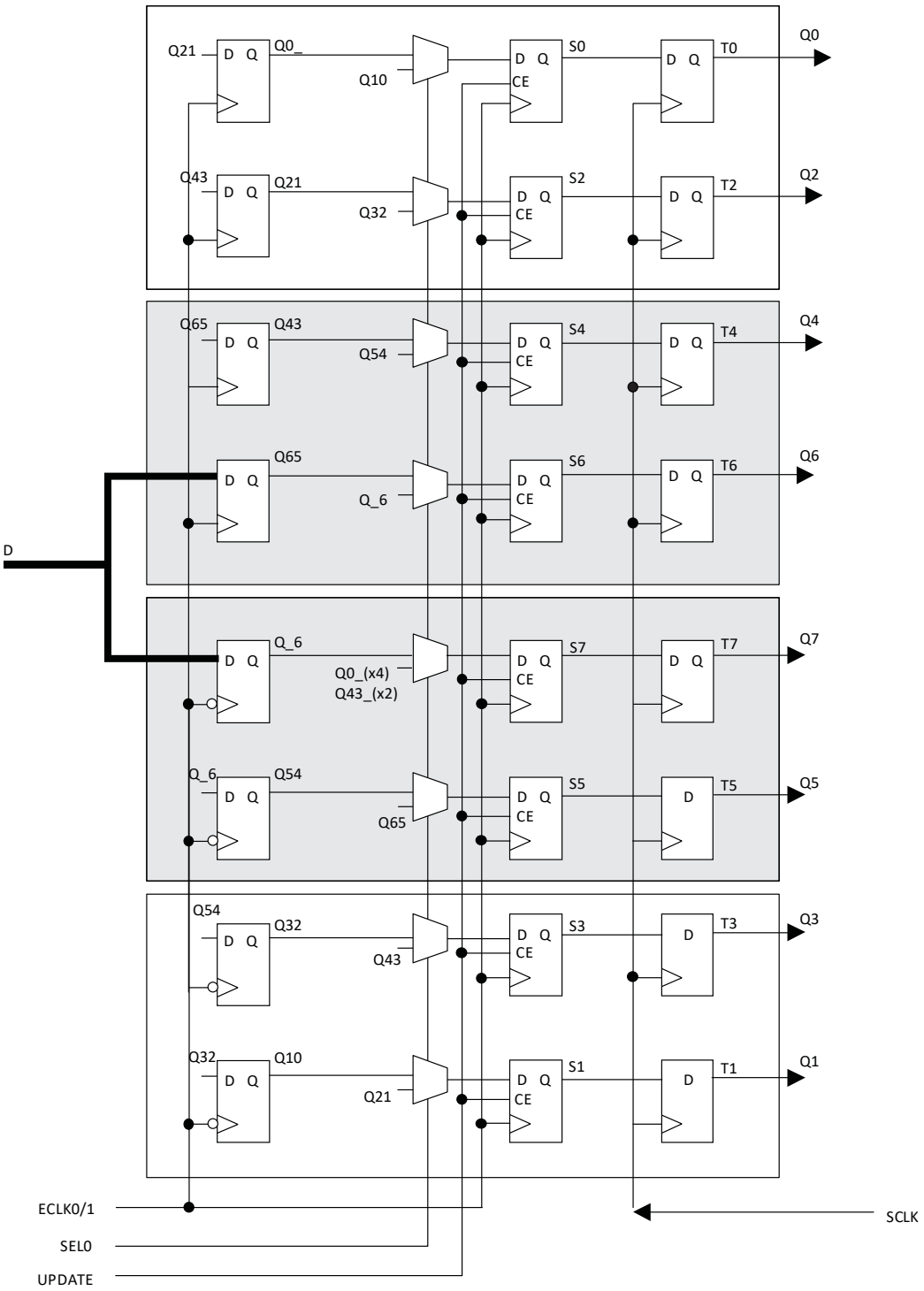



**Figure 2.16. Input Gearbox**

More information on the input gearbox is available in Implementing High-Speed Interfaces with MachXO2 Devices (FPGA-TN-02153).

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 2.9. Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2.10 shows the gearbox signals.

**Table 2.10. Output Gearbox Signal List**

| Name | I/O Type | Description |
|---|---|---|
| Q | Output | High-speed data output |
| D[7:0] | Input | Low-speed data from device core |
| Video TX(7:1): D[6:0] | — | — |
| GDDRX4(8:1): D[7:0] | — | — |
| GDDRX2(4:1)(IOL-A): D[3:0] | — | — |
| GDDRX2(4:1)(IOL-C): D[7:4] | — | — |
| SCLK | Input | Slow-speed system clock |
| ECLK [1:0] | Input | High-speed edge clock |
| RST | Input | Reset |

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the highspeed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysI/O buffer. Figure 2.17 shows the output gearbox block diagram.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

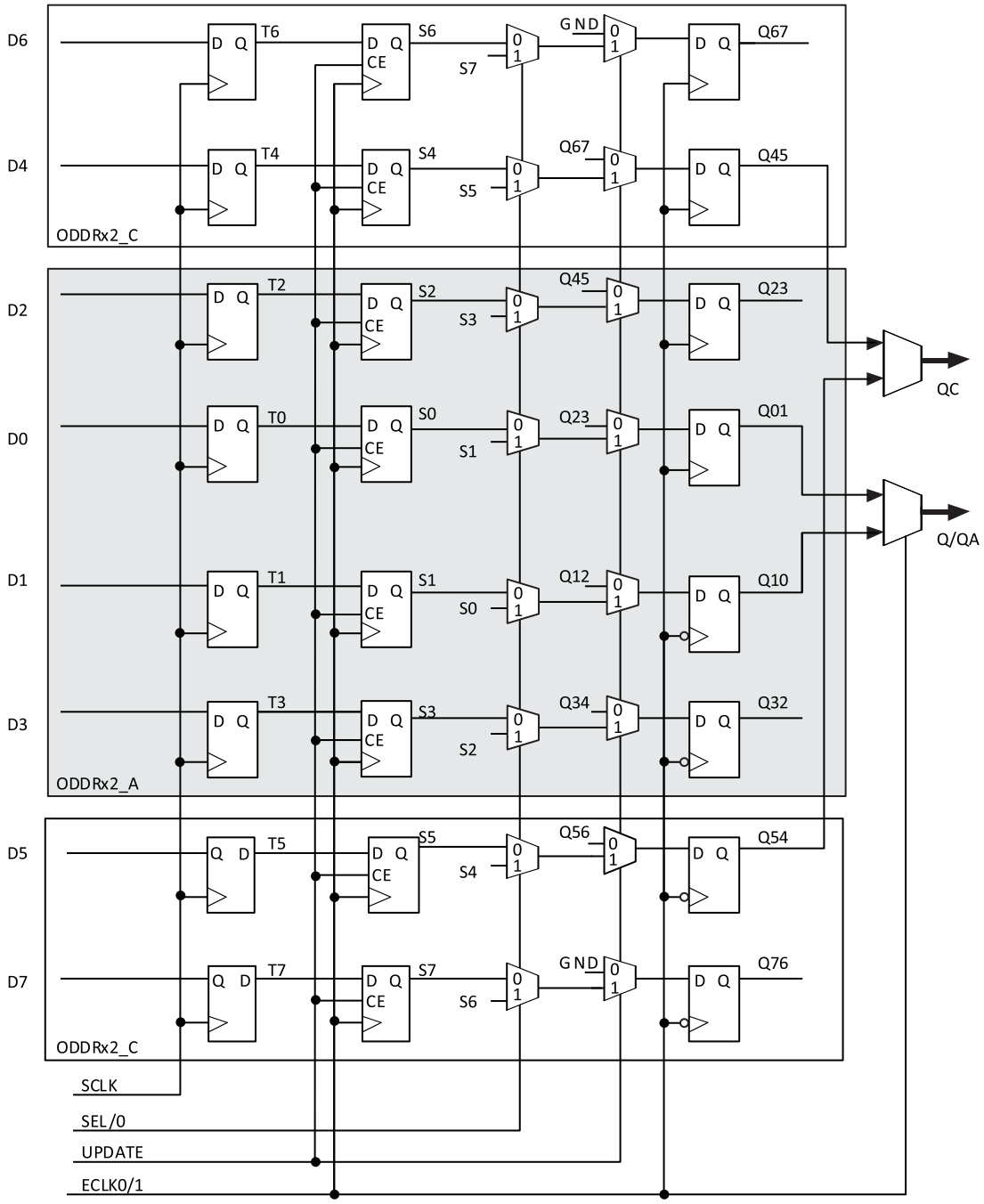



**Figure 2.17. Output Gearbox**

More information on the output gearbox is available in Implementing High-Speed Interfaces with MachXO2 Devices (FPGA-TN-02153).

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 2.10. DDR Memory Support

Certain PICs on the right edge of MachXO2-640U, MachXO2-1200/U and larger devices, have additional circuitry to allow the implementation of DDR memory interfaces. There are two groups of 14 or 12 PIOs each on the right edge with additional circuitry to implement DDR memory interfaces. This capability allows the implementation of up to 16-bit wide memory interfaces. One PIO from each group contains a control element, the DQS Read/Write Block, to facilitate the generation of clock and control signals (DQSR90, DQSW90, DDRCLKPOL and DATAVALID). These clock and control signals are distributed to the other PIO in the group through dedicated low skew routing.

## 2.11. DQS Read Write Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Read Write block provides the required clock alignment for DDR memory interfaces. DQSR90 and DQSW90 signals are generated by the DQS Read Write block from the DQS input.

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the read cycle) is unknown. The MachXO2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This circuit changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each read cycle for the correct clock polarity. Prior to the read operation in DDR memories, DQS is in tri-state (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit in the DQS Read Write block detects the first DQS rising edge after the preamble state and generates the DDRCLKPOL signal. This signal is used to control the polarity of the clock to the synchronizing registers.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration signals (6-bit bus) from a DLL on the right edge of the device. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

## 2.12. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, SSTL, HSTL, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO2 devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) and referenced input buffers (SSTL and HSTL) are powered using I/O supply voltage ($V_{CCIO}$). Each sysI/O bank has its own $V_{CCIO}$. In addition, each bank has a voltage reference, $V_{REF}$, which allows the use of referenced input buffers independent of the bank $V_{CCIO}$.

MachXO2-256 and MachXO2-640 devices contain single-ended ratioed input buffers and single-ended output buffers with complementary outputs on all the I/O banks. Note that the single-ended input buffers on these devices do not contain PCI clamps. In addition to the single-ended I/O buffers these two devices also have differential and referenced input buffers on all I/O. The I/O are arranged in pairs, the two pads in the pair are described as "T" and "C", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 devices contain three types of sysI/O buffer pairs.

1. Left and Right sysI/O Buffer Pairs

   The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential and referenced input buffers.

2. Bottom sysI/O Buffer Pairs

   The sysI/O buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential and referenced input buffers. Only the I/O on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after $V_{CC}$ and $V_{CCIO}$ are at valid operating levels and the device has been configured.

3. Top sysI/O Buffer Pairs

   The sysI/O buffer pairs in the top bank of the device consist of two single-ended output drivers and two singleended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential and referenced I/O buffers. Half of the sysI/O buffer pairs on the top edge have true differential outputs. The sysI/O buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver. The referenced input buffer can also be configured as a differential input buffer.

### 2.12.1. Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$ and $V_{CCIO0}$ have reached $V_{PORUP}$ level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all VCCIO banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pulldown to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to $V_{CCIO}$ as the default functionality). The I/O pins will maintain the blank configuration until $V_{CC}$ and $V_{CCIO}$ (for I/O banks containing configuration I/O) have reached $V_{PORUP}$ levels at which time the I/O will take on the user-configured settings only after a proper download/configuration.

### 2.12.2. Supported Standards

The MachXO2 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO2-640U, MachXO2-1200/U and higher devices support on-chip LVDS output buffers on approximately 50% of the I/O on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO2 devices. PCI support is provided in the bottom bank of theMachXO2-640U, MachXO2-1200/U and higher density devices. Table 2.11 summarizes the I/O characteristics of the MachXO2 PLDs.

Table 2.11 and Table 2.12 show the I/O standards (together with their supply and reference voltages) supported by the MachXO2 devices. For further information on utilizing the sysI/O buffer to support a variety of standards see MachXO2 sysIO Usage Guide (FPGA-TN-02158).

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Table 2.11. I/O Support Device by Device**

| | MachXO2-256, MachXO2-640 | MachXO2-640U, MachXO2-1200 | MachXO2-1200U, MachXO2-2000/U, MachXO2-4000, MachXO2-7000 |
|---|---|---|---|
| Number of I/O Banks | 4 | 4 | 6 |
| Type of Input Buffers | Single-ended (all I/O banks)<br>Differential Receivers (all I/O banks) | Single-ended (all I/O banks)<br>Differential Receivers (all I/O banks)<br>Differential input termination (bottom side) | Single-ended (all I/O banks)<br>Differential Receivers (all I/O banks)<br>Differential input termination (bottom side) |
| Types of Output Buffers | Single-ended buffers with complementary outputs (all I/O Banks) | Single-ended buffers with complementary outputs (all I/O banks)<br>Differential buffers with true LVDS outputs (50% on top side) | Single-ended buffers with complementary outputs (all I/O banks)<br>Differential buffers with true LVDS outputs (50% on top side) |
| Differential Output Emulation Capability | All I/O Banks | All I/O Banks | All I/O Banks |
| PCI Clamp Support | No | Clamp on bottom side only | Clamp on bottom side only |

**Table 2.12. Supported Input Standards**

| | VCCIO (Typ.) | | | | |
|---|---|---|---|---|---|
| **Input Standard** | **3.3 V** | **2.5 V** | **1.8 V** | **1.5 V** | **1.2 V** |
| **Single Ended Interfaces** | | | | | |
| LVTTL | ✓ | ✓[2] | ✓[2] | ✓[2] | |
| LVCMOS33 | ✓ | ✓[2] | ✓[2] | ✓[2] | |
| LVCMOS25 | ✓[2] | ✓ | ✓[2] | ✓[2] | |
| LVCMOS18 | ✓[2] | ✓[2] | ✓ | ✓[2] | |
| LVCMOS15 | ✓[2] | ✓[2] | ✓[2] | ✓ | ✓[2] |
| LVCMOS12 | ✓[2] | ✓[2] | ✓[2] | ✓[2] | ✓ |
| PCI[1] | ✓ | | | | |
| SSTL18 (Class I, Class II) | ✓ | ✓ | ✓ | ✓ | |
| SSTL25 (Class I, Class II) | ✓ | ✓ | | | |
| HSTL18 (Class I, Class II) | ✓ | ✓ | ✓ | ✓ | |
| **Differential Interfaces** | | | | | |
| LVDS | ✓ | ✓ | | | |
| MIPI[3] | ✓ | ✓ | | | |
| Differential SSTL18 Class I, II | ✓ | ✓ | ✓ | ✓ | |
| Differential SSTL25 Class I, II | ✓ | ✓ | | | |
| Differential HSTL18 Class I, II | ✓ | ✓ | ✓ | ✓ | |

**Notes:**

1. Bottom banks of MachXO2-640U, MachXO2-1200/U and higher density devices only.
2. Reduced functionality. Refer to MachXO sysIO Usage Guide (FPGA-TN-02169) for more details.
3. These interfaces can be emulated with external resistors in all devices. Refer to MIPI D-PHY Bandwidth Matrix and Implementation (FPGA-TN-02090) for more details.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Table 2.13. Supported Output Standards**

| Output Standard | VCCIO (Typ.) |
|---|---|
| **Single-Ended Interfaces** | |
| LVTTL | 3.3 |
| LVCMOS33 | 3.3 |
| LVCMOS25 | 2.5 |
| LVCMOS18 | 1.8 |
| LVCMOS15 | 1.5 |
| LVCMOS12 | 1.2 |
| LVCMOS33, Open Drain | — |
| LVCMOS25, Open Drain | — |
| LVCMOS18, Open Drain | — |
| LVCMOS15, Open Drain | — |
| LVCMOS12, Open Drain | — |
| PCI333 | 3.3 |
| SSTL25 (Class I) | 2.5 |
| SSTL18 (Class I) | 1.8 |
| HSTL18(Class I) | 1.8 |
| **Differential Interfaces** | |
| LVDS[1, 2] | 2.5, 3.3 |
| BLVDS, MLVDS, RSDS[2] | 2.5 |
| LVPECL[2] | 3.3 |
| MIPI[2] | 2.5 |
| Differential SSTL18 | 1.8 |
| Differential SSTL25 | 2.5 |
| Differential SSTL25 | 1.8 |

**Notes:**

1. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### 2.12.3. sysI/O Buffer Banks

The numbers of banks vary between the devices of this family. MachXO2-1200U, MachXO2-2000/U and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO2-1200 and lower density devices have four banks (one bank per side). Figure 2.18 and Figure 2.19 show the sysI/O banks and their associated supplies for all devices.

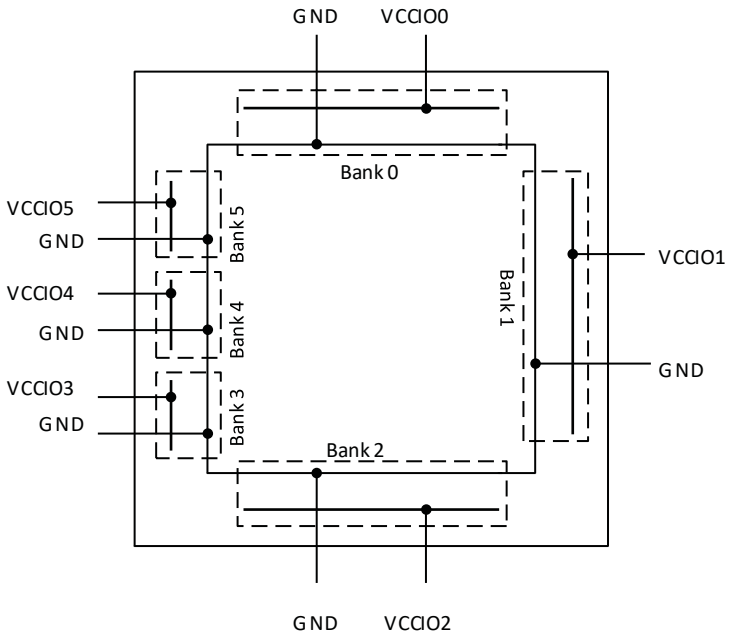



**Figure 2.18. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000 and MachXO2-7000 Banks**

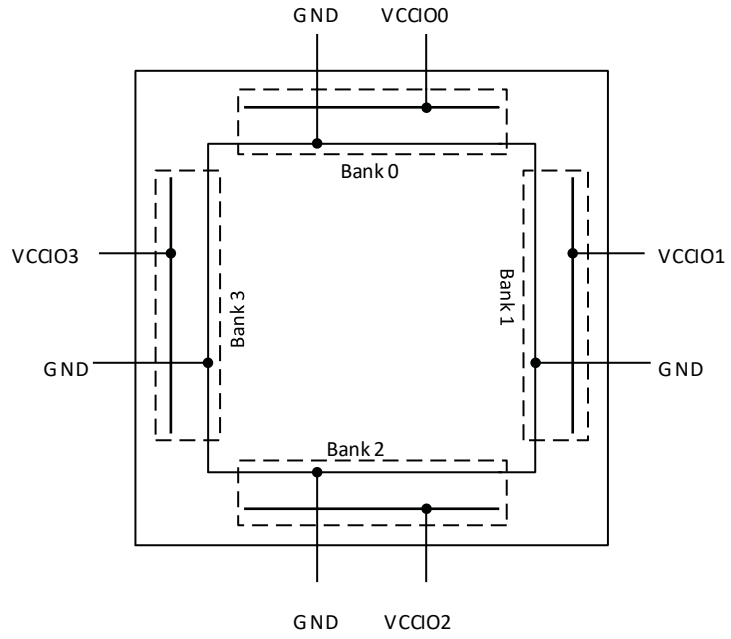



**Figure 2.19. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 2.13. Hot Socketing

The MachXO2 devices have been carefully designed to ensure predictable behavior during power-up and powerdown. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO2 ideal for many multiple power supply and hot-swap applications.

## 2.14. On-chip Oscillator

Every MachXO2 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2.14 lists all the available MCLK frequencies.

**Table 2.14. Available MCLK Frequencies**

| MCLK (MHz, Nominal) | MCLK (MHz, Nominal) | MCLK (MHz, Nominal) |
|---|---|---|
| 2.08 (default) | 9.17 | 33.25 |
| 2.46 | 10.23 | 38 |
| 3.17 | 13.3 | 44.33 |
| 4.29 | 14.78 | 53.2 |
| 5.54 | 20.46 | 66.5 |
| 7 | 26.6 | 88.67 |
| 8.31 | 29.56 | 133 |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 2.15. Embedded Hardened IP Functions and User Flash Memory

All MachXO2 devices provide embedded hardened functions such as SPI, $I^2C$ and Timer/Counter. MachXO2-640/U and higher density devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2.20.

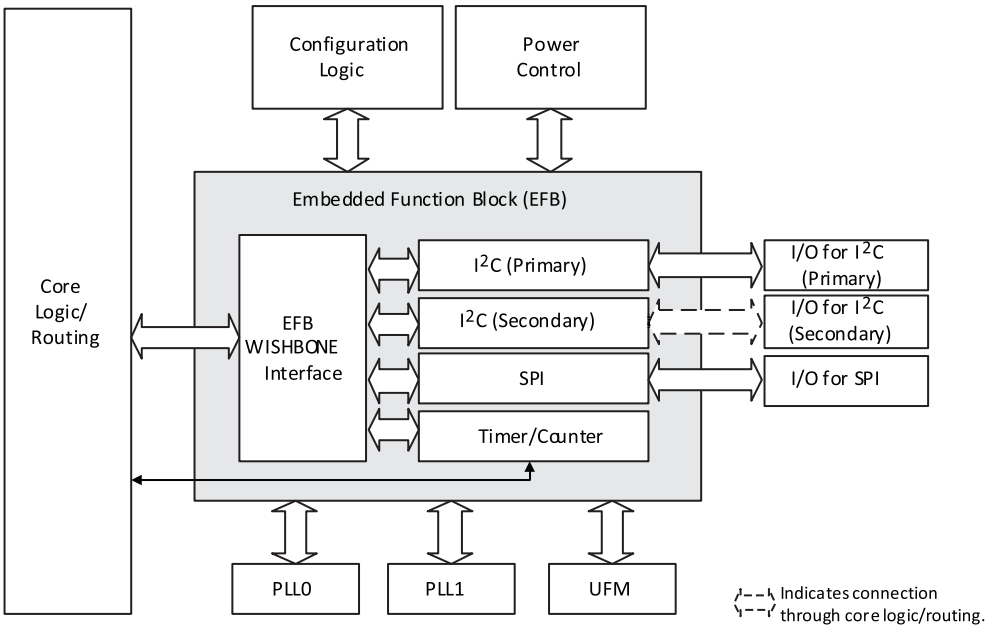



**Figure 2.20. MachXO2-256, MachXO2-640/U and MachXO2-1200 Banks**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### 2.15.1. Hardened I²C IP Core

Every MachXO2 device contains two I²C IP cores. These are the primary and secondary I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I²C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

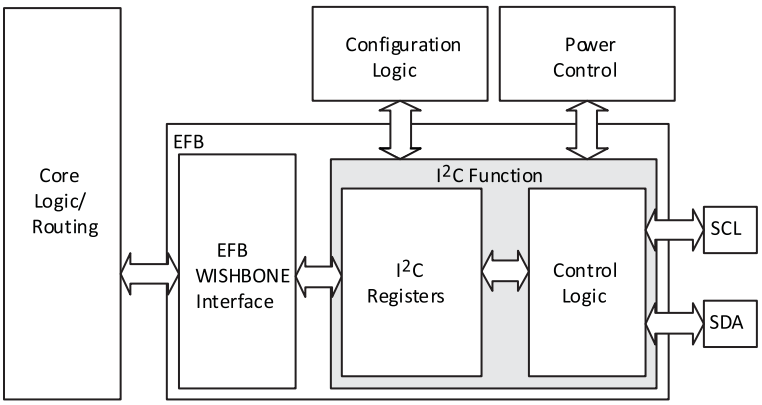



**Figure 2.21. I²C Core Block Diagram**

Table 2.15 describes the signals interfacing with the I²C cores.

**Table 2.15. Supported Input Standards**

| Signal Name | I/O | Description |
|---|---|---|
| i2c_scl | Bi-directional | Bi-directional clock line of the I²C core. The signal is an output if the I²C core is in master mode. The signal is an input if the I²C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device. |
| i2c_sda | Bi-directional | Bi-directional data line of the I²C core. The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I²C ports in each MachXO2 device. |
| i2c_irqo | Output | Interrupt request output signal of the I²C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I²C register definitions. |
| cfg_wake | Output | Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab. |
| cfg_stdby | Output | Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I²C Tab. |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### 2.15.2. Hardened SPI IP Core

Every MachXO2 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO2 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02025) (Appendix B)
- Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (FPGA-TN-02162)

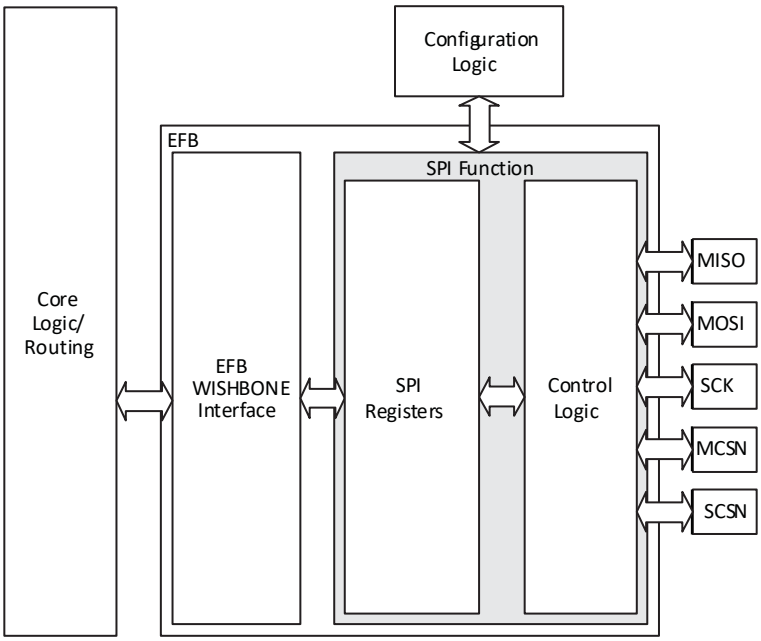



**Figure 2.22. SPI Core Block Diagram**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

Table 2.16 describes the signals interfacing with the SPI cores.

**Table 2.16. SPI Core Signal Description**

| Signal Name | I/O | Master/Slave | Description |
|---|---|---|---|
| spi_csn[0] | O | Master | SPI master chip-select output |
| spi_csn[1..7] | O | Master | Additional SPI chip-select outputs (total up to eight slaves) |
| spi_scsn | I | Slave | SPI slave chip-select input |
| spi_irq | O | Master/Slave | Interrupt request |
| spi_clk | I/O | Master/Slave | SPI clock. Output in master mode. Input in slave mode. |
| spi_miso | I/O | Master/Slave | SPI data. Input in master mode. Output in slave mode. |
| spi_mosi | I/O | Master/Slave | SPI data. Output in master mode. Input in slave mode. |
| ufm_sn | I | Slave | Configuration Slave Chip Select (active low), dedicated for selecting the User Flash Memory (UFM). |
| cfg_stdby | O | Master/Slave | Stand-by signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab. |
| cfg_wake | O | Master/Slave | Wake-up signal – To be connected only to the power module of the MachXO2 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab. |

### 2.15.3. Hardened Timer/Counter

MachXO2 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
- Watchdog timer
- Clear timer on compare match
- Fast PWM
- Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

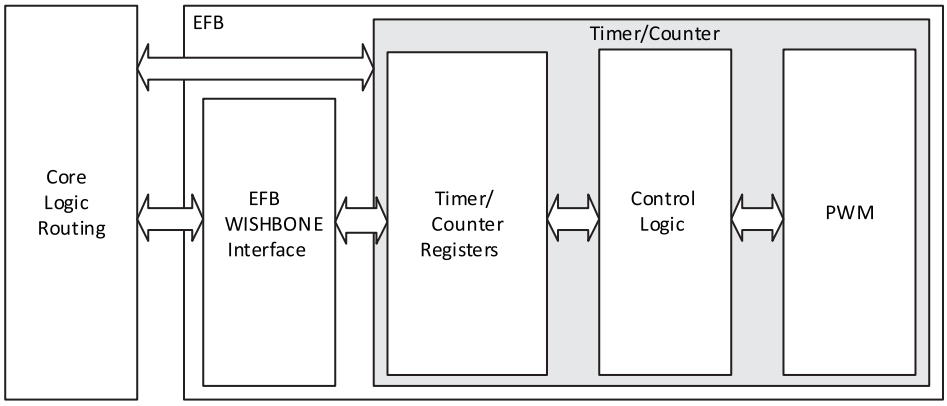



**Figure 2.23. Timer/Counter Block Diagram**

**Table 2.17. Timer/Counter Signal Description**

| Port | I/O | Description |
|---|---|---|
| tc_clki | I | Timer/Counter input clock signal |
| tc_rstn | I | Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled |
| tc_ic | I | Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping. |
| tc_int | O | Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers |
| tc_oc | O | Timer counter output signal |

For more details on these embedded functions, refer to Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (TN1205).

## 2.16. User Flash Memory (UFM)

MachXO2-640/U and higher density devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, $I^2C$ and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, refer to Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (TN1205).

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 2.17. Standby Mode and Power Saving Options

MachXO2 devices are available in three options for maximum flexibility: ZE, HC and HE devices. The ZE devices have ultra low static and dynamic power consumption. These devices use a 1.2 V core voltage that further reduces power consumption. The HC and HE devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V VCC and 3.3 V VCC while the HE devices operate at 1.2 V VCC.

MachXO2 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO2 devices support an ultra low power Stand-by mode. While most of these features are available in all three device types, these features are mainly intended for use with MachXO2 ZE devices to manage power consumption.

In the stand-by mode the MachXO2 devices are powered on and configured. Internal logic, I/O and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate $I^2C$ or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO2 devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

**Table 2.18. MachXO2 Power Saving Features Description**

| Device Subsystem | Feature Description |
|---|---|
| Bandgap | The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices. |
| Power-On-Reset (POR) | The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe VCC drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable. |
| On-Chip Oscillator | The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode. |
| PLL | Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off. |
| I/O Bank Controller | Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/O such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/O off dynamically on a per bank selection. |
| Dynamic Clock Enable for Primary Clock Nets | Each primary clock net can be dynamically disabled to save power. |
| Power Guard | Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources. |

For more details on the standby mode refer to Power Estimation and Management for MachXO2 Devices (FPGA-TN-02161).

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 2.18. Power-On-Reset

MachXO2 devices have power-on-reset circuitry to monitor $V_{CCINT}$ and $V_{CCIO}$ voltage levels during power-up and operation. At power-up, the POR circuitry monitors $V_{CCINT}$ and $V_{CCIO0}$ (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the $V_{PORUP}$ level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For devices without voltage regulators (ZE and HE devices), $V_{CCINT}$ is the same as the $V_{CC}$ supply voltage. For devices with voltage regulators (HC devices), $V_{CCINT}$ is regulated from the $V_{CC}$ supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time (tREFRESH) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/O are held in tristate. I/O are released to user functionality once the device has finished configuration. Note that for HC devices, a separate POR circuit monitors external $V_{CC}$ voltage in addition to the POR circuit that monitors the internal postregulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor $V_{CCINT}$ levels. If $V_{CCINT}$ drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the $V_{CCINT}$ and $V_{CCIO}$ voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once a ZE or HE device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the $V_{CC}$ supply dropping below $V_{CC}$ (min) they should not shut down the bandgap or POR circuit.

The power-up sequence is described below.

1. I/O tri-state with a weak pull down.
2. VCC/VCCAUX/VCCIO reaches minimal voltage level as recommended in the POR voltage table in the DC and Switching Characteristics section.
3. POR (Power-On-Reset) for internal circuitry de-asserted.
4. Device performs PPT test to ensure Flash to SRAM transfer will be reliable.
5. Flash to SRAM transfer.
6. SRAM Done bit set.
7. Device wake up sequence including GSR.
8. Device is active.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 2.19. Configuration and Testing

This section describes the configuration and testing features of the MachXO2 family.

### 2.19.1. IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/O: TDI, TDO, TCK and TMS. The test access port shares its power supply with $V_{CCIO}$ Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see Boundary Scan Testability with Lattice sysIO Capability (AN8066) and Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02025).

### 2.19.2. Device Configuration

All MachXO2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through $I^2C$ or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532

In-System Configuration specification. There are various ways to configure a MachXO2 device:

1. Internal Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard $I^2C$ Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/O if they are not required for configuration. See MachXO2 Programming and Configuration Usage Guide (TN1204) for more information about using the dual-use pins as general purpose I/O.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO2 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash memory, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash memory. For more details, refer to MachXO2 Programming and Configuration Usage Guide (TN1204).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to MachXO2 Programming and Configuration Usage Guide (TN1204).

#### TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02025) for details.

When implementing background programming of the on-chip Flash, care must be taken for the operation of the PLL. For devices that have two PLLs (XO2-2000U, -4000 and -7000), the system must put the RPLL (Right-side PLL) in reset state during the background Flash programming. More detailed description can be found in MachXO2 Programming and Configuration Usage Guide (TN1204).

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO2 devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile Flash memory spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and non-volatile Flash memory spaces is allowed.
2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to MachXO2 Programming and Configuration Usage Guide (TN1204).

### Dual Boot

MachXO2 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the on-chip Flash. The golden image MUST reside in an external SPI Flash. For more details, refer to MachXO2 Programming and Configuration Usage Guide (TN1204).

### Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to MachXO2 Soft Error Detection Usage Guide (TN1206).

## 2.20. TraceID

Each MachXO2 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, $I^2C$, or JTAG interfaces.

## 2.21. Density Shifting

The MachXO2 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO2 migration files.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# 3. DC and Switching Characteristics

## 3.1. Absolute Maximum Ratings

**Table 3.1. Absolute Maximum Ratings[1, 2, 3]**

| | MachXO2 ZE/HE (1.2 V) | MachXO2 HC (2.5 V / 3.3 V) |
|---|---|---|
| Supply Voltage $V_{CC}$ | –0.5 V to 1.32 V | –0.5 V to 3.75 V |
| Output Supply Voltage $V_{CCIO}$ | –0.5 V to 3.75 V | –0.5 V to 3.75 V |
| I/O Tristate Voltage Applied[4, 5] | –0.5 V to 3.75 V | –0.5 V to 3.75 V |
| Dedicated Input Voltage Applied[4] | –0.5 V to 3.75 V | –0.5 V to 4.25 V |
| Storage Temperature (Ambient) | –55 °C to 155 °C | –55 °C to 155 °C |
| Junction Temperature ($T_J$) | –40 °C to 125 °C | –40 °C to 125 °C |

**Notes:**

1. Stress above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (VIHMAX + 2) volts is permitted for a duration of <20 ns.
5. The dual function $I^2C$ pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

## 3.2. Recommended Operating Conditions

**Table 3.2. Recommended Operating Conditions[1]**

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| VCC[1] | Core Supply Voltage for 1.2 V Devices | 1.14 | 1.26 | V |
| | Core Supply Voltage for 2.5 V / 3.3 V Devices | 2.375 | 3.6 | V |
| VCCIO[1,2,3] | I/O Driver Supply Voltage | 1.14 | 3.6 | V |
| $t_{JCOM}$ | Junction Temperature Commercial Operation | 0 | 85 | °C |
| $t_{JIND}$ | Junction Temperature Industrial Operation | –40 | 100 | °C |

**Notes:**

1. Like power supplies must be tied together. For example, if $V_{CCIO}$ and $V_{CC}$ are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. $V_{CCIO}$ pins of unused I/O banks should be connected to the $V_{CC}$ power supply on boards.

## 3.3. Power Supply Ramp Rates

**Table 3.3. Power Supply Ramp Rates**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp rates for all power supplies. | 0.01 | — | 100 | V/ms |

**Note:** Assumes monotonic ramp rates.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.4. Power-On-Reset Voltage Levels

**Table 3.4. Power Supply Ramp Rates[1, 2, 3, 4, 5]**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{PORUP}$ | Power-On-Reset ramp up trip point (band gap based circuit monitoring $V_{CCINT}$ and $V_{CCIO0}$) | 0.9 | — | 1.06 | V |
| $V_{PORUPEXT}$ | Power-On-Reset ramp up trip point (band gap based circuit monitoring external $V_{CC}$ power supply) | 1.5 | — | 2.1 | V |
| $V_{PORDNBG}$ | Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CCINT}$) | 0.75 | — | 0.93 | V |
| $V_{PORDNBGEXT}$ | Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CC}$) | 0.98 | — | 1.33 | V |
| $V_{PORDNSRAM}$ | Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{CCINT}$) | — | 0.6 | — | V |
| $V_{PORDNSRAMEXT}$ | Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{CC}$) | — | 0.96 | — | V |

**Notes:**

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators $V_{CCINT}$ is the same as the $V_{CC}$ supply voltage. For devices with voltage regulators, $V_{CCINT}$ is regulated from the $V_{CC}$ supply voltage.
3. Note that $V_{PORUP}$ (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below $V_{PORUP}$ (min.).
4. $V_{PORUPEXT}$ is for HC devices only. In these devices a separate POR circuit monitors the external $V_{CC}$ power supply.
5. $V_{CCIO0}$ does not have a Power-On-Reset ramp down trip point. $V_{CCIO0}$ must remain within the Recommended Operating Conditions to ensure proper operation.

## 3.5. Programming/Erase Specifications

**Table 3.5. Programming/Erase Specifications**

| Symbol | Parameter | Min. | Max.[1] | Units |
|---|---|---|---|---|
| $N_{PROGCYC}$ | Flash Programming cycles per $t_{RETENTION}$ | — | 10,000 | Cycles |
| | Flash functional programming cycles | — | 100,000 | |
| $t_{RETENTION}$ | Data retention at 100 °C junction temperature | 10 | — | Years |
| | Data retention at 85 °C junction temperature | 20 | — | |

**Note:**

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

## 3.6. Hot Socketing Specifications

**Table 3.6. Hot Socketing Specifications[1, 2, 3]**

| Symbol | Parameter | Condition | Max. | Units |
|---|---|---|---|---|
| $I_{DK}$ | Input or I/O leakage Current | 0 < VIN < VIH (MAX) | +/–1000 | µA |

**Notes:**

1. Insensitive to sequence of $V_{CC}$ and $V_{CCIO}$. However, assumes monotonic rise/fall rates for $V_{CC}$ and $V_{CCIO}$.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. $I_{DK}$ is additive to $I_{PU}$, $I_{PD}$ or $I_{BH}$.

## 3.7. ESD Performance

Refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.8. DC Electrical Characteristics

Over Recommended Operating Conditions

**Table 3.7. DC Electrical Characteristics**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 4] | Input or I/O Leakage | Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX) | — | — | +175 | µA |
| | | Clamp OFF and $V_{IN} = V_{CCIO}$ | –10 | — | 10 | µA |
| | | Clamp OFF and VCCIO –0.97 V < $V_{IN}$ < $V_{CCIO}$ | –175 | — | — | µA |
| | | Clamp OFF and 0 V < $V_{IN}$ < $V_{CCIO}$ –0.97 V | — | — | 10 | µA |
| | | Clamp OFF and $V_{IN}$ = GND | — | — | 10 | µA |
| | | Clamp ON and 0 V < $V_{IN}$ < $V_{CCIO}$ | — | — | 10 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | 0 < $V_{IN}$ < 0.7 $V_{CCIO}$ | –30 | — | -309 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) < $V_{IN}$ < $V_{CCIO}$ | 30 | — | 305 | µA |
| $I_{BHLS}$ | Bus Hold Low sustaining current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High sustaining current | $V_{IN}$ = 0.7 $V_{CCIO}$ | –30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive current | 0 ≤ $V_{IN}$ ≤ $V_{CCIO}$ | — | — | 305 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive current | 0 ≤ $V_{IN}$ ≤ $V_{CCIO}$ | — | — | –309 | µA |
| $V_{BHT}$[3] | Bus Hold Trip Points | — | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1 | I/O Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, $V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{IH}$ (MAX) | 3 | 5 | 9 | pF |
| $V_{HYST}$ | Hysteresis for Schmitt Trigger Inputs[5] | $V_{CCIO}$ = 3.3 V, Hysteresis = Large | — | 450 | — | mV |
| | | $V_{CCIO}$ = 2.5 V, Hysteresis = Large | — | 250 | — | mV |
| | | $V_{CCIO}$ = 1.8 V, Hysteresis = Large | — | 125 | — | mV |
| | | $V_{CCIO}$ = 1.5 V, Hysteresis = Large | — | 100 | — | mV |
| | | $V_{CCIO}$ = 3.3 V, Hysteresis = Small | — | 250 | — | mV |
| | | $V_{CCIO}$ = 2.5 V, Hysteresis = Small | — | 150 | — | mV |
| | | $V_{CCIO}$ = 1.8 V, Hysteresis = Small | — | 60 | — | mV |
| | | $V_{CCIO}$ = 1.5 V, Hysteresis = Small | — | 40 | — | mV |

**Notes:**

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_A$ 25 °C, f = 1.0 MHz.
3. Refer to $V_{IL}$ and $V_{IH}$ in the sysI/O Single-Ended DC Electrical Characteristics table of this document.
4. When $V_{IH}$ is higher than $V_{CCIO}$, a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the high-tolow transition. For true LVDS output pins in MachXO2-640U, MachXO2-1200/U and larger devices, VIH must be less than or equal to $V_{CCIO}$.
5. With bus keeper circuit turned on. For more details, refer to MachXO2 sysIO Usage Guide (TN1202).

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.9. Static Supply Current – ZE Devices

**Table 3.8. Static Supply Current – ZE Devices[1, 2, 3, 6]**

| Symbol | Parameter | Device | Typ.[4] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO2-256ZE | 18 | µA |
| | | LCMXO2-640ZE | 28 | µA |
| | | LCMXO2-1200ZE | 56 | µA |
| | | LCMXO2-2000ZE | 80 | µA |
| | | LCMXO2-4000ZE | 124 | µA |
| | | LCMXO2-7000ZE | 189 | µA |
| $I_{CCIO}$ | Bank Power Supply[5] $V_{CCIO}$ = 2.5 V | All devices | 1 | µA |

**Notes:**

1. For further information on supply current, refer to Power Estimation and Management for MachXO2 Devices (TN1198).
2. Assumes programmed blank pattern with the following characteristics: all outputs are tri-stated, all inputs configured as LVCMOS and held at $V_{CCIO}$ or GND, on-chip oscillator is off, and on-chip PLL is off. To estimate power for your specific case, refer to the Power Calculator tool.
3. Frequency = 0 MHz.
4. $T_J$ = 25°C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

## 3.10. Static Power Consumption Contribution of Different Components – ZE Devices

The table below can be used for approximating static power consumption. For a more accurate power analysis for your design, use the Power Calculator tool.

**Table 3.9. Static Power Consumption Contribution of Different Components – ZE Devices**

| Symbol | Parameter | Typ. | Units |
|---|---|---|---|
| IDCBG | Bandgap DC power contribution | 101 | µA |
| IDCPOR | POR DC power contribution | 38 | µA |
| IDCIOBANKCONTROLLER | DC power contribution per I/O bank controller | 143 | µA |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.11. Static Supply Current – HC/HE Devices

**Table 3.10. Static Supply Current – HC/HE Devices[1, 2, 3, 6]**

| Symbol | Parameter | Device | Typ.[4] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO2-256HC | 1.15 | mA |
| | | LCMXO2-640HC | 1.84 | mA |
| | | LCMXO2-640UHC | 3.48 | mA |
| | | LCMXO2-1200HC | 3.49 | mA |
| | | LCMXO2-1200UHC | 4.80 | mA |
| | | LCMXO2-2000HC | 4.80 | mA |
| | | LCMXO2-2000UHC | 8.44 | mA |
| | | LCMXO2-4000HC | 8.45 | mA |
| | | LCMXO2-7000HC | 12.87 | mA |
| | | LCMXO2-2000HE | 1.39 | mA |
| | | LCMXO2-4000HE | 2.55 | mA |
| | | LCMXO2-7000HE | 4.06 | mA |
| $I_{CCIO}$ | Bank Power Supply[5] $V_{CCIO}$ = 2.5 V | All devices | 0 | mA |

**Notes:**

1. For further information on supply current, refer to Power Estimation and Management for MachXO2 Devices (TN1198).
2. Assumes programmed blank pattern with the following characteristics: all outputs are tri-stated, all inputs configured as LVCMOS and held at $V_{CCIO}$ or GND, on-chip oscillator is off, and on-chip PLL is off. To estimate power for your specific case, refer to the Power Calculator tool.
3. Frequency = 0 MHz.
4. $T_J$ = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO2 peak start-up current data, use the Power Calculator tool.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.12. Programming and Erase Flash Supply Current – HC/HE Devices

**Table 3.11. Programming and Erase Flash Supply Current – HC/HE Devices[1, 2, 3, 4]**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO2-256HC | 14.6 | mA |
| | | LCMXO2-640HC | 16.1 | mA |
| | | LCMXO2-640UHC | 18.8 | mA |
| | | LCMXO2-1200HC | 18.8 | mA |
| | | LCMXO2-1200UHC | 22.1 | mA |
| | | LCMXO2-2000HC | 22.1 | mA |
| | | LCMXO2-2000UHC | 26.8 | mA |
| | | LCMXO2-4000HC | 26.8 | mA |
| | | LCMXO2-7000HC | 33.2 | mA |
| | | LCMXO2-2000HE | 18.3 | mA |
| | | LCMXO2-2000UHE | 20.4 | mA |
| | | LCMXO2-4000HE | 20.4 | mA |
| | | LCMXO2-7000HE | 23.9 | mA |
| $I_{CCIO}$ | Bank Power Supply[6] | All devices | 0 | mA |

**Notes:**

1. For further information on supply current, refer to Power Estimation and Management for MachXO2 Devices (TN1198).
2. Assumes all inputs are held at $V_{CCIO}$ or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. $T_J$ = 25 °C, power supplies at nominal voltage.
6. Per bank. $V_{CCIO}$ = 2.5 V. Does not include pull-up/pull-down.

## 3.13. Programming and Erase Flash Supply Current – ZE Devices

**Table 3.12. Programming and Erase Flash Supply Current – ZE Devices[1, 2, 3, 4]**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO2-256ZE | 13 | mA |
| | | LCMXO2-640ZE | 14 | mA |
| | | LCMXO2-1200ZE | 15 | mA |
| | | LCMXO2-2000ZE | 17 | mA |
| | | LCMXO2-4000ZE | 18 | mA |
| | | LCMXO2-7000ZE | 20 | mA |
| $I_{CCIO}$ | Bank Power Supply[6] | All devices | 0 | mA |

**Notes:**

1. For further information on supply current, refer to Power Estimation and Management for MachXO2 Devices (TN1198).
2. Assumes all inputs are held at $V_{CCIO}$ or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. TJ = 25 °C, power supplies at nominal voltage.
6. Per bank. $V_{CCIO}$ = 2.5 V. Does not include pull-up/pull-down.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.14. sysI/O Recommended Operating Conditions

**Table 3.13. sysI/O Recommended Operating Conditions**

| Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVCMOS 3.3 | 3.135 | 3.3 | 3.6 | — | — | — |
| LVCMOS 2.5 | 2.375 | 2.5 | 2.625 | — | — | — |
| LVCMOS 1.8 | 1.71 | 1.8 | 1.89 | — | — | — |
| LVCMOS 1.5 | 1.425 | 1.5 | 1.575 | — | — | — |
| LVCMOS 1.2 | 1.14 | 1.2 | 1.26 | — | — | — |
| LVTTL | 3.135 | 3.3 | 3.6 | — | — | — |
| PCI[3] | 3.135 | 3.3 | 3.6 | — | — | — |
| SSTL25 | 2.375 | 2.5 | 2.625 | 1.15 | 1.25 | 1.35 |
| SSTL18 | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| HSTL18 | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| LVCMOS25R33 | 3.135 | 3.3 | 3.6 | 1.1 | 1.25 | 1.4 |
| LVCMOS18R33 | 3.135 | 3.3 | 3.6 | 0.75 | 0.9 | 1.05 |
| LVCMOS18R25 | 2.375 | 2.5 | 2.625 | 0.75 | 0.9 | 1.05 |
| LVCMOS15R33 | 3.135 | 3.3 | 3.6 | 0.6 | 0.75 | 0.9 |
| LVCMOS15R25 | 2.375 | 2.5 | 2.625 | 0.6 | 0.75 | 0.9 |
| LVCMOS12R33[4] | 3.135 | 3.3 | 3.6 | 0.45 | 0.6 | 0.75 |
| LVCMOS12R25[4] | 2.375 | 2.5 | 2.625 | 0.45 | 0.6 | 0.75 |
| LVCMOS10R33[4] | 3.135 | 3.3 | 3.6 | 0.35 | 0.5 | 0.65 |
| LVCMOS10R25[4] | 2.375 | 2.5 | 2.625 | 0.35 | 0.5 | 0.65 |
| LVDS25[1, 2] | 2.375 | 2.5 | 2.625 | — | — | — |
| LVDS33[1, 2] | 3.135 | 3.3 | 3.6 | — | — | — |
| LVPECL[1] | 3.135 | 3.3 | 3.6 | — | — | — |
| BLVDS[1] | 2.375 | 2.5 | 2.625 | — | — | — |
| RSDS[1] | 2.375 | 2.5 | 2.625 | | | |
| SSTL18D | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL25D | 2.375 | 2.5 | 2.625 | 1.15 | 1.25 | 1.35 |
| HSTL18D | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |

**Notes:**

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. MachXO2-640U, MachXO2-1200/U and larger devices have dedicated LVDS buffers.
3. Input on the bottom bank of the MachXO2-640U, MachXO2-1200/U and larger devices only.
4. Supported only for inputs and BIDIs for all ZE devices, and –6 speed grade for HE and HC devices.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.15. sysI/O Single-Ended DC Electrical Characteristics

**Table 3.14. sysI/O Single-Ended DC Electrical Characteristics[1, 2]**

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$ Max.[4] (mA) | $I_{OH}$ Max.[4] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min. (V)[3] | Max. (V) | Min. (V) | Max. (V) | | | | |
| LVCMOS 3.3 LVTTL | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ – 0.4 | 4 | –4 |
| | | | | | | | 8 | –8 |
| | | | | | | | 12 | –12 |
| | | | | | | | 16 | –16 |
| | | | | | | | 24 | –24 |
| | | | | | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| LVCMOS 2.5 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | $V_{CCIO}$ – 0.4 | 4 | –4 |
| | | | | | | | 8 | –8 |
| | | | | | | | 12 | –12 |
| | | | | | | | 16 | –16 |
| | | | | | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| LVCMOS 1.8 | –0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ – 0.4 | 4 | –4 |
| | | | | | | | 8 | –8 |
| | | | | | | | 12 | –12 |
| | | | | | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| LVCMOS 1.5 | –0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ – 0.4 | 4 | –4 |
| | | | | | | | 8 | –8 |
| | | | | | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| LVCMOS 1.2 | –0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ – 0.4 | 4 | –2 |
| | | | | | | | 8 | –6 |
| | | | | | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| PCI | –0.3 | 0.3 $V_{CCIO}$ | 0.5 $V_{CCIO}$ | 3.6 | 0.1 $V_{CCIO}$ | 0.9 $V_{CCIO}$ | 1.5 | –0.5 |
| SSTL25 Class I | –0.3 | $V_{REF}$ – 0.18 | $V_{REF}$ + 0.18 | 3.6 | 0.54 | $V_{CCIO}$ - 0.62 | 8 | 8 |
| SSTL25 Class II | –0.3 | $V_{REF}$ – 0.18 | $V_{REF}$ + 0.18 | 3.6 | NA | NA | NA | NA |
| SSTL18 Class I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 3.6 | 0.40 | $V_{CCIO}$ - 0.40 | 8 | 8 |
| SSTL18 Class II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 3.6 | NA | NA | NA | NA |
| HSTL18 Class I | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.40 | $V_{CCIO}$ - 0.40 | 8 | 8 |
| HSTL18 Class II | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | NA | NA | NA | NA |
| LVCMOS25R33 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | NA | NA | NA | NA |
| LVCMOS18R33 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | NA | NA | NA | NA |
| LVCMOS18R25 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | NA | NA | NA | NA |
| LVCMOS15R33 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | NA | NA | NA | NA |
| LVCMOS15R25 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | NA | NA | NA | NA |
| LVCMOS12R33 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.40 | NA Open Drain | 24, 16, 12, 8, 4 | NA Open Drain |
| LVCMOS12R25 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.40 | NA Open Drain | 16, 12, 8, 4 | NA Open Drain |
| LVCMOS10R33 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.40 | NA Open Drain | 24, 16, 12, 8, 4 | NA Open Drain |
| LVCMOS10R25 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.40 | NA Open Drain | 16, 12, 8, 4 | NA Open Drain |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Notes:**

1. MachXO2 devices allow LVCMOS inputs to be placed in I/O banks where $V_{CCIO}$ is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO2 devices allow for LVCMOS referenced I/O which follow applicable JEDEC specifications. For more details about mixed mode operation, refer to MachXO2 sysIO Usage Guide (TN1202).
3. The dual function $I^2C$ pins SCL and SDA are limited to a $V_{IL}$ min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. “n” is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. I/O Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

| Input Standard | $V_{CCIO}$ (V) | $V_{IL}$ Max. (V) |
|---|---|---|
| LVCMOS 33 | 1.5 | 0.685 |
| LVCMOS 25 | 1.5 | 0.687 |
| LVCMOS 18 | 1.5 | 0.655 |

## 3.16. sysI/O Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of MachXO2-640U, MachXO2-1200/U and higher density devices in the MachXO2 PLD family.

### 3.16.1. LVDS

Over Recommended Operating Conditions

**Table 3.15. LVDS**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | $V_{CCIO}$ = 3.3 V | 0 | — | 2.605 | V |
| | | $V_{CCIO}$ = 2.5 V | 0 | — | 2.05 | V |
| $V_{THD}$ | Differential Input Threshold | | ±100 | — | | mV |
| $V_{CM}$ | Input Common Mode Voltage | $V_{CCIO}$ = 3.3 V | 0.05 | — | 2.6 | V |
| | | $V_{CCIO}$ = 2.5 V | 0.05 | — | 2.0 | V |
| $I_{IN}$ | Input current | Power on | — | — | ±10 | µA |
| $V_{OH}$ | Output high voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ω | — | 1.375 | — | V |
| $V_{OL}$ | Output low voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ω | 0.90 | 1.025 | — | V |
| $V_{OD}$ | Output voltage differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 Ω | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | | — | — | 50 | mV |
| $V_{OS}$ | Output voltage offset | ($V_{OP}$ + $V_{OM}$)/2, $R_T$ = 100 Ω | 1.125 | 1.20 | 1.395 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between H and L | | — | — | 50 | mV |
| $I_{OSD}$ | Output short circuit current | $V_{OD}$ = 0 V driver outputs shorted | — | — | 24 | mA |

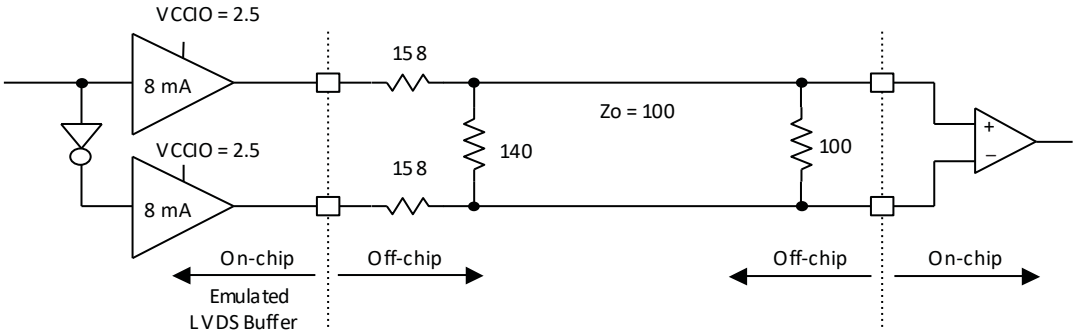
© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### 3.16.2. LVDS Emulation

MachXO2 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3.1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3.1 are industry standard values for 1% resistors.




Note: All resistors are ±1%.

**Figure 3.1. LVDS Using External Resistors (LVDS25E)**

**Table 3.16. LVDS25E DC Conditions**

Over Recommended Operating Conditions

**Table 3.17. LVDS25E DC Conditions**

| Parameter | Description | Typ. | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ω |
| $R_S$ | Driver series resistor | 158 | Ω |
| $R_P$ | Driver parallel resistor | 140 | Ω |
| $R_T$ | Receiver termination | 100 | Ω |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100.5 | Ω |
| $I_{DC}$ | DC output current | 6.03 | mA |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### 3.16.3. BLVDS

The MachXO2 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bi-directional multi-point differential signals.

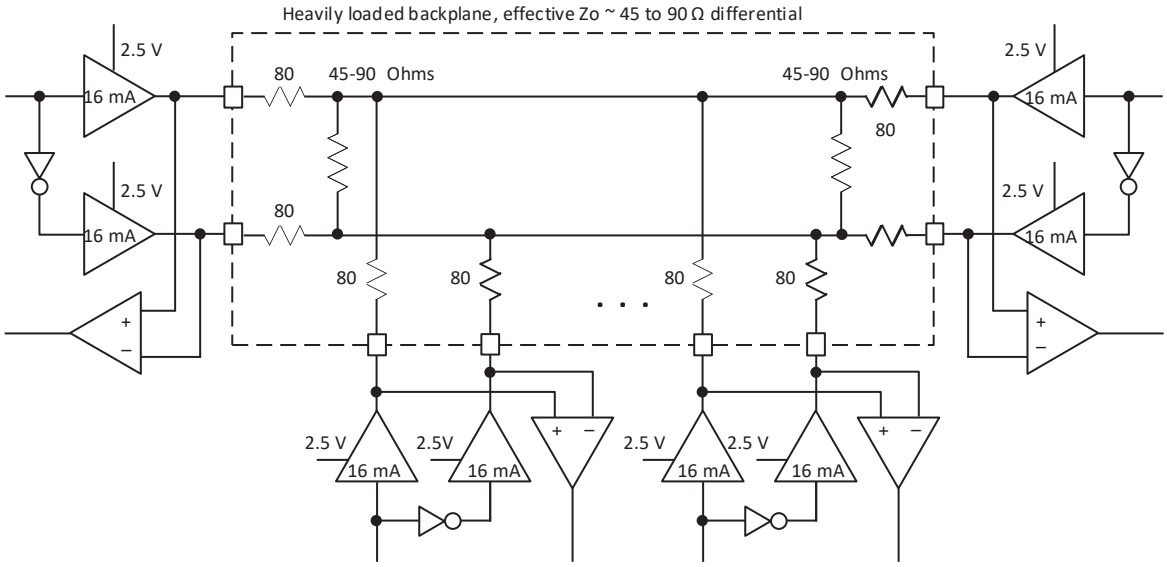



**Figure 3.2. BLVDS Multi-point Output Example**

Over Recommended Operating Conditions

**Table 3.18. BLVDS DC Conditions**

| Symbol | Description | Nominal | | Units |
|---|---|---|---|---|
| | | Zo = 45 | Zo = 90 | |
| $Z_{OUT}$ | Output impedance | 20 | 20 | Ω |
| $R_S$ | Driver series resistance | 80 | 80 | Ω |
| $R_{TLEFT}$ | Left end termination | 45 | 90 | Ω |
| $R_{TRIGHT}$ | Right end termination | 45 | 90 | Ω |
| $V_{OH}$ | Output high voltage | 1.376 | 1.480 | V |
| $V_{OL}$ | Output low voltage | 1.124 | 1.020 | V |
| $V_{OD}$ | Output differential voltage | 0.253 | 0.459 | V |
| $V_{CM}$ | Output common mode voltage | 1.250 | 1.250 | V |
| $I_{DC}$ | DC output current | 11.236 | 10.204 | mA |

**Note:** For input buffer, see Table 3.15.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### 3.16.4. LVPECL

The MachXO2 family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

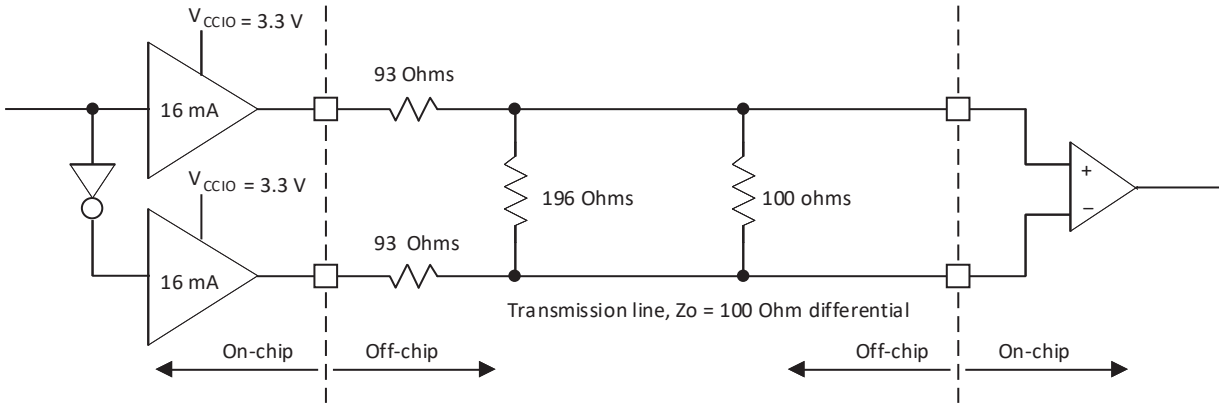



**Figure 3.3. Differential LVPECL**

Over Recommended Operating Conditions

**Table 3.19. LVPECL DC Conditions**

| Symbol | Description | Nominal | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ω |
| $R_S$ | Driver series resistor | 93 | Ω |
| $R_P$ | Driver parallel resistor | 196 | Ω |
| $R_T$ | Receiver termination | 100 | Ω |
| $V_{OH}$ | Output high voltage | 2.05 | V |
| $V_{OL}$ | Output low voltage | 1.25 | V |
| $V_{OD}$ | Output differential voltage | 0.80 | V |
| $V_{CM}$ | Output common mode voltage | 1.65 | V |
| $Z_{BACK}$ | Back impedance | 100.5 | Ω |
| $I_{DC}$ | DC output current | 12.11 | mA |

**Note:** For input buffer, see Table 3.15.

For further information on LVPECL, BLVDS and other differential interfaces, see details of additional technical documentation at the end of the data sheet.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### 3.16.5. RSDS

The MachXO2 family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.4 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3.4 are industry standard values for 1% resistors.

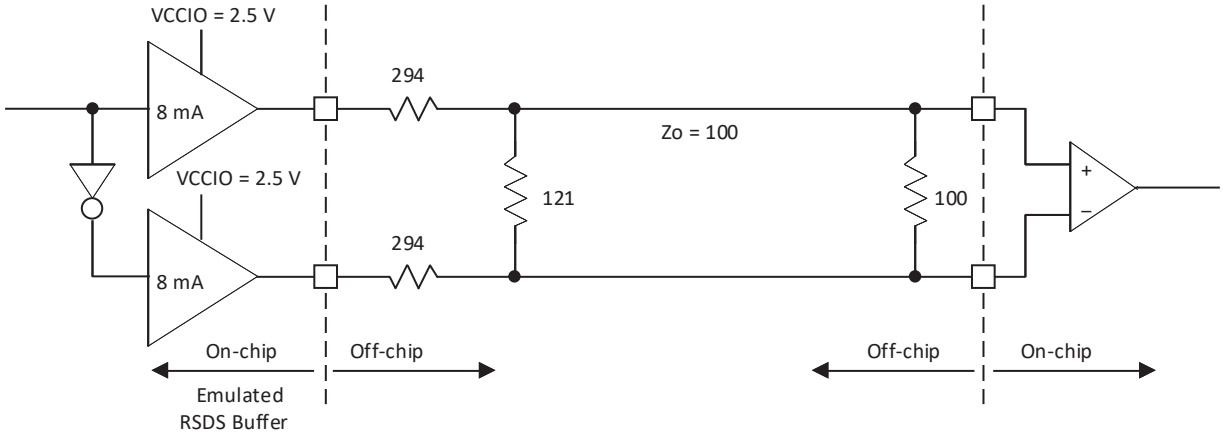



**Figure 3.4. RSDS (Reduced Swing Differential Standard)**

**Table 3.20. RSDS DC Conditions**

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ω |
| $R_S$ | Driver series resistor | 294 | Ω |
| $R_P$ | Driver parallel resistor | 121 | Ω |
| $R_T$ | Receiver termination | 100 | Ω |
| $V_{OH}$ | Output high voltage | 1.35 | V |
| $V_{OL}$ | Output low voltage | 1.15 | V |
| $V_{OD}$ | Output differential voltage | 0.20 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 101.5 | Ω |
| $I_{DC}$ | DC output current | 3.66 | mA |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# 3.17. Typical Building Block Function Performance – HC/HE Devices

## 3.17.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

**Table 3.21. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)**

| Function | –6 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 8.9 | ns |
| 4:1 MUX | 7.5 | ns |
| 16:1 MUX | 8.3 | ns |

## 3.17.2. Register-to-Register Performance

**Table 3.22. Register-to-Register Performance**

| Function | –6 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 412 | MHz |
| 16-bit adder | 297 | MHz |
| 16-bit counter | 324 | MHz |
| 64-bit counter | 161 | MHz |
| **Embedded Memory Functions** | | |
| 1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers) | 183 | MHz |
| **Distributed Memory Functions** | | |
| 16x4 Pseudo-Dual Port RAM (one PFU) | 500 | MHz |

**Note:** The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# 3.18. Typical Building Block Function Performance – ZE Devices

## 3.18.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

**Table 3.23. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)**

| Function | -6 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 8.9 | ns |
| 4:1 MUX | 7.5 | ns |
| 16:1 MUX | 8.3 | ns |

## 3.18.2. Register-to-Register Performance

**Table 3.24. Register-to-Register Performance**

| Function | -6 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 412 | MHz |
| 16-bit adder | 297 | MHz |
| 16-bit counter | 324 | MHz |
| 64-bit counter | 161 | MHz |
| **Embedded Memory Functions** | | |
| 1024x9 True-Dual Port RAM<br>(Write Through or Normal, EBR output registers) | 183 | MHz |
| **Distributed Memory Functions** | | |
| 16x4 Pseudo-Dual Port RAM (one PFU) | 500 | MHz |

**Note:** The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

# 3.19. Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.20. Maximum sysI/O Buffer Performance

**Table 3.25. Maximum sysI/O Buffer Performance**

| I/O Standard | Max. Speed | Units |
|---|---|---|
| LVDS25 | 400 | MHz |
| LVDS25E | 150 | MHz |
| RSDS25 | 150 | MHz |
| RSDS25E | 150 | MHz |
| BLVDS25 | 150 | MHz |
| BLVDS25E | 150 | MHz |
| MLVDS25 | 150 | MHz |
| MLVDS25E | 150 | MHz |
| LVPECL33 | 150 | MHz |
| LVPECL33E | 150 | MHz |
| SSTL25_I | 150 | MHz |
| SSTL25_II | 150 | MHz |
| SSTL25D_I | 150 | MHz |
| SSTL25D_II | 150 | MHz |
| SSTL18_I | 150 | MHz |
| SSTL18_II | 150 | MHz |
| SSTL18D_I | 150 | MHz |
| SSTL18D_II | 150 | MHz |
| HSTL18_I | 150 | MHz |
| HSTL18_II | 150 | MHz |
| HSTL18D_I | 150 | MHz |
| HSTL18D_II | 150 | MHz |
| PCI33 | 134 | MHz |
| LVTTL33 | 150 | MHz |
| LVTTL33D | 150 | MHz |
| LVCMOS33 | 150 | MHz |
| LVCMOS33D | 150 | MHz |
| LVCMOS25 | 150 | MHz |
| LVCMOS25D | 150 | MHz |
| LVCMOS25R33 | 150 | MHz |
| LVCMOS18 | 150 | MHz |
| LVCMOS18D | 150 | MHz |
| LVCMOS18R33 | 150 | MHz |
| LVCMOS18R25 | 150 | MHz |
| LVCMOS15 | 150 | MHz |
| LVCMOS15D | 150 | MHz |
| LVCMOS15R33 | 150 | MHz |
| LVCMOS15R25 | 150 | MHz |
| LVCMOS12 | 91 | MHz |
| LVCMOS12D | 91 | MHz |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.21. MachXO2 External Switching Characteristics – HC/HE Devices

Over Recommended Operating Conditions

**Table 3.26. MachXO2 External Switching Characteristics – HC/HE Devices[1, 2, 3, 4, 5, 6, 7]**

| Parameter | Description | Device | –6 | | –5 | | –4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Clocks** | | | | | | | | | |
| **Primary Clocks** | | | | | | | | | |
| $f_{MAX_PRI8}$ | Frequency for Primary Clock Tree | All MachXO2 devices | — | 388 | — | 323 | — | 269 | MHz |
| $t_{W_PRI}$ | Clock Pulse Width for Primary Clock | All MachXO2 devices | 0.5 | — | 0.6 | — | 0.7 | — | ns |
| $t_{SKEW_PRI}$ | Primary Clock Skew Within a Device | MachXO2-256HC-HE | — | 912 | — | 939 | — | 975 | ps |
| | | MachXO2-640HC-HE | — | 844 | — | 871 | — | 908 | ps |
| | | MachXO2-1200HC-HE | — | 868 | — | 902 | — | 951 | ps |
| | | MachXO2-2000HC-HE | — | 867 | — | 897 | — | 941 | ps |
| | | MachXO2-4000HC-HE | — | 865 | — | 892 | — | 931 | ps |
| | | MachXO2-7000HC-HE | — | 902 | — | 942 | — | 989 | ps |
| **Edge Clock** | | | | | | | | | |
| $f_{MAX_EDGE8}$ | Frequency for Edge Clock | MachXO2-1200 and larger devices | — | 400 | — | 333 | — | 278 | MHz |
| **Pin-LUT-Pin Propagation Delay** | | | | | | | | | |
| $t_{PD}$ | Best case propagation delay through one LUT-4 | All MachXO2 devices | — | 6.72 | — | 6.96 | — | 7.24 | ns |
| **General I/O Pin Parameters (Using Primary Clock without PLL)** | | | | | | | | | |
| $t_{CO}$ | Clock to Output – PIO Output Register | MachXO2-256HC-HE | — | 7.13 | — | 7.30 | — | 7.57 | ns |
| | | MachXO2-640HC-HE | — | 7.15 | — | 7.30 | — | 7.57 | ns |
| | | MachXO2-1200HC-HE | — | 7.44 | — | 7.64 | — | 7.94 | ns |
| | | MachXO2-2000HC-HE | — | 7.46 | — | 7.66 | — | 7.96 | ns |
| | | MachXO2-4000HC-HE | — | 7.51 | — | 7.71 | — | 8.01 | ns |
| | | MachXO2-7000HC-HE | — | 7.54 | — | 7.75 | — | 8.06 | ns |
| $t_{SU}$ | Clock to Data Setup – PIO Input Register | MachXO2-256HC-HE | –0.06 | — | –0.06 | — | –0.06 | — | ns |
| | | MachXO2-640HC-HE | –0.06 | — | –0.06 | — | –0.06 | — | ns |
| | | MachXO2-1200HC-HE | –0.17 | — | –0.17 | — | –0.17 | — | ns |
| | | MachXO2-2000HC-HE | –0.20 | — | –0.20 | — | –0.20 | — | ns |
| | | MachXO2-4000HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-7000HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| $t_H$ | Clock to Data Hold – PIO Input Register | MachXO2-256HC-HE | 1.75 | — | 1.95 | — | 2.16 | — | ns |
| | | MachXO2-640HC-HE | 1.75 | — | 1.95 | — | 2.16 | — | ns |
| | | MachXO2-1200HC-HE | 1.88 | — | 2.12 | — | 2.36 | — | ns |
| | | MachXO2-2000HC-HE | 1.89 | — | 2.13 | — | 2.37 | — | ns |
| | | MachXO2-4000HC-HE | 1.94 | — | 2.18 | — | 2.43 | — | ns |
| | | MachXO2-7000HC-HE | 1.98 | — | 2.23 | — | 2.49 | — | ns |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Parameter | Description | Device | –6 | | –5 | | –4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{SU_DEL}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-256HC-HE | 1.42 | — | 1.59 | — | 1.96 | — | ns |
| | | MachXO2-640HC-HE | 1.41 | — | 1.58 | — | 1.96 | — | ns |
| | | MachXO2-1200HC-HE | 1.63 | — | 1.79 | — | 2.17 | — | ns |
| | | MachXO2-2000HC-HE | 1.61 | — | 1.76 | — | 2.13 | — | ns |
| | | MachXO2-4000HC-HE | 1.66 | — | 1.81 | — | 2.19 | — | ns |
| | | MachXO2-7000HC-HE | 1.53 | — | 1.67 | — | 2.03 | — | ns |
| $t_{H_DEL}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-256HC-HE | –0.24 | — | –0.24 | — | –0.24 | — | ns |
| | | MachXO2-640HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-1200HC-HE | –0.24 | — | –0.24 | — | –0.24 | — | ns |
| | | MachXO2-2000HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-4000HC-HE | –0.25 | — | –0.25 | — | –0.25 | — | ns |
| | | MachXO2-7000HC-HE | –0.21 | — | –0.21 | — | –0.21 | — | ns |
| $f_{MAX_IO}$ | Clock Frequency of I/O and PFU Register | All MachXO2 devices | — | 388 | — | 323 | — | 269 | MHz |
| **General I/O Pin Parameters (Using Edge Clock without PLL)** | | | | | | | | | |
| $t_{COE}$ | Clock to Output – PIO Output Register | MachXO2-1200HC-HE | — | 7.53 | — | 7.76 | — | 8.10 | ns |
| | | MachXO2-2000HC-HE | — | 7.53 | — | 7.76 | — | 8.10 | ns |
| | | MachXO2-4000HC-HE | — | 7.45 | — | 7.68 | — | 8.00 | ns |
| | | MachXO2-7000HC-HE | — | 7.53 | — | 7.76 | — | 8.10 | ns |
| $t_{SUE}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200HC-HE | –0.19 | — | –0.19 | — | –0.19 | — | ns |
| | | MachXO2-2000HC-HE | –0.19 | — | –0.19 | — | –0.19 | — | ns |
| | | MachXO2-4000HC-HE | –0.16 | — | –0.16 | — | –0.16 | — | ns |
| | | MachXO2-7000HC-HE | –0.19 | — | –0.19 | — | –0.19 | — | ns |
| $t_{HE}$ | Clock to Data Hold – PIO Input Register | MachXO2-1200HC-HE | 1.97 | — | 2.24 | — | 2.52 | — | ns |
| | | MachXO2-2000HC-HE | 1.97 | — | 2.24 | — | 2.52 | — | ns |
| | | MachXO2-4000HC-HE | 1.89 | — | 2.16 | — | 2.43 | — | ns |
| | | MachXO2-7000HC-HE | 1.97 | — | 2.24 | — | 2.52 | — | ns |
| $t_{SU_DELE}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200HC-HE | 1.56 | — | 1.69 | — | 2.05 | — | ns |
| | | MachXO2-2000HC-HE | 1.56 | — | 1.69 | — | 2.05 | — | ns |
| | | MachXO2-4000HC-HE | 1.74 | — | 1.88 | — | 2.25 | — | ns |
| | | MachXO2-7000HC-HE | 1.66 | — | 1.81 | — | 2.17 | — | ns |
| $t_{H_DELE}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-1200HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-2000HC-HE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-4000HC-HE | –0.34 | — | –0.34 | — | –0.34 | — | ns |
| | | MachXO2-7000HC-HE | –0.29 | — | –0.29 | — | –0.29 | — | ns |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Parameter | Description | Device | –6 | | –5 | | –4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **General I/O Pin Parameters (Using Primary Clock with PLL)** | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output – PIO Output Register | MachXO2-1200HC-HE | — | 5.97 | — | 6.00 | — | 6.13 | ns |
| | | MachXO2-2000HC-HE | — | 5.98 | — | 6.01 | — | 6.14 | ns |
| | | MachXO2-4000HC-HE | — | 5.99 | — | 6.02 | — | 6.16 | ns |
| | | MachXO2-7000HC-HE | — | 6.02 | — | 6.06 | — | 6.20 | ns |
| $t_{SUPLL}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200HC-HE | 0.36 | — | 0.36 | — | 0.65 | — | ns |
| | | MachXO2-2000HC-HE | 0.36 | — | 0.36 | — | 0.63 | — | ns |
| | | MachXO2-4000HC-HE | 0.35 | — | 0.35 | — | 0.62 | — | ns |
| | | MachXO2-7000HC-HE | 0.34 | — | 0.34 | — | 0.59 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold – PIO Input Register | MachXO2-1200HC-HE | 0.41 | — | 0.48 | — | 0.55 | — | ns |
| | | MachXO2-2000HC-HE | 0.42 | — | 0.49 | — | 0.56 | — | ns |
| | | MachXO2-4000HC-HE | 0.43 | — | 0.50 | — | 0.58 | — | ns |
| | | MachXO2-7000HC-HE | 0.46 | — | 0.54 | — | 0.62 | — | ns |
| $t_{SU_DELPLL}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200HC-HE | 2.88 | — | 3.19 | — | 3.72 | — | ns |
| | | MachXO2-2000HC-HE | 2.87 | — | 3.18 | — | 3.70 | — | ns |
| | | MachXO2-4000HC-HE | 2.96 | — | 3.28 | — | 3.81 | — | ns |
| | | MachXO2-7000HC-HE | 3.05 | — | 3.35 | — | 3.87 | — | ns |
| $t_{H_DELPLL}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-1200HC-HE | –0.83 | — | –0.83 | — | –0.83 | — | ns |
| | | MachXO2-2000HC-HE | –0.83 | — | –0.83 | — | –0.83 | — | ns |
| | | MachXO2-4000HC-HE | –0.87 | — | –0.87 | — | –0.87 | — | ns |
| | | MachXO2-7000HC-HE | –0.91 | — | –0.91 | — | –0.91 | — | ns |
| **Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After CLK | All MachXO2 devices, all sides | — | 0.317 | — | 0.344 | — | 0.368 | UI |
| $t_{DVE}$ | Input Data Hold After CLK | | 0.742 | — | 0.702 | — | 0.668 | — | UI |
| $f_{DATA}$ | DDRX1 Input Data Speed | | — | 300 | — | 250 | — | 208 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK Frequency | | — | 150 | — | 125 | — | 104 | MHz |
| **Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 11]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before CLK | All MachXO2 devices, all sides | 0.566 | — | 0.560 | — | 0.538 | — | ns |
| $t_{HO}$ | Input Data Hold After CLK | | 0.778 | — | 0.879 | — | 1.090 | — | ns |
| $f_{DATA}$ | DDRX1 Input Data Speed | | — | 300 | — | 250 | — | 208 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK Frequency | | — | 150 | — | 125 | — | 104 | MHz |
| **Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After CLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only | — | 0.316 | — | 0.342 | — | 0.364 | UI |
| $t_{DVE}$ | Input Data Hold After CLK | | 0.710 | — | 0.675 | — | 0.679 | — | UI |
| $f_{DATA}$ | DDRX2 Serial Input Data Speed | | — | 664 | — | 554 | — | 462 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency | | — | 332 | — | 277 | — | 231 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 166 | — | 139 | — | 116 | MHz |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Parameter | Description | Device | –6 | | –5 | | –4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 11]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before CLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only | 0.233 | — | 0.219 | — | 0.198 | — | ns |
| $t_{HO}$ | Input Data Hold After CLK | | 0.287 | — | 0.287 | — | 0.344 | — | ns |
| $f_{DATA}$ | DDRX2 Serial Input Data Speed | | — | 664 | — | 554 | — | 462 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency | | — | 332 | — | 277 | — | 231 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 166 | — | 139 | — | 116 | MHz |
| **Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After ECLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only | — | 0.290 | — | 0.320 | — | 0.345 | UI |
| $t_{DVE}$ | Input Data Hold After ECLK | | 0.739 | — | 0.699 | — | 0.703 | — | UI |
| $f_{DATA}$ | DDRX4 Serial Input Data Speed | | — | 756 | — | 630 | — | 524 | Mbps |
| $f_{DDRX4}$ | DDRX4 ECLK Frequency | | — | 378 | — | 315 | — | 262 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 95 | — | 79 | — | 66 | MHz |
| **Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[9, 11]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before ECLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only | 0.233 | — | 0.219 | — | 0.198 | — | ns |
| $t_{HO}$ | Input Data Hold After ECLK | | 0.287 | — | 0.287 | — | 0.344 | — | ns |
| $f_{DATA}$ | DDRX4 Serial Input Data Speed | | — | 756 | — | 630 | — | 524 | Mbps |
| $f_{DDRX4}$ | DDRX4 ECLK Frequency | | — | 378 | — | 315 | — | 262 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 95 | — | 79 | — | 66 | MHz |
| **7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9, 11]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After ECLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only | — | 0.290 | — | 0.320 | — | 0.345 | UI |
| $t_{DVE}$ | Input Data Hold After ECLK | | 0.739 | — | 0.699 | — | 0.703 | — | UI |
| $f_{DATA}$ | DDR71 Serial Input Data Speed | | — | 756 | — | 630 | — | 524 | Mbps |
| $f_{DDR71}$ | DDR71 ECLK Frequency | | — | 378 | — | 315 | — | 262 | MHz |
| $f_{CLKIN}$ | 7:1 Input Clock Frequency (SCLK) (minimum limited by PLL) | | — | 108 | — | 90 | — | 75 | MHz |
| **Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DIA}$ | Output Data Invalid After CLK Output | All MachXO2 devices, all sides | — | 0.520 | — | 0.550 | — | 0.580 | ns |
| $t_{DIB}$ | Output Data Invalid Before CLK Output | | — | 0.520 | — | 0.550 | — | 0.580 | ns |
| $f_{DATA}$ | DDRX1 Output Data Speed | | — | 300 | — | 250 | — | 208 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK frequency | | — | 150 | — | 125 | — | 104 | MHz |
| **Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[9, 11]** | | | | | | | | | |
| $t_{DVB}$ | Output Data Valid Before CLK Output | All MachXO2 devices, all sides | 1.210 | — | 1.510 | — | 1.870 | — | ns |
| $t_{DVA}$ | Output Data Valid After CLK Output | | 1.210 | — | 1.510 | — | 1.870 | — | ns |
| $f_{DATA}$ | DDRX1 Output Data Speed | | — | 300 | — | 250 | — | 208 | Mbps |
| fDDRX1 | DDRX1 SCLK Frequency (minimum limited by PLL) | | — | 150 | — | 125 | — | 104 | MHz |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Parameter | Description | Device | –6 | | –5 | | –4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DIA}$ | Output Data Invalid After CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only | — | 0.200 | — | 0.215 | — | 0.230 | ns |
| $t_{DIB}$ | Output Data Invalid Before CLK Output | | — | 0.200 | — | 0.215 | — | 0.230 | ns |
| $f_{DATA}$ | DDRX2 Serial Output Data Speed | | — | 664 | — | 554 | — | 462 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK frequency | | — | 332 | — | 277 | — | 231 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 166 | — | 139 | — | 116 | MHz |
| **Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 11]** | | | | | | | | | |
| $t_{DVB}$ | Output Data Valid Before CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only | 0.535 | — | 0.670 | — | 0.830 | — | ns |
| $t_{DVA}$ | Output Data Valid After CLK Output | | 0.535 | — | 0.670 | — | 0.830 | — | ns |
| $f_{DATA}$ | DDRX2 Serial Output Data Speed | | — | 664 | — | 554 | — | 462 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency (minimum limited by PLL) | | — | 332 | — | 277 | — | 231 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 166 | — | 139 | — | 116 | MHz |
| **Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DIA}$ | Output Data Invalid After CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only | — | 0.200 | — | 0.215 | — | 0.230 | ns |
| $t_{DIB}$ | Output Data Invalid Before CLK Output | | — | 0.200 | — | 0.215 | — | 0.230 | ns |
| $f_{DATA}$ | DDRX4 Serial Output Data Speed | | — | 756 | — | 630 | — | 524 | Mbps |
| $f_{DDRX4}$ | DDRX4 ECLK Frequency | | — | 378 | — | 315 | — | 262 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 95 | — | 79 | — | 66 | MHz |
| **Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 11]** | | | | | | | | | |
| $t_{DVB}$ | Output Data Valid Before CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only | 0.455 | — | 0.570 | — | 0.710 | — | ns |
| $t_{DVA}$ | Output Data Valid After CLK Output | | 0.455 | — | 0.570 | — | 0.710 | — | ns |
| $f_{DATA}$ | DDRX4 Serial Output Data Speed | | — | 756 | — | 630 | — | 524 | Mbps |
| $f_{DDRX4}$ | DDRX4 ECLK Frequency (minimum limited by PLL) | | — | 378 | — | 315 | — | 262 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 95 | — | 79 | — | 66 | MHz |
| **7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 11]** | | | | | | | | | |
| $t_{DIB}$ | Output Data Invalid Before CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only | — | 0.160 | — | 0.180 | — | 0.200 | ns |
| $t_{DIA}$ | Output Data Invalid After CLK Output | | — | 0.160 | — | 0.180 | — | 0.200 | ns |
| $f_{DATA}$ | DDR71 Serial Output Data Speed | | — | 756 | — | 630 | — | 524 | Mbps |
| $f_{DDR71}$ | DDR71 ECLK Frequency | | — | 378 | — | 315 | — | 262 | MHz |
| $f_{CLKOUT}$ | 7:1 Output Clock Frequency (SCLK) (minimum limited by PLL) | | — | 108 | — | 90 | — | 75 | MHz |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Parameter | Description | Device | –6 | | –5 | | –4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **LPDDR[9, 11]** | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only[12] | — | 0.369 | — | 0.395 | — | 0.421 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.529 | — | 0.530 | — | 0.527 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM LPDDR Serial Data Speed | | — | 280 | — | 250 | — | 208 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 140 | — | 125 | — | 104 | MHz |
| $f_{LPDDR}$ | LPDDR Data Transfer Rate | | 0 | 280 | 0 | 250 | 0 | 208 | Mbps |
| **DDR[9, 11]** | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only[12] | — | 0.350 | — | 0.387 | — | 0.414 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.545 | — | 0.538 | — | 0.532 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 300 | — | 250 | — | 208 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 150 | — | 125 | — | 104 | MHz |
| $f_{MEM_DDR}$ | MEM DDR Data Transfer Rate | | N/A | 300 | N/A | 250 | N/A | 208 | Mbps |
| **DDR[9, 11]** | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only[12] | — | 0.360 | — | 0.378 | — | 0.406 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.555 | — | 0.549 | — | 0.542 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 300 | — | 250 | — | 208 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 150 | — | 125 | — | 104 | MHz |
| $f_{MEM_DDR2}$ | MEM DDR2 Data Transfer Rate | | N/A | 300 | N/A | 250 | N/A | 208 | Mbps |

**Notes:**

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode tSU = tHO = (tDVE - tDVA - 0.03 ns)/2.
7. The tSU_DEL and tH_DEL values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
8. This number for general purpose usage. Duty cycle tolerance is +/– 10%.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

9. Duty cycle is +/–5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. Advance information for MachXO2 devices in 48 QFN packages.
12. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

## 3.22. MachXO2 External Switching Characteristics – ZE Devices

Over Recommended Operating Conditions

**Table 3.27. MachXO2 External Switching Characteristics – ZE Devices[1, 2, 3, 4, 5, 6, 7]**

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Clocks** | | | | | | | | | |
| **Primary Clocks** | | | | | | | | | |
| $fM_{AX_PRI}$[8] | Frequency for Primary Clock Tree | All MachXO2 devices | — | 150 | — | 125 | — | 104 | MHz |
| $t_{W_PRI}$ | Clock Pulse Width for Primary Clock | All MachXO2 devices | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| $t_{SKEW_PRI}$ | Primary Clock Skew Within a Device | MachXO2-256ZE | — | 1250 | — | 1272 | — | 1296 | ps |
| | | MachXO2-640ZE | — | 1161 | — | 1183 | — | 1206 | ps |
| | | MachXO2-1200ZE | — | 1213 | — | 1267 | — | 1322 | ps |
| | | MachXO2-2000ZE | — | 1204 | — | 1250 | — | 1296 | ps |
| | | MachXO2-4000ZE | — | 1195 | — | 1233 | — | 1269 | ps |
| | | MachXO2-7000ZE | — | 1243 | — | 1268 | — | 1296 | ps |
| **Edge Clock** | | | | | | | | | |
| $f_{MAX_EDGE}$[8] | Frequency for Edge Clock | MachXO2-1200 and larger devices | — | 210 | — | 175 | — | 146 | MHz |
| **Pin-LUT-Pin Propagation Delay** | | | | | | | | | |
| $t_{PD}$ | Best case propagation delay through one LUT-4 | All MachXO2 devices | — | 9.35 | — | 9.78 | — | 10.21 | ns |
| **General I/O Pin Parameters (Using Primary Clock without PLL)** | | | | | | | | | |
| $t_{CO}$ | Clock to Output – PIO Output Register | MachXO2-256ZE | — | 10.46 | — | 10.86 | — | 11.25 | ns |
| | | MachXO2-640ZE | — | 10.52 | — | 10.92 | — | 11.32 | ns |
| | | MachXO2-1200ZE | — | 11.24 | — | 11.68 | — | 12.12 | ns |
| | | MachXO2-2000ZE | — | 11.27 | — | 11.71 | — | 12.16 | ns |
| | | MachXO2-4000ZE | — | 11.28 | — | 11.78 | — | 12.28 | ns |
| | | MachXO2-7000ZE | — | 11.22 | — | 11.76 | — | 12.30 | ns |
| $t_{SU}$ | Clock to Data Setup – PIO Input Register | MachXO2-256ZE | –0.21 | — | –0.21 | — | –0.21 | — | ns |
| | | MachXO2-640ZE | –0.22 | — | –0.22 | — | –0.22 | — | ns |
| | | MachXO2-1200ZE | –0.25 | — | –0.25 | — | –0.25 | — | ns |
| | | MachXO2-2000ZE | –0.27 | — | –0.27 | — | –0.27 | — | ns |
| | | MachXO2-4000ZE | –0.31 | — | –0.31 | — | –0.31 | — | ns |
| | | MachXO2-7000ZE | –0.33 | — | –0.33 | — | –0.33 | — | ns |
| $t_H$ | Clock to Data Hold – PIO Input Register | MachXO2-256ZE | 3.96 | — | 4.25 | — | 4.65 | — | ns |
| | | MachXO2-640ZE | 4.01 | — | 4.31 | — | 4.71 | — | ns |
| | | MachXO2-1200ZE | 3.95 | — | 4.29 | — | 4.73 | — | ns |
| | | MachXO2-2000ZE | 3.94 | — | 4.29 | — | 4.74 | — | ns |
| | | MachXO2-4000ZE | 3.96 | — | 4.36 | — | 4.87 | — | ns |
| | | MachXO2-7000ZE | 3.93 | — | 4.37 | — | 4.91 | — | ns |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{SU_DEL}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-256ZE | 2.62 | — | 2.91 | — | 3.14 | — | ns |
| | | MachXO2-640ZE | 2.56 | — | 2.85 | — | 3.08 | — | ns |
| | | MachXO2-1200ZE | 2.30 | — | 2.57 | — | 2.79 | — | ns |
| | | MachXO2-2000ZE | 2.25 | — | 2.50 | — | 2.70 | — | ns |
| | | MachXO2-4000ZE | 2.39 | — | 2.60 | — | 2.76 | — | ns |
| | | MachXO2-7000ZE | 2.17 | — | 2.33 | — | 2.43 | — | ns |
| $t_{H_DEL}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-256ZE | –0.44 | — | –0.44 | — | –0.44 | — | ns |
| | | MachXO2-640ZE | –0.43 | — | –0.43 | — | –0.43 | — | ns |
| | | MachXO2-1200ZE | –0.28 | — | –0.28 | — | –0.28 | — | ns |
| | | MachXO2-2000ZE | –0.31 | — | –0.31 | — | –0.31 | — | ns |
| | | MachXO2-4000ZE | –0.34 | — | –0.34 | — | –0.34 | — | ns |
| | | MachXO2-7000ZE | –0.21 | — | –0.21 | — | –0.21 | — | ns |
| $f_{MAX_IO}$ | Clock Frequency of I/O and PFU Register | All MachXO2 devices | — | 150 | — | 125 | — | 104 | MHz |
| **General I/O Pin Parameters (Using Edge Clock without PLL)** | | | | | | | | | |
| $t_{COE}$ | Clock to Output – PIO Output Register | MachXO2-1200ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| | | MachXO2-2000ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| | | MachXO2-4000ZE | — | 10.89 | — | 11.28 | — | 11.67 | ns |
| | | MachXO2-7000ZE | — | 11.10 | — | 11.51 | — | 11.91 | ns |
| $t_{SUE}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200ZE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-2000ZE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| | | MachXO2-4000ZE | –0.15 | — | –0.15 | — | –0.15 | — | ns |
| | | MachXO2-7000ZE | –0.23 | — | –0.23 | — | –0.23 | — | ns |
| $t_{HE}$ | Clock to Data Hold – PIO Input Register | MachXO2-1200ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| | | MachXO2-2000ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| | | MachXO2-4000ZE | 3.60 | — | 3.89 | — | 4.28 | — | ns |
| | | MachXO2-7000ZE | 3.81 | — | 4.11 | — | 4.52 | — | ns |
| $t_{SU_DELE}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200ZE | 2.78 | — | 3.11 | — | 3.40 | — | ns |
| | | MachXO2-2000ZE | 2.78 | — | 3.11 | — | 3.40 | — | ns |
| | | MachXO2-4000ZE | 3.11 | — | 3.48 | — | 3.79 | — | ns |
| | | MachXO2-7000ZE | 2.94 | — | 3.30 | — | 3.60 | — | ns |
| $t_{H_DELE}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-1200ZE | –0.29 | — | -0.29 | — | –0.29 | — | ns |
| | | MachXO2-2000ZE | –0.29 | — | -0.29 | — | –0.29 | — | ns |
| | | MachXO2-4000ZE | –0.46 | — | -0.46 | — | –0.46 | — | ns |
| | | MachXO2-7000ZE | –0.37 | — | -0.37 | — | –0.37 | — | ns |
| **General I/O Pin Parameters (Using Primary Clock with PLL)** | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output – PIO Output Register | MachXO2-1200ZE | — | 7.95 | — | 8.07 | — | 8.19 | ns |
| | | MachXO2-2000ZE | — | 7.97 | — | 8.10 | — | 8.22 | ns |
| | | MachXO2-4000ZE | — | 7.98 | — | 8.10 | — | 8.23 | ns |
| | | MachXO2-7000ZE | — | 8.02 | — | 8.14 | — | 8.26 | ns |
| $t_{SUPLL}$ | Clock to Data Setup – PIO Input Register | MachXO2-1200ZE | 0.85 | — | 0.85 | — | 0.89 | — | ns |
| | | MachXO2-2000ZE | 0.84 | — | 0.84 | — | 0.86 | — | ns |
| | | MachXO2-4000ZE | 0.84 | — | 0.84 | — | 0.85 | — | ns |
| | | MachXO2-7000ZE | 0.83 | — | 0.83 | — | 0.81 | — | ns |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{HPLL}$ | Clock to Data Hold – PIO Input Register | MachXO2-1200ZE | 0.66 | — | 0.68 | — | 0.80 | — | ns |
| | | MachXO2-2000ZE | 0.68 | — | 0.70 | — | 0.83 | — | ns |
| | | MachXO2-4000ZE | 0.68 | — | 0.71 | — | 0.84 | — | ns |
| | | MachXO2-7000ZE | 0.73 | — | 0.74 | — | 0.87 | — | ns |
| $t_{SU_DELPLL}$ | Clock to Data Setup – PIO Input Register with Data Input Delay | MachXO2-1200ZE | 5.14 | — | 5.69 | — | 6.20 | — | ns |
| | | MachXO2-2000ZE | 5.11 | — | 5.67 | — | 6.17 | — | ns |
| | | MachXO2-4000ZE | 5.27 | — | 5.84 | — | 6.35 | — | ns |
| | | MachXO2-7000ZE | 5.15 | — | 5.71 | — | 6.23 | — | ns |
| $t_{H_DELPLL}$ | Clock to Data Hold – PIO Input Register with Input Data Delay | MachXO2-1200ZE | –1.36 | — | –1.36 | — | –1.36 | — | ns |
| | | MachXO2-2000ZE | –1.35 | — | –1.35 | — | –1.35 | — | ns |
| | | MachXO2-4000ZE | –1.43 | — | –1.43 | — | –1.43 | — | ns |
| | | MachXO2-7000ZE | –1.41 | — | –1.41 | — | –1.41 | — | ns |
| **Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After CLK | All MachXO2 devices, all sides | — | 0.382 | — | 0.401 | — | 0.417 | UI |
| $t_{DVE}$ | Input Data Hold After CLK | | 0.670 | — | 0.684 | — | 0.693 | — | UI |
| $f_{DATA}$ | DDRX1 Input Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| **Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[9, 11]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before CLK | All MachXO2 devices, all sides | 1.319 | — | 1.412 | — | 1.462 | — | ns |
| $t_{HO}$ | Input Data Hold After CLK | | 0.717 | — | 1.010 | — | 1.340 | — | ns |
| $f_{DATA}$ | DDRX1 Input Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| **Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After CLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only | — | 0.361 | — | 0.346 | — | 0.334 | UI |
| $t_{DVE}$ | Input Data Hold After CLK | | 0.602 | — | 0.625 | — | 0.648 | — | UI |
| $f_{DATA}$ | DDRX2 Serial Input Data Speed | | — | 280 | — | 234 | — | 194 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency | | — | 140 | — | 117 | — | 97 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 59 | — | 49 | MHz |
| **Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[9, 11]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before CLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only | 0.472 | — | 0.672 | — | 0.865 | — | ns |
| $t_{HO}$ | Input Data Hold After CLK | | 0.363 | — | 0.501 | — | 0.743 | — | ns |
| $f_{DATA}$ | DDRX2 Serial Input Data Speed | | — | 280 | — | 234 | — | 194 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency | | — | 140 | — | 117 | — | 97 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 59 | — | 49 | MHz |
| **Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After ECLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only | — | 0.307 | — | 0.316 | — | 0.326 | UI |
| $t_{DVE}$ | Input Data Hold After ECLK | | 0.662 | — | 0.650 | — | 0.649 | — | UI |
| $f_{DATA}$ | DDRX4 Serial Input Data Speed | | — | 420 | — | 352 | — | 292 | Mbps |
| $f_{DDRX4}$ | DDRX4 ECLK Frequency | | — | 210 | — | 176 | — | 146 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 53 | — | 44 | — | 37 | MHz |
| **Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[9, 11]** | | | | | | | | | |
| $t_{SU}$ | Input Data Setup Before ECLK | MachXO2-640U, MachXO2-1200/U | 0.434 | — | 0.535 | — | 0.630 | — | ns |
| $t_{HO}$ | Input Data Hold After ECLK | | 0.385 | — | 0.395 | — | 0.463 | — | ns |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{DATA}$ | DDRX4 Serial Input Data Speed | and larger devices, bottom side only | — | 420 | — | 352 | — | 292 | Mbps |
| $f_{DDRX4}$ | DDRX4 ECLK Frequency | | — | 210 | — | 176 | — | 146 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 53 | — | 44 | — | 37 | MHz |
| **7:1 LVDS Inputs – GDDR71_RX.ECLK.7.1[9, 11]** | | | | | | | | | |
| $t_{DVA}$ | Input Data Valid After ECLK | MachXO2-640U, MachXO2-1200/U and larger devices, bottom side only | — | 0.307 | — | 0.316 | — | 0.326 | UI |
| $t_{DVE}$ | Input Data Hold After ECLK | | 0.662 | — | 0.650 | — | 0.649 | — | UI |
| $f_{DATA}$ | DDR71 Serial Input Data Speed | | — | 420 | — | 352 | — | 292 | Mbps |
| $f_{DDR71}$ | DDR71 ECLK Frequency | | — | 210 | — | 176 | — | 146 | MHz |
| $f_{CLKIN}$ | 7:1 Input Clock Frequency (SCLK) (minimum limited by PLL) | | — | 60 | — | 50 | — | 42 | MHz |
| **Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DIA}$ | Output Data Invalid After CLK Output | All MachXO2 devices, all sides | — | 0.850 | — | 0.910 | — | 0.970 | ns |
| $t_{DIB}$ | Output Data Invalid Before CLK Output | | — | 0.850 | — | 0.910 | — | 0.970 | ns |
| $f_{DATA}$ | DDRX1 Output Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK frequency | | — | 70 | — | 58 | — | 49 | MHz |
| **Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[9, 11]** | | | | | | | | | |
| $t_{DVB}$ | Output Data Valid Before CLK Output | All MachXO2 devices, all sides | 2.720 | — | 3.380 | — | 4.140 | — | ns |
| $t_{DVA}$ | Output Data Valid After CLK Output | | 2.720 | — | 3.380 | — | 4.140 | — | ns |
| $f_{DATA}$ | DDRX1 Output Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{DDRX1}$ | DDRX1 SCLK Frequency (minimum limited by PLL) | | — | 70 | — | 58 | — | 49 | MHz |
| **Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DIA}$ | Output Data Invalid After CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only | — | 0.270 | — | 0.300 | — | 0.330 | ns |
| $t_{DIB}$ | Output Data Invalid Before CLK Output | | — | 0.270 | — | 0.300 | — | 0.330 | ns |
| $f_{DATA}$ | DDRX2 Serial Output Data Speed | | — | 280 | — | 234 | — | 194 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK frequency | | — | 140 | — | 117 | — | 97 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 59 | — | 49 | MHz |
| **Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[9, 11]** | | | | | | | | | |
| $t_{DVB}$ | Output Data Valid Before CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only | 1.445 | — | 1.760 | — | 2.140 | — | ns |
| $t_{DVA}$ | Output Data Valid After CLK Output | | 1.445 | — | 1.760 | — | 2.140 | — | ns |
| $f_{DATA}$ | DDRX2 Serial Output Data Speed | | — | 280 | — | 234 | — | 194 | Mbps |
| $f_{DDRX2}$ | DDRX2 ECLK Frequency (minimum limited by PLL) | | — | 140 | — | 117 | — | 97 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 59 | — | 49 | MHz |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[9, 11]** | | | | | | | | | |
| $t_{DIA}$ | Output Data Invalid After CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only | — | 0.270 | — | 0.300 | — | 0.330 | ns |
| $t_{DIB}$ | Output Data Invalid Before CLK Output | | — | 0.270 | — | 0.300 | — | 0.330 | ns |
| $f_{DATA}$ | DDRX4 Serial Output Data Speed | | — | 420 | — | 352 | — | 292 | Mbps |
| $f_{DDRX4}$ | DDRX4 ECLK Frequency | | — | 210 | — | 176 | — | 146 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 53 | — | 44 | — | 37 | MHz |
| **Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[9, 11]** | | | | | | | | | |
| $t_{DVB}$ | Output Data Valid Before CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only | 0.873 | — | 1.067 | — | 1.319 | — | ns |
| $t_{DVA}$ | Output Data Valid After CLK Output | | 0.873 | — | 1.067 | — | 1.319 | — | ns |
| $f_{DATA}$ | DDRX4 Serial Output Data Speed | | — | 420 | — | 352 | — | 292 | Mbps |
| $f_{DDRX4}$ | DDRX4 ECLK Frequency (minimum limited by PLL) | | — | 210 | — | 176 | — | 146 | MHz |
| $f_{SCLK}$ | SCLK Frequency | | — | 53 | — | 44 | — | 37 | MHz |
| **7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[9, 11]** | | | | | | | | | |
| $t_{DIB}$ | Output Data Invalid Before CLK Output | MachXO2-640U, MachXO2-1200/U and larger devices, top side only | — | 0.240 | — | 0.270 | — | 0.300 | ns |
| $t_{DIA}$ | Output Data Invalid After CLK Output | | — | 0.240 | — | 0.270 | — | 0.300 | ns |
| $f_{DATA}$ | DDR71 Serial Output Data Speed | | — | 420 | — | 352 | — | 292 | Mbps |
| $f_{DDR71}$ | DDR71 ECLK Frequency | | — | 210 | — | 176 | — | 146 | MHz |
| $f_{CLKOUT}$ | 7:1 Output Clock Frequency (SCLK) (minimum limited by PLL) | | — | 60 | — | 50 | — | 42 | MHz |
| **LPDDR[9, 11]** | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only[12] | — | 0.349 | — | 0.381 | — | 0.396 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.665 | — | 0.630 | — | 0.613 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM LPDDR Serial Data Speed | | — | 120 | — | 110 | — | 96 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 60 | — | 55 | — | 48 | MHz |
| $f_{LPDDR}$ | LPDDR Data Transfer Rate | | 0 | 120 | 0 | 110 | 0 | 96 | Mbps |
| **DDR[9, 11]** | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only[12] | — | 0.347 | — | 0.374 | — | 0.393 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.665 | — | 0.637 | — | 0.616 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Parameter | Description | Device | –3 | | –2 | | –1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| $f_{MEM_DDR}$ | MEM DDR Data Transfer Rate | | N/A | 140 | N/A | 116 | N/A | 98 | Mbps |
| **DDR2[9, 11]** | | | | | | | | | |
| $t_{DVADQ}$ | Input Data Valid After DQS Input | MachXO2-1200/U and larger devices, right side only[12] | — | 0.372 | — | 0.394 | — | 0.410 | UI |
| $t_{DVEDQ}$ | Input Data Hold After DQS Input | | 0.690 | — | 0.658 | — | 0.618 | — | UI |
| $t_{DQVBS}$ | Output Data Invalid Before DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Output Data Invalid After DQS Output | | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{DATA}$ | MEM DDR Serial Data Speed | | — | 140 | — | 116 | — | 98 | Mbps |
| $f_{SCLK}$ | SCLK Frequency | | — | 70 | — | 58 | — | 49 | MHz |
| $f_{MEM_DDR2}$ | MEM DDR2 Data Transfer Rate | | N/A | 140 | N/A | 116 | N/A | 98 | Mbps |

**Notes:**

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0 pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18. LPDDR timing numbers based in LVCMOS18.
5. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
6. For Generic DDRX1 mode tSU = tHO = (tDVE - tDVA - 0.03 ns)/2.
7. The tSU_DEL and tH_DEL values use the SCLK_ZERHOLD default step size. Each step is 167 ps (–3), 182 ps (–2), 195 ps (–1).
8. This number for general purpose usage. Duty cycle tolerance is +/–10%.
9. Duty cycle is +/– 5% for system usage.
10. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
11. Advance information for MachXO2 devices in 48 QFN packages.
12. DDR memory interface not supported in QN84 (84 QFN) and SG32 (32 QFN) packages.

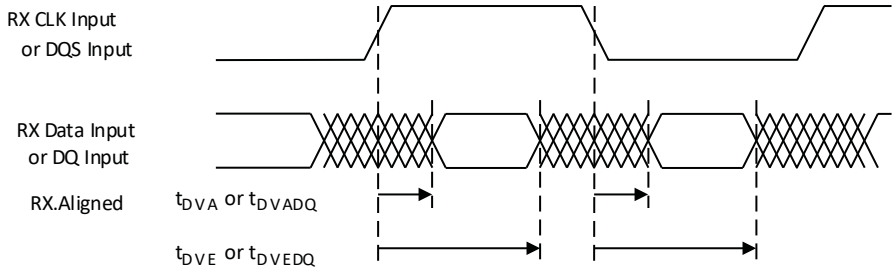



**Figure 3.5. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

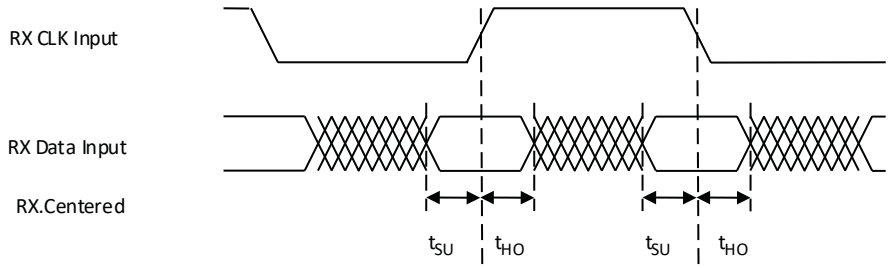



**Figure 3.6. Receiver RX.CLK.Centered Waveforms**

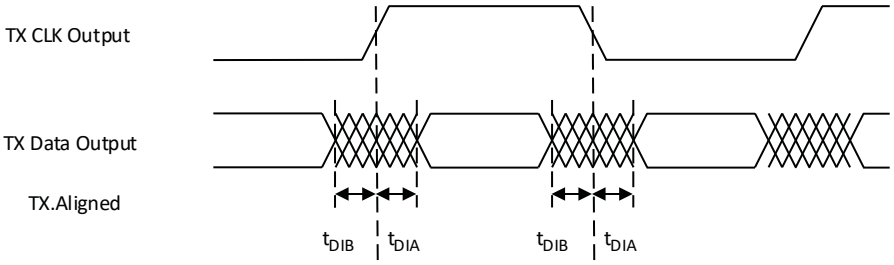



**Figure 3.7. Transmitter TX.CLK.Aligned Waveforms**

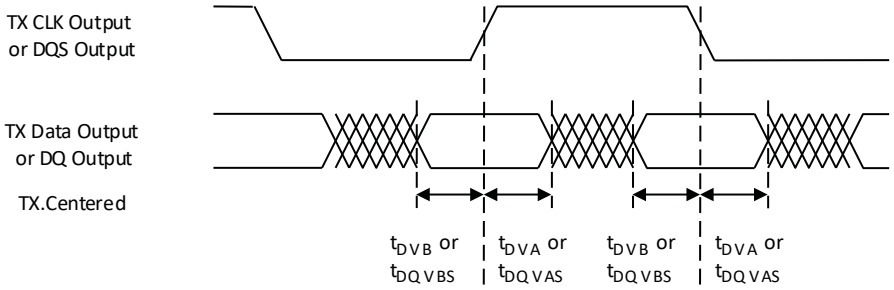



**Figure 3.8. Transmitter TX.CLK.Centered and MEM DDR Output Waveforms**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

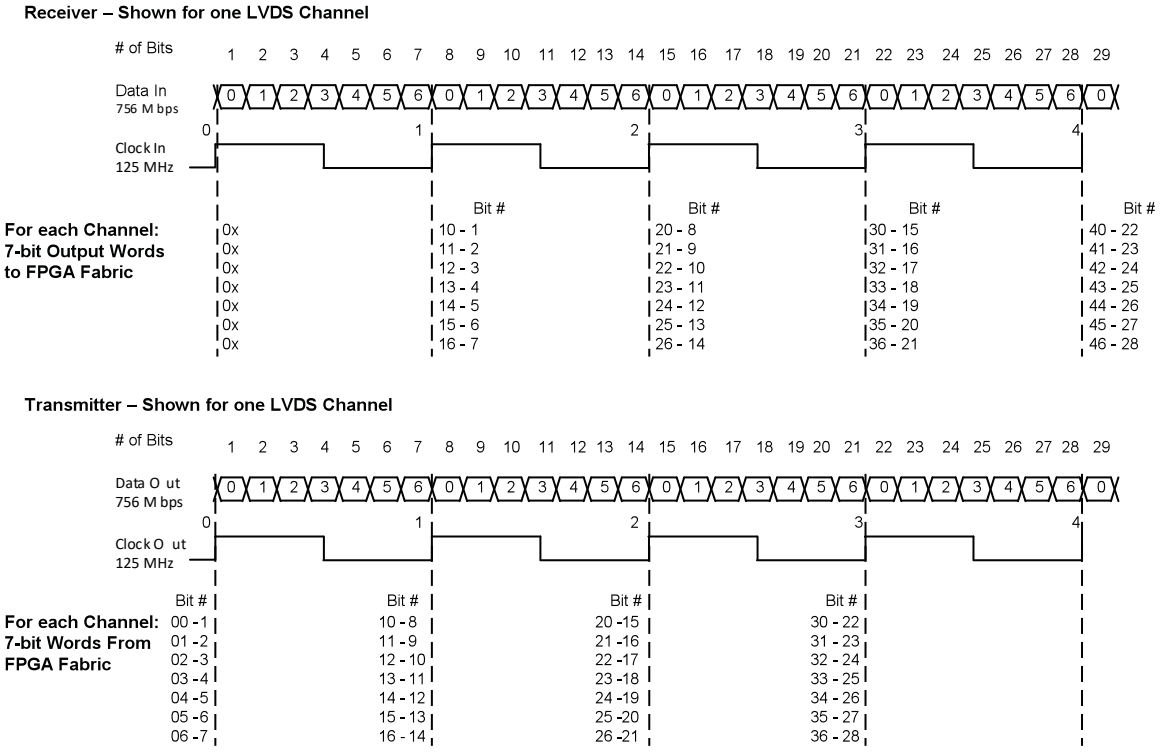



**Figure 3.9. GDDR71 Video Timing Waveforms**

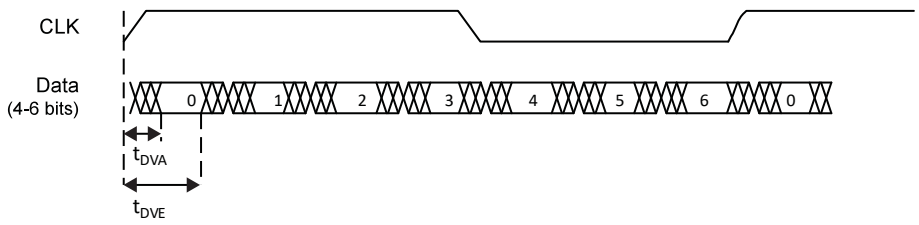



**Figure 3.10. Receiver GDDR71_RX. Waveforms**

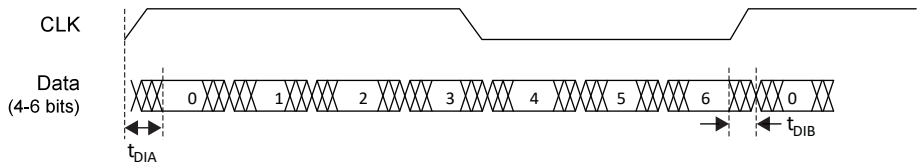



**Figure 3.11. Transmitter GDDR71_TX. Waveforms**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.23. sysCLOCK PLL Timing

Over Recommended Operating Conditions

**Table 3.28. sysCLOCK PLL Timing**

| Parameter | Descriptions | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | | 7 | 400 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS, CLKOS2) | | 1.5625 | 400 | MHz |
| $f_{OUT}$[2] | Output Frequency (CLKOS3 cascaded from CLKOS2) | | 0.0122 | 400 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 200 | 800 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | | 7 | 400 | MHz |
| **AC Characteristics** | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Without duty trim selected[3] | 45 | 55 | % |
| $t_{DT_TRIM}$[7] | Edge Duty Trim Accuracy | | –75 | 75 | % |
| $t_{PH}$[4] | Output Phase Accuracy | | –6 | 6 | % |
| $t_{OPJIT}$[1,8] | Output Clock Period Jitter | $f_{OUT}$ > 100 MHz | — | 150 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.007 | UIPP |
| | Output Clock Cycle-to-cycle Jitter | $f_{OUT}$ > 100 MHz | — | 180 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.009 | UIPP |
| | Output Clock Phase Jitter | $f_{PFD}$ > 100 MHz | — | 160 | ps p-p |
| | | $f_{PFD}$ < 100 MHz | — | 0.011 | UIPP |
| | Output Clock Period Jitter (Fractional-N) | $f_{OUT}$ > 100 MHz | — | 230 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.12 | UIPP |
| | Output Clock Cycle-to-cycle Jitter (Fractional-N) | $f_{OUT}$ > 100 MHz | — | 230 | ps p-p |
| | | $f_{OUT}$ < 100 MHz | — | 0.12 | UIPP |
| $t_{SPO}$ | Static Phase Offset | Divider ratio = integer | –120 | 120 | ps |
| $t_W$ | Output Clock Pulse Width | At 90% or 10%3 | 0.9 | — | ns |
| $t_{LOCK}$[2,5] | PLL Lock-in Time | | — | 15 | ms |
| $t_{UNLOCK}$ | PLL Unlock Time | | — | 50 | ns |
| $t_{IPJIT}$[6] | Input Clock Period Jitter | $f_{PFD}$ > 20 MHz | — | 1,000 | ps p-p |
| | | $f_{PFD}$ < 20 MHz | — | 0.02 | UIPP |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | ns |
| $t_{STABLE}$[5] | STANDBY High to PLL Stable | | — | 15 | ms |
| $t_{RST}$ | RST/RESETM Pulse Width | | 1 | — | ns |
| $t_{RSTREC}$ | RST Recovery Time | | 1 | — | ns |
| $t_{RST_DIV}$ | RESETC/D Pulse Width | | 10 | — | ns |
| $t_{RSTREC_DIV}$ | RESETC/D Recovery Time | | 1 | — | ns |
| $t_{ROTATE\text{-}SETUP}$ | PHASESTEP Setup Time | | 10 | — | ns |
| $t_{ROTATE_WD}$ | PHASESTEP Pulse Width | | 4 | — | VCO Cycles |

**Notes:**

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after tLOCK for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See MachXO2 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02157) for more details.
5. At minimum fPFD. As the fPFD increases the time will decrease to approximately 60% the value listed.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

## 3.24. MachXO2 Oscillator Output Frequency

**Table 3.29. MachXO2 Oscillator Output Frequency**

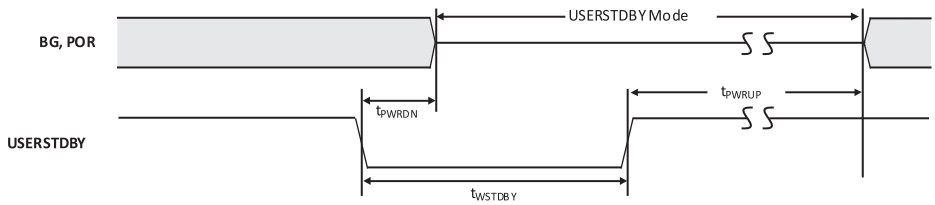
| Symbol | Parameter | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|
| $f_{MAX}$ | Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C) | 125.685 | 133 | 140.315 | MHz |
| | Oscillator Output Frequency (Industrial Grade Devices, –40 °C to 100 °C) | 124.355 | 133 | 141.645 | MHz |
| $t_{DT}$ | Output Clock Duty Cycle | 43 | 50 | 57 | % |
| $t_{OPJIT}$ | Output Clock Period Jitter | 0.01 | 0.012 | 0.02 | UIPP |
| $t_{STABLEOSC}$ | STDBY Low to Oscillator Stable | 0.01 | 0.05 | 0.1 | µs |

**Note:** Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies will be smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

## 3.25. MachXO2 Standby Mode Timing – HC/HE Devices

**Table 3.30. MachXO2 Standby Mode Timing – HC/HE Devices**

| Symbol | Parameter | Device | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PWRDN}$ | USERSTDBY High to Stop | All | — | — | 9 | ns |
| $t_{PWRUP}$ | USERSTDBY Low to Power-Up | LCMXO2-256 | | — | | µs |
| | | LCMXO2-640 | | — | | µs |
| | | LCMXO2-640U | | — | | µs |
| | | LCMXO2-1200 | 20 | — | 50 | µs |
| | | LCMXO2-1200U | | — | | µs |
| | | LCMXO2-2000 | | — | | µs |
| | | LCMXO2-2000U | | — | | µs |
| | | LCMXO2-4000 | | — | | µs |
| | | LCMXO2-7000 | | — | | µs |
| $t_{WSTDBY}$ | USERSTDBY Pulse Width | All | 18 | — | — | ns |




© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.26. MachXO2 Standby Mode Timing – ZE Devices

**Table 3.31. MachXO2 Standby Mode Timing – ZE Devices**

| Symbol | Parameter | Device | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PWRDN}$ | USERSTDBY High to Stop | All | — | — | 13 | ns |
| $t_{PWRUP}$ | USERSTDBY Low to Power-Up | LCMXO2-256 | | — | | µs |
| | | LCMXO2-640 | | — | | µs |
| | | LCMXO2-1200 | 20 | — | 50 | µs |
| | | LCMXO2-2000 | | — | | µs |
| | | LCMXO2-4000 | | — | | µs |
| | | LCMXO2-7000 | | — | | µs |
| $t_{WSTDBY}$ | USERSTDBY Pulse Width | All | 19 | — | — | ns |
| $t_{BNDGAPSTBL}$ | USERSTDBY High to Bandgap Stable | All | — | — | 15 | ns |

## 3.27. Flash Download Time

**Table 3.32. Flash Download Time**

| Symbol | Parameter | Device | Typ. | Units |
|---|---|---|---|---|
| $t_{REFRESH}$ | POR to Device I/O Active | LCMXO2-256 | 0.6 | ms |
| | | LCMXO2-640 | 1.0 | ms |
| | | LCMXO2-640U | 1.9 | ms |
| | | LCMXO2-1200 | 1.9 | ms |
| | | LCMXO2-1200U | 1.4 | ms |
| | | LCMXO2-2000 | 1.4 | ms |
| | | LCMXO2-2000U | 2.4 | ms |
| | | LCMXO2-4000 | 2.4 | ms |
| | | LCMXO2-7000 | 3.8 | ms |

**Notes:**

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.
2. The Flash download time is measured starting from the maximum voltage of POR trip point.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.28. JTAG Port Timing Specifications

**Table 3.33. JTAG Port Timing Specifications**

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{MAX}$ | TCK clock frequency | — | 25 | MHz |
| $t_{BTCPH}$ | TCK [BSCAN] clock pulse width high | 20 | — | ns |
| $t_{BTCPL}$ | TCK [BSCAN] clock pulse width low | 20 | — | ns |
| $t_{BTS}$ | TCK [BSCAN] setup time | 10 | — | ns |
| $t_{BTH}$ | TCK [BSCAN] hold time | 8 | — | ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | — | 10 | ns |
| $t_{BTCOEN}$ | TAP controller falling edge of clock to valid enable | — | 10 | ns |
| $t_{BTCRS}$ | BSCAN test capture register setup time | 8 | — | ns |
| $t_{BTCRH}$ | BSCAN test capture register hold time | 20 | — | ns |
| $t_{BUTCO}$ | BSCAN test update register, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to valid disable | — | 25 | ns |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to valid enable | — | 25 | ns |

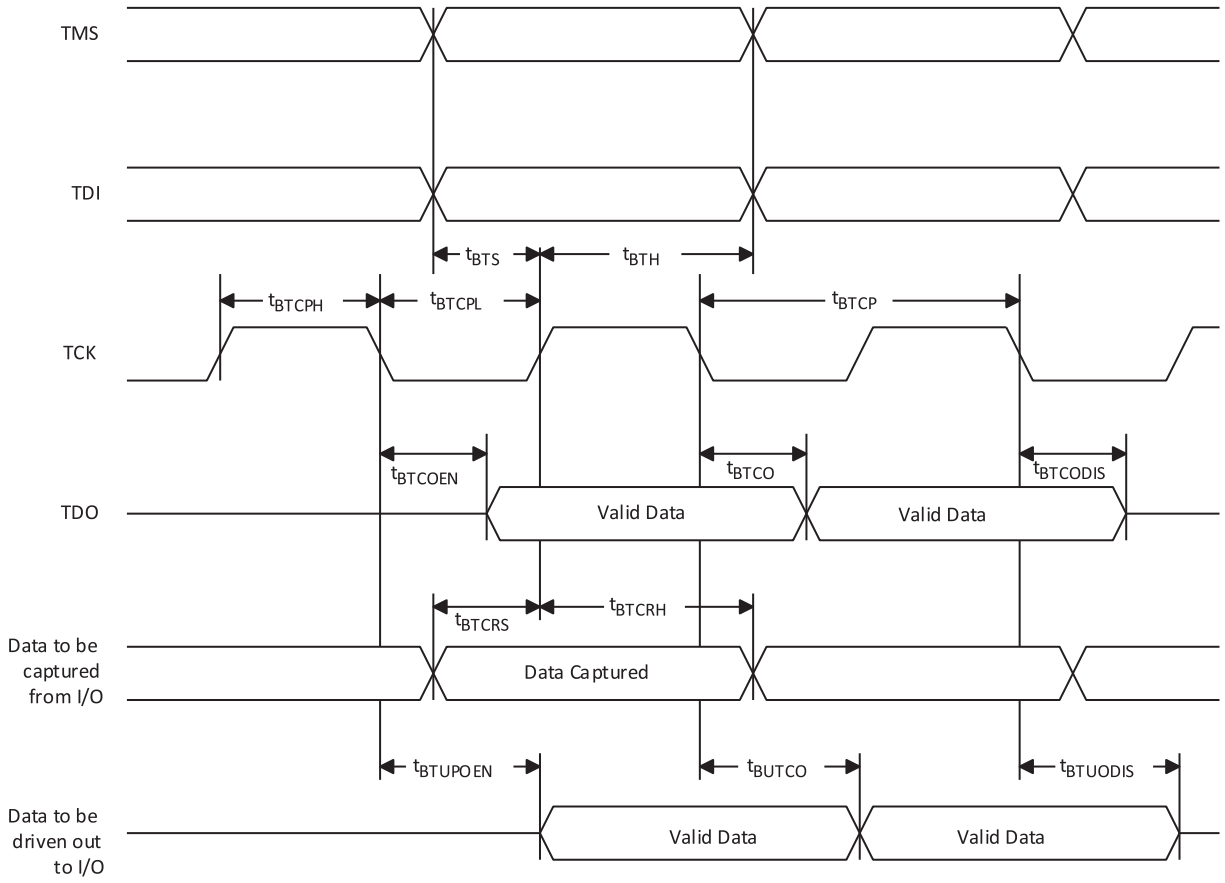



**Figure 3.12. JTAG Port Timing Waveforms**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.29. sysCONFIG Port Timing Specifications

**Table 3.34. sysCONFIG Port Timing Specifications**

| Symbol | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|
| **All Configuration Modes** | | | | | |
| $t_{PRGM}$ | PROGRAMN low pulse accept | | 55 | — | ns |
| $t_{PRGMJ}$ | PROGRAMN low pulse rejection | | — | 25 | ns |
| $t_{INITL}$ | INITN low time | LCMXO2-256 | — | 30 | µs |
| | | LCMXO2-640 | — | 35 | µs |
| | | LCMXO2-640U/ LCMXO2-1200 | — | 55 | µs |
| | | LCMXO2-1200U/ LCMXO2-2000 | — | 70 | µs |
| | | LCMXO2-2000U/ LCMXO2-4000 | — | 105 | µs |
| | | LCMXO2-7000 | — | 130 | µs |
| $t_{DPPINIT}$ | PROGRAMN low to INITN low | | — | 150 | ns |
| $t_{DPPDONE}$ | PROGRAMN low to DONE low | | — | 150 | ns |
| $t_{IODISS}$ | PROGRAMN low to I/O disable | | — | 120 | ns |
| **Slave SPI** | | | | | |
| $f_{MAX}$ | CCLK clock frequency | | — | 66 | MHz |
| $t_{CCLKH}$ | CCLK clock pulse width high | | 7.5 | — | ns |
| $t_{CCLKL}$ | CCLK clock pulse width low | | 7.5 | — | ns |
| $t_{STSU}$ | CCLK setup time | | 2 | — | ns |
| $t_{STH}$ | CCLK hold time | | 0 | — | ns |
| $t_{STCO}$ | CCLK falling edge to valid output | | — | 10 | ns |
| $t_{STOZ}$ | CCLK falling edge to valid disable | | — | 10 | ns |
| $t_{STOV}$ | CCLK falling edge to valid enable | | — | 10 | ns |
| $t_{SCS}$ | Chip select high time | | 25 | — | ns |
| $t_{SCSS}$ | Chip select setup time | | 3 | — | ns |
| $t_{SCSH}$ | Chip select hold time | | 3 | — | ns |
| **Master SPI** | | | | | |
| $f_{MAX}$ | MCLK clock frequency | | — | 133 | MHz |
| $t_{MCLKH}$ | MCLK clock pulse width high | | 3.75 | — | ns |
| $t_{MCLKL}$ | MCLK clock pulse width low | | 3.75 | — | ns |
| $t_{STSU}$ | MCLK setup time | | 5 | — | ns |
| $t_{STH}$ | MCLK hold time | | 1 | — | ns |
| $t_{CSSPI}$ | INITN high to chip select low | | 100 | 200 | ns |
| $t_{MCLK}$ | INITN high to first MCLK edge | | 0.75 | 1 | µs |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 3.30. I²C Port Timing Specifications

**Table 3.35. I²C Port Timing Specifications**

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{MAX}$ | Maximum SCL clock frequency | — | 400 | kHz |

**Notes:**

1. MachXO2 supports the following modes:
   - Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
   - Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
2. Refer to the I²C specification for timing requirements.

## 3.31. SPI Port Timing Specifications

**Table 3.36. SPI Port Timing Specifications**

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{MAX}$ | Maximum SCK clock frequency | — | 45 | MHz |

**Note:** Applies to user mode only. For configuration mode timing specifications, refer to Table 3.34 in this data sheet.

## 3.32. Switching Test Conditions

Figure 3.12 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3.6.

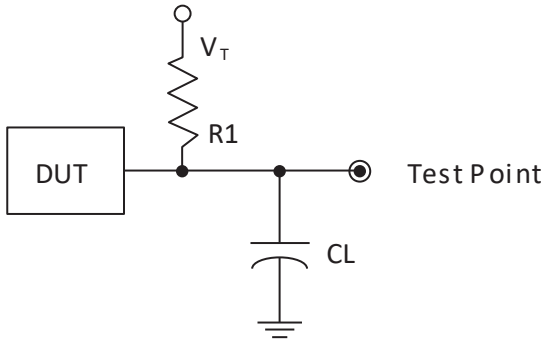



**Figure 3.13. Output Test Load, LVTTL and LVCMOS Standards**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Table 3.37. Test Fixture Required Components, Non-Terminated Interfaces**

| Test Condition | R1 | CL | Timing Ref. | VT |
|---|---|---|---|---|
| LVTTL and LVCMOS settings (L -> H, H -> L) | ∞ | 0pF | LVTTL, LVCMOS 3.3 = 1.5 V | — |
| | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVTTL and LVCMOS 3.3 (Z -> H) | 188 | 0pF | 1.5 V | $V_{OL}$ |
| LVTTL and LVCMOS 3.3 (Z -> L) | | | 1.5 V | $V_{OH}$ |
| Other LVCMOS (Z -> H) | | | $V_{CCIO}/2$ | $V_{OL}$ |
| Other LVCMOS (Z -> L) | | | $V_{CCIO}/2$ | $V_{OH}$ |
| LVTTL + LVCMOS (H -> Z) | | | $V_{OH} – 0.15$ V | $V_{OL}$ |
| LVTTL + LVCMOS (L -> Z) | | | $V_{OL} – 0.15$ V | $V_{OH}$ |

**Note:** Output test conditions for all other interfaces are determined by the respective standards.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# 4. Pinout Information

## 4.1. Signal Descriptions

**Table 4.1. Signal Descriptions**

| Signal Name | I/O | Descriptions |
|---|---|---|
| **General Purpose** | | |
| P[Edge] [Row/Column Number]_[A/B/C/D] | I/O | [Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).<br>[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.<br>[A/B/C/D] indicates the PIO within the group to which the pad is connected.<br>Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/O for user logic.<br>During configuration of the user-programmable I/O, the user has an option to tri-state the I/O and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/O to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/O will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/O with pull-up resistors enabled when the device is erased. |
| NC | — | No connect. |
| GND | — | GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. For QFN 48 package, the exposed die pad is the device ground. |
| VCC | — | VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply. |
| VCCIOx | — | VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply. |
| **PLL and Clock Functions** (Used as user-programmable I/O pins when not used for PLL or clock pins) | | |
| [LOC]_GPLL[T, C]_IN | — | Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement. |
| [LOC]_GPLL[T, C]_FB | — | Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement. |
| PCLK [n]_[2:0] | — | Primary Clock pads. One to three clock pads per side. |
| **Test and Programming** (Dual function pins used for test access port and during sysCONFIG™) | | |
| TMS | I | Test Mode Select input pin, used to control the 1149.1 state machine. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. |
| TDI | I | Test Data input pin, used to load data into the device using an 1149.1 state machine. |
| TDO | O | Output pin – Test Data output pin used to shift data out of the device using 1149.1. |
| JTAGENB | I | Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:<br>If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O. If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.<br>For more details, refer to MachXO2 Programming and Configuration Usage Guide (TN1204). |
| **Configuration** (Dual function pins used during sysCONFIG) | | |
| PROGRAMN | I | Initiates configuration sequence when asserted low. During configuration, or when reserved as PROGRAMN in user mode, this pin always has an active pull-up. |
| INITN | I/O | Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, or when reserved as INITn in user mode, this pin has an active pull-up. |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Signal Name | I/O | Descriptions |
|---|---|---|
| DONE | I/O | Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. During configuration, or when reserved as DONE in user mode, this pin has an active pull-up. |
| MCLK/CCLK | I/O | Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes. |
| SN | I | Slave SPI active low chip select input. |
| CSSPIN | I/O | Master SPI active low chip select output. |
| SI/SPISI | I/O | Slave SPI serial data input and master SPI serial data output. |
| SO/SPISO | I/O | Slave SPI serial data output and master SPI serial data input. |
| SCL | I/O | Slave $I^2C$ clock input and master $I^2C$ clock output. |
| SDA | I/O | Slave $I^2C$ data input and master $I^2C$ data output. |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 4.2. Pinout Information Summary

**Table 4.2. MachXO2-256/MachXO2-640/MachXO2-640U Pin Summary**

| | MachXO2-256 | | | | | MachXO2-640 | | | MachXO2-640U |
|---|---|---|---|---|---|---|---|---|---|
| | 32 QFN[1] | 48 QFN[3] | 64 ucBGA | 100 TQFP | 132 csBGA | 48 QFN[3] | 100 TQFP | 132 csBGA | 144 TQFP |
| **General Purpose I/O per Bank** | | | | | | | | | |
| Bank 0 | 8 | 10 | 9 | 13 | 13 | 10 | 18 | 19 | 27 |
| Bank 1 | 2 | 10 | 12 | 14 | 14 | 10 | 20 | 20 | 26 |
| Bank 2 | 9 | 10 | 11 | 14 | 14 | 10 | 20 | 20 | 28 |
| Bank 3 | 2 | 10 | 12 | 14 | 14 | 10 | 20 | 20 | 26 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Total General Purpose Single Ended I/O** | 21 | 40 | 44 | 55 | 55 | 40 | 78 | 79 | 107 |
| **Differential I/O per Bank** | | | | | | | | | |
| Bank 0 | 4 | 5 | 5 | 7 | 7 | 5 | 9 | 10 | 14 |
| Bank 1 | 1 | 5 | 6 | 7 | 7 | 5 | 10 | 10 | 13 |
| Bank 2 | 4 | 5 | 5 | 7 | 7 | 5 | 10 | 10 | 14 |
| Bank 3 | 1 | 5 | 6 | 7 | 7 | 5 | 10 | 10 | 13 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Total General Purpose Differential I/O** | 10 | 20 | 22 | 28 | 28 | 20 | 39 | 40 | 54 |
| **Dual Function I/O** | 22 | 25 | 27 | 29 | 29 | 25 | 29 | 29 | 33 |
| **High-speed Differential I/O** | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7 |
| **Gearboxes** | | | | | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7 |
| **DQS Groups** | | | | | | | | | |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 |
| **VCCIO Pins** | | | | | | | | | |
| Bank 0 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 3 |
| Bank 1 | 1 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 3 |
| Bank 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 3 |
| Bank 3 | 1 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 3 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **VCC** | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 4 |
| **GND[2]** | 2 | 1 | 8 | 8 | 8 | 1 | 8 | 10 | 12 |
| **NC** | 0 | 0 | 1 | 26 | 58 | 0 | 3 | 32 | 8 |
| **Reserved for Configuration** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **Total Count of Bonded Pins** | 32 | 49 | 64 | 100 | 132 | 49 | 100 | 132 | 144 |

**Notes:**

1. Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.
2. For 48 QFN package, exposed die pad is the device ground.
3. 48-pin QFN information is 'Advanced'.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Table 4.3. MachXO2-1200/MachXO2-1200U Pin Summary**

| | MachXO2-1200 | | | | | | MachXO2-1200U |
|---|---|---|---|---|---|---|---|
| | 100 TQFP | 132 csBGA | 144 TQFP | 25 WLCSP | 32 QFN* | 36 WLCSP | 256 ftBGA |
| **General Purpose I/O per Bank** | | | | | | | |
| Bank 0 | 18 | 25 | 27 | 11 | 9 | 15 | 50 |
| Bank 1 | 21 | 26 | 26 | 0 | 2 | 0 | 52 |
| Bank 2 | 20 | 28 | 28 | 7 | 9 | 9 | 52 |
| Bank 3 | 20 | 25 | 26 | 0 | 2 | 4 | 16 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 16 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 20 |
| **Total General Purpose Single Ended I/O** | 79 | 104 | 107 | 18 | 22 | 28 | 206 |
| **Differential I/O per Bank** | | | | | | | |
| Bank 0 | 9 | 13 | 14 | 5 | 4 | 7 | 25 |
| Bank 1 | 10 | 13 | 13 | 0 | 1 | 0 | 26 |
| Bank 2 | 10 | 14 | 14 | 2 | 4 | 4 | 26 |
| Bank 3 | 10 | 12 | 13 | 0 | 1 | 2 | 8 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 8 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 10 |
| **Total General Purpose Differential I/O** | 39 | 52 | 54 | 7 | 10 | 14 | 103 |
| **Dual Function I/O** | 31 | 33 | 33 | 18 | 22 | 25 | 33 |
| **High-speed Differential I/O** | | | | | | | |
| Bank 0 | 4 | 7 | 7 | 0 | 0 | 3 | 14 |
| **Gearboxes** | | | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 4 | 7 | 7 | 0 | 0 | 3 | 14 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 5 | 7 | 7 | 0 | 2 | 2 | 14 |
| **DQS Groups** | | | | | | | |
| Bank 1 | 1 | 2 | 2 | 0 | 0 | 0 | 2 |
| **VCCIO Pins** | | | | | | | |
| Bank 0 | 2 | 3 | 3 | 1 | 2 | 1 | 4 |
| Bank 1 | 2 | 3 | 3 | 0 | 1 | 0 | 4 |
| Bank 2 | 2 | 3 | 3 | 1 | 2 | 1 | 4 |
| Bank 3 | 3 | 3 | 3 | 0 | 1 | 1 | 1 |
| Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 2 |
| Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| **VCC** | 2 | 4 | 4 | 2 | 2 | 2 | 8 |
| **GND** | 8 | 10 | 12 | 2 | 2 | 2 | 24 |
| **NC** | 1 | 1 | 8 | 0 | 0 | 0 | 1 |
| **Reserved for Configuration** | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **Total Count of Bonded Pins** | 100 | 132 | 144 | 25 | 32 | 36 | 256 |

***Note:** Lattice recommends soldering the central thermal pad onto the top PCB ground for improved thermal resistance.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Table 4.4. MachXO2-2000/MachXO2-2000U Pin Summary**

| | MachXO2-2000 | | | | | | MachXO2-2000U |
|---|---|---|---|---|---|---|---|
| | 49 WLCSP | 100 TQFP | 132 csBGA | 144 TQFP | 256 caBGA | 256 ftBGA | 484 ftBGA |
| **General Purpose I/O per Bank** | | | | | | | |
| Bank 0 | 19 | 18 | 25 | 27 | 50 | 50 | 70 |
| Bank 1 | 0 | 21 | 26 | 28 | 52 | 52 | 68 |
| Bank 2 | 13 | 20 | 28 | 28 | 52 | 52 | 72 |
| Bank 3 | 0 | 6 | 7 | 8 | 16 | 16 | 24 |
| Bank 4 | 0 | 6 | 8 | 10 | 16 | 16 | 16 |
| Bank 5 | 6 | 8 | 10 | 10 | 20 | 20 | 28 |
| **Total General Purpose Single-Ended I/O** | 38 | 79 | 104 | 111 | 206 | 206 | 278 |
| **Differential I/O per Bank** | | | | | | | |
| Bank 0 | 7 | 9 | 13 | 14 | 25 | 25 | 35 |
| Bank 1 | 0 | 10 | 13 | 14 | 26 | 26 | 34 |
| Bank 2 | 6 | 10 | 14 | 14 | 26 | 26 | 36 |
| Bank 3 | 0 | 3 | 3 | 4 | 8 | 8 | 12 |
| Bank 4 | 0 | 3 | 4 | 5 | 8 | 8 | 8 |
| Bank 5 | 3 | 4 | 5 | 5 | 10 | 10 | 14 |
| **Total General Purpose Differential I/O** | 16 | 39 | 52 | 56 | 103 | 103 | 139 |
| **Dual Function I/O** | 24 | 31 | 33 | 33 | 33 | 33 | 37 |
| **High-speed Differential I/O** | | | | | | | |
| Bank 0 | 5 | 4 | 8 | 9 | 14 | 14 | 18 |
| **Gearboxes** | | | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 5 | 4 | 8 | 9 | 14 | 14 | 18 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 6 | 10 | 14 | 14 | 14 | 14 | 18 |
| **DQS Groups** | | | | | | | |
| Bank 1 | 0 | 1 | 2 | 2 | 2 | 2 | 2 |
| **VCCIO Pins** | | | | | | | |
| Bank 0 | 2 | 2 | 3 | 3 | 4 | 4 | 10 |
| Bank 1 | 0 | 2 | 3 | 3 | 4 | 4 | 10 |
| Bank 2 | 1 | 2 | 3 | 3 | 4 | 4 | 10 |
| Bank 3 | 0 | 1 | 1 | 1 | 1 | 1 | 3 |
| Bank 4 | 0 | 1 | 1 | 1 | 2 | 2 | 4 |
| Bank 5 | 1 | 1 | 1 | 1 | 1 | 1 | 3 |
| **VCC** | 2 | 2 | 4 | 4 | 8 | 8 | 12 |
| **GND** | 4 | 8 | 10 | 12 | 24 | 24 | 48 |
| **NC** | 0 | 1 | 1 | 4 | 1 | 1 | 105 |
| **Reserved for Configuration** | 1 | 1 | 1 | 1 | v | 1 | 1 |
| **Total Count of Bonded Pins** | 39 | 100 | 132 | 144 | 256 | 256 | 484 |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Table 4.5. MachXO2-4000 Pin Summary**

| | MachXO2-4000 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | **81 WLCSP** | **84 QFN** | **132 csBGA** | **144 TQFP** | **184 csBGA** | **256 caBGA** | **256 ftBGA** | **332 caBGA** | **484 fpBGA** |
| **General Purpose I/O per Bank** | | | | | | | | | |
| Bank 0 | 29 | 26 | 25 | 27 | 37 | 50 | 50 | 68 | 70 |
| Bank 1 | 0 | 10 | 26 | 29 | 37 | 52 | 52 | 68 | 68 |
| Bank 2 | 20 | 22 | 28 | 29 | 39 | 52 | 52 | 70 | 72 |
| Bank 3 | 7 | 0 | 7 | 9 | 10 | 16 | 16 | 24 | 24 |
| Bank 4 | 0 | 9 | 8 | 10 | 12 | 16 | 16 | 16 | 16 |
| Bank 5 | 7 | 0 | 10 | 10 | 15 | 20 | 20 | 28 | 28 |
| **Total General Purpose Single Ended I/O** | 63 | 67 | 104 | 114 | 150 | 206 | 206 | 274 | 278 |
| **Differential I/O per Bank** | | | | | | | | | |
| Bank 0 | 14 | 12 | 13 | 14 | 18 | 25 | 25 | 34 | 35 |
| Bank 1 | 0 | 4 | 13 | 14 | 18 | 26 | 26 | 34 | 34 |
| Bank 2 | 10 | 11 | 14 | 14 | 19 | 26 | 26 | 35 | 36 |
| Bank 3 | 3 | 0 | 3 | 4 | 4 | 8 | 8 | 12 | 12 |
| Bank 4 | 0 | 4 | 4 | 5 | 6 | 8 | 8 | 8 | 8 |
| Bank 5 | 3 | 0 | 5 | 5 | 7 | 10 | 10 | 14 | 14 |
| **Total General Purpose Differential I/O** | 30 | 31 | 52 | 56 | 72 | 103 | 103 | 137 | 139 |
| **Dual Function I/O** | 25 | 28 | 37 | 37 | 37 | 37 | 37 | 37 | 37 |
| **High-speed Differential I/O** | | | | | | | | | |
| Bank 0 | 10 | 8 | 8 | 9 | 8 | 18 | 18 | 18 | 18 |
| **Gearboxes** | | | | | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 10 | 8 | 8 | 9 | 9 | 18 | 18 | 18 | 18 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 10 | 11 | 14 | 14 | 12 | 18 | 18 | 18 | 18 |
| **DQS Groups** | | | | | | | | | |
| Bank 1 | 0 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| **VCCIO Pins** | | | | | | | | | |
| Bank 0 | 3 | 3 | 3 | 3 | 3 | 4 | 4 | 4 | 10 |
| Bank 1 | 0 | 1 | 3 | 3 | 3 | 4 | 4 | 4 | 10 |
| Bank 2 | 2 | 2 | 3 | 3 | 3 | 4 | 4 | 4 | 10 |
| Bank 3 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 2 | 3 |
| Bank 4 | 0 | 1 | 1 | 1 | 1 | 2 | 2 | 1 | 4 |
| Bank 5 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 2 | 3 |
| **VCC** | 4 | 4 | 4 | 4 | 4 | 8 | 8 | 8 | 12 |
| **GND** | 6 | 4 | 10 | 12 | 16 | 24 | 24 | 27 | 48 |
| **NC** | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 5 | 105 |
| **Reserved for configuration** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **Total Count of Bonded Pins** | 81 | 84 | 132 | 144 | 184 | 256 | 256 | 332 | 484 |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Table 4.6. MachXO2-7000 Pin Summary**

| | MachXO2-7000 | | | | | |
|---|---|---|---|---|---|---|
| | **144 TQFP** | **256 caBGA** | **256 ftBGA** | **332 caBGA** | **400 caBGA** | **484 fpBGA** |
| **General Purpose I/O per Bank** | | | | | | |
| Bank 0 | 27 | 50 | 50 | 68 | 83 | 82 |
| Bank 1 | 29 | 52 | 52 | 70 | 84 | 84 |
| Bank 2 | 29 | 52 | 52 | 70 | 84 | 84 |
| Bank 3 | 9 | 16 | 16 | 24 | 28 | 28 |
| Bank 4 | 10 | 16 | 16 | 16 | 24 | 24 |
| Bank 5 | 10 | 20 | 20 | 30 | 32 | 32 |
| **Total General Purpose Single Ended I/O** | 114 | 206 | 206 | 278 | 335 | 334 |
| **Differential I/O per Bank** | | | | | | |
| Bank 0 | 14 | 25 | 25 | 34 | 42 | 41 |
| Bank 1 | 14 | 26 | 26 | 35 | 42 | 42 |
| Bank 2 | 14 | 26 | 26 | 35 | 42 | 42 |
| Bank 3 | 4 | 8 | 8 | 12 | 14 | 14 |
| Bank 4 | 5 | 8 | 8 | 8 | 12 | 12 |
| Bank 5 | 5 | 10 | 10 | 15 | 16 | 16 |
| **Total General Purpose Differential I/O** | 56 | 103 | 103 | 139 | 168 | 167 |
| **Dual Function I/O** | 37 | 37 | 37 | 37 | 37 | 37 |
| **High-speed Differential I/O** | | | | | | |
| Bank 0 | 9 | 20 | 20 | 21 | 21 | 21 |
| **Gearboxes** | | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 9 | 20 | 20 | 21 | 21 | 21 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 14 | 20 | 20 | 21 | 21 | 21 |
| **DQS Groups** | | | | | | |
| Bank 1 | 2 | 2 | 2 | 2 | 2 | 2 |
| **VCCIO Pins** | | | | | | |
| Bank 0 | 3 | 4 | 4 | 4 | 5 | 10 |
| Bank 1 | 3 | 4 | 4 | 4 | 5 | 10 |
| Bank 2 | 3 | 4 | 4 | 4 | 5 | 10 |
| Bank 3 | 1 | 1 | 1 | 2 | 2 | 3 |
| Bank 4 | 1 | 2 | 2 | 1 | 2 | 4 |
| Bank 5 | 1 | 1 | 1 | 2 | 2 | 3 |
| **VCC** | 4 | 8 | 8 | 8 | 10 | 12 |
| **GND** | 12 | 24 | 24 | 27 | 33 | 48 |
| **NC** | 1 | 1 | 1 | 1 | 0 | 49 |
| **Reserved for Configuration** | 1 | 1 | 1 | 1 | 1 | 1 |
| **Total Count of Bonded Pins** | 144 | 256 | 256 | 332 | 400 | 484 |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 4.3. For Further Information

For further information regarding logic signal connections for various packages, refer to the MachXO2 Device Pinout Files.

## 4.4. Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Users must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

### 4.4.1. For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- Power Estimation and Management for MachXO2 Devices (TN1198)
- The Power Calculator tool is included with the Lattice design tools, or as a standalone download from www.latticesemi.com/software

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# 5. Ordering Information

## 5.1. MachXO2 Part Number Description

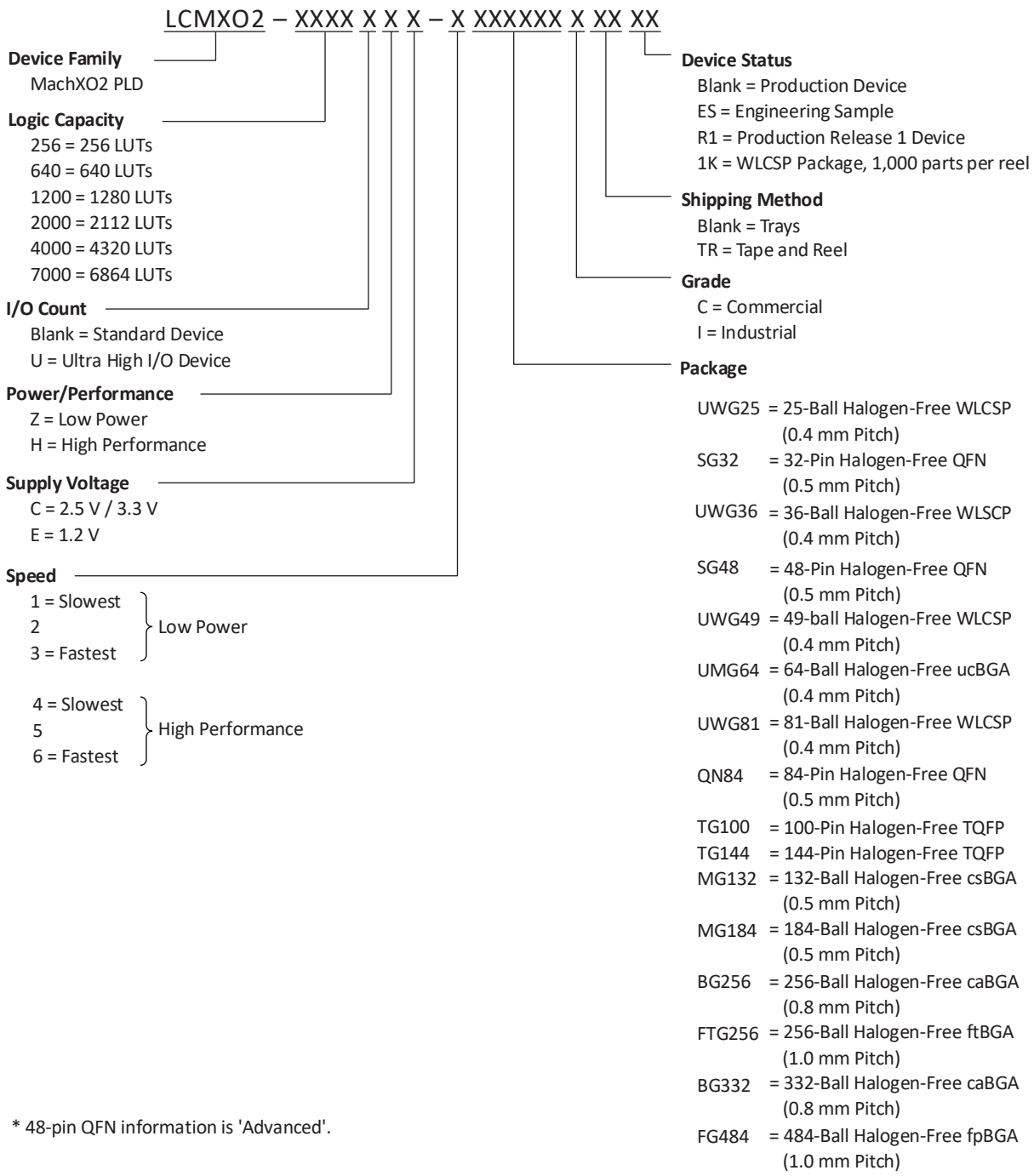



**Figure 5.1. MachXO2 Part Number Description**

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 5.2. Ordering Information

MachXO2 devices have top-side markings, for commercial and industrial grades, as shown below:

**Notes:**

1. Markings are abbreviated for small packages.
2. See PCN 05A-12 for information regarding a change to the top-side mark logo.

### 5.2.1. Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging

**Table 5.1. Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging**

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256ZE-1SG32C | 256 | 1.2 V | –1 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256ZE-2SG32C | 256 | 1.2 V | –2 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256ZE-3SG32C | 256 | 1.2 V | –3 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256ZE-1UMG64C | 256 | 1.2 V | –1 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256ZE-2UMG64C | 256 | 1.2 V | –2 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256ZE-3UMG64C | 256 | 1.2 V | –3 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256ZE-1TG100C | 256 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256ZE-2TG100C | 256 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256ZE-3TG100C | 256 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256ZE-1MG132C | 256 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256ZE-2MG132C | 256 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256ZE-3MG132C | 256 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640ZE-1TG100C | 640 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640ZE-2TG100C | 640 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640ZE-3TG100C | 640 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640ZE-1MG132C | 640 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640ZE-2MG132C | 640 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640ZE-3MG132C | 640 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-1SG32C | 1280 | 1.2 V | –1 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200ZE-2SG32C | 1280 | 1.2 V | –2 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200ZE-3SG32C | 1280 | 1.2 V | –3 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200ZE-1TG100C | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-2TG100C | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-3TG100C | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-1MG132C | 1280 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-2MG132C | 1280 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-3MG132C | 1280 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-1TG144C | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200ZE-2TG144C | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200ZE-3TG144C | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000ZE-1TG100C | 2112 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000ZE-2TG100C | 2112 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000ZE-3TG100C | 2112 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000ZE-1MG132C | 2112 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000ZE-2MG132C | 2112 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000ZE-3MG132C | 2112 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000ZE-1TG144C | 2112 | 1.2 V | –1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000ZE-2TG144C | 2112 | 1.2 V | –2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000ZE-3TG144C | 2112 | 1.2 V | –3 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000ZE-1BG256C | 2112 | 1.2 V | –1 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000ZE-2BG256C | 2112 | 1.2 V | –2 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000ZE-3BG256C | 2112 | 1.2 V | –3 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000ZE-1FTG256C | 2112 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000ZE-2FTG256C | 2112 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000ZE-3FTG256C | 2112 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000ZE-1QN84C | 4320 | 1.2 V | –1 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000ZE-2QN84C | 4320 | 1.2 V | –2 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000ZE-3QN84C | 4320 | 1.2 V | –3 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000ZE-1MG132C | 4320 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000ZE-2MG132C | 4320 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000ZE-3MG132C | 4320 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000ZE-1TG144C | 4320 | 1.2 V | –1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000ZE-2TG144C | 4320 | 1.2 V | –2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000ZE-3TG144C | 4320 | 1.2 V | –3 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000ZE-1BG256C | 4320 | 1.2 V | –1 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000ZE-2BG256C | 4320 | 1.2 V | –2 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000ZE-3BG256C | 4320 | 1.2 V | –3 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000ZE-1FTG256C | 4320 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000ZE-2FTG256C | 4320 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000ZE-3FTG256C | 4320 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000ZE-1BG332C | 4320 | 1.2 V | –1 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000ZE-2BG332C | 4320 | 1.2 V | –2 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000ZE-3BG332C | 4320 | 1.2 V | –3 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000ZE-1FG484C | 4320 | 1.2 V | –1 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000ZE-2FG484C | 4320 | 1.2 V | –2 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000ZE-3FG484C | 4320 | 1.2 V | –3 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000ZE-1TG144C | 6864 | 1.2 V | –1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000ZE-2TG144C | 6864 | 1.2 V | –2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000ZE-3TG144C | 6864 | 1.2 V | –3 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000ZE-1BG256C | 6864 | 1.2 V | –1 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000ZE-2BG256C | 6864 | 1.2 V | –2 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000ZE-3BG256C | 6864 | 1.2 V | –3 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000ZE-1FTG256C | 6864 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000ZE-2FTG256C | 6864 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000ZE-3FTG256C | 6864 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000ZE-1BG332C | 6864 | 1.2 V | –1 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000ZE-2BG332C | 6864 | 1.2 V | –2 | Halogen-Free caBGA | 332 | COM |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000ZE-3BG332C | 6864 | 1.2 V | –3 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000ZE-1FG484C | 6864 | 1.2 V | –1 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000ZE-2FG484C | 6864 | 1.2 V | –2 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000ZE-3FG484C | 6864 | 1.2 V | –3 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-1200ZE-1TG100CR1[1] | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-2TG100CR1[1] | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-3TG100CR1[1] | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200ZE-1MG132CR1[1] | 1280 | 1.2 V | –1 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-2MG132CR1[1] | 1280 | 1.2 V | –2 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-3MG132CR1[1] | 1280 | 1.2 V | –3 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200ZE-1TG144CR1[1] | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200ZE-2TG144CR1[1] | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200ZE-3TG144CR1[1] | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 144 | COM |

**Note:**

1. Specifications for the “LCMXO2-1200ZE-speed package CR1” are the same as the “LCMXO2-1200ZE-speed package C” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

### 5.2.2. High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

**Table 5.2. High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging**

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256HC-4SG32C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256HC-5SG32C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256HC-6SG32C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 32 | COM |
| LCMXO2-256HC-4SG48C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | COM |
| LCMXO2-256HC-5SG48C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | COM |
| LCMXO2-256HC-6SG48C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | COM |
| LCMXO2-256HC-4UMG64C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256HC-5UMG64C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256HC-6UMG64C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free ucBGA | 64 | COM |
| LCMXO2-256HC-4TG100C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256HC-5TG100C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256HC-6TG100C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-256HC-4MG132C | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256HC-5MG132C | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-256HC-6MG132C | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640HC-4SG48C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | COM |
| LCMXO2-640HC-5SG48C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | COM |
| LCMXO2-640HC-6SG48C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | COM |
| LCMXO2-640HC-4TG100C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640HC-5TG100C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640HC-6TG100C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-640HC-4MG132C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640HC-5MG132C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640HC-6MG132C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-640UHC-4TG144C | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-640UHC-5TG144C | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-640UHC-6TG144C | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200HC-4SG32C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200HC-5SG32C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200HC-6SG32C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 32 | COM |
| LCMXO2-1200HC-4TG100C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-5TG100C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-6TG100C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-4MG132C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-5MG132C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-6MG132C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-4TG144C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200HC-5TG144C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200HC-6TG144C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200UHC-4FTG256C | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-1200UHC-5FTG256C | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-1200UHC-6FTG256C | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000HC-4TG100C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HC-5TG100C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HC-6TG100C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HC-4MG132C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HC-5MG132C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HC-6MG132C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HC-4TG144C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HC-5TG144C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HC-6TG144C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HC-4BG256C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HC-5BG256C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HC-6BG256C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HC-4FTG256C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000HC-5FTG256C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000HC-6FTG256C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000UHC-4FG484C | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHC-5FG484C | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHC-6FG484C | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HC-4QN84C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-5QN84C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-6QN84C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 84 | COM |
| LCMXO2-4000HC-4MG132C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-5MG132C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-6MG132C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HC-4TG144C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-5TG144C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-6TG144C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HC-4BG256C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-5BG256C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | COM |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-4000HC-6BG256C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HC-4FTG256C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-5FTG256C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-6FTG256C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HC-4BG332C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-5BG332C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-6BG332C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HC-4FG484C | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HC-5FG484C | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HC-6FG484C | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HC-4TG144C | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HC-5TG144C | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HC-6TG144C | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HC-4BG256C | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HC-5BG256C | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HC-6BG256C | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HC-4FTG256C | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HC-5FTG256C | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HC-6FTG256C | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HC-4BG332C | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HC-5BG332C | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HC-6BG332C | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HC-4FG400C | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 400 | COM |
| LCMXO2-7000HC-5FG400C | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 400 | COM |
| LCMXO2-7000HC-6FG400C | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 400 | COM |
| LCMXO2-7000HC-4FG484C | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HC-5FG484C | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HC-6FG484C | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-1200HC-4TG100CR[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-5TG100CR[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-6TG100CR[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-1200HC-4MG132CR[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-5MG132CR[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-6MG132CR[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-1200HC-4TG144CR[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200HC-5TG144CR[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-1200HC-6TG144CR[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | COM |

**Note:**

1. Specifications for the “LCMXO2-1200HC-speed package CR1” are the same as the “LCMXO2-1200HC-speed package C” devices respectively, except as specified in the R1 Device Specifications of this data sheet.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### 5.2.3. High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging

**Table 5.3. High-Performance Commercial Grade Devices without Voltage Regulator, Halogen Free (RoHS) Packaging**

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000HE-4TG100C | 2112 | 1.2 V | –4 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HE-5TG100C | 2112 | 1.2 V | –5 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HE-6TG100C | 2112 | 1.2 V | –6 | Halogen-Free TQFP | 100 | COM |
| LCMXO2-2000HE-4TG144C | 2112 | 1.2 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HE-5TG144C | 2112 | 1.2 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HE-6TG144C | 2112 | 1.2 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-2000HE-4MG132C | 2112 | 1.2 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HE-5MG132C | 2112 | 1.2 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HE-6MG132C | 2112 | 1.2 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-2000HE-4BG256C | 2112 | 1.2 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HE-5BG256C | 2112 | 1.2 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HE-6BG256C | 2112 | 1.2 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-2000HE-4FTG256C | 2112 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000HE-5FTG256C | 2112 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000HE-6FTG256C | 2112 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-2000UHE-4FG484C | 2112 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHE-5FG484C | 2112 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-2000UHE-6FG484C | 2112 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HE-4TG144C | 4320 | 1.2 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HE-5TG144C | 4320 | 1.2 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HE-6TG144C | 4320 | 1.2 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-4000HE-4MG132C | 4320 | 1.2 V | –4 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HE-5MG132C | 4320 | 1.2 V | –5 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HE-6MG132C | 4320 | 1.2 V | –6 | Halogen-Free csBGA | 132 | COM |
| LCMXO2-4000HE-4BG256C | 4320 | 1.2 V | –4 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HE-4MG184C | 4320 | 1.2 V | –4 | Halogen-Free csBGA | 184 | COM |
| LCMXO2-4000HE-5MG184C | 4320 | 1.2 V | –5 | Halogen-Free csBGA | 184 | COM |
| LCMXO2-4000HE-6MG184C | 4320 | 1.2 V | –6 | Halogen-Free csBGA | 184 | COM |
| LCMXO2-4000HE-5BG256C | 4320 | 1.2 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HE-6BG256C | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-4000HE-4FTG256C | 4320 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HE-5FTG256C | 4320 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HE-6FTG256C | 4320 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-4000HE-4BG332C | 4320 | 1.2 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HE-5BG332C | 4320 | 1.2 V | –5 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HE-6BG332C | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-4000HE-4FG484C | 4320 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HE-5FG484C | 4320 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-4000HE-6FG484C | 4320 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HE-4TG144C | 6864 | 1.2 V | –4 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-5TG144C | 6864 | 1.2 V | –5 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-6TG144C | 6864 | 1.2 V | –6 | Halogen-Free TQFP | 144 | COM |
| LCMXO2-7000HE-4BG256C | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 256 | COM |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HE-5BG256C | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HE-6BG256C | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 256 | COM |
| LCMXO2-7000HE-4FTG256C | 6864 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-5FTG256C | 6864 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-6FTG256C | 6864 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | COM |
| LCMXO2-7000HE-4BG332C | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-5BG332C | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-6BG332C | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 332 | COM |
| LCMXO2-7000HE-4FG484C | 6864 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HE-5FG484C | 6864 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | COM |
| LCMXO2-7000HE-6FG484C | 6864 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | COM |

## 5.3. Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

**Table 5.4. Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging**

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256ZE-1SG32I | 256 | 1.2 V | –1 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-2SG32I | 256 | 1.2 V | –2 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-3SG32I | 256 | 1.2 V | –3 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256ZE-1UMG64I | 256 | 1.2 V | –1 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-2UMG64I | 256 | 1.2 V | –2 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-3UMG64I | 256 | 1.2 V | –3 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256ZE-1TG100I | 256 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-2TG100I | 256 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-3TG100I | 256 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256ZE-1MG132I | 256 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256ZE-2MG132I | 256 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256ZE-3MG132I | 256 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640ZE-1TG100I | 640 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-2TG100I | 640 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-3TG100I | 640 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640ZE-1MG132I | 640 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640ZE-2MG132I | 640 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640ZE-3MG132I | 640 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-1UWG25ITR[1] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1UWG25ITR50[3] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1UWG25ITR1K[2] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 25 | IND |
| LCMXO2-1200ZE-1UWG36ITR[1] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 36 | IND |
| LCMXO2-1200ZE-1UWG36ITR1K[2] | 1280 | 1.2 V | –1 | Halogen-Free WLCSP | 36 | IND |
| LCMXO2-1200ZE-1SG32I | 1280 | 1.2 V | –1 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-2SG32I | 1280 | 1.2 V | –2 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-3SG32I | 1280 | 1.2 V | –3 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200ZE-1TG100I | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-2TG100I | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-3TG100I | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-1MG132I | 1280 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-1200ZE-2MG132I | 1280 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-3MG132I | 1280 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-1TG144I | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-2TG144I | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-3TG144I | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000ZE-1UWG49ITR[1] | 2112 | 1.2 V | –1 | Halogen-Free WLCSP | 49 | IND |
| LCMXO2-2000ZE-1UWG49ITR50[3] | 2112 | 1.2 V | –1 | Halogen-Free WLCSP | 49 | IND |
| LCMXO2-2000ZE-1UWG49ITR1K[2] | 2112 | 1.2 V | –1 | Halogen-Free WLCSP | 49 | IND |
| LCMXO2-2000ZE-1TG100I | 2112 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000ZE-2TG100I | 2112 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000ZE-3TG100I | 2112 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000ZE-1MG132I | 2112 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000ZE-2MG132I | 2112 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000ZE-3MG132I | 2112 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000ZE-1TG144I | 2112 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000ZE-2TG144I | 2112 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000ZE-3TG144I | 2112 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000ZE-1BG256I | 2112 | 1.2 V | –1 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000ZE-2BG256I | 2112 | 1.2 V | –2 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000ZE-3BG256I | 2112 | 1.2 V | –3 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000ZE-1FTG256I | 2112 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000ZE-2FTG256I | 2112 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000ZE-3FTG256I | 2112 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000ZE-1UWG81ITR[1] | 4320 | 1.2 V | –1 | Halogen-Free WLCSP | 81 | IND |
| LCMXO2-4000ZE-1UWG81ITR1K[2] | 4320 | 1.2 V | –1 | Halogen-Free WLCSP | 81 | IND |
| LCMXO2-4000ZE-1QN84I | 4320 | 1.2 V | –1 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000ZE-2QN84I | 4320 | 1.2 V | –2 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000ZE-3QN84I | 4320 | 1.2 V | –3 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000ZE-1MG132I | 4320 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000ZE-2MG132I | 4320 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000ZE-3MG132I | 4320 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000ZE-1TG144I | 4320 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000ZE-2TG144I | 4320 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000ZE-3TG144I | 4320 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000ZE-1BG256I | 4320 | 1.2 V | –1 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000ZE-2BG256I | 4320 | 1.2 V | –2 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000ZE-3BG256I | 4320 | 1.2 V | –3 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000ZE-1FTG256I | 4320 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000ZE-2FTG256I | 4320 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000ZE-3FTG256I | 4320 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000ZE-1BG332I | 4320 | 1.2 V | –1 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000ZE-2BG332I | 4320 | 1.2 V | –2 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000ZE-3BG332I | 4320 | 1.2 V | –3 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000ZE-1FG484I | 4320 | 1.2 V | –1 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000ZE-2FG484I | 4320 | 1.2 V | –2 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000ZE-3FG484I | 4320 | 1.2 V | –3 | Halogen-Free fpBGA | 484 | IND |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000ZE-1TG144I | 6864 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000ZE-2TG144I | 6864 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000ZE-3TG144I | 6864 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000ZE-1BG256I | 6864 | 1.2 V | –1 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000ZE-2BG256I | 6864 | 1.2 V | –2 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000ZE-3BG256I | 6864 | 1.2 V | –3 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000ZE-1FTG256I | 6864 | 1.2 V | –1 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000ZE-2FTG256I | 6864 | 1.2 V | –2 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000ZE-3FTG256I | 6864 | 1.2 V | –3 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000ZE-1BG332I | 6864 | 1.2 V | –1 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000ZE-2BG332I | 6864 | 1.2 V | –2 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000ZE-3BG332I | 6864 | 1.2 V | –3 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000ZE-1FG484I | 6864 | 1.2 V | –1 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000ZE-2FG484I | 6864 | 1.2 V | –2 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000ZE-3FG484I | 6864 | 1.2 V | –3 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-1200ZE-1TG100IR1[4] | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-2TG100IR1[4] | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-3TG100IR1[4] | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200ZE-1MG132IR1[4] | 1280 | 1.2 V | –1 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-2MG132IR1[4] | 1280 | 1.2 V | –2 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-3MG132IR1[4] | 1280 | 1.2 V | –3 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200ZE-1TG144IR1[4] | 1280 | 1.2 V | –1 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-2TG144IR1[4] | 1280 | 1.2 V | –2 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200ZE-3TG144IR1[4] | 1280 | 1.2 V | –3 | Halogen-Free TQFP | 144 | IND |

**Notes:**

1. This part number has a tape and reel quantity of 5,000 units with a minimum order quantity of 10,000 units. Order quantities must be in increments of 5,000 units. For example, a 10,000 unit order will be shipped in two reels with one reel containing 5,000 units and the other reel with less than 5,000 units (depending on test yields). Unserviced backlog will be canceled.
2. This part number has a tape and reel quantity of 1,000 units with a minimum order quantity of 1,000. Order quantities must be in increments of 1,000 units. For example, a 5,000 unit order will be shipped as 5 reels of 1000 units each.
3. This part number has a tape and reel quantity of 50 units with a minimum order quantity of 50. Order quantities must be in increments of 50 units. For example, a 1,000 unit order will be shipped as 20 reels of 50 units each.
4. Specifications for the “LCMXO2-1200ZE-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### 5.3.1. High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging

**Table 5.5. High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging**

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-256HC-4SG32I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-5SG32I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-6SG32I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 32 | IND |
| LCMXO2-256HC-4SG48I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-5SG48I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-6SG48I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | IND |
| LCMXO2-256HC-4UMG64I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-5UMG64I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-6UMG64I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free ucBGA | 64 | IND |
| LCMXO2-256HC-4TG100I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-5TG100I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-6TG100I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-256HC-4MG132I | 256 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256HC-5MG132I | 256 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-256HC-6MG132I | 256 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640HC-4SG48I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-5SG48I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-6SG48I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 48 | IND |
| LCMXO2-640HC-4TG100I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-5TG100I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-6TG100I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-640HC-4MG132I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640HC-5MG132I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640HC-6MG132I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-640UHC-4TG144I | 640 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-640UHC-5TG144I | 640 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-640UHC-6TG144I | 640 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200HC-4SG32I | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200HC-5SG32I | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200HC-6SG32I | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 32 | IND |
| LCMXO2-1200HC-4TG100I | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-5TG100I | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-6TG100I | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-4MG132I | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-5MG132I | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-6MG132I | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-4TG144I | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200HC-5TG144I | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200HC-6TG144I | 1280 | 2.5 V/ 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200UHC-4FTG256I | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-1200UHC-5FTG256I | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-1200UHC-6FTG256I | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000HC-4TG100I | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000HC-5TG100I | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000HC-6TG100I | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000HC-4MG132I | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000HC-5MG132I | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000HC-6MG132I | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000HC-4TG144I | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000HC-5TG144I | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000HC-6TG144I | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000HC-4BG256I | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000HC-5BG256I | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000HC-6BG256I | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000HC-4FTG256I | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000HC-5FTG256I | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000HC-6FTG256I | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000UHC-4FG484I | 2112 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-2000UHC-5FG484I | 2112 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-2000UHC-6FG484I | 2112 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HC-4QN84I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-5QN84I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-6QN84I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free QFN | 84 | IND |
| LCMXO2-4000HC-4TG144I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-5TG144I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-6TG144I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HC-4MG132I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-5MG132I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-6MG132I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HC-4BG256I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-5BG256I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-6BG256I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HC-4FTG256I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-5FTG256I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-6FTG256I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HC-4BG332I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-5BG332I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-6BG332I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HC-4FG484I | 4320 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HC-5FG484I | 4320 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HC-6FG484I | 4320 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HC-4TG144I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-5TG144I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-6TG144I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HC-4BG256I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-5BG256I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-6BG256I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HC-4FTG256I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-5FTG256I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free ftBGA | 256 | IND |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HC-6FTG256I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HC-4BG332I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-5BG332I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-6BG332I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HC-4FG400I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-5FG400I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-6FG400I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 400 | IND |
| LCMXO2-7000HC-4FG484I | 6864 | 2.5 V / 3.3 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HC-5FG484I | 6864 | 2.5 V / 3.3 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HC-6FG484I | 6864 | 2.5 V / 3.3 V | –6 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-1200HC-4TG100IR[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-5TG100IR[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-6TG100IR[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-1200HC-4MG132IR[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-5MG132IR[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-6MG132IR[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-1200HC-4TG144IR[1] | 1280 | 2.5 V / 3.3 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200HC-5TG144IR[1] | 1280 | 2.5 V / 3.3 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-1200HC-6TG144IR[1] | 1280 | 2.5 V / 3.3 V | –6 | Halogen-Free TQFP | 144 | IND |

**Note:**

1. Specifications for the “LCMXO2-1200HC-speed package IR1” are the same as the “LCMXO2-1200ZE-speed package I” devices respectively, except as specified in the R1 Device Specifications section of this data sheet.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 5.4. High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging

**Table 5.6. High Performance Industrial Grade Devices Without Voltage Regulator, Halogen Free (RoHS) Packaging**

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-2000HE-4TG100I | 2112 | 1.2 V | –4 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000HE-5TG100I | 2112 | 1.2 V | –5 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000HE-6TG100I | 2112 | 1.2 V | –6 | Halogen-Free TQFP | 100 | IND |
| LCMXO2-2000HE-4MG132I | 2112 | 1.2 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000HE-5MG132I | 2112 | 1.2 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000HE-6MG132I | 2112 | 1.2 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-2000HE-4TG144I | 2112 | 1.2 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000HE-5TG144I | 2112 | 1.2 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000HE-6TG144I | 2112 | 1.2 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-2000HE-4BG256I | 2112 | 1.2 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000HE-5BG256I | 2112 | 1.2 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000HE-6BG256I | 2112 | 1.2 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-2000HE-4FTG256I | 2112 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000HE-5FTG256I | 2112 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000HE-6FTG256I | 2112 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-2000UHE-4FG484I | 2112 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-2000UHE-5FG484I | 2112 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-2000UHE-6FG484I | 2112 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HE-4MG132I | 4320 | 1.2 V | –4 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HE-5MG132I | 4320 | 1.2 V | –5 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HE-6MG132I | 4320 | 1.2 V | –6 | Halogen-Free csBGA | 132 | IND |
| LCMXO2-4000HE-4TG144I | 4320 | 1.2 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HE-5TG144I | 4320 | 1.2 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HE-6TG144I | 4320 | 1.2 V | –6 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-4000HE-4MG184I | 4320 | 1.2 V | –4 | Halogen-Free csBGA | 184 | IND |
| LCMXO2-4000HE-5MG184I | 4320 | 1.2 V | –5 | Halogen-Free csBGA | 184 | IND |
| LCMXO2-4000HE-6MG184I | 4320 | 1.2 V | –6 | Halogen-Free csBGA | 184 | IND |
| LCMXO2-4000HE-4BG256I | 4320 | 1.2 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HE-5BG256I | 4320 | 1.2 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HE-6BG256I | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-4000HE-4FTG256I | 4320 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HE-5FTG256I | 4320 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HE-6FTG256I | 4320 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-4000HE-4BG332I | 4320 | 1.2 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HE-5BG332I | 4320 | 1.2 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HE-6BG332I | 4320 | 1.2 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-4000HE-4FG484I | 4320 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HE-5FG484I | 4320 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-4000HE-6FG484I | 4320 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HE-4TG144I | 6864 | 1.2 V | –4 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HE-5TG144I | 6864 | 1.2 V | –5 | Halogen-Free TQFP | 144 | IND |
| LCMXO2-7000HE-6TG144I | 6864 | 1.2 V | –6 | Halogen-Free TQFP | 144 | IND |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

| Part Number | LUTs | Supply Voltage | Grade | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO2-7000HE-4BG256I | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HE-5BG256I | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HE-6BG256I | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 256 | IND |
| LCMXO2-7000HE-4FTG256I | 6864 | 1.2 V | –4 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HE-5FTG256I | 6864 | 1.2 V | –5 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HE-6FTG256I | 6864 | 1.2 V | –6 | Halogen-Free ftBGA | 256 | IND |
| LCMXO2-7000HE-4BG332I | 6864 | 1.2 V | –4 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HE-5BG332I | 6864 | 1.2 V | –5 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HE-6BG332I | 6864 | 1.2 V | –6 | Halogen-Free caBGA | 332 | IND |
| LCMXO2-7000HE-4FG484I | 6864 | 1.2 V | –4 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HE-5FG484I | 6864 | 1.2 V | –5 | Halogen-Free fpBGA | 484 | IND |
| LCMXO2-7000HE-6FG484I | 6864 | 1.2 V | –6 | Halogen-Free fpBGA | 484 | IND |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

## 5.5. R1 Device Specifications

The LCMXO2-1200ZE/HC "R1" devices have the same specifications as their Standard (non-R1) counterparts except as listed below. For more details on the R1 to Standard migration refer to Designing for Migration from MachXO2-1200-R1 to Standard Non-R1) Devices (AN8086).

- The User Flash Memory (UFM) cannot be programmed through the internal WISHBONE interface. It can still be programmed through the JTAG/SPI/$I^2C$ ports.
- The on-chip differential input termination resistor value is higher than intended. It is approximately 200 Ω as opposed to the intended 100 Ω. It is recommended to use external termination resistors for differential inputs. The on-chip termination resistors can be disabled through Lattice design software.
- Soft Error Detection logic may not produce the correct result when it is run for the first time after configuration. To use this feature, discard the result from the first operation. Subsequent operations will produce the correct result.
- Under certain conditions, IIH exceeds data sheet specifications. The following table provides more details:

**Table 5.7. R1 Device Specifications**

| Condition | Clamp | Pad Rising IIH Max. | Pad Falling IIH Min. | Steady State Pad High IIH | Steady State Pad Low IIL |
|---|---|---|---|---|---|
| VPAD > VCCIO | OFF | 1 mA | –1 mA | 1 mA | 10 µA |
| VPAD = VCCIO | ON | 10 µA | –10 µA | 10 µA | 10 µA |
| VPAD = VCCIO | OFF | 1 mA | –1 mA | 1 mA | 10 µA |
| VPAD < VCCIO | OFF | 10 µA | –10 µA | 10 µA | 10 µA |

- The user SPI interface does not operate correctly in some situations. During master read access and slave write access, the last byte received does not generate the RRDY interrupt.
- In GDDRX2, GDDRX4 and GDDR71 modes, ECLKSYNC may have a glitch in the output under certain conditions, leading to possible loss of synchronization.
- When using the hard $I^2C$ IP core, the $I^2C$ status registers I2C_1_SR and I2C_2_SR may not update correctly.
- PLL Lock signal glitches high when coming out of standby. This glitch lasts for about 10 µsec before returning low.
- Dual boot only available on HC devices, requires tying VCC and VCCIO2 to the same 3.3 V or 2.5 V supply.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# 6. Supplemental Information

A variety of technical notes for the MachXO2 family are available on the Lattice website.

- Power Estimation and Management for MachXO2 Devices (TN1198)
- MachXO2 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02157)
- Memory Usage Guide for MachXO2 Devices (FPGA-TN-02159)
- MachXO2 sysI/O Usage Guide (TN1202)
- Implementing High-Speed Interfaces with MachXO2 Devices (TN1203)
- MachXO2 Programming and Configuration Usage Guide (TN1204)
- Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (TN1205)
- MachXO2 SRAM CRC Error Detection Usage Guide (TN1206)
- Using TraceID in MachXO2 Devices (FPGA-TN-02084)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02025)
- MIPI D-PHY Bandwidth Matrix and Implementation (FPGA-TN-02090)
- Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices (AN8086)
- Boundary Scan Testability with Lattice sysIO Capability (AN8066)
- MachXO2 Device Pinout Files
- Thermal Management document
- Lattice design tools

For further information on interface standards, refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, LVDS, DDR, DDR2, LPDDR): www.jedec.org
- PCI: www.pcisig.com

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

# Revision History

**Revision 3.7, June 2021**

| Section | Change Summary |
|---|---|
| Acronyms in This Document | Added items. |
| Architecture | • Added a graphical MUX symbol in Figure 2.16. Input Gearbox.<br>• Changed *pull-up* to *pull-down* in the power-up sequence described in the Power-On-Reset section. |
| DC and Switching Characteristics | • Removed footnote indicators from Absolute Maximum Ratings heading.<br>• Added $V_{REF}$ (V) values for SSTL18D, SSTL25D, and HSTL18D in Table 3.13. sysI/O Recommended Operating Conditions. |
| — | Corrected superscript formatting in Table 1.1, Table 2.13, Table 3.10, Table 3.14, and Table 3.26. |

**Revision 3.6, December 2020**

| Section | Change Summary |
|---|---|
| All | Updated document template. |
| Introduction | Added 36-ball WLCSP and 81-ball WLCSP to Table 1.1. MachXO2 Family Selection Guide. |
| Pinout Information | • Added 36-WLCSP to Table 4.3. MachXO2-1200/MachXO2-1200U Pin Summary.<br>• Updated Table 4.5. MachXO2-4000 Pin Summary. Added 81-WLCSP and adjusted values of 84 QFN packages. |
| Ordering Information | • Added 36-ball WLCSP and 81-ball WLCSP to Figure 5.1. MachXO2 Part Number Description.<br>• Added part numbers: LCMXO2-1200ZE-1UWG36ITR , LCMXO2-1200ZE-1UWG36ITR1K, LCMXO2-4000ZE-1UWG81ITR, and LCMXO2-4000ZE-1UWG81ITR1K. |
| All | Updated document numbers of referenced technical notes. |

**Revision 3.5, October 2020**

| Section | Change Summary |
|---|---|
| DC and Switching Characteristics | Revised footnote 2 in the Static Supply Current – ZE Devices and Static Supply Current – HC/HE Devices tables. |

**Revision 3.4, June 2019**

| Section | Change Summary |
|---|---|
| All | • Changed document number from DS1035 to FPGA-DS-02056.<br>  • Added Disclaimers section.<br>  • Minor editorial and style changes. |
| Introduction | Added MIPI D-PHY Emulated to Features section. |
| Architecture | • Added MIPI D-PHY Bandwidth Matrix and Implementation reference to Table 2.12 footnote 3.<br>• Added power-up sequence to the Power-On-Reset section. |
| DC and Switching Characteristics | • Removed C2 row from the DC Electrical Characteristics table.<br>• Removed footnote 11 from MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables. |
| Supplemental Information | Added MIPI D-PHY Bandwidth Matrix and Implementation reference. |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Revision 3.3, March 2017**

| Section | Change Summary |
|---|---|
| DC and Switching Characteristics | • Updated the Absolute Maximum Ratings section. Added standards.<br>• Updated the sysI/O Recommended Operating Conditions section. Added standards.<br>• Updated the sysI/O Single-Ended DC Electrical Characteristics section. Added standards.<br>• Updated the MachXO2 External Switching Characteristics – HC/HE Devices section.<br>• Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$. The parameter descriptions were also modified.<br>• Updated the MachXO2 External Switching Characteristics – ZE Devices section.<br>• Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, the $D_{VB}$ and the $D_{VA}$ parameters were changed to $D_{IB}$ and $D_{IA}$. The parameter descriptions were also modified.<br>• Updated the sysCONFIG Port Timing Specifications section.<br>• Corrected the $t_{INITL}$ units from ns to µs. |
| Pinout Information | • Updated the Signal Descriptions section. Revised the descriptions of the PROGRAMN, INITN, and DONE signals.<br>• Updated the Pinout Information Summary section. Added footnote to MachXO2-1200 32 QFN. |
| Ordering Information | • Updated the MachXO2 Part Number Description section. Corrected the MG184, BG256, FTG256 package information. Added “(0.8 mm Pitch)” to BG332.<br>• Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section.<br>  • Updated LCMXO2-1200ZE-1UWG25ITR50 footnote.<br>  • Corrected footnote numbering typo.<br>  • Added the LCMXO2-2000ZE-1UWG49ITR50 and LCMXO2-2000ZE-1UWG49ITR1K part numbers. Updated/added footnote/s. |

**Revision 3.2, May 2016**

| Section | Change Summary |
|---|---|
| All | • Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.<br>• Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12. |
| Introduction | • Updated the Features section. Revised Table 1.1. MachXO2 Family Selection Guide.<br>  • Added ‘Advanced’ 48 QFN package.<br>  • Revised footnote 6.<br>  • Added footnote 9. |
| DC and Switching Characteristics | • Updated the MachXO2 External Switching Characteristics – HC/HE Devices section. Added footnote 12.<br>• Updated the MachXO2 External Switching Characteristics – ZE Devices section. Added footnote 12. |
| Pinout Information | • Updated the Signal Descriptions section. Added information on GND signal.<br>• Updated the Pinout Information Summary section.<br>  • Added ‘Advanced’ MachXO2-256 48 QFN values.<br>  • Added ‘Advanced’ MachXO2-640 48 QFN values.<br>  • Added footnote to GND.<br>  • Added footnotes 2 and 3. |
| Ordering Information | • Updated the MachXO2 Part Number Description section. Added ‘Advanced’ SG48 package and revised footnote.<br>• Updated the Ordering Information section.<br>  • Added part numbers for ‘Advanced’ QFN 48 package. |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

### Revision 3.1, March 2016

| Section | Change Summary |
|---|---|
| Introduction | • Updated the Features section. Revised Table 1.1, MachXO2 Family Selection Guide.<br>  • Added 32 QFN value for XO2-1200.<br>  • Added 84 QFN (7 mm x 7 mm, 0.5 mm) package.<br>  • Modified package name to 100-pin TQFP.<br>  • Modified package name to 144-pin TQFP.<br>  • Added footnote. |
| Architecture | Updated the Typical I/O Behavior During Power-up section. Removed reference to TN1202. |
| DC and Switching Characteristics | Updated the sysCONFIG Port Timing Specifications section. Revised $t_{DPPDONE}$ and $t_{DPPINIT}$ Max. values per PCN 03A-16, released March 2016. |
| Pinout Information | • Updated the Pinout Information Summary section.<br>  • Added MachXO2-1200 32 QFN values.<br>  • Added 'Advanced' MachXO2-4000 84 QFN values. |
| Ordering Information | • Updated the MachXO2 Part Number Description section. Added 'Advanced' QN84 package and footnote.<br>• Updated the Ordering Information section.<br>  • Added part numbers for 1280 LUTs QFN 32 package.<br>  • Added part numbers for 4320 LUTs QFN 84 package. |

### Revision 3.0, March 2015

| Section | Change Summary |
|---|---|
| Introduction | • Updated the Features section. Revised Table 1.1. MachXO2 Family Selection Guide.<br>• Changed 64-ball ucBGA dimension. |
| Architecture | Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins. |

### Revision 2.9, December 2014

| Section | Change Summary |
|---|---|
| Introduction | • Updated the Features section. Revised Table 1.1, MachXO2 Family Selection Guide.<br>  • Removed XO2-4000U data.<br>  • Removed 400-ball ftBGA.<br>  • Removed 25-ball WLCSP value for XO2-2000U. |
| DC and Switching Characteristics | • Updated the Recommended Operating Conditions section. Adjusted Max. values for $V_{CC}$ and $V_{CCIO}$.<br>• Updated the sysI/O Recommended Operating Conditions section. Adjusted Max. values for LVCMOS 3.3, LVTTL, PCI, LVDS33 and LVPECL. |
| Pinout Information | Updated the Pinout Information Summary section. Removed MachXO2-4000U. |
| Ordering Information | • Updated the MachXO2 Part Number Description section. Removed BG400 package.<br>• Updated the High-Performance Commercial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers.<br>• Updated the High-Performance Industrial Grade Devices with Voltage Regulator, Halogen Free (RoHS) Packaging section. Removed LCMXO2-4000UHC part numbers. |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Revision 2.8, November 2014**

| Section | Change Summary |
|---|---|
| Introduction | • Updated the Features section.<br>  • Revised I/O under Flexible Logic Architecture.<br>  • Revised standby power under Ultra Low Power Devices.<br>  • Revise input frequency range under Flexible On-Chip Clocking.<br>• Updated Table 1.1, MachXO2 Family Selection Guide.<br>  • Added XO2-4000U data.<br>  • Removed HE and ZE device options for XO2-4000.<br>  • Added 400-ball ftBGA. |
| Pinout Information | Updated the Pinout Information Summary section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400. |
| Ordering Information | • Updated the MachXO2 Part Number Description section. Added BG400 package.<br>• Updated the Ordering Information section. Added MachXO2-4000U caBGA400 and MachXO2-7000 caBGA400 part numbers. |

**Revision 2.7, October 2014**

| Section | Change Summary |
|---|---|
| Ordering Information | Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Fixed typo in LCMXO2-2000ZE-1UWG49ITR part number package. |
| Architecture | Updated the Supported Standards section. Added MIPI information to Table 2.12. Supported Input Standards and Table 2.13. Supported Output Standards. |
| DC and Switching Characteristics | • Updated the BLVDS section. Changed output impedance nominal values in Table 3.3, BLVDS DC Condition.<br>• Updated the LVPECL section. Changed output impedance nominal value in Table 3.4, LVPECL DC Condition.<br>• Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values. |

**Revision 2.6, July 2014**

| Section | Change Summary |
|---|---|
| DC and Switching Characteristics | • Updated sysI/O Single-Ended DC Electrical Characteristics section. Updated footnote 4.<br>• Updated Register-to-Register Performance section. Updated footnote. |
| Ordering Information | • Updated UW49 package to UWG49 in MachXO2 Part Number Description.<br>• Updated LCMXO2-2000ZE-1UWG49CTR package in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging. |

**Revision 2.5, May 2014**

| Section | Change Summary |
|---|---|
| Architecture | Updated TransFR (Transparent Field Reconfiguration) section. Updated TransFR description for PLL use during background Flash programming. |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Revision 2.4, February 2014**

| Section | Change Summary |
|---|---|
| Introduction | Included the 49 WLCSP package in the MachXO2 Family Selection Guide table. |
| Architecture | Added information to Standby Mode and Power Saving Options section. |
| Pinout Information | Added the XO2-2000 49 WLCSP in the Pinout Information Summary table. |
| Ordering Information | • Added UW49 package in MachXO2 Part Number Description.<br>• Added and LCMXO2-2000ZE-1UWG49CTR in Ultra Low Power Commercial Grade Devices, Halogen Free (RoHS) Packaging section.<br>• Added and LCMXO2-2000ZE-1UWG49ITR in Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging section. |

**Revision 2.3, December 2013**

| Section | Change Summary |
|---|---|
| Architecture | Updated information on CLKOS output divider in sysCLOCK Phase Locked Loops (PLLs) section. |
| DC and Switching Characteristics | • Updated Static Supply Current – ZE Devices table.<br>• Updated footnote 4 in sysI/O Single-Ended DC Electrical Characteristics table; Updated VIL Max. (V) data for LVCMOS 25 and LVCMOS 28.<br>• Updated VOS test condition in sysI/O Differential Electrical Characteristics - LVDS table. |

**Revision 2.2, September 2013**

| Section | Change Summary |
|---|---|
| Architecture | • Removed $I^2C$ Clock-Stretching feature per PCN #10A-13.<br>• Removed information on PDPR memory in RAM Mode section.<br>• Updated Supported Input Standards table. |
| DC and Switching Characteristics | Updated Power-On-Reset Voltage Levels table. |

**Revision 2.1, June 2013**

| Section | Change Summary |
|---|---|
| Architecture | • Architecture Overview – Added information on the state of the register on power-up and after configuration.<br>• sysCLOCK Phase Locked Loops (PLLs) section – Added missing cross reference to sysCLOCK PLL Timing table. |
| DC and Switching Characteristics | • Added slew rate information to footnote 2 of the MachXO2 External Switching Characteristics – HC/HE Devices and the MachXO2 External Switching Characteristics – ZE Devices tables.<br>• Power-On-Reset Voltage Levels table – Added symbols. |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Revision 2.0, January 2013**

| Section | Change Summary |
|---|---|
| Introduction | Updated the total number I/O to include JTAGENB. |
| Architecture | • Supported Output Standards table – Added 3.3 VCCIO (Typ.) to LVDS row.<br>• Changed SRAM CRC Error Detection to Soft Error Detection. |
| DC and Switching Characteristics | • Power Supply Ramp Rates table – Updated Units column for tRAMP symbol.<br>• Added new Maximum sysI/O Buffer Performance table.<br>• sysCLOCK PLL Timing table – Updated Min. column values for fIN, fOUT, fOUT2 and fPFD parameters. Added tSPO parameter. Updated footnote 6.<br>• MachXO2 Oscillator Output Frequency table – Updated symbol name for tSTABLEOSC.<br>• DC Electrical Characteristics table – Updated conditions for IIL, IIH symbols.<br>• Corrected parameters tDQVBS and tDQVAS<br>• Corrected MachXO2 ZE parameters tDVADQ and tDVEDQ |
| Pinout Information | Included the MachXO2-4000HE 184 csBGA package. |
| Ordering Information | Updated part number. |

**Revision 1.9, April 2012**

| Section | Change Summary |
|---|---|
| Architecture | Removed references to TN1200. |
| Ordering Information | • Updated the Device Status portion of the MachXO2 Part Number Description to include the 50 parts per reel for the WLCSP package.<br>• Added new part number and footnote 2 for LCMXO2-1200ZE-1UWG25ITR50.<br>• Updated footnote 1 for LCMXO2-1200ZE-1UWG25ITR. |
| Supplemental Information | Removed references to TN1200. |

**Revision 1.8, March 2012**

| Section | Change Summary |
|---|---|
| Introduction | Added 32 QFN packaging information to Features bullets and MachXO2 Family Selection Guide table. |
| DC and Switching Characteristics | Changed ‘STANDBY’ to ‘USERSTDBY’ in Standby Mode timing diagram. |
| Pinout Information | • Removed footnote from Pin Information Summary tables.<br>• Added 32 QFN package to Pin Information Summary table. |
| Ordering Information | • Updated Part Number Description and Ordering Information tables for 32 QFN package.<br>• Updated topside mark diagram in the Ordering Information section. |

**Revision 1.7, February 2012**

| Section | Change Summary |
|---|---|
| All | Updated document with new corporate logo. |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Revision 1.6, February 2012**

| Section | Change Summary |
|---|---|
| All | Data sheet status changed from preliminary to final. |
| Introduction | MachXO2 Family Selection Guide table – Removed references to 49-ball WLCSP. |
| DC and Switching Characteristics | • Updated Flash Download Time table.<br>• Modified Storage Temperature in the Absolute Maximum Ratings section.<br>• Updated $I_{DK}$ max in Hot Socket Specifications table.<br>• Modified Static Supply Current tables for ZE and HC/HE devices.<br>• Updated Power Supply Ramp Rates table.<br>• Updated Programming and Erase Supply Current tables.<br>• Updated data in the External Switching Characteristics table.<br>• Corrected Absolute Maximum Ratings for Dedicated Input Voltage Applied for LCMXO2 HC.<br>• DC Electrical Characteristics table – Minor corrections to conditions for $I_{IL}$, $I_{IH}$. |
| Pinout Information | • Removed references to 49-ball WLCSP.<br>• Signal Descriptions table – Updated description for GND, VCC, and VCCIOx.<br>• Updated Pin Information Summary table – Number of VCCIOs, GNDs, VCCs, and Total Count of Bonded Pins for MachXO2-256, 640, and 640U and Dual Function I/O for MachXO2-4000 332caBGA. |
| Ordering Information | Removed references to 49-ball WLCSP |

**Revision 1.4, August 2011**

| Section | Change Summary |
|---|---|
| Architecture | Updated information in Clock/Control Distribution Network and sysCLOCK Phase Locked Loops (PLLs). |
| DC and Switching Characteristics | Updated $I_{IL}$ and $I_{IH}$ conditions in the DC Electrical Characteristics table. |
| Pinout Information | • Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.<br>• Updated Pin Information Summary table: Dual Function I/O, DQS Groups Bank 1, Total General Purpose Single-Ended I/O, Differential I/O Per Bank, Total Count of Bonded Pins, Gearboxes.<br>• Added column of data for MachXO2-2000 49 WLCSP. |
| Ordering Information | • Updated R1 Device Specifications text section with information on migration from MachXO2-1200-R1 to Standard (non-R1) devices.<br>• Corrected Supply Voltage typo for part numbers: LCMX02-2000UHE-4FG484I, LCMX02-2000UHE-5FG484I, LCMX02-2000UHE-6FG484I.<br>• Added footnote for WLCSP package parts. |
| Supplemental Information | Removed reference to Stand-alone Power Calculator for MachXO2 Devices. Added reference to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (non-R1) Devices. |

**Revision 1.3, May 2011**

| Section | Change Summary |
|---|---|
| Multiple | Replaced “SED” with “SRAM CRC Error Detection” throughout the document. |
| DC and Switching Characteristics | Added footnote 1 to Program Erase Specifications table. |
| Pinout Information | • Updated Pin Information Summary tables.<br>• Signal name SO/SISPISO changed to SO/SPISO in the Signal Descriptions table. |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

**Revision 1.2, April 2011**

| Section | Change Summary |
|---|---|
| All | Data sheet status changed from Advance to Preliminary. |
| Introduction | Updated MachXO2 Family Selection Guide table. |
| Architecture | • Updated Supported Input Standards table.<br>• Updated sysMEM Memory Primitives diagram.<br>• Added differential SSTL and HSTL I/O standards. |
| DC and Switching Characteristics | • Updates following parameters: POR voltage levels, DC electrical characteristics, static supply current for ZE/HE/HC devices, static power consumption contribution of different components – ZE devices, programming and erase Flash supply current.<br>• Added VREF specifications to sysI/O recommended operating conditions.<br>• Updating timing information based on characterization.<br>• Added differential SSTL and HSTL I/O standards. |
| Ordering Information | • Added Ordering Part Numbers for R1 devices, and devices in WLCSP packages.<br>• Added R1 device specifications. |

**Revision 1.1, January 2011**

| Section | Change Summary |
|---|---|
| All | Included ultra-high I/O devices. |
| DC and Switching Characteristics | • Recommended Operating Conditions table – Added footnote 3.<br>• DC Electrical Characteristics table – Updated data for IIL, IIH. VHYST typical values updated.<br>• Generic DDRX2 Outputs with Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for TDIA and TDIB.<br>• Generic DDRX4 Outputs with Clock and Data Aligned at Pin (GDDRX4_TX.ECLK.Aligned) Using PCLK Pin for Clock Input tables – Updated data for TDIA and TDIB.<br>• Power-On-Reset Voltage Levels table - clarified note 3.<br>• Clarified VCCIO related recommended operating conditions specifications.<br>• Added power supply ramp rate requirements.<br>• Added Power Supply Ramp Rates table.<br>• Updated Programming/Erase Specifications table.<br>• Removed references to $V_{CCP}$. |
| Pinout Information | • Included number of 7:1 and 8:1 gearboxes (input and output) in the pin information summary tables.<br>• Removed references to VCCP. |

**Revision 1.0, November 2010**

| Section | Change Summary |
|---|---|
| All | Initial release. |

© 2010-2021 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Downloaded from Arrow.com.

www.latticesemi.com

Downloaded from Arrow.com.