Continued from preceding page

- DSP
  - FAVOR40 90MIPS
  - Audio CODEC: G.711, G.729A, and G.722
  - Jitter buffer control
  - Echo canceller
  - Melody function
  - PCM I/F
  - Power-saving mode
- Ethernet MAC: 2 channels
  - Protocol engine
  - Send/receive buffers: 16-KByte on-chip buffer memory
- A/D and D/A converters: two channels
- Package: SQFP208
- Supply voltages: I/O: 3.3 V, internal: 1.8 V

Specitications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}18$*1		-0.3 to +2.16	V
	$V_{DD}33$*2		-0.3 to +3.96	V
I/O voltages	V_I33, V_O33		-0.3 to $V_{DD}3$ +0.3 (Max 3.96V)	V
I/O current	I_I, I_O*3		±20	mA
Allowable power dissipation	Pd max	Ta ≤ 70°C	900	mW
Operating temperature	Topr		-30 to +70	°C
Storage temperature	Tstg		-55 to +125	°C

Note: *1: Internal and I/O supply voltage
*2: Analog section and 3.3-V I/O supply voltage
*3: Per individual basic I/O cell

Allowable Operating Ranges at Ta = –30 to +70 °C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}18$		1.62	1.8	1.98	V
	$V_{DD}33$		3.0	3.3	3.6	V
Input voltage	$V_{IN}33$		0	—	$V_{DD}33$	V

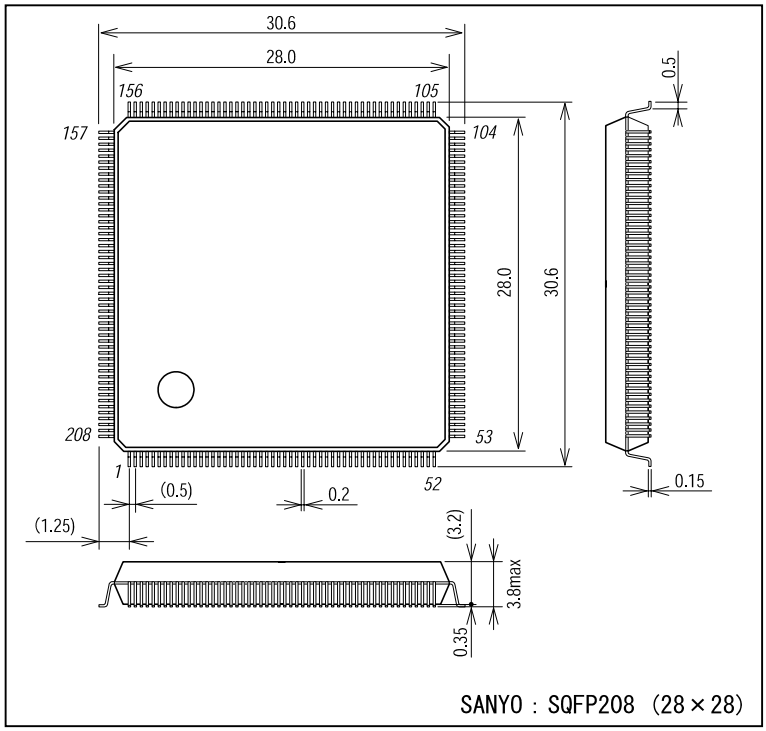
DC Characteristics at Ta = –30 to +70 °C, $V_{DD}33$ = 3.0 V to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage	V_{IH}	CMOS level pins	2.0	—	—	V
Input low level voltage	V_{IL}		—	—	0.3 $V_{DD}33$	V
Input high level voltage	V_{IH}	CMOS level Schmidt trigger pins	2.0	—	—	V
Input low level voltage	V_{IL}		—	—	0.3 $V_{DD}33$	V
Output high level voltage	V_{OH}	I_{OH} = –4 mA	$V_{DD}33$ –0.4	—	—	V
Output low level voltage	V_{OL}	I_{OL} = 4 mA	—	—	0.4	V
Output leakage current	I_{OZ}	When generating HiZ output	-10	—	+10	µA
Pull-down resistance	R_{DN}		50	100	200	kΩ
Pull-up resistance	R_{UP}		50	100	200	kΩ
Oscillator frequency	$f_{CLK}1$			8.192		MHz
Current drain	$I_{DD}18$	In operation ($V_{DD}18$)	—	100	—	mA
	$I_{DD}33$	In operation ($V_{DD}33$)	—	40	—	mA

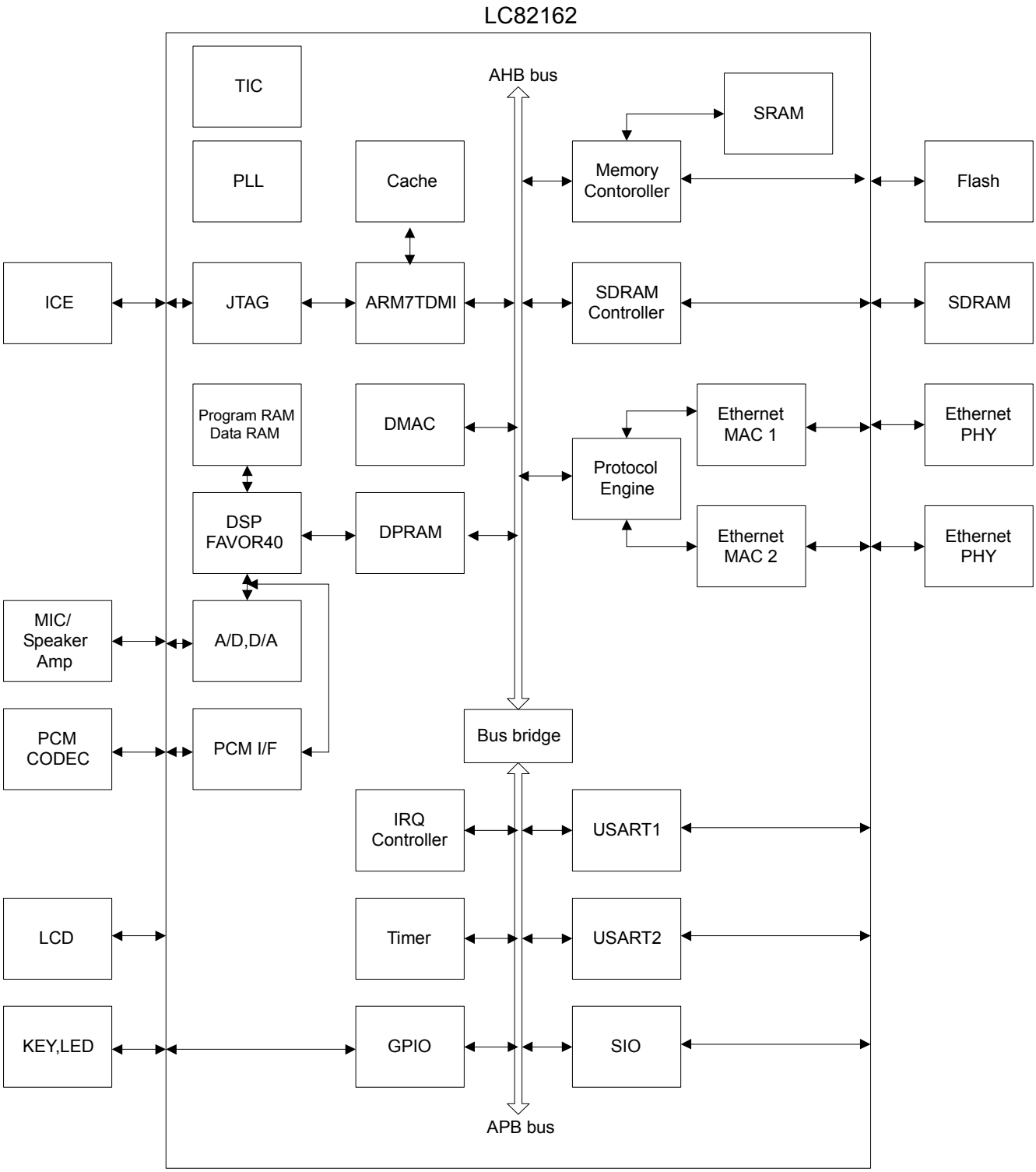
Package Dimensions

unit : mm

3210 [LC82162]



Block Diagram



Pin Functions

I/O		Pin type			
I	Input pin	3IC	3.3 V CMOS input	3O8	3.3 V 8 mA output
O	Output pin	3IS	3.3 V Schmitt input	3T4	3.3 V 4 mA tristate output
B	Bidirectional pin	3ICD	3.3 V CMOS input pull-down	3A	3.3 V analog
P	Power supply pin	3ICU	3.3 V CMOS input pull-up	1A	1.8 V analog
NC	Unused	3O4	3.3 V 4 mA output	X	Oscillator amplifier

Pin No.	Pin name	I/O	Pin type	Function
1	DGND	P		Digital system ground
2	A15	O	3O4	Address bus
3	A14	O	3O4	
4	A13	O	3O4	
5	A12	O	3O4	
6	A11	O	3O4	
7	A10	O	3O4	
8	A9	O	3O4	
9	A8	O	3O4	
10	A7	O	3O4	
11	A6	O	3O4	
12	A5	O	3O4	
13	TEST3	I	3ICD	Test pin
14	TEST2	I	3ICD	Test pin
15	TEST1	I	3ICD	Test pin
16	PVDD18	P		PLL power supply (+1.8 V)
17	PGND	P		PLL ground
18	VCNT1	O	1A	PLL1 VCO control
19	WAITn/PB12	B	3IC/3T4	External wait signal, or I/O port
20	RSTOUTn	O	3O4	Watchdog timer reset output
21	TEST0	I	3ICD	Test pin
22	ROMBUSW	I	3ICD	Memory bus width selection
23	A4	O	3O4	Address bus
24	A3	O	3O4	
25	A2	O	3O4	
26	A1	O	3O4	
27	A0	O	3O4	
28	MWRLn	O	3O4	External memory write signal
29	MWRHn	O	3O4	External memory write signal
30	MRDn	O	3O4	External memory read signal
31	RESETn	I	3IS	Reset
32	XTAL1	I	X	Crystal oscillator connection (8.192 MHz)
33	XTAL2	O	X	
34	DVDD3	P		Digital system power supply (+3.3 V)
35	DGND	P		Digital system ground
36	CS0n	O	3O4	External memory chip select 0
37	CS1n/PD4	B	3ICU/3T4	External memory chip select 1 or I/O port
38	DQM3	O	3O4	SDRAM byte mask 3
39	DQM2	O	3O4	SDRAM byte mask 2
40	DRCS1n	O	3O4	SDRAM chip select 1
41	DRCS0n	O	3O4	SDRAM chip select 0
42	RASn	O	3O4	Row address strobe
43	CASn	O	3O4	Column address strobe
44	DRCLK	O	3O8	SDRAM clock
45	DRWE	O	3O4	SDRAM write enable
46	DQM1	O	3O4	SDRAM byte mask 1
47	DQM0	O	3O4	SDRAM byte mask 0
48	M1_TXEN	O	3O4	MAC1 transmit enable

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Pin No.	Pin name	I/O	Pin type	Function
49	M1_TXCLK	I	3IC	MAC1 transmit clock
50	M1_TXD3	O	3O4	MAC1 transmit data
51	M1_TXD2	O	3O4	MAC1 transmit data
52	DVDD18	P		Digital system power supply (+1.8 V)
53	DGND	P		Digital system ground
54	M1_TXD1	O	3O4	MAC1 transmit data
55	M1_TXD0	O	3O4	MAC1 transmit data
56	M1_RXCLK	I	3IC	MAC1 receive clock
57	M1_RXDV	I	3IC	MAC1 receive data valid
58	M1_RXER	I	3IC	MAC1 receive data error
59	M1_RXD3	I	3IC	MAC1 receive data
60	M1_RXD2	I	3IC	MAC1 receive data
61	M1_RXD1	I	3IC	MAC1 receive data
62	M1_RXD0	I	3IC	MAC1 receive data
63	M1_CRS	I	3IC	MAC1 carrier sense
64	M1_COL	I	3IC	MAC1 collision detection
65	M1_MDC	O	3O4	MAC1 MII control clock
66	M1_MDIO	B	3IC/3T4	MAC1 MII control data
67	M2_TXEN	O	3O4	MAC2 transmit enable
68	DVDD33	P		Digital system power supply (+3.3 V)
69	DGND	P		Digital system ground
70	M2_TXCLK	I	3IC	MAC2 transmit clock
71	M2_TXD3	O	3O4	MAC2 transmit data
72	M2_TXD2	O	3O4	MAC2 transmit data
73	M2_TXD1	O	3O4	MAC2 transmit data
74	M2_TXD0	O	3O4	MAC2 transmit data
75	M2_RXCLK	I	3IC	MAC2 receive clock
76	M2_RXDV	I	3IC	MAC2 receive data valid
77	M2_RXER	I	3IC	MAC2 receive data error
78	M2_RXD3	I	3IC	MAC2 receive data
79	M2_RXD2	I	3IC	MAC2 receive data
80	M2_RXD1	I	3IC	MAC2 receive data
81	M2_RXD0	I	3IC	MAC2 receive data
82	M2_CRS	I	3IC	MAC2 carrier sense
83	M2_COL	I	3IC	MAC2 collision detection
84	M2_MDC	O	3O4	MAC2 MII control clock
85	M2_MDIO	B	3IC/3T4	MAC2 MII control data
86	DVDD18	P		Digital system power supply (+1.8 V)
87	DGND	P		Digital system ground
88	BIGEND	I	3ICD	Endian selection
89	DIVCK/PB11	B	3IC/3T4	Divided clock output or I/O port
90	PCMIN/PB10	B	3IC/3T4	PCM data input or I/O port
91	PCMCLK/PB9	B	3IC/3T4	PCM clock output or I/O port
92	PCMSYNC1/PB8	B	3IC/3T4	PCM synchronous signal 1 or I/O port
93	PCMSYNC2/PB7	B	3IC/3T4	PCM synchronous signal 2 or I/O port
94	PCMOUT/PB6	B	3IC/3T4	PCM data output or I/O port
95	XDACK/PB5	B	3IC/3T4	Debugging control signal or I/O port
96	DSOD/PB4	B	3IC/3T4	
97	DWR/PB3	B	3IC/3T4	
98	DCK/PB2	B	3IC/3T4	
99	DSL/PB1	B	3IC/3T4	
100	DSID/PB0	B	3IC/3T4	
101	DBG15/PA15	B	3IC/3T4	debugging data output or I/O port
102	DBG14/PA14	B	3IC/3T4	debugging data output or I/O port
103	DBG13/PA13	B	3IC/3T4	debugging data output or I/O port

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Pin No.	Pin name	I/O	Pin type	Function
104	DVDD33	P		Digital system power supply (+3.3 V)
105	DGND	P		Digital system ground
106	AVDD33	P		Analog system power supply (+3.3 V)
107	AGND	P		Analog system ground
108	HSIN	I	3A	Handset input
109	MICIN	I	3A	Microphone input
110	VREF	O	3A	Analog block reference voltage output
111	HSOUT	O	3A	Handset output
112	SPOUT	O	3A	Speaker output
113	AVDD33	P		Analog system power supply (+3.3 V)
114	AGND	P		Analog system ground
115	DBG12/PA12	B	3IC/3T4	debugging data output or I/O port
116	DBG11/PA11	B	3IC/3T4	
117	DBG10/PA10	B	3IC/3T4	
118	DBG9/PA9	B	3IC/3T4	
119	DBG8/PA8	B	3IC/3T4	
120	DVDD33	P		Digital system power supply (+3.3 V)
121	DGND	P		Digital system ground
122	DBG7/PA7	B	3IC/3T4	debugging data output or I/O port
123	DBG6/PA6	B	3IC/3T4	
124	DBG5/PA5	B	3IC/3T4	
125	DBG4/PA4	B	3IC/3T4	
126	DBG3/PA3	B	3IC/3T4	
127	DBG2/PA2	B	3IC/3T4	
128	DBG1/PA1	B	3IC/3T4	
129	DBG0/PA0	B	3IC/3T4	
130	SCK/PC15	B	3IC/3O4	SIO serial clock or I/O port
131	SDI/PD0	B	3IC/3T4	SIO serial data input or I/O port
132	SDO/PC14	B	3IC/3T4	SIO serial data output or I/O port
133	IRQ3/PD3	B	3IC/3T4	External interrupt 3 or I/O port
134	IRQ2/PD2	B	3IC/3T4	External interrupt 2 or I/O port
135	IRQ1/PD1	B	3IC/3T4	External interrupt 1 or I/O port
136	CTSn2/PC0	B	3IC/3T4	USART2 clear to send signal or I/O port
137	DSRn2/PC1	B	3IC/3T4	USART2 data set ready signal or I/O port
138	PVDD18	P		PLL power supply (+1.8 V)
139	PGND	P		PLL ground
140	VCNT2	O	2A	PLL2 VCO control
141	CS2n/PD5	B	3ICU/3T4	External memory chip select 2 or I/O port
142	CS3n/PD6	B	3ICU/3T4	External memory chip select 3 or I/O port
143	RTSn2/PC8	B	3IC/3T4	USART2 request to send signal or I/O port
144	DTRn2/PC9	B	3IC/3T4	USART2 data terminal ready signal or I/O port
145	EXCK2/PC2	B	3IC/3T4	USART2 external clock input or I/O port
146	TXD2/PC10	B	3IC/3T4	USART2 serial data output or I/O port
147	RXD2/PC3	B	3IC/3T4	USART2 serial data input or I/O port
148	TRSTIN	I	3ICD	JTAG reset
149	RTCK	O	3O4	JTAG synchronous clock output
150	TCK	I	3ICU	JTAG clock input
151	TMS	I	3ICU	JTAG mode selection
152	TDI	I	3ICU	JTAG data input
153	TDO	O	3O4	JTAG data output
154	D31	B	3IC/3T4	
155	D30	B	3IC/3T4	
156	DVDD18	P		Digital system power supply (+1.8 V)
157	DGND	P		Digital system ground

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Pin No.	Pin name	I/O	Pin type	Function
158	D29	B	3IC/3T4	Data bus
159	D28	B	3IC/3T4	
160	D27	B	3IC/3T4	
161	D26	B	3IC/3T4	
162	D25	B	3IC/3T4	
163	D24	B	3IC/3T4	
164	D23	B	3IC/3T4	
165	D22	B	3IC/3T4	
166	D21	B	3IC/3T4	
167	D20	B	3IC/3T4	
168	D19	B	3IC/3T4	
169	D18	B	3IC/3T4	
170	D17	B	3IC/3T4	
171	D16	B	3IC/3T4	
172	DVDD33	P		Digital system power supply (+3.3 V)
173	DGND	P		Digital system ground
174	D15	B	3IC/3T4	Data bus
175	D14	B	3IC/3T4	
176	D13	B	3IC/3T4	
177	D12	B	3IC/3T4	
178	D11	B	3IC/3T4	
179	D10	B	3IC/3T4	
180	D9	B	3IC/3T4	
181	D8	B	3IC/3T4	
182	D7	B	3IC/3T4	
183	D6	B	3IC/3T4	
184	D5	B	3IC/3T4	
185	D4	B	3IC/3T4	
186	D3	B	3IC/3T4	
187	D2	B	3IC/3T4	
188	D1	B	3IC/3T4	
189	D0	B	3IC/3T4	
190	DVDD18	P		Digital system power supply (+1.8 V)
191	DGND	P		Digital system ground
192	CTSn1/PC4	B	3IC/3T4	USART1 clear to send signal or I/O port
193	DSRn1/PC5	B	3IC/3T4	USART1 data set ready signal or I/O port
194	RTSn1/PC11	B	3IC/3T4	USART1 request to send signal or I/O port
195	DTRn1/PC12	B	3IC/3T4	USART1 data terminal ready signal or I/O port
196	EXCK1/PC6	B	3IC/3T4	USART1 external clock input or I/O port
197	TXD1/PC13	B	3IC/3T4	USART1 serial data output or I/O port
198	RXD1/PC7	B	3IC/3T4	USART1 serial data input or I/O port
199	A24	O	3O4	Address bus
200	A23	O	3O4	
201	A22	O	3O4	
202	A21	O	3O4	
203	A20	O	3O4	
204	A19	O	3O4	
205	A18	O	3O4	
206	A17	O	3O4	
207	A16	O	3O4	
208	DVDD33	P		Digital system power supply (+3.3 V)

Pin Functions

External Memory Interface (67 pins)			
	D[31:0]	I/O	Data bus for external memory and SDRAM
	A[24:0]	O	Address bus for external memory and SDRAM
	CS0n	O	External ROM or flash memory chip select
	CS1n/PD4	O	External memory chip select 1 This pin includes a pull-up resistance (typ: 100 kΩ).
	CS2n/PD5	O	External memory chip select 2 This pin includes a pull-up resistance (typ: 100 kΩ).
	CS3n/PD6	O	External memory chip select 3 This pin includes a pull-up resistance (typ: 100 kΩ).
	MWRLn	O	Low-byte write signal, little endian 8-bit upon selection of 32-bit bus write signal upon selection of bus, and write signal or lower-byte write signal upon selection of 16-bit bus
	MWRHn	O	Upper-byte write signal; Upper-byte write signal or upper-byte selection signal upon selection of 16-bit bus, and write signal upon selection of big-endian 8-bit bus
	MRDn	O	Read signal
	ROMBUSW	I	Bus-width selection in the CSOn area: L: 32-bit, H: 16-bit, This pin includes a pull-down resistance (typ: 100 kΩ).
	BIGEND	I	Endian selection - H: Big endian, L: Little endian This pin includes a pull-down resistance (typ: 100 kΩ).
	WAITn/PB12	I	External wait input (low active)
SDRAM Controller (10 pins)			
	DRCS0n	O	Chip select 0; chip select on the 32-bit width SDRAM side or 16-bit width SDRAM lower side
	DRCS1n	O	Chip select 1; chip select on the 16-bit width SDRAM upper side (D[31:16])
	RASn	O	Row address strobe
	CASn	O	Column address strobe
	DRCLK	O	Clocks; ARM block clock is generated
	DRWE	O	Write enable
	DQM[3:0]	O	Byte mask: corresponds to DQM3:D31-D24, DQM2:D23-D16, DQM1:D15-D8, and DQM0:D7-D0 L: enable, H: mask
External Interrupts (3 pins)			
	IRQ[3:1]/PD[3:1]	I	External interrupt signal input
MAC Interface (34 pins)			
	M1_TXEN	O	Transmit enable
	M1_TXCLK	I	Transmit clock
	M1_TXD[3:0]	O	Transmit data
	M1_RXCLK	I	Receive clock
	M1_RXDV	I	Receive data valid
	M1_RXER	I	Receive error
	M1_RXD[3:0]	I	Receive data
	M1_CRS	I	Carrier sense
	M1_COL	I	Collision detection
	M1_MDC	O	MII control clock
	M1_MDIO	I/O	MII control data
	M2_TXEN	O	Transmit enable
	M2_TXCLK	I	Transmit clock
	M2_TXD[3:0]	O	Transmit data
	M2_RXCLK	I	Receive clock
	M2_RXDV	I	Receive data valid
	M2_RXER	I	Receive error
	M2_RXD[3:0]	I	Receive data
	M2_CRS	I	Carrier sense
	M2_COL	I	Collision detection
	M2_MDC	O	MII control clock
	M2_MDIO	I/O	MII control data

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USART (14 pins)			
	RXD1/PC7	I	Serial data input
	TXD1/PC13	O	Serial data output
	EXCK1/PC6	I	External clock input
	DTRn1/PC12	O	Data terminal ready signal
	RTSn1/PC11	O	Request to send signal
	DSRn1/PC5	I	Data set ready signal
	CTSn1/PC4	I	Clear to send signal
	RXD2/PC3	I	Serial data input
	TXD2/PC10	O	Serial data output
	EXCK2/PC2	I	External clock input
	DTRn2/PC9	O	Data terminal ready signal
	RTSn2/PC8	O	Request to send signal
	DSRn2/PC1	I	Data set ready signal
	CTSn2/PC0	I	Clear to send signal
SIO (3 pins)			
	SCK/PC15	I/O	Serial clock
	SDI/PD0	I	Serial data input
	SDO/PC14	O	Serial data output
PCM interface (5 pins)			
	PCMIN/PB10	I	PCM data input
	PCMOUT/PB6	O	PCM data output
	PCMCLK/PB9	O	PCM clock output
	PCMSYNC1/PB8	O	PCM synchronous signal output 1
	PCMSYNC2/PB7	O	PCM synchronous signal output 2
I/O Port			
Shared function ports			
	PA[15:0]	I/O	
	PB[12:0]	I/O	
	PC[15:0]	I/O	
	PD[6:0]	I/O	
JTAG (6 pins)			
	TRSTN	I	Reset: This pin includes a pull-down resistance (typ: 100 kΩ).
	RTCK	O	Synchronous clock output
	TCK	I	Clock: This pin includes a pull-up resistance (typ: 100 kΩ).
	TMS	I	Mode selection: This pin includes a pull-up resistance (typ: 100 kΩ).
	TDI	I	Data input: This pin includes a pull-up resistance (typ: 100 kΩ).
	TDO	O	Data output
Analog Pins (5 pins)			
	HSIN	I	Handset input
	HSOUT	O	Handset output
	MICIN	I	Microphone input
	SPOUT	O	Speaker output
	VREF	O	Analog block reference voltage output

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Debugging signal (22 pins)			
	DBG[15:0]/PA[15:0]	O	Data output for DSP debugging
	XDACK/PB5	O	Debug mode acknowledge output
	DSOD/PB4	O	Debug serial data output
	DWR/PB3	I	Debug register write enable signal input
	DCK/PB2	I	Debug serial clock input
	DSL/PB1	I	Debug register select input
	DSID/PB0	I	Debug serial data input
Other Pins (11 pins)			
	DIVCK/PB11	O	Divided Clock Signal Output
	VCNT1	O	PLL1 VCO control
	VCNT2	O	PLL2 VCO control
	RESETn	I	Reset signal input
	RSTOUTn	O	Watchdog timer reset signal output (low active)
	XTAL1	I	Crystal oscillator connection (8.192 MHz)
	XTAL2	O	
	TEST[3:0]	I	Test pin: These pins include pull-down resistances (typ: 100 kΩ). Set TEST [2:0] to OPEN or “L” in the normal operation. TEST3 is used to set cache function setting. H: cache ON, L: cache OFF Set TEST3 to “H” when using cache memory.
Power Supply (28 pins)			
	DVDD33	Power supply	Digital system power supply (+3.3 V)
	DVDD18	Power supply	Digital system power supply (1.8 V)
	DGND	Power supply	Digital system ground
	AVDD33	Power supply	Analog system power supply (3.3 V)
	AGND	Power supply	Analog system ground
	PVDD18	Power supply	PLL power supply (1.8 V)
	PGND	Power supply	PLL ground

Clocks

The clock is supplied in three blocks: the DSP block, the ARM block, and the analog block. An 8.192 MHz external oscillator element is used.

The DSP block operating clock is variable that can be set within the range from 40 to 60 MHz with register settings. The DSP block clock frequency can be dropped to 1/2 to 1/16 of its usual frequency according to the system control block register settings. It is also possible to completely power down the system by stopping the clock.

The ARM block consists of the ARM7 itself, peripheral circuits, and the Ethernet MAC block. The ARM block operating clock is variable that can be set within the range from 24.6 to 59.4 MHz with register settings. The ARM block clock frequency can be dropped to 1/2 to 1/16 of its usual frequency according to system control block register settings in the power-saving mode. Stopping the clock can power down the peripheral block clock frequency and EthernetMAC blocks.

An analog block is used as A/D converter and D/A converter. The analog block operates at a 4.096 MHz clock. The register setting, which stops this clock to reduce power consumption, is provided.

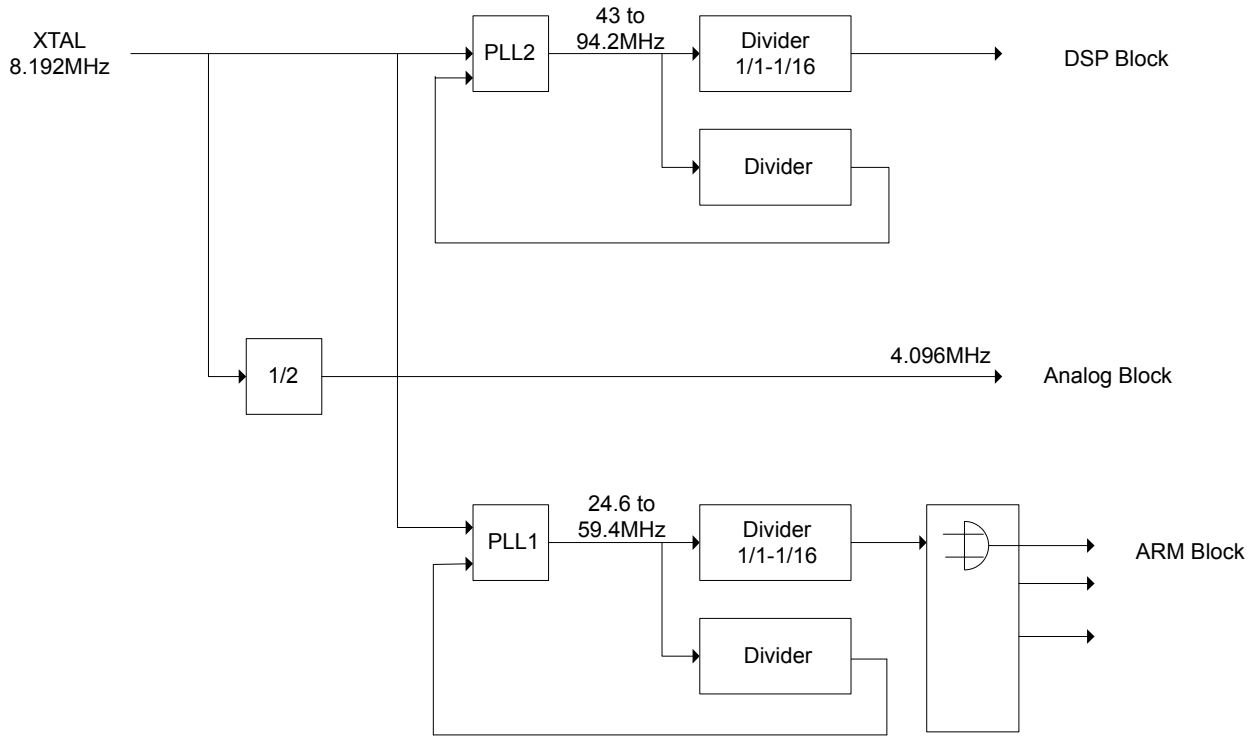


Figure 1 Clock System Diagram

ARM7

The ARM7TDMI is a high-speed low-power 32-bit RISC core. It features an internal 8-KB unified cache. It also includes the 4-KB working SRAM.

The bus consists of an AMBA bus, and the following items are allocated to the AHB bus: the ARM7 itself, which is a master bus, a DMA controller, a slave memory controller, the SDRAM controller, the protocol engine, and DSP interface memory. The following peripheral blocks are allocated to the APB bus: the interrupt controller, timers, the USART circuits, the SIO circuit, and the GPIO circuit.

The ARM7 CPU can access external flash memory or ROM with a 16-bit or 32-bit bus width, 32-bit width SDRAM, 8-bit or 16-bit width SRAM, flash memory, and I/O devices using the 25-bit address bus and 32-bit data bus of the external memory interface.

Table 8-1 shows a CPU memory map: After a reset, the user program is executed starting at 0x00000000 address located in external memory (CSO). The external memory (CSO) area can be swapped with the internal SRAM area by setting the remap register to 1.

Table 1 Memory Map

At Reset			After Remapping		
Address	Contents	Size	Address	Contents	Size
00000000-01FFFFFF	External memory (CSO)	32 MB	00000000-00000FFF	Internal SRAM	4 KB
			00001000-01FFFFFF	(Reserved)	
02000000-03FFFFFF	(Reserved)		←		
04000000-04000FFF	Memory controller		←		
04001000-04001FFF	Interrupt controller		←		
04002000-04002FFF	REMAP		←		
04003000-04003FFF	(Reserved)		←		
04004000-04004FFF	DMA controller		←		
04005000-0401FFFF	(Reserved)		←		
04020000-04021FFF	Protocol engine/MAC		←		
04022000-04023FFF	DSP I/F		←		
04024000-0402FFFF	(Reserved)		←		
04030000-0403FFFF	DSP debug I/F		←		
04040000-05FFFFFF	(Reserved)		←		
06000000-06000FFF	GPIO		←		
06001000-06001FFF	Plain timer		←		
06002000-06003FFF	(Reserved)		←		
06004000-06004FFF	USART1		←		
06006000-0601FFFF	(Reserved)		←		
06020000-06020FFF	System control		←		
06021000-06021FFF	Multi-function timers		←		
06022000-06022FFF	SDRAM controller		←		
06023000-06023FFF	SIO		←		
06024000-06024FFF	USART2		←		
06025000-07FFFFFF	(Reserved)		←		
08000000-09FFFFFF	External memory (CS0)	32 MB	←		
0A000000-0BFFFFFF	External memory (CS1)	32 MB	←		
0C000000-0DFFFFFF	External memory (CS2)	32 MB	←		
0E000000-0FFFFFFF	External memory (CS3)	32 MB	←		
10000000-13FFFFFF	SDRAM	64 MB	←		
14000000-FFFFFFFF	(Reserved)		←		

DSP

The DSP used in this IC is the Sanyo-designed FAVOR40 DSP. This DSP includes a built-in 44K-word program RAM and a 32K-word data RAM. Use the DSP API function to down load the DSP program in the RAM program area upon power-ON by an ARM from the external flash memory to the program RAM. The CPU and the DSP interface using a 2K × 16-bit dual-port RAM.

All the DSP functions are provided as a CPU API program library. The following functions are provided by this API:

- Register driver for the DSP control
- DSP program execution
- System control
- Path and volume control
- Voice CODEC
- Hands-free function
- User buffer access
- Melody submission
- Tone/DTMF/RBT transmission settings
- Tone/DTMF detection
- FSK transmission and detection
- PCM Interface control

System Control Block

The system control block controls the system clock and the power saving mode of the various blocks.

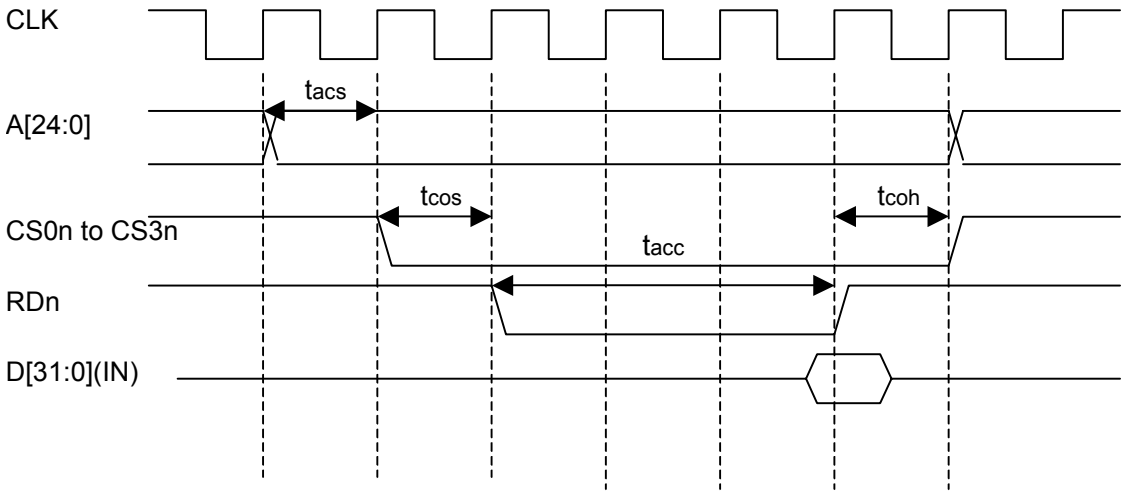
- DSP clock frequency settings
- Power saving mode control (DSP and CPU clock divisor settings)
- Peripheral block power saving mode control
- DSP power saving mode settings and power saving mode recovery control

Memory Controller

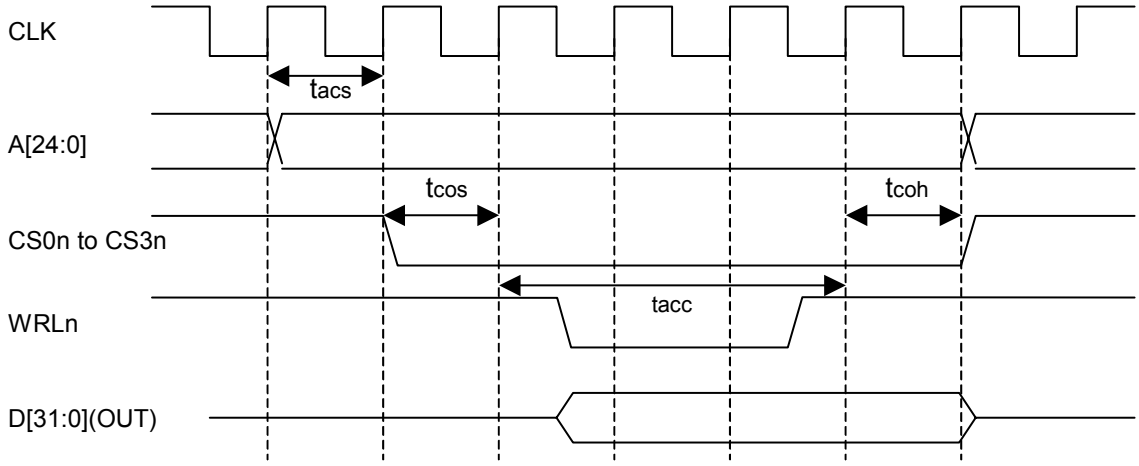
The memory controller controls the External memory access.

- External address space can be divided into areas 0 to 3 and each area can be independently set.
  - — Generates chip selects (CS0n to CS3n) to areas 0 to 3
  - — Selection between 8-bit and 16-bit access (areas 1 to 3)
  - — Selection between 16-bit or 32-bit access (area 0)
- Cycle count settings (0 to 7 cycles) for address setup (Tacs) relative to chip select, chip select setup (Tcos) relative to output enable (write enable), and chip select hold (Tcoh) relative to output enable (write enable).
- Output enable (write enable) wait state settings
  - — Programmable wait states (0 to 15 wait states, 1 to 16 cycles, can be set)
- Support for both little endian and big endian
- Access by minimum 1 wait (2-cycle) upon write

Read Timing



Write Timing

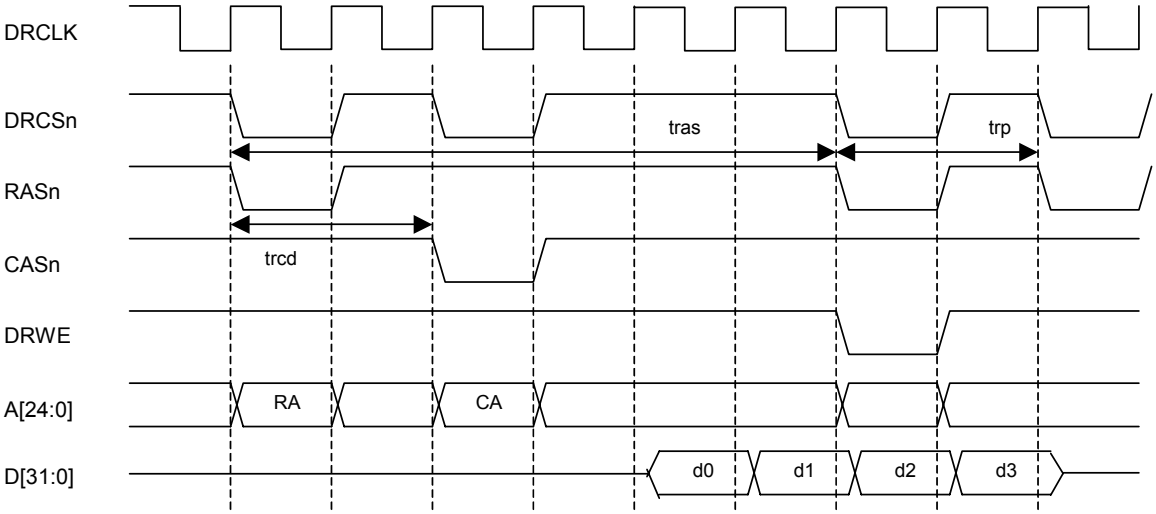


SDRAM Controller

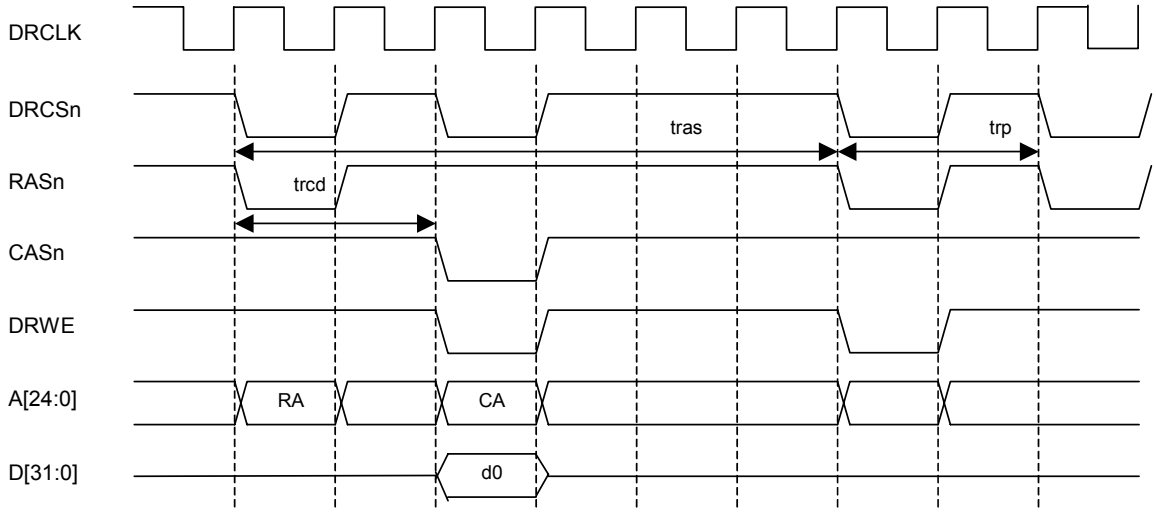
This SDRAM controller controls access to an SDRAM space of a maximum of 64 Mbyte.

- 32-bit access by a single connection to the 32-bit width SDRAM or two 16-bit width SDRAM connections
- supports 64-/128-/256-Mbit SDRAM
- Four-word burst read, single write
- Auto refresh
- CAS latency 2 or 3
- The following times can be set: RAS to CAS delay (trcd), RAS to precharge delay (tras), and precharge to RAS delay (trp)

Read Cycle



Write Cycle



Ethernet MAC

Two 10/100-Mbps EthernetMAC channels are included. The IC connects to an external PHY using an MII interface. MAC1 is for use in a WAN, and MAC2 for use in a LAN. Flow control between the two MACs is controlled by the protocol engine.

- Data rate: 10 or 100 Mbps
- MII interface with an external PHY
- Frame generation, CRC generation and checking
- Address filtering
  - Unicast and multicast support:
- Full-duplex and half-duplex operation
- Flow control (in full-duplex mode)
  - Pause frame generation
- CSMA/CD protocol (in half-duplex mode)
  - Collision detection and automatic resend
- VLAN support

Protocol Engine

The protocol engine implements a part of the network protocol stack processing (TCP/IP, UDP/IP) in hardware. The high-speed communication can be realized without increasing system clock frequency because mounting the protocol engine remarkably decreases the load of the host processor.

The protocol engine locates in between of the host processor (ARM) and the network interface (EthernetMAC) to perform the simultaneous send and receive data buffering as well as to check and process data conforming to the protocol. Besides, the protocol engine incorporate with two ports; a WAN port, which mainly connects to the external network (such as internet) and a LAN port, which connects to PC and others, to perform the simple router process, which automatically transfers frames between ports.

- Basic functions:
  - Packet-receive function
  - Packet-send function
  - Interrupt function
  - Buffer control function
- Expanded Reception functions:
  - Filtering function
  - Checksum verify function
  - Header data separation function

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- Expanded Transmission functions:
  - Automatic header generation function
  - Checksum calculation function
  - Host table function
- ARP functions:
  - Address automatic resolution
  - Post-ARP automatic transmission function
  - Automatic response function
- Bypass between WAN and LAN functions:
  - Transfer from WAN to LAN function
  - Transfer from LAN to WAN function
  - TOS value conversion function
- VLAN functions:
  - Filtering function
  - VLAN-tag auto-delete function
  - VLAN-tag auto-generation function

Interrupt Controller

This interrupt controller circuit supports 24 internal interrupts and 3 external interrupts.

- Two interrupt vectors (FIQ/IRQ)
- The interrupt is recognized using the status register. Software controls the priorities.
- Either rising edge detection, falling edge detection, or level detection can be selected for the external interrupts.
- Interrupts can be enabled/disabled on a per-interrupt basis.
- The FIQ or IRQ vector can be selected for each interrupt.
- Noise filters are available to remove noise from interrupts 1 and 2.

Table 15-1 Interrupt Allocation

No.	Interrupt factor	Internal/external
1	External interrupt 1	External
2	External interrupt 2	External
3	External interrupt 3	External
4	DSP1	Internal
5	DSP2	Internal
6	DSP3	Internal
7	DSP4	Internal
8	DSP5	Internal
9	DSP6	Internal
10	DSP7	Internal
11	DSP8	Internal
12	Watchdog timer	Internal
13	Basic timer	Internal
14	DMA controller CH1	Internal
15	DMA controller CH2	Internal
16	SIO	Internal
17	USART1	Internal
18	USART2	Internal
19	GPIO	Internal
20	Protocol engine	Internal
21	Multi-function timer CH1 compare/match A	Internal
22	Multi-function timer CH1 compare/match B	Internal
23	Multi-function timer CH1 overflow	Internal
24	Multi-function timer CH2 compare/match A	Internal
25	Multi-function timer CH2 compare/match B	Internal
26	Multi-function timer CH2 overflow	Internal
27	Protocol engine (LAN)	Internal

DMA Controller

The LC82162 provides a 2-channel DMA controller.
Channel 1 is allocated to the protocol engine transmission port, and channel 2 is allocated to the protocol engine reception port.

- Memory to memory transfers
- The transfer start operation can be performed either in software or by a DREQ start.
- Transfer units: byte, half word, and word
- Provides single and block transfer modes

Multifunction Timer

The multifunction timer (MTM) consists of two 16-bit channels (systems).

- Each channel has two data registers, and the operating mode and prescaler settings can be set individually for each channel.
- Each channel supports the following operating modes:
  - — Waveform output based on a compare/match operation:
    Either a 0-output, a 1-output, or a toggle output can be selected.
  - — Counter clear function:
    The counter can be cleared by compare match operations.
  - — Synchronous operation:
    Simultaneous write to multiple timer/counters (TCNT).
    Simultaneous clear by compare match operations.
    Simultaneous input or output from various registers based on synchronous counter operations.
  - — Buffer operation:
    Automatic rewrite of the output compare registers is supported.
  - — Buffer operation:
    A value from a data register can be transferred to a compare buffer on the occurrence of a compare match, a counter clear, or an overflow.
  - — Interrupt factor:
    Each channel is provided with two shared-function match interrupts and one overflow interrupt. Requests for these interrupts can be generated independently.

Watchdog Timer

The LC82162 provides two independent built-in timers: watchdog timer and the basic timer, for system monitoring.
The basic timer counts a certain period of time and generates the basic timer interrupt based on that count.
In contrast, the watchdog timer counts a certain period of time and generates either the watchdog timer interrupt or a system reset based on that count.

- Watchdog timer (can also be used to generate the watchdog timer interrupt):
  - — Counter operating clock selection function
  - — Operation mode switch function (watchdog timer interrupt/reset switch)
  - — Generating reset/interrupt upon overflow
  - — Watchdog timer reset signal external output enable/disable function
  - — Watchdog timer start/stop function
- Basic timer:
  - — Counter operating clock selection function
  - — Generating interrupt signal upon overflow
  - — Basic timer start/stop function

USART

The LC82162 provides two built-in USART (Universal synchronous/asynchronous receiver transmitter) circuits for serial data communication.

- Synchronous/asynchronous functions
  - — Synchronous mode • 5- to 8-bit character length
    Internal/external synchronization
    1- or 2-character synchronization (internal synchronization)
    Synchronous character automatic insertion
  - — Asynchronous mode • 5- to 8-bit character length
    Clock rate: × 1, × 16, and × 64
    Stop bit (1, 1.5, and 2)
    Break character transmission
    False start bit detection
    Automatic break state detection
- Full-duplex, double FIFO system (reception: 16 bytes, transmission: 4 bytes)
- Detection of parity, overrun, and framing errors
- Built-in baud rate generators (Independent send/receive system circuits. Available in switching to an external clock)
- Baud rate: 7.7 K to 3.2 M baud (when a 51.2 MHz clock is used)

SIO

The LC82162 provides a single-channel clock synchronous 3-wire full-duplex serial interface.

- Single-channel synchronous serial interface
- Transfer clock selection function:
  - — Internal clock (with variable clock cycles)
  - — External clock
- Transfer clock polarity switching function:
  The polarity of the serial interface transfer clock can be switched. The level (high or low) of the SCK pin when no communication operation is being performed can be set.
- Data length change function:
  - — 8-bit transfer
  - — 16-bit transfer
- Transfer bit length control function:
  - — 1-frame (8-bit/16-bit) transfer
  - — Continuous transfer
- LSB first/MSB first switching function
- Error detection function
  - — Over-run error:
  - — Reception register overwrite error

Divided Clock Signal Output

A divided clock signal output with a frequency in the range between 12.2 Hz and 800 kHz can be generated from the DIVCK pin.

PCM I/F

A PCM I/F is a 2-channel PCM data interface.

- Data format: μ-Law/A-Law, 16-bit linear
- MSB first/LSB first change function
- Transfer clock frequency: 256 kHz, 512 kHz, 1.024 MHz, and 2.048 MHz
- Long-frame synchronous mode/short-frame synchronous mode
- Data padding-from-the-end/padding-from-the-start change function (in μ-Law or A-Law mode)
- dECO connection mode

GPIO

GPIO refers to the general-purpose I/O ports. The I/O specification is available in units of bit.
A part of the ports can be used by switching to the dedicated signal port.
The PB[7:0] pins can be used as key input pins.

Table 23-1 Port Multifunction Table

PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8
DBG15	DBG14	DBG13	DBG12	DBG11	DBG10	DBG9	DBG9
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
DBG7	DBG6	DBG5	DBG4	DBG3	DBG2	DBG1	DBG0
			PB12	PB11	PB10	PB9	PB8
			nWAIT	DIVCK	PCMIN	PCMCLK	PCMSYNC1
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
PCMSYNC2	PCMOUT	XDACK	DSOD	DWR	DCK	DSL	DSID
PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
SCK	SDO	TXD1	DTRn1	RTSn1	TXD2	DTRn2	RTSn2
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RXD1	EXCK1	DSRn1	CTSn1	RXD2	EXCK2	DSRn2	CTSn2
	PD6	PD5	PD4	PD3	PD2	PD1	PD0
	CS3n	CS2n	CS1n	IRQ3	IRQ2	IRQ1	SDI

*: Pins DBG[15:0], DSID, DSL, DCK, DWR, DSOD, and XDACK are used for debug pins. They are not usually used.