Order Number(s):

LAN9218i-MT for 100-pin, TQFP Lead-free RoHS Compliant package with E3 Finish (Matte Tin) (-40 to +85°C Temp Range)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

General Description

The LAN9218i is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9218i has been specifically architected to provide the highest performance possible for any given architecture. The LAN9218i is fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant, and supports HP Auto-MDIX.

The LAN9218i includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 16-bit and 32-bit microprocessors and microcontrollers . The LAN9218i includes large transmit and receive data FIFOs with a high-speed host bus interface to accommodate high bandwidth, high latency applications. In addition, the LAN9218i memory buffer architecture allows highly efficient use of memory resources by optimizing packet granularity.

Applications

The LAN9218i is well suited for many high performance embedded applications, including:

- High-end cable, satellite and IP set-top boxes
- Video distribution systems
- Multi-room PVR (Personal Video Recorder)
- Digital video recorders
- High-definition televisions
- Digital media clients/servers
- Home gateways

The LAN9218i also supports features which reduce or eliminate packet loss. Its internal 16-KByte SRAM can hold over 200 received packets. If the receive FIFO gets too full, the LAN9218i can automatically generate flow control packets to the remote node, or assert back-pressure on the remote node by generating network collisions.

The LAN9218i supports numerous power management and wakeup features. The LAN9218i can be placed in a reduced power mode and can be programmed to issue an external wake signal via several methods, including “Magic Packet”, “Wake on LAN” and “Link Status Change”. This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command.

Block Diagram

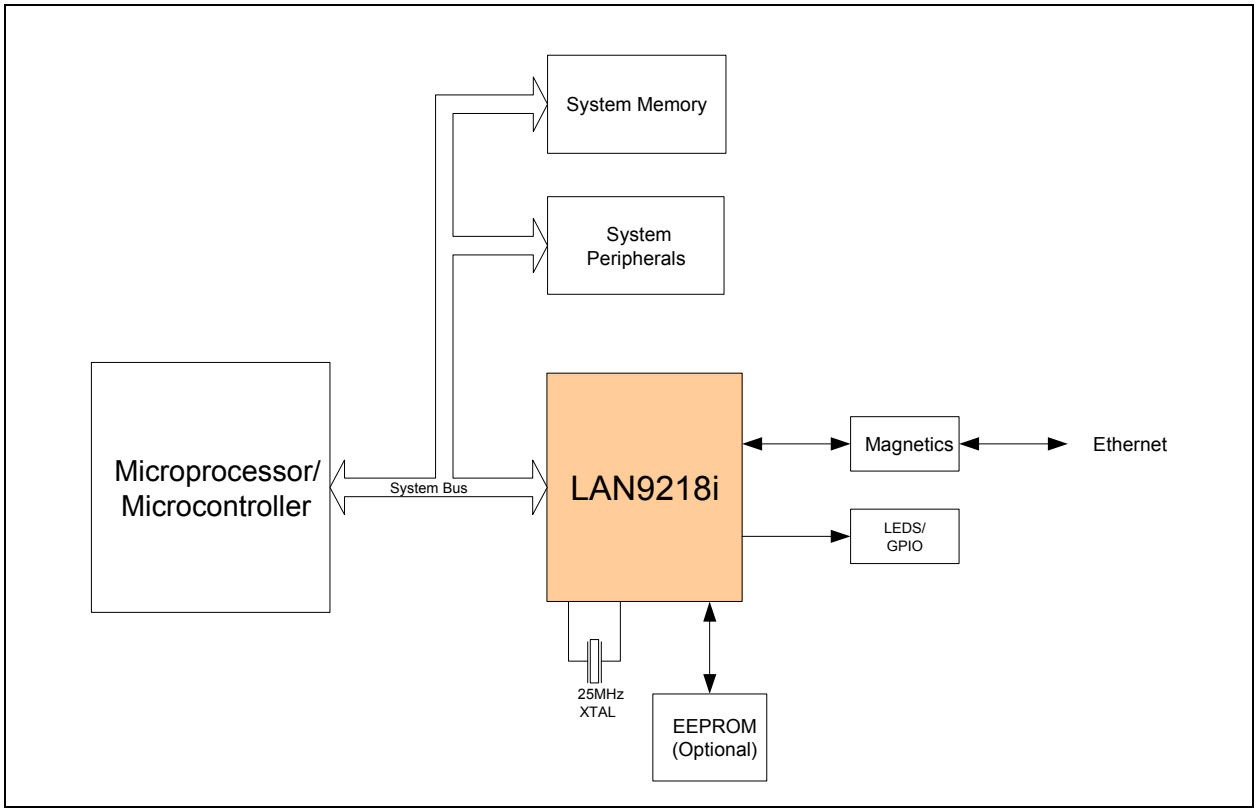

Figure 1 System Block Diagram

PRODUCT PREVIEW

Package Outline

100-TQFP Package

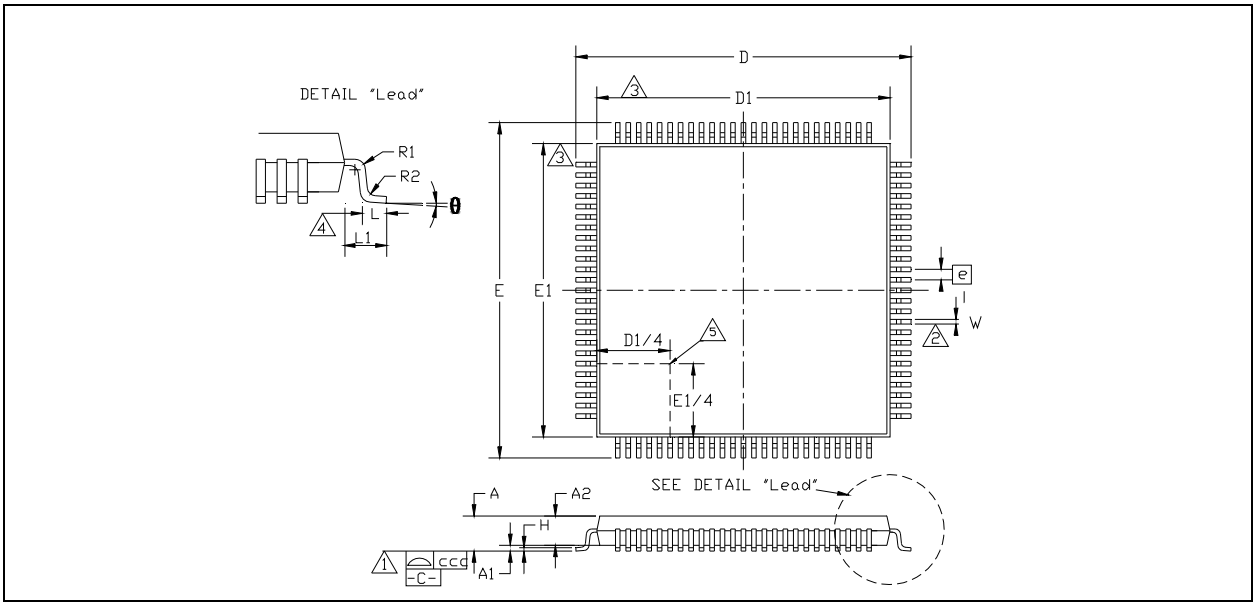

Figure 2 100-Pin TQFP Package Definition

Table 1 100-Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	15.80	~	16.20	X Span
D1	13.90	~	14.10	X body Size
E	15.80	~	16.20	Y Span
E1	13.90	~	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0^o	~	7^o	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.