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Figure 1. Block diagram of L4995

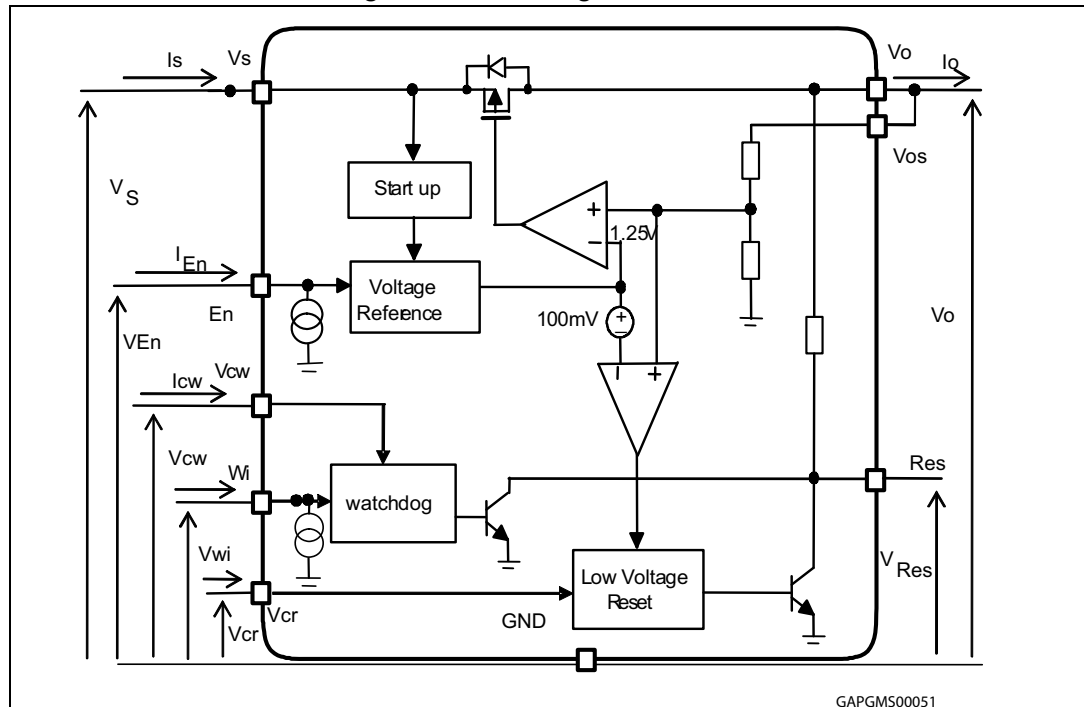


Figure 2. Block diagram of L4995A

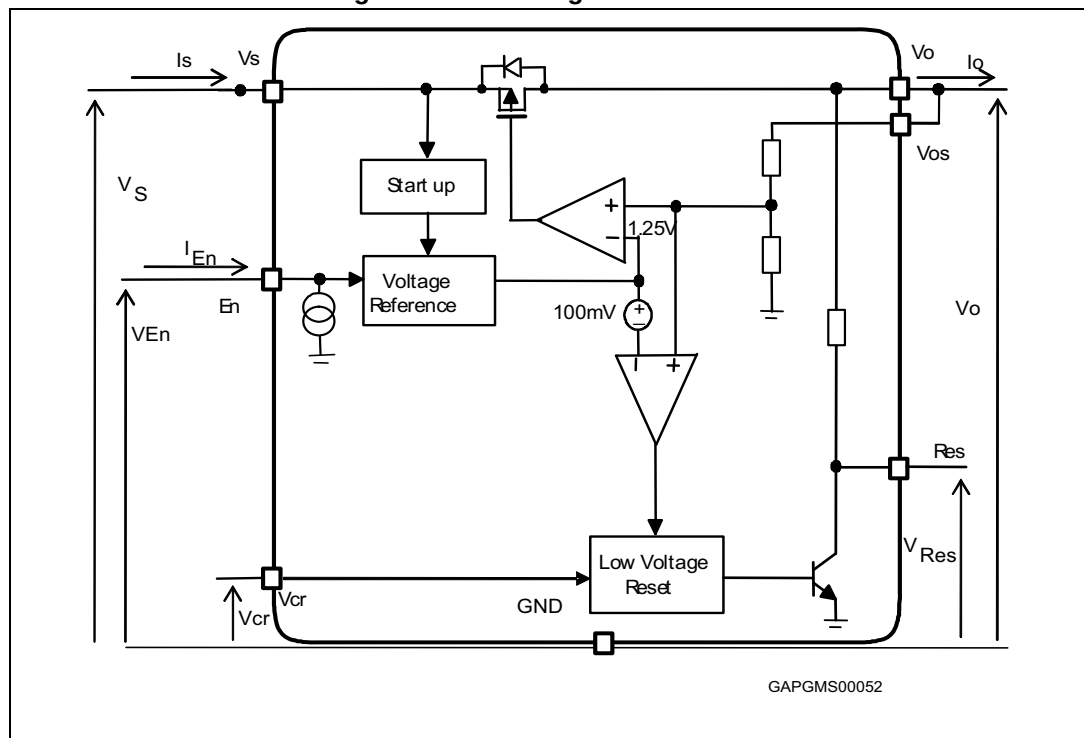


Figure 3. Block diagram of L4995R

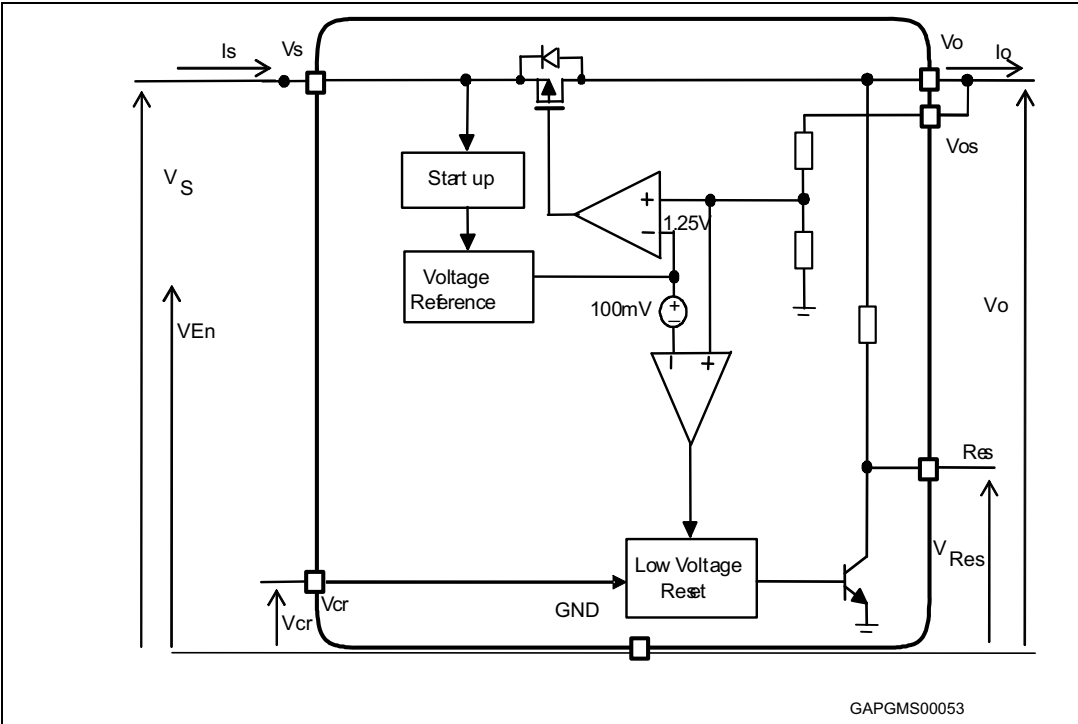


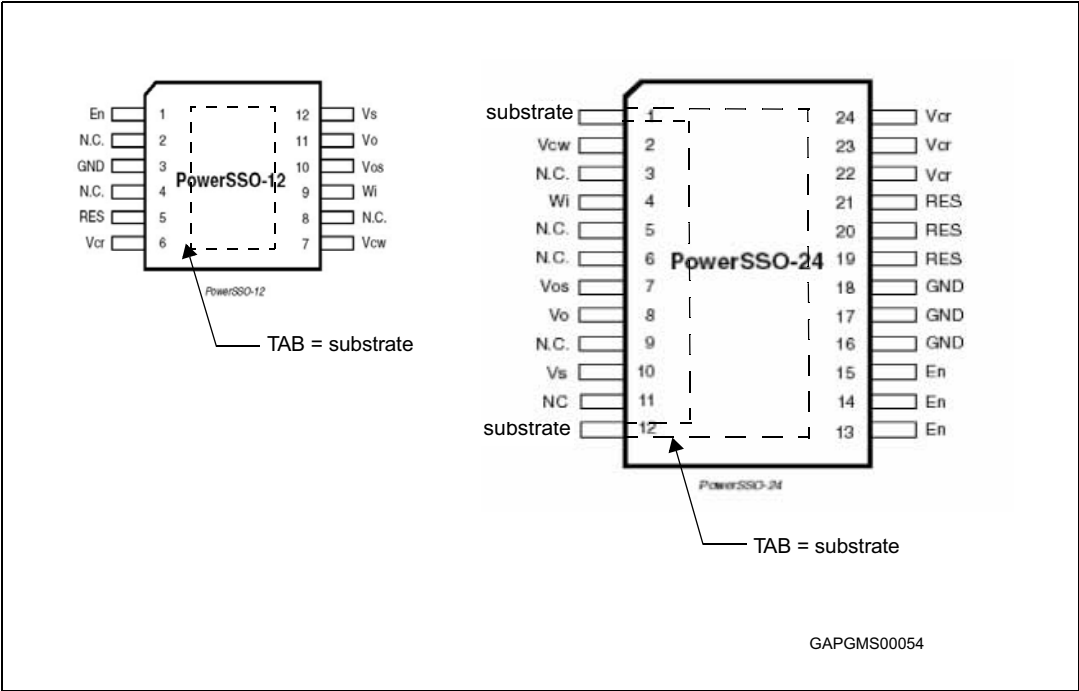
Table 2. Pins descriptions

Pin name	PowerSSO-12 pin #	PowerSSO-24 pin #	Function
E_n	1	13, 14, 15	Enable input (L4995 and L4996A only, otherwise not connected). If high regulator, watchdog and reset are operating. If low regulator, watchdog and reset are shutdown. Connect to V_s if not used.
NC	2, 4, 8	3, 5, 6, 9, 11	Not connected.
GND	3	16, 17, 18	Ground reference.
-	TAB	TAB, 1, 12	Substrate of the chip: connect the pins or the TAB to GND.
R_{es}	5	19, 20, 21	Reset output. It is pulled down when output voltage goes below V_{o_th} or frequency at W_i is too low. Leave floating if not used.
V_{cr}	6	22, 23, 24	Reset timing adjust. A capacitor between V_{cr} pin and GND. Sets the reset delay time (trd). Leave floating if Reset is not used.
V_{cw}	7	2	Watchdog timer adjust (L4995 only, otherwise not connected). A capacitor between V_{cw} pin and GND. Sets the time response of the watchdog monitor.

Table 2. Pins descriptions (continued)

Pin name	PowerSSO-12 pin #	PowerSSO-24 pin #	Function
W_i	9	4	Watchdog input (L4995 only, otherwise not connected). If the frequency at this input pin is too low, the Reset output is activated.
V_{os}	10	7	Regulator voltage output sensing.
V_o	11	8	5 voltage regulator output. Block to ground with a capacitor >100nF (needed for regulator stability).
V_S	12	10	Supply voltage. Block to ground directly at V_S pin with a ceramic capacitor (e.g. 200nF).

Figure 4. Pins configurations (L4995)



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{VSDC}	DC supply voltage	- 0.3 to 40	V
I_{VSDC}	Input current	Internally limited	
$V_{VO}^{(1)}$	DC output voltage	- 0.3 to 6	V
I_{VO}	DC output current	Internally limited	
V_{WI}	Watchdog input voltage	-0.3 to $V_{VO} + 0.3$	V
V_{OD}	R_{ES} output voltage	-0.3 to $V_{VO} + 0.3$	V
I_{OD}	R_{ES} output current	Internally limited	
V_{CR}	V_{CR} voltage	- 0.3 to $V_{VO} + 0.3$	V
V_{CW}	Watchdog delay voltage	- 0.3 to $V_{VO} + 0.3$	V
V_{EN}	Enable input	- 0.3 to $V_{VSDC} + 0.3$	V
T_J	Junction temperature	- 40 to 150	°C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	± 2	kV
V_{ESD}	ESD voltage level (CDM AEC-Q100-011)	750	V

1. Using the typical application schematic with $C_{out} = 10 \mu F$ and $I_{out} = 0 A$, when the regulator is switched-on, an overshoot exceeding 6 V could occur. This behavior does not impact the reliability of the regulator.

2.2 Thermal data

For details, please refer to [Section 4.1: PowerSSO-12 thermal data](#) and [Section 4.2: PowerSSO-24 thermal data](#).

Table 4. Thermal data⁽¹⁾

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance Junction to Case: PowerSSO-12	5	°K/W
	PowerSSO-24	4	°K/W
R _{thj-amb}	Thermal resistance Junction to Ambient: PowerSSO-12	52	°K/W
	PowerSSO-24	38	°K/W

1. The values quoted are for PCB 77mm x 86mm x 1.6mm, FR4, double layer; Copper thickness 0.070mm
Copper area 3cm² Thermal Vias, Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm.

2.3 Electrical characteristics

Values specified in this section are for V_S = 5.6V to 31V, T_J = -40 °C to +150 °C unless otherwise stated.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V _O	V _{O_ref}	Output voltage	V _S = 5.6 to 31V I _O = 0 to 500mA	4.9	5.00	5.1	V
V _O	I _{short}	Short circuit current	V _S = 13.5V ⁽¹⁾	550	800	1050	mA
V _O	I _{lim} ⁽²⁾	Output current limitation	V _S = 13.5V ⁽¹⁾	600	900	1250	mA
V _S , V _O	V _{line}	Line regulation voltage	V _S = 5.6 to 31V I _O = 0 to 500mA			25	mV
V _O	V _{load}	Load regulation voltage	I _O = 0 to 500mA			25	mV
V _S , V _O	V _{dp} ⁽³⁾	Drop voltage	I _O = 400mA		270	500	mV
V _S , V _O	SVR	Ripple rejection	f _r = 100 Hz ⁽⁴⁾	55			dB
V _S , V _O	I _{qs}	Current consumption with regulator disabled	V _S = 13.5V, E _n = low		3	10	μA
V _S , V _O	I _{qn_1}	Current consumption with regulator enabled	V _S = 13.5V, I _O < 1mA,		90	160	μA
V _S , V _O	I _{qn_50}	Current consumption with regulator enabled	V _S = 13.5V, I _O = 50mA,		290	400	μA

Table 5. General (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S, V_O	I_{qn_150}	Current consumption with regulator enabled	$V_S = 13.5V$, $I_O = 150mA$,		740	1000	μA
V_S, V_O	I_{qn_250}	Current consumption with regulator enabled	$V_S = 13.5V$, $I_O = 250mA$,		1	1.4	mA
V_S, V_O	I_{qn_500}	Current consumption with regulator enabled	$V_S = 13.5V$, $I_O = 500mA$,		2.1	2.7	mA
	T_w	Thermal protection temperature		150		190	$^{\circ}C$
	T_{w_hy}	Thermal protection temperature hysteresis			10		$^{\circ}C$

1. See [Figure 28](#).
2. Measured output current when the output voltage has dropped 100mV from its nominal value obtained at $V_S=13.5V$ and $I_O=250mA$.
3. V_S-V_O measured when the output voltage has dropped 100mV from its nominal value obtained at $V_S=13.5V$ and $I_O=250mA$.
4. Guaranteed by design.

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{es}	V_{res_l}	Reset output low voltage	$R_{ext} = 5k\Omega$ to V_O , $V_O > 1V$			0.4	V
R_{es}	I_{Res_lkg}	Reset output high leakage current	$V_{Res} = 5V$			1	μA
R_{es}	R_{Res}	Pull up internal resistance (versus V_O)		10	20	40	$k\Omega$
R_{es}	V_{O_th}	V_O out of regulation threshold	$V_S = 5.6$ to $31V$ $I_O = 1$ to $500mA$	6%	8%	10%	below V_{O_ref}
V_{cr}	V_{Rlth}	Reset delay circuit low threshold	$V_S = 13.5V$	10%	13%	16%	V_{O_ref}
V_{cr}	V_{Rhth}	Reset delay circuit high threshold	$V_S = 13.5V$	44%	47%	50%	V_{O_ref}
V_{cr}	I_{cr}	Charge current	$V_S = 13.5V$	8	15	30	μA
V_{cr}	I_{dr}	Discharge current	$V_S = 13.5V$	8	15	30	μA
R_{es}	T_{rr}	Reset reaction time ⁽¹⁾	$V_O = V_{O_th} - 100mV$	100	250	700	μs
R_{es}	T_{rd}	Reset delay time	$V_S = 13.5V$, $C_{tr} = 47nF$	12	33	73	ms

1. When V_O becomes lower than 4V, the reset reaction time decreases down to $2\mu s$ assuring a faster reset condition in this particular case.

Table 7. Watchdog

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
W _i	V _{ih}	Input high voltage	V _S = 13.5V	3.5			V
W _i	V _{il}	Input low voltage	V _S = 13.5V			1.5	V
W _i	V _{ih}	Input hysteresis	V _S = 13.5V		500		mV
W _i	I _{wi}	Pull down current	V _S = 13.5V V _{wi} = 3.5V		6	10	μA
V _{cw}	V _{wlth}	Low threshold	V _S = 13.5V	10%	13%	16%	V _{o_ref}
V _{cw}	V _{whth}	High threshold	V _S = 13.5V	44%	47%	50%	V _{o_ref}
V _{cw}	I _{cwc}	Charge current	V _S = 13.5V, V _{cw} = 0.1V	5	10	20	μA
V _{cw}	I _{cwd}	Discharge current	V _S = 13.5V, V _{cw} = 2.5V	1.25	2.5	5	μA
V _{cw}	T _{wop}	Watchdog period	V _S = 13.5V, C _{tw} = 47nF	20	40	80	ms
R _{es}	t _{wol}	Watchdog output low time	V _S = 13.5V, C _{tw} = 47nF	4	8	16	ms

Table 8. Enable

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E _n	V _{En_low}	E _n input low voltage				1	V
E _n	V _{En_high}	E _n input high voltage		3			V
E _n	V _{En_hyst}	E _n input hysteresis			830		mV
E _n	I _{En}	Pull down current	V _S = 13.5V		10	18	μA

2.4 Electrical characteristics curves

Figure 5. Output voltage vs T_j

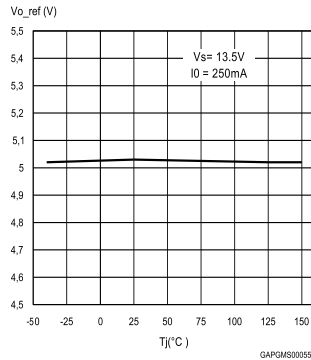


Figure 6. Output voltage vs V_s

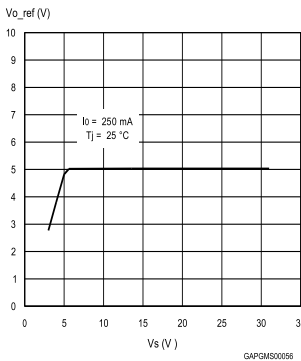


Figure 7. Drop voltage vs output current

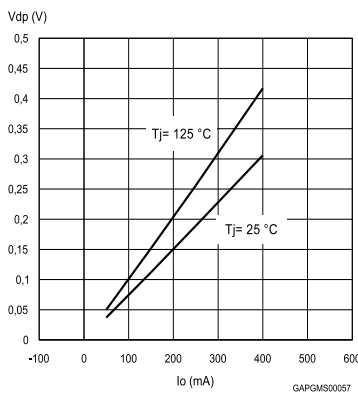


Figure 8. Current consumption vs output current

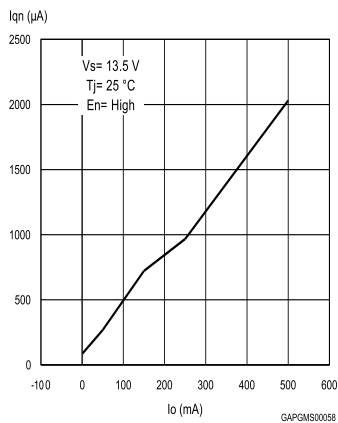


Figure 9. Current consumption vs input voltage

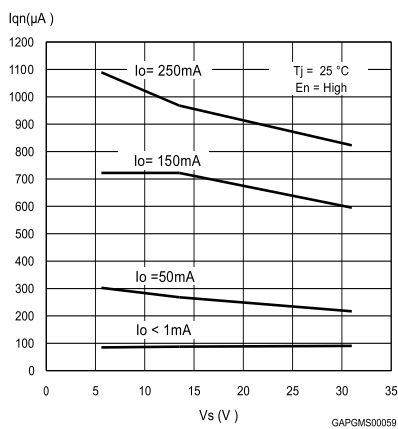


Figure 10. Current limitation vs T_j

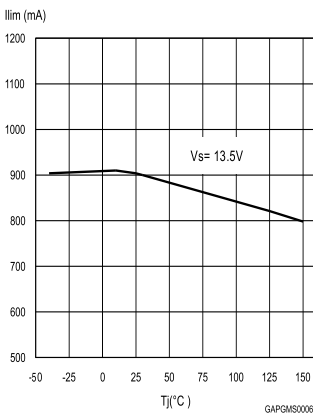


Figure 11. Current limitation vs input voltage

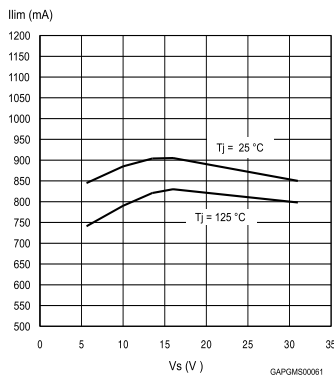


Figure 12. Short circuit current vs input voltage

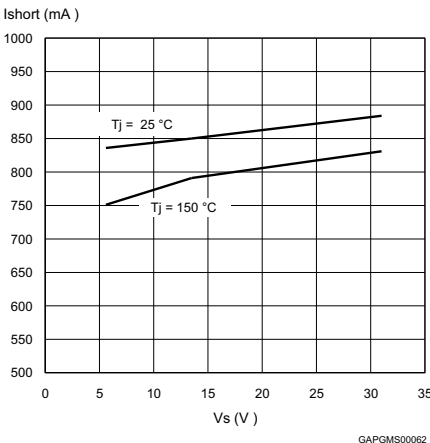


Figure 13. Output voltage vs enable voltage

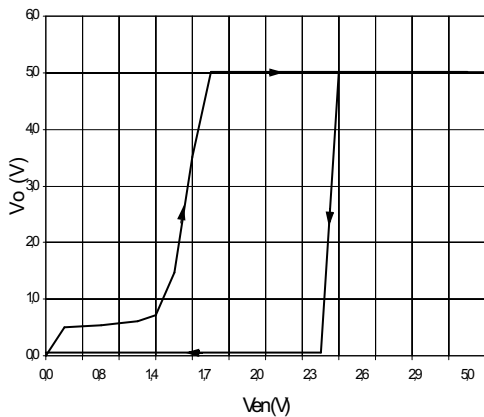


Figure 14. V_{En_high} vs T_j

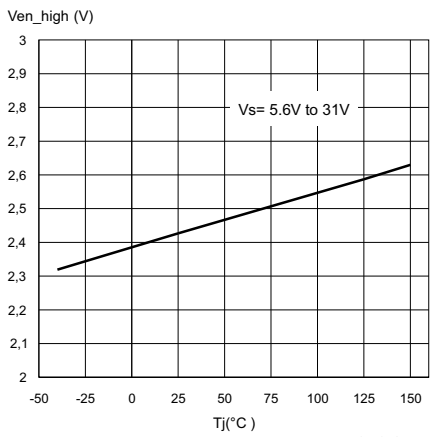


Figure 15. V_{EN_LOW} vs T_j

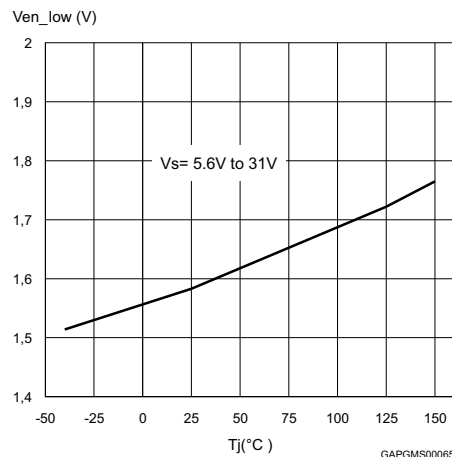


Figure 16. V_{Rhth} vs T_j

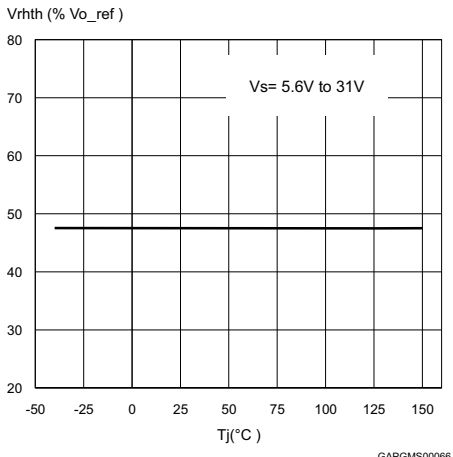


Figure 17. V_{Rlth} vs T_j

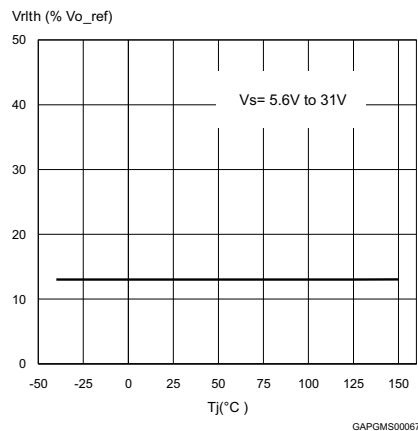


Figure 18. V_{whth} vs T_j

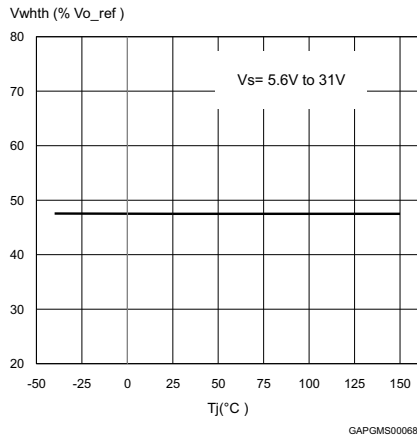


Figure 19. V_{wlth} vs T_j

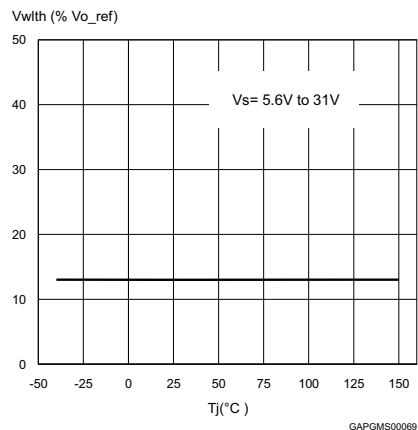


Figure 20. I_{cr} and I_{cwc} vs T_j

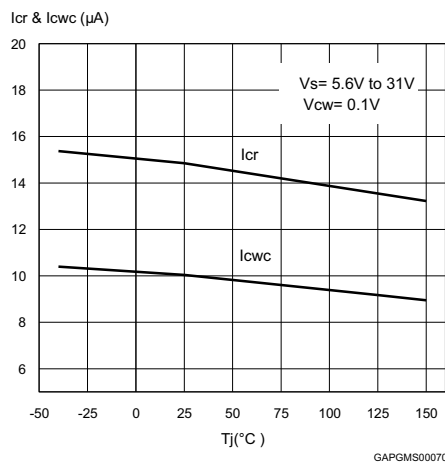


Figure 21. I_{dr} and I_{cwd} vs T_j

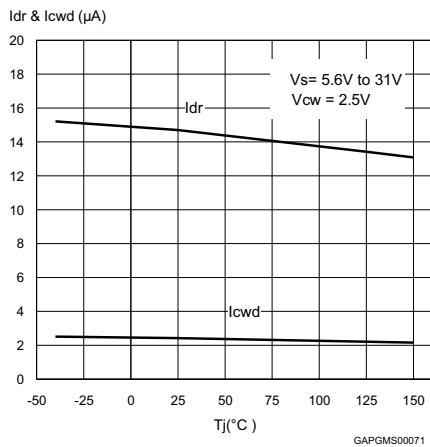
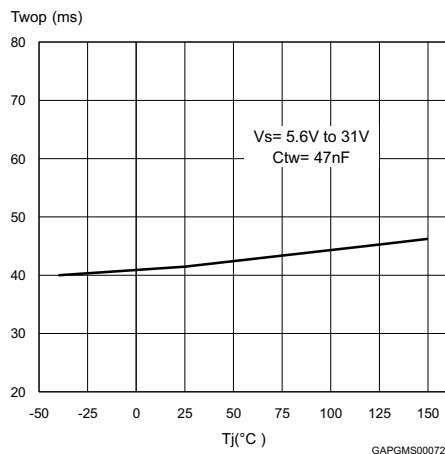
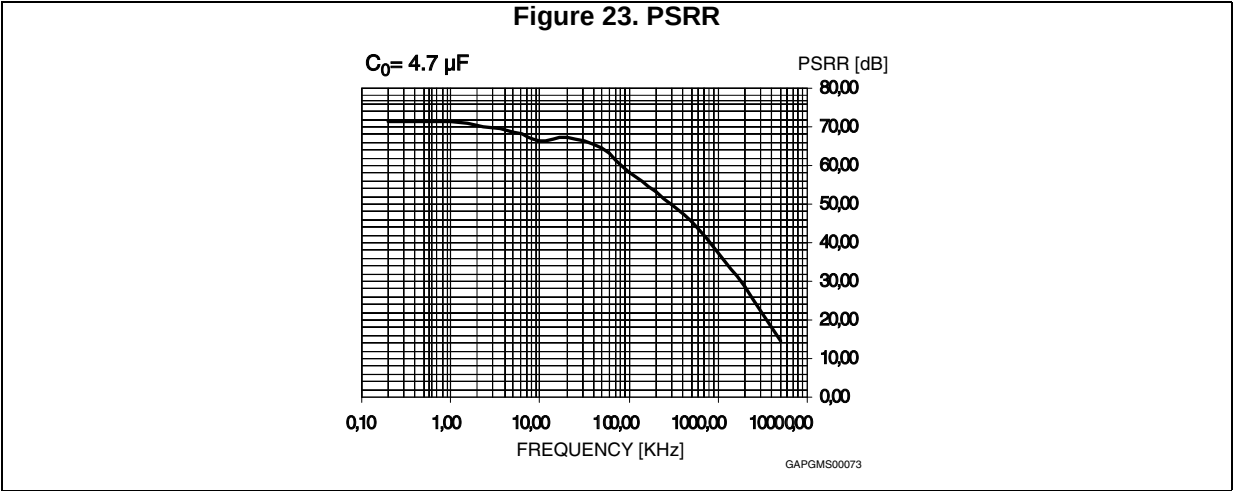


Figure 22. T_{wop} vs T_j





2.5 Test circuit and waveforms plot

2.5.1 Load regulation

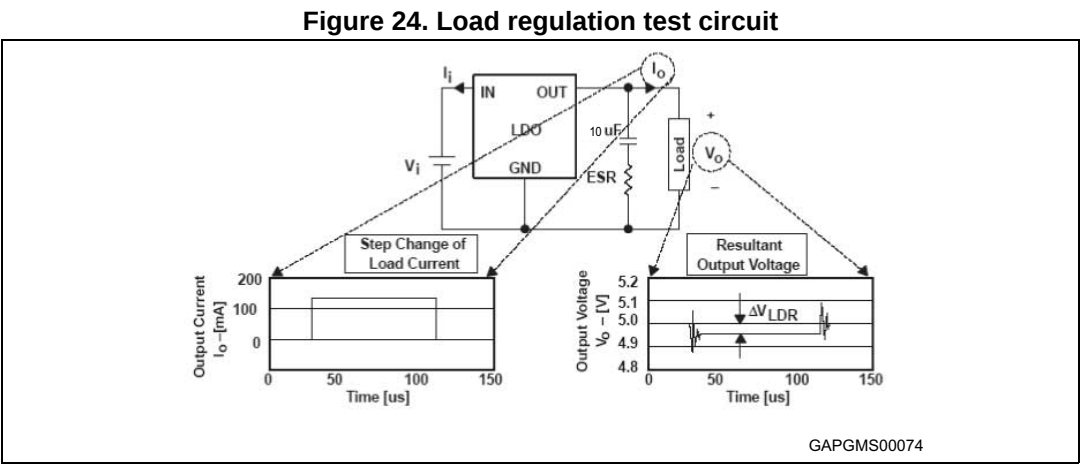
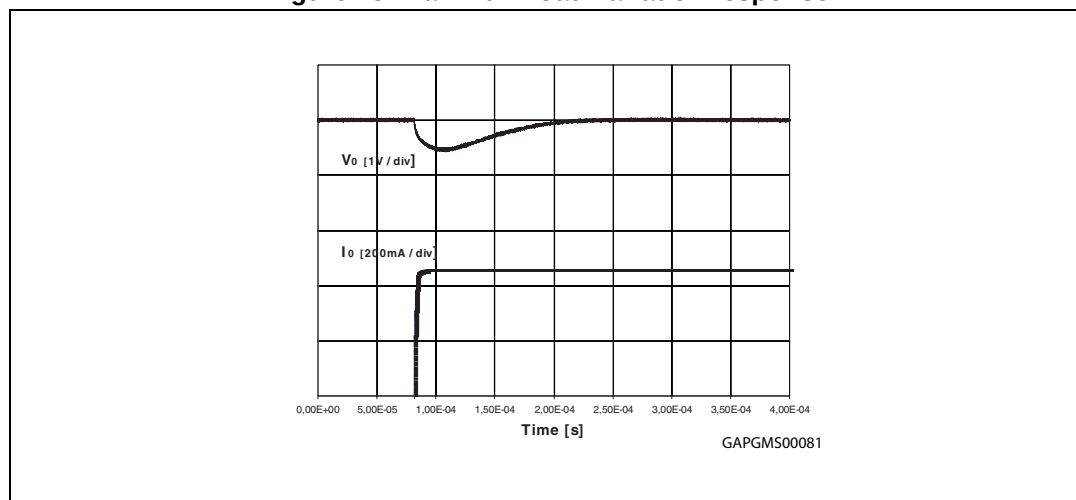
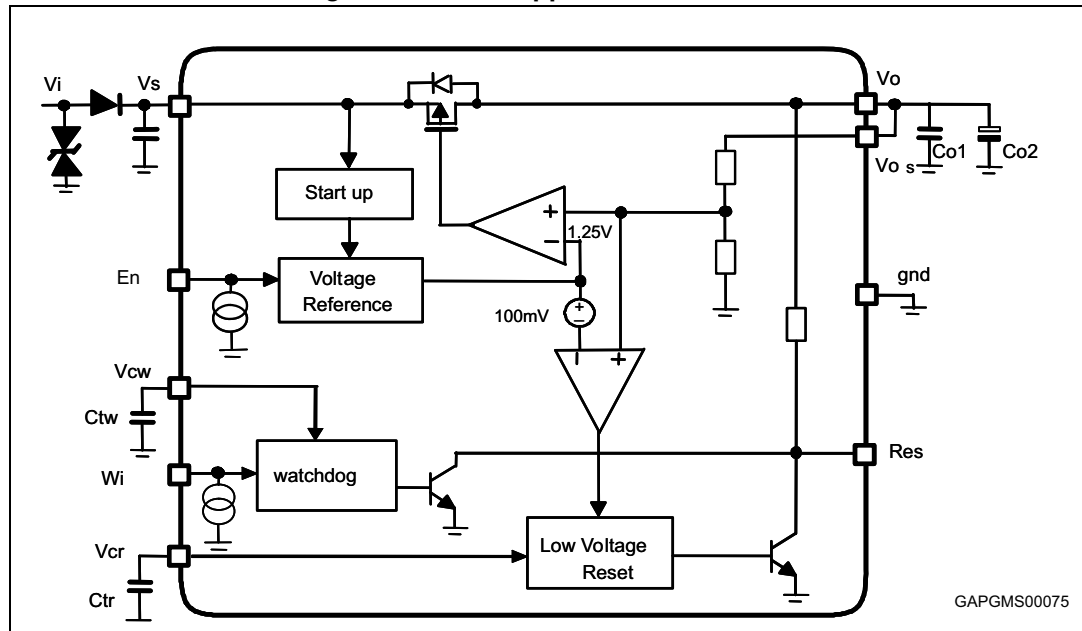


Figure 25. Maximum load variation response



3 Application information

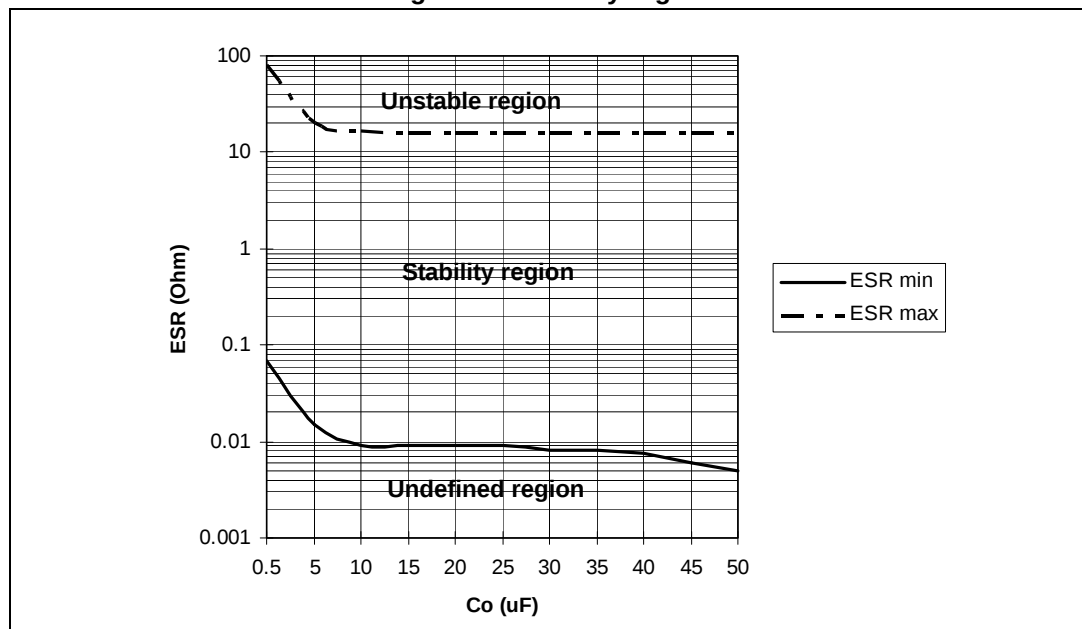
Figure 26. L4995 application schematic



Note:

The input capacitor $C_s > 200\text{nF}$ is necessary for the smoothing of line disturbances. The output capacitor $C_{o1} > 100\text{nF}$ is necessary for the stability of the regulation loop. In order to dampen output voltage oscillations during high load current surges, it is recommended an additional electrolytic capacitor $C_{o2} > 10\mu\text{F}$ to be placed at the output pin.

Figure 27. Stability region



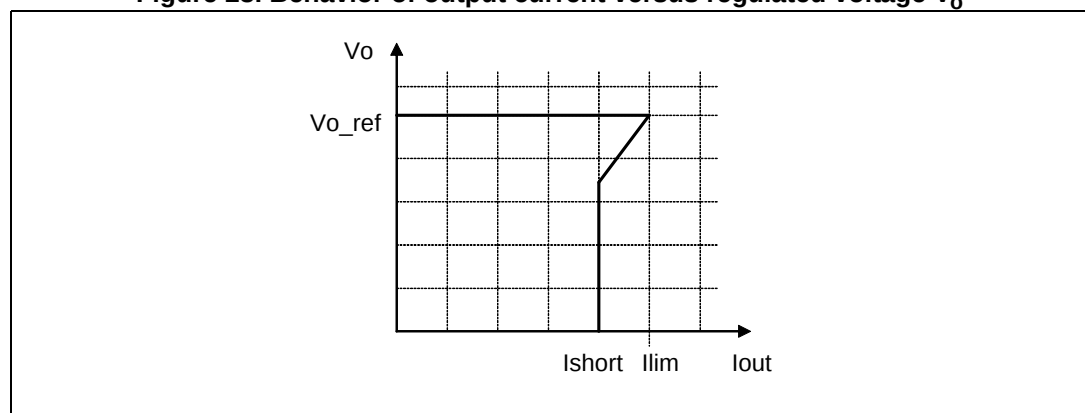
Note: The curve which describes the minimum ESR is derived from characterization data on the regulator with connected ceramic capacitors which feature low ESR values (at 100 kHz). Any capacitor with further lower ESR than the given plot value must be evaluated in each and every case.

3.1 Voltage regulator

Voltage regulator uses a p-channel transistor as a regulating element. With this structure, very low dropout voltage at current up to 500mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. A short circuit protection to GND is provided.

The voltage regulator is active when E_n is high.

Figure 28. Behavior of output current versus regulated voltage V_o



3.2 Reset

The reset circuit supervises the output voltage V_o . The V_{o_th} reset threshold is defined with the internal reference voltage and a resistor output divider. If the output voltage becomes lower than V_{o_th} then R_{es} goes low with a reaction time t_{rr} . The reset low signal is guaranteed for an output voltage V_o greater than 1V.

When the output voltage becomes higher than V_{o_th} then R_{es} goes high with a delay t_{rd} . This delay is obtained by an internal oscillator.

The oscillator period is given by:

Equation 1

$$T_{osc} = [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{cr} + [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{dr}$$

where:

I_{cr} : is an internally generated charge current

I_{dr} : is an internally generated discharge current

V_{Rth} , V_{Rlth} : are two voltages defined with the output voltage and a resistor output divider

C_{tr} : is an external capacitance.

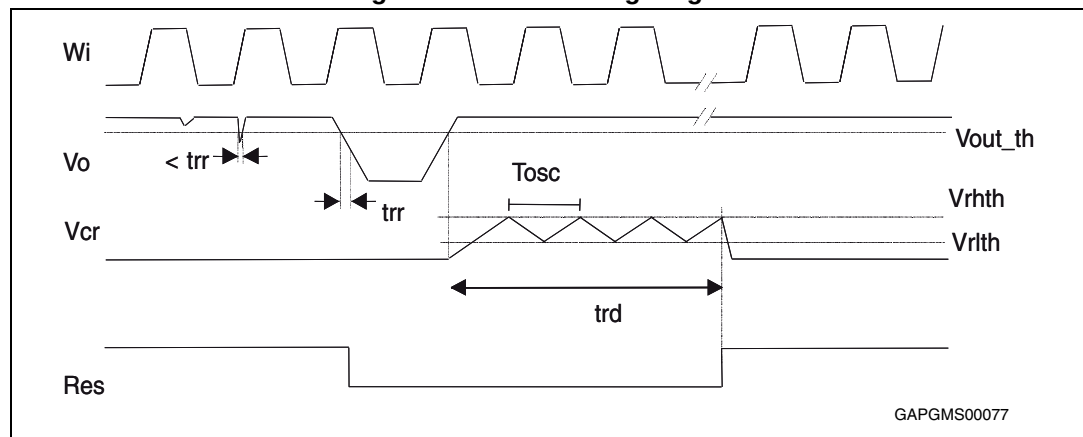
t_{rd} is given by:

Equation 2

$$t_{rd} = (V_{Rth} \times C_{tr}) / I_{cr} + 3 \times T_{osc}$$

Reset is active when E_n is high.

Figure 29. Reset timing diagram



3.3 Watchdog

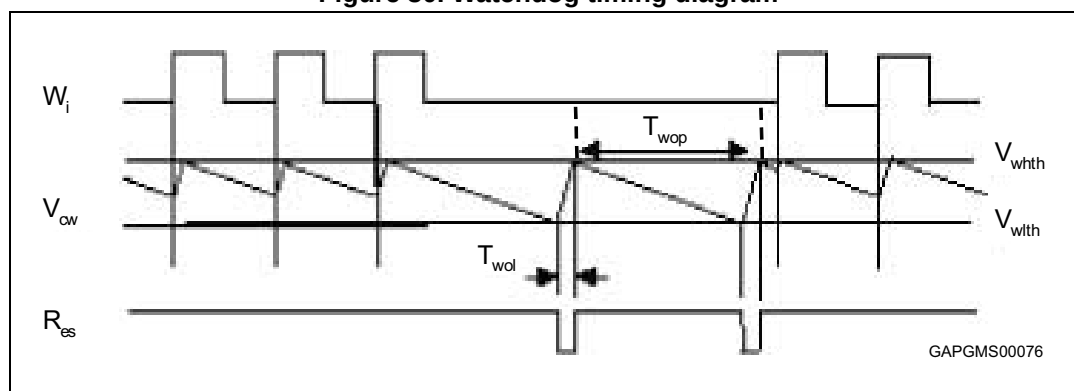
A connected microcontroller is monitored by the watchdog input W_i . If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, C_{tw} . The watchdog circuit discharges the capacitor C_{tw} with the constant current I_{cwd} . If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth} . In order to calculate the minimum time t , during which the micro-controller must output the positive edge, the following equation can be used:

Equation 3

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times t$$

Every W_i positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, V_{whth} , the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor C_{tw} .

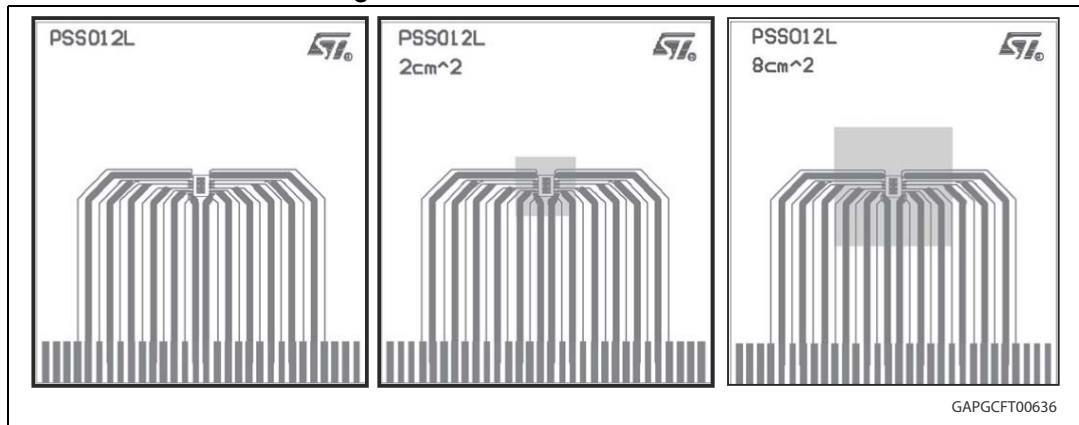
Figure 30. Watchdog timing diagram



4 Package and PCB thermal data

4.1 PowerSSO-12 thermal data

Figure 31. PowerSSO-12 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 μ m (front and back side) Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, Footprint dimension 4.1 mm x 6.5 mm).

Figure 32. $R_{thj-amb}$ vs PCB copper area in open box free air condition

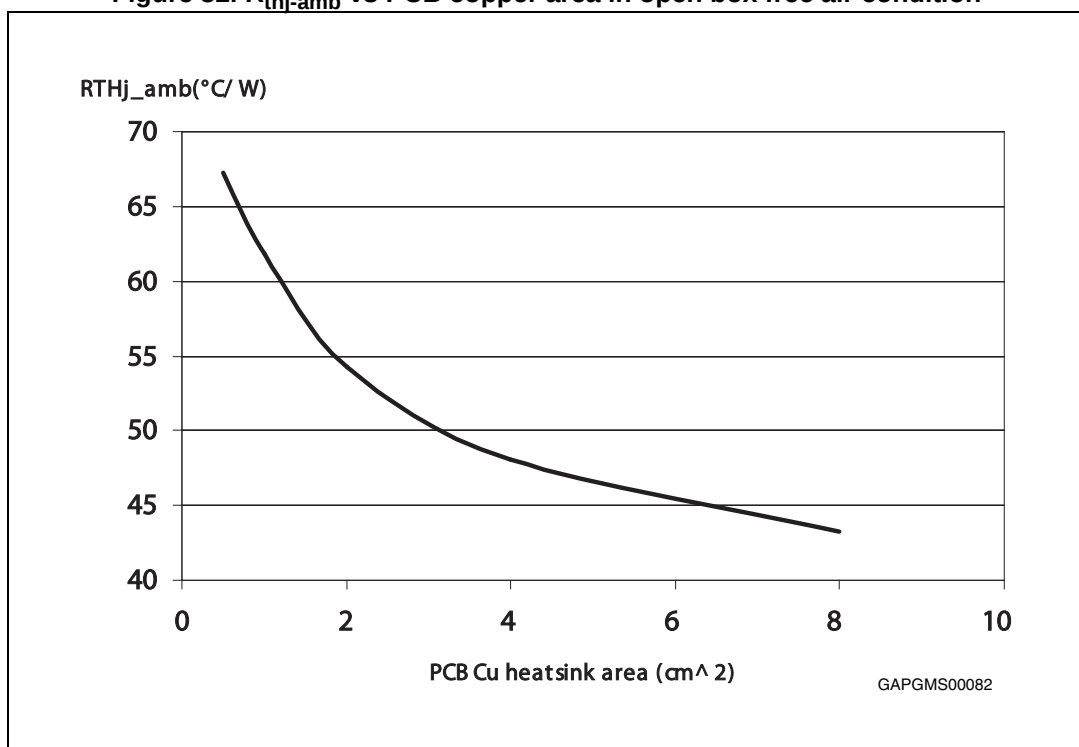
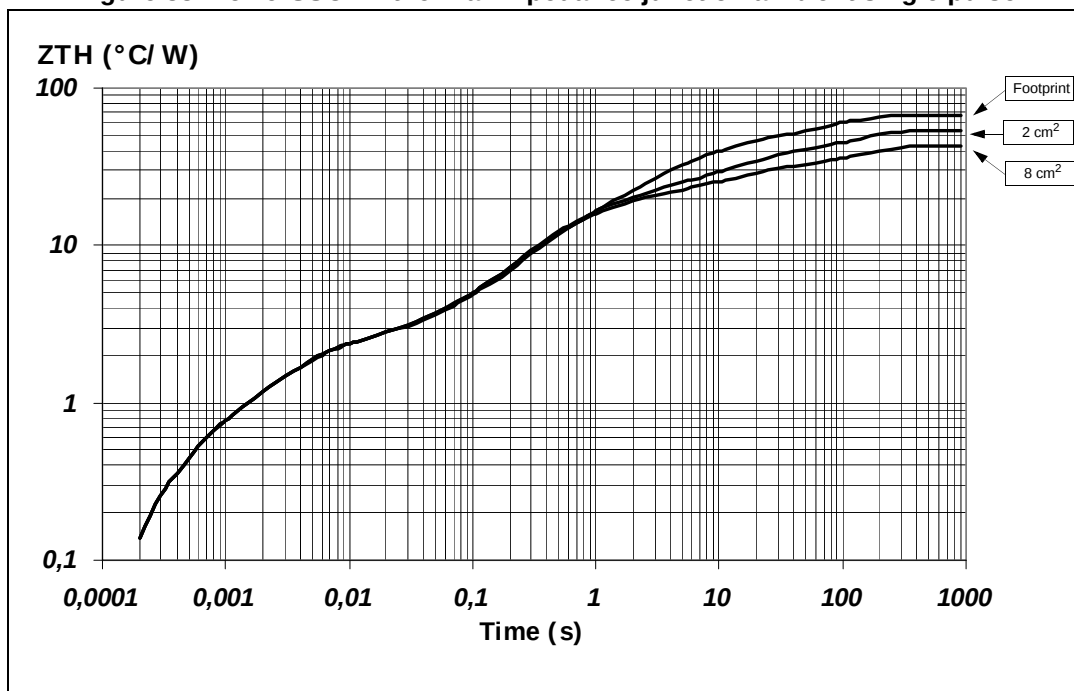


Figure 33. PowerSSO-12 thermal impedance junction ambient single pulse



Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 34. Thermal fitting model of Vreg in PowerSSO-12

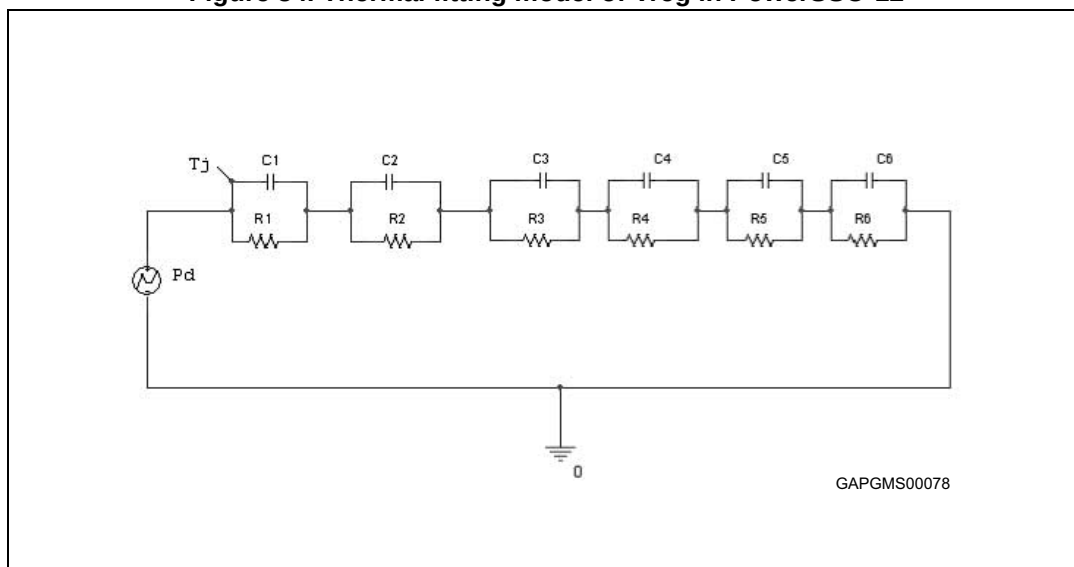
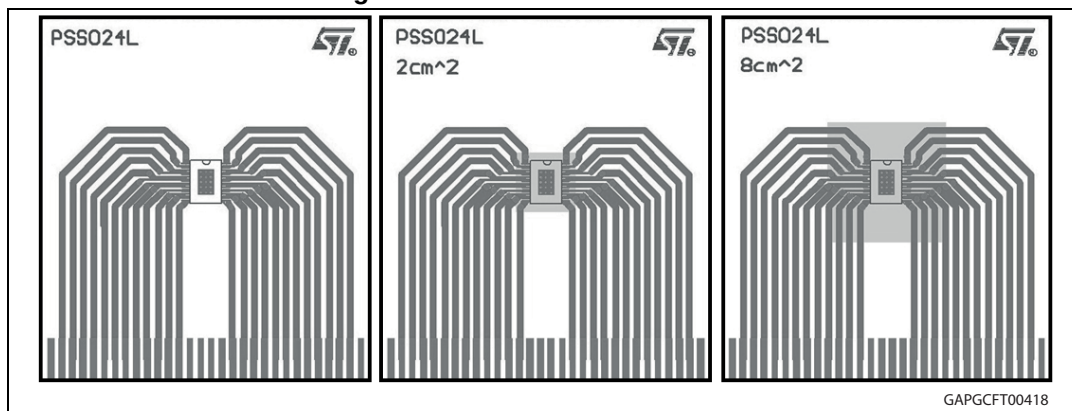


Table 9. PowerSSO-12 thermal parameter

Area/island (cm ²)	Footprint	2	8
R1 (°C/W)	0.45		
R2 (°C/W)	1.79		
R3 (°C/W)	7		
R4 (°C/W)	10	10	9
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

4.2 PowerSSO-24 thermal data

Figure 35. PowerSSO-24 PC board



Note:

Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 μ m (front and back side) Thermal via separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, Footprint dimension 4.1 mm x 6.5 mm).

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition

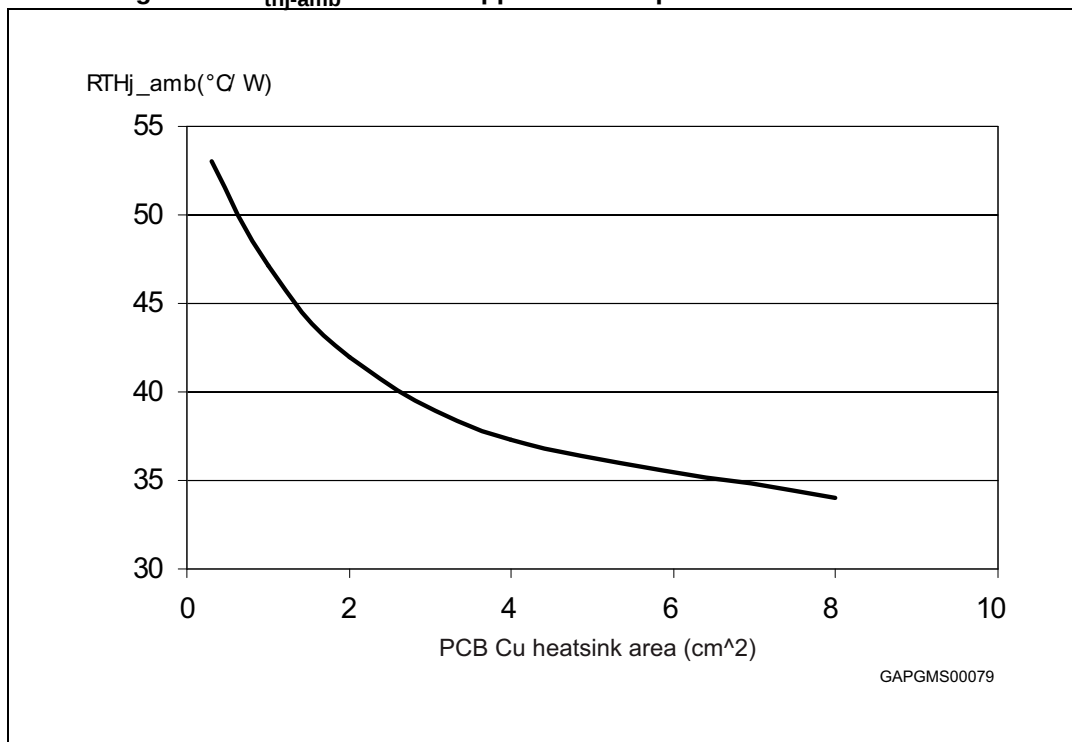
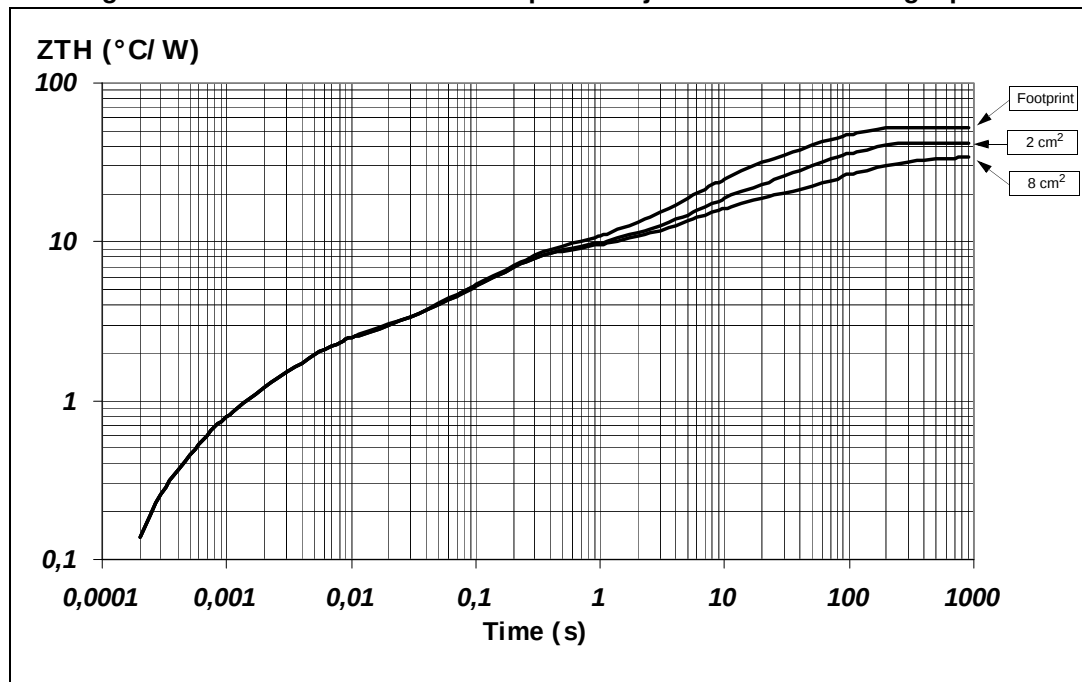


Figure 37. PowerSSO-24 thermal impedance junction ambient single pulse



Equation 5: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

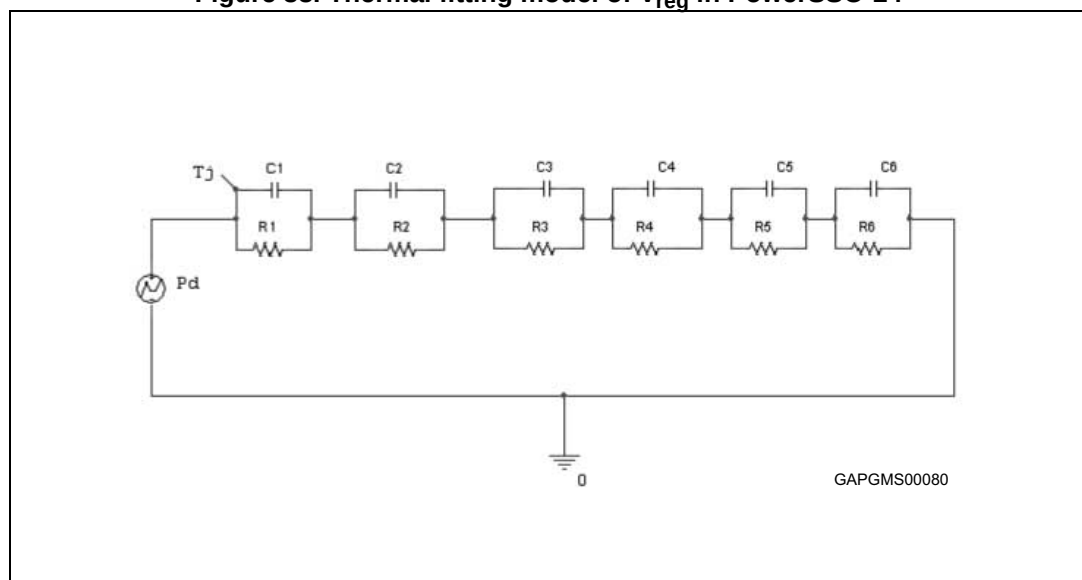
Figure 38. Thermal fitting model of V_{reg} in PowerSSO-24

Table 10. PowerSSO-24 thermal parameter

Area/island (cm ²)	Footprint	2	8
R1 (°C/W)	0.45		
R2 (°C/W)	1.79		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 39. PowerSSO-12 package dimensions

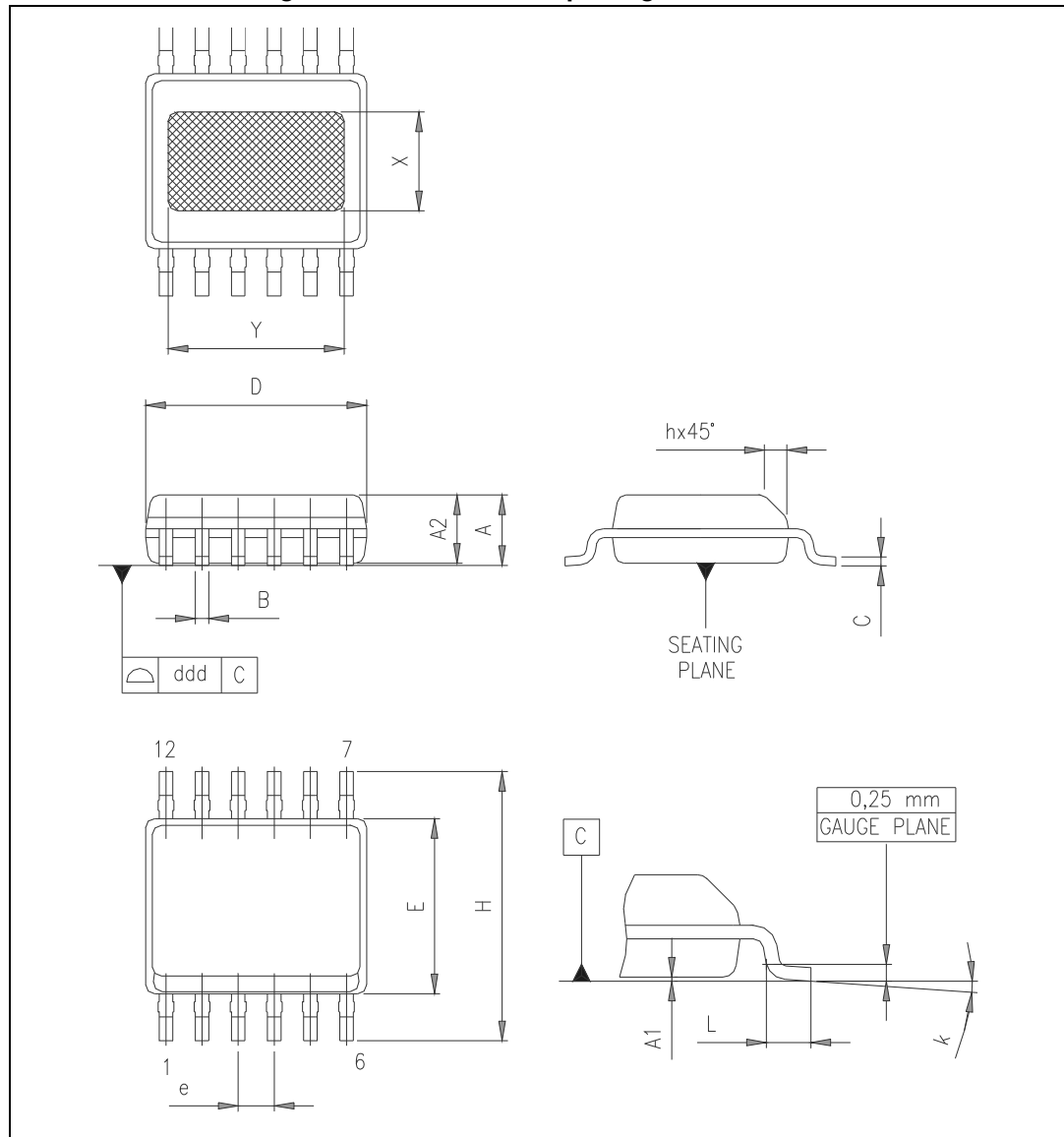


Table 11. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	2.200		2.800
Y	2.900		3.500
ddd			0.100

5.2 PowerSSO-24 mechanical data

Figure 40. PowerSSO-24 package dimensions

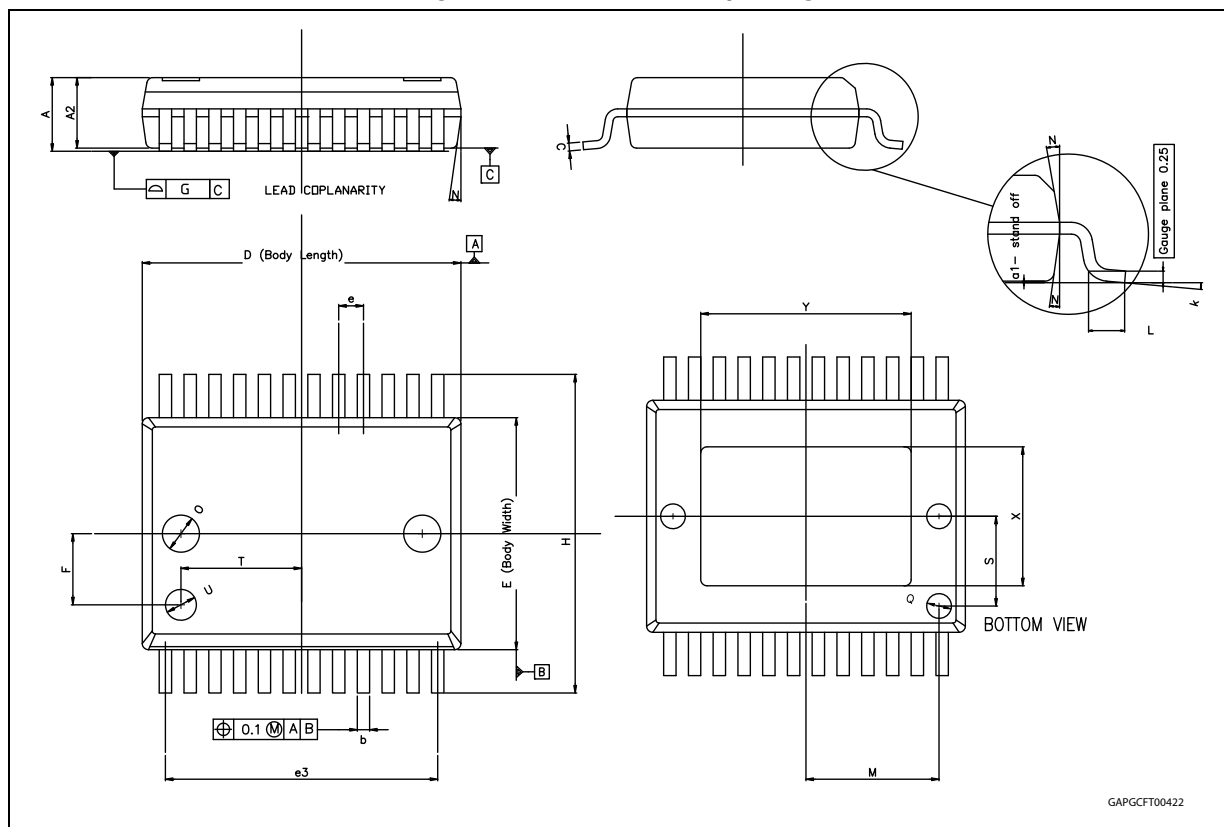


Table 12. PowerSSO-24 mechanical data⁽¹⁾⁽²⁾

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.45
A2	2.15		2.35
a1	0		0.10
b	0.33		0.51
c	0.23		0.32
D ⁽³⁾	10.10		10.50
E ⁽³⁾	7.40		7.60
e		0.8	
e3		8.8	
F		2.3	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1	
N			10°
X	4.1		4.7
Y	6.5 4.9 ⁽⁴⁾		7.1 5.5 ⁽⁴⁾

1. No intrusion allowed inwards the leads.
2. Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side
3. "D and E" do not include mold Flash or protusions.
Mold Flash or protusions shall not exceed 0.15 mm.
4. Variations for small window leadframe option.

5.3 PowerSSO-12 packing information

Figure 41. PowerSSO-12 tube shipment (no suffix)

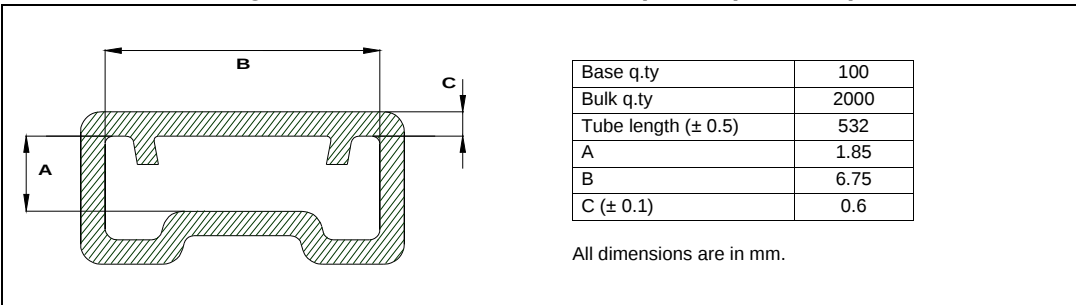
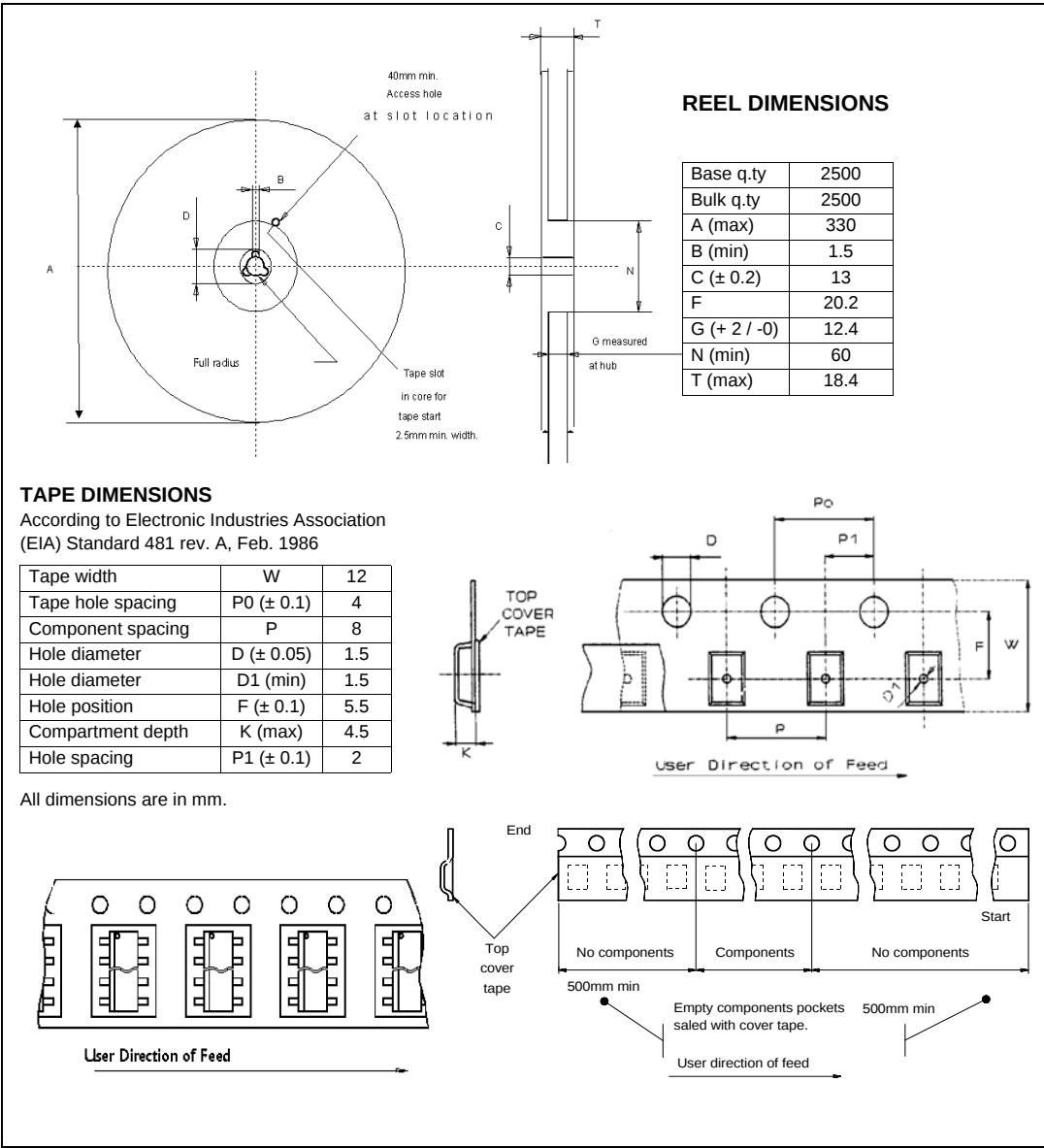


Figure 42. PowerSSO-12 tape and reel shipment (suffix "TR")



5.4 PowerSSO-24 packing information

Figure 43. PowerSSO-24 tube shipment (no suffix)

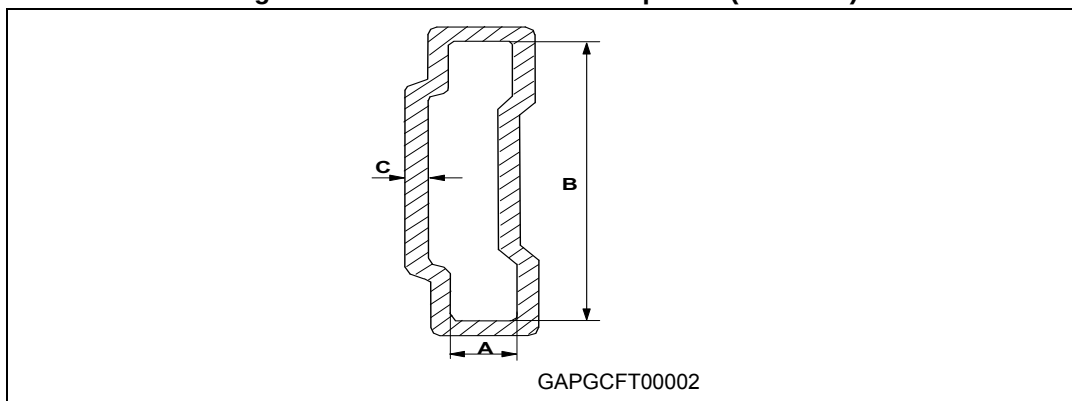
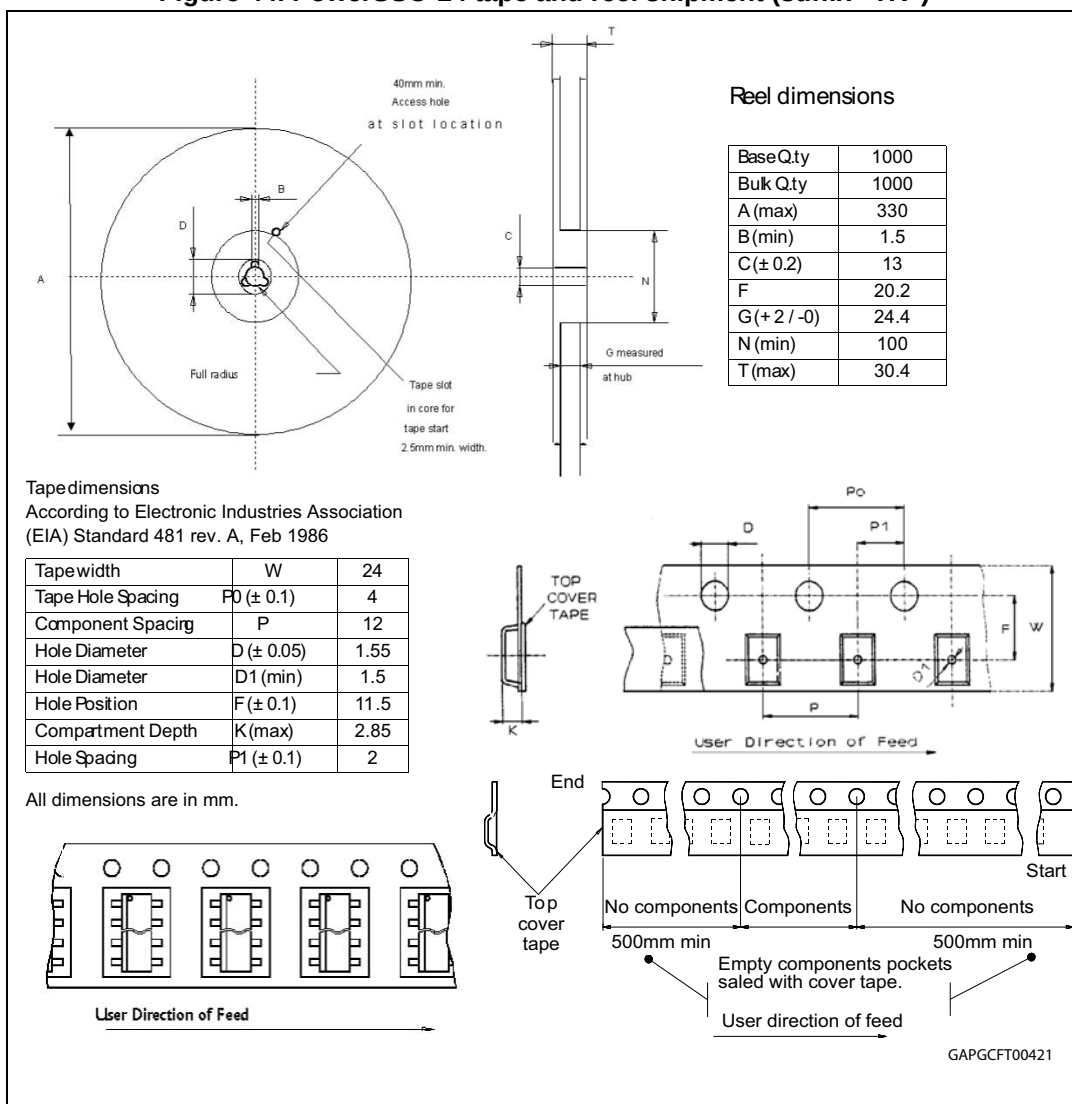


Figure 44. PowerSSO-24 tape and reel shipment (suffix "TR")



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
26-May-2006	1	Initial release.
05-Jan-2007	2	L4995A and L4995R versions added: Features section updated and table added. Table 1 updated. Table 5: General, Watchdog Iwi entry updated. Figure 2: Block diagram of L4995A and Figure 3: Block diagram of L4995R added. Table 2: Pins descriptions updated. Table 4: Thermal data updated. List of tables and List of figures added. Packaging information provided in new format. Table 11: PowerSSO-12 mechanical data X and Y values updated. Some sections reformatted for clarity. New disclaimer added.
18-May-2007	3	Updated Table 2: Pins descriptions. Updated Figure 4: Pins configurations (L4995). Table 1: Device summary changed title.
09-Jul-2007	4	Updated Table 2: Pins descriptions .
09-Aug-2007	5	Updated Table 2: Pins descriptions. Updated Table 12: PowerSSO-24 mechanical data.

Table 13. Document revision history (continued)

Date	Revision	Changes
07-Dec-2007	6	Updated Section 2.2: Thermal data: – corrected note changing single layer with double layer. Updated Table 5: General: – changed I_{short} typ. value from 750 to 800 mA – added I_{short} max. value – changed I_{lim} typ. value from 820 to 900 mA – added I_{lim} max. value – added I_{lim} note – added V_{dp} note – changed I_{qn_1} typ. value from 110 to 90 μA – added I_{qn_1} max. value – added I_{qn_50} max. value – added I_{qn_150} max. value – changed I_{qn_250} typ. value from 1.2 to 1 mA – added I_{qn_250} max. value – changed I_{qn_500} typ. value from 2.4 to 2.1 mA – added I_{qn_500} max. value Updated Table 6: Reset: – changed V_{Rlth} parameter definition from “Reset timing low” to “Reset delay circuit low threshold” – changed V_{Rhth} parameter definition from “Reset timing high” to “Reset delay circuit high threshold” – added T_{rd} min. and max. values Updated Table 7: Watchdog: – added I_{wi} max value Updated Table 8: Enable: – changed Pull down current symbol from R_{En} to I_{En} – changed I_{En} typ. value from 2.5 to 10 μA – added I_{En} max. value Added Section 2.4: Electrical characteristics curves. Added Section 2.5: Test circuit and waveforms plot. Added Section 4: Package and PCB thermal data
03-Oct-2008	7	Updated PowerSSO-24 information: – changed Figure 40: PowerSSO-24 package dimensions – changed Table 12: PowerSSO-24 mechanical data.
19-Mar-2009	8	Updated Table 4: Thermal data
19-May-2009	9	Updated Table 2: Pins descriptions. Updated Figure 4: Pins configurations (L4995) – Changed GND to substrate

Table 13. Document revision history (continued)

Date	Revision	Changes
24-Jun-2009	10	Table 12: PowerSSO-24 mechanical data: – Deleted A (min) value – Changed A (max) value from 2.50 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Updated K row – Changed L (min) value from 0.6 to 0.55 – Changed L (max) value from 1 to 0.85
12-Jul-2010	11	Added Figure 27: Stability region .
09-Mar-2012	12	Added footnote in Table 3: Absolute maximum ratings .
17-Oct-2012	13	Table 6: Reset: – T_{rd}: updated min, typ and max values
20-Sep-2013	14	Updated disclaimer.
17-Sep-2018	15	Updated title and Features . Minor text changes.

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