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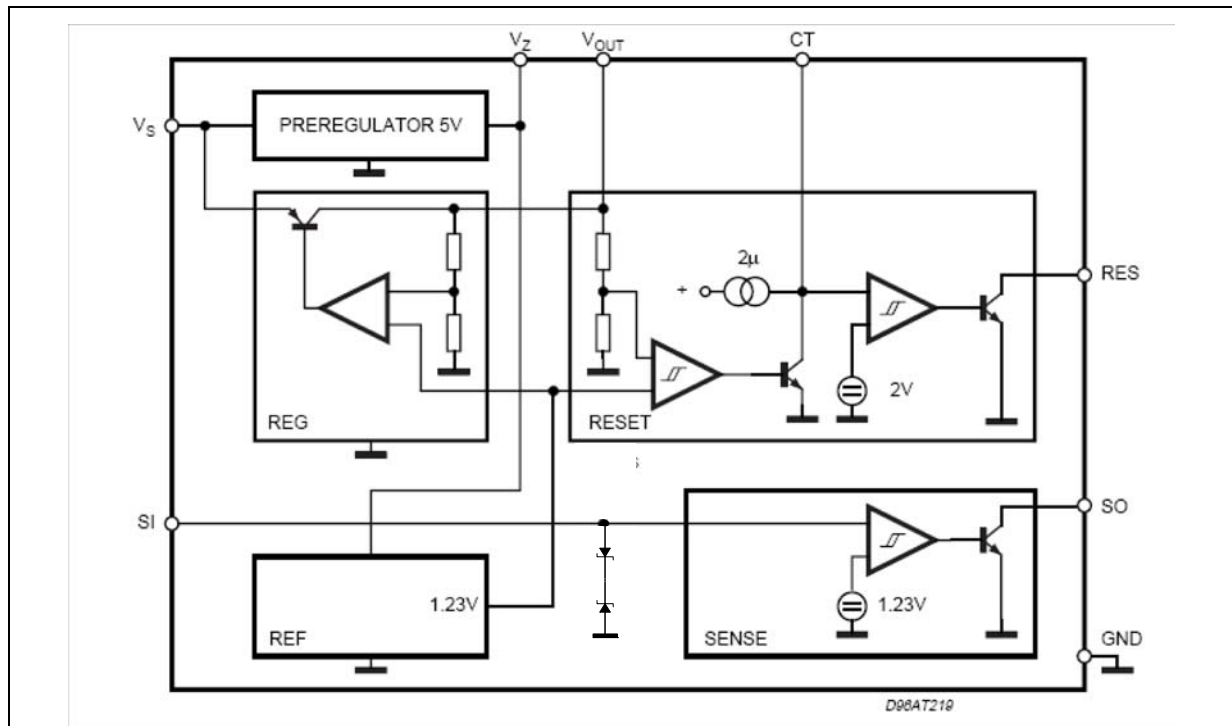
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1 Block diagram and pin description

Figure 1. Block diagram



Note: The block diagram illustrates only a major internal device functionality and it is not intended to mimic any details of hardware design

Figure 2. Configuration diagram (top view)

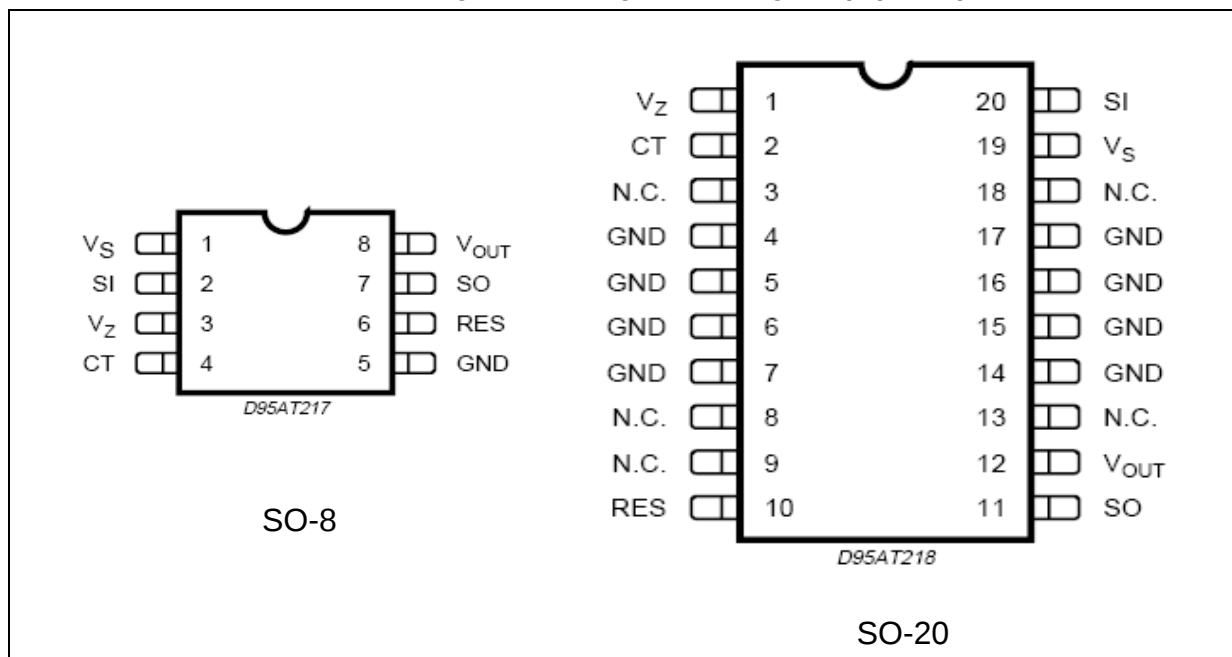


Table 2. Pin definitions and functions

Pin N°		Symbol	Function
SO-8	SO-20		
1	19	V_S	Input supply voltage. Block to GND via an external capacitor (see Figure 3).
2	20	S_I	Sense input pin to supervise input voltage. Connect via an external voltage divider connected to V_S and to GND.
3	1	V_Z	Preregulator output voltage. For details, see Section 3.4: Preregulator .
4	2	C_T	Reset pulse delay adjustment. Connecting this pin via a capacitor to GND
5	4, 5, 6, 7, 14, 15, 16, 17	GND	Ground reference
6	10	RES	Reset output. It is pulled down when the output voltage goes below V_{RT} .
7	11	S_O	Sense output. This open collector pin must be connected to V_{OUT} via an external resistor. It is pulled down whenever the S_I voltage becomes lower than an internal voltage.
8	12	V_{OUT}	Output voltage. Block to GND via an external capacitor (see Figure 3)
-	3, 8, 9, 13, 18	NC	Not connected pins

2 Electrical specifications

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{SDC}	DC operating supply voltage	28	V
V_{STR}	Transient supply voltage ($T < 1s$)	40	V
I_O	Output current	Internally limited	
V_O	Output voltage	20	V
V_{RES}, V_{SO}	Output voltage	20	V
I_{RES}, I_{SO}	Output current	5	mA
V_{CT}	Reset delay voltage	7	V
V_{SIDC}	Sense input voltage	28	V
V_Z	Preregulator output voltage	7	V
I_Z	Preregulator output current	5	mA
T_J	Junction temperature	-40 to +150	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Note: The circuit is ESD protected according to MIL-STD-883C.

2.2 Thermal data

Table 4. Thermal data

Symbol	Description	SO-8	SO20L	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient (max)	200	50	°C/W
$R_{th\ j-pins}$	Thermal Resistance Junction-pins (max)		15	°C/W
TJSD	Thermal Shutdown Junction temperature	165		°C

2.3 Electrical characteristics

$V_S = 14\text{ V}$; $-40\text{ °C} < T_J < 125\text{ °C}$ unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_O	Output voltage	$T_J = 25\text{ °C}$; $I_O = 1\text{ mA}$	4.95	5	5.05	V
V_O	Output voltage	$6\text{ V} < V_{IN} < 28\text{ V}$, $1\text{ mA} < I_O < 50\text{ mA}$	4.90	5	5.10	V
V_O	Output voltage	$V_{IN} = 40\text{ V}$; $T < 1\text{ s}$; $5\text{ mA} < I_O < 100\text{ mA}$	4.75		5.25	V
V_{DP}	Dropout voltage	$I_O = 10\text{ mA}$		0.1	0.25	V
		$I_O = 50\text{ mA}$		0.2	0.4	V
		$I_O = 100\text{ mA}$		0.3	0.5	V
V_{IO}	Input to output voltage difference in undervoltage condition	$V_{IN} = 4\text{ V}$, $I_O = 35\text{ mA}$			0.4	V
$I_{outh}^{(1)}$	Max output leakage	$V_{IN} = 25\text{ V}$, $V_O = 5.5\text{ V}$	20	50	80	μA
V_{OL}	Line regulation	$6\text{ V} < V_{IN} < 28\text{ V}$; $I_O = 1\text{ mA}$			20	mV
V_{OLO}	Load regulation	$1\text{ mA} < I_O < 100\text{ mA}$			30	mV
I_{LIM}	Current limit	$V_O = 4.5\text{ V}$	105	200	400	mA
		$V_O = 4.5\text{ V}$; $T_J = 25\text{ °C}$	120		400	mA
		$V_O = 0\text{ V}^{(2)}$		100		mA
I_{QSE}	Quiescent current	$I_O = 0.3\text{ mA}$; $T_J < 100\text{ °C}$		200	300	μA
I_Q	Quiescent current	$I_O = 100\text{ mA}$			5	mA

1. With this test we guarantee that with no output current the output voltage will not exceed 5.5V

2. Foldback characteristic

Table 6. Reset

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage			$V_O - 0.5\text{ V}$		V
V_{RTH}	Reset threshold hysteresis		50	100	200	mV
t_{RD}	Reset pulse delay	$C_T = 100\text{ nF}$; $T_R \geq 100\text{ }\mu\text{s}$	55	100	180	ms
V_{RL}	Reset output low voltage	$R_{RES} = 10\text{ K}\Omega$ to V_O $V_S \geq 1.5\text{ V}$			0.4	V
I_{RH}	Reset output high leakage current	$V_{RES} = 5\text{ V}$			1	μA
V_{CTth}	Delay comparator threshold			2		V
$V_{CTth, hy}$	Delay comparator threshold hysteresis			100		mV

Table 7. Sense

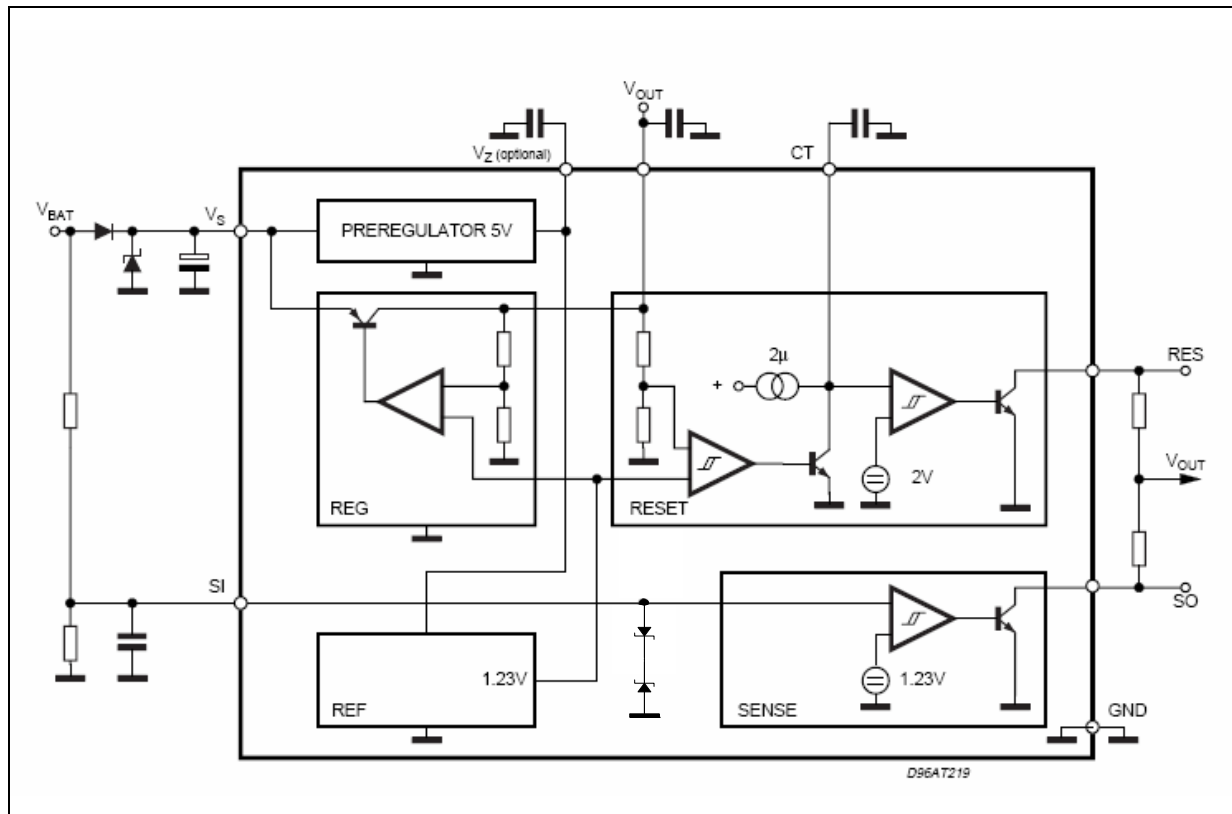
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{st}	Sense low threshold		1.16	1.23	1.35	V
V_{sth}	Sense threshold hysteresis		20	100	200	mV
V_{SL}	Sense output low voltage	$V_{SI} \leq 1.16 \text{ V}$; $V_S \geq 3 \text{ V}$ $R_{SO} = 10 \text{ K}\Omega$ to V_O			0.4	V
I_{SH}	Sense output leakage	$V_{SO} = 5 \text{ V}$; $V_{SI} \geq 1.5 \text{ V}$			1	μA
I_{SI}	Sense input current	$V_{SI} = 0$	-20	-8	-3	μA

Table 8. Preregulator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_Z	Preregulator output voltage	$I_Z = 10 \mu\text{A}$	4.5	5	6	V
I_Z	Preregulator output current				10	μA

3 Application information

Figure 3. Application circuit



Note: For stability: $C_S \geq 1\mu\text{F}$, $C_O \geq 4.7\mu\text{F}$, $\text{ESR} < 10\Omega$ at 10KHz. Recommended for application: $C_S = C_O = 10\mu\text{F}$ to $100\mu\text{F}$

3.1 Supply voltage transient

High supply voltage transients can cause a reset output signal disturbance. For supply voltages greater than 8V the circuit shows a high immunity of the reset output against supply transients of more than $100\text{V}/\mu\text{s}$. For supply voltages less than 8V supply transients of more than $0.4\text{V}/\mu\text{s}$ can cause a reset signal disturbance.

To improve the transient behaviour for supply voltages less than 8V a capacitor at pin V_Z can be used.

This capacitor ($C_3 \leq 1\mu\text{F}$) reduces also the output noise.

3.2 Functional description

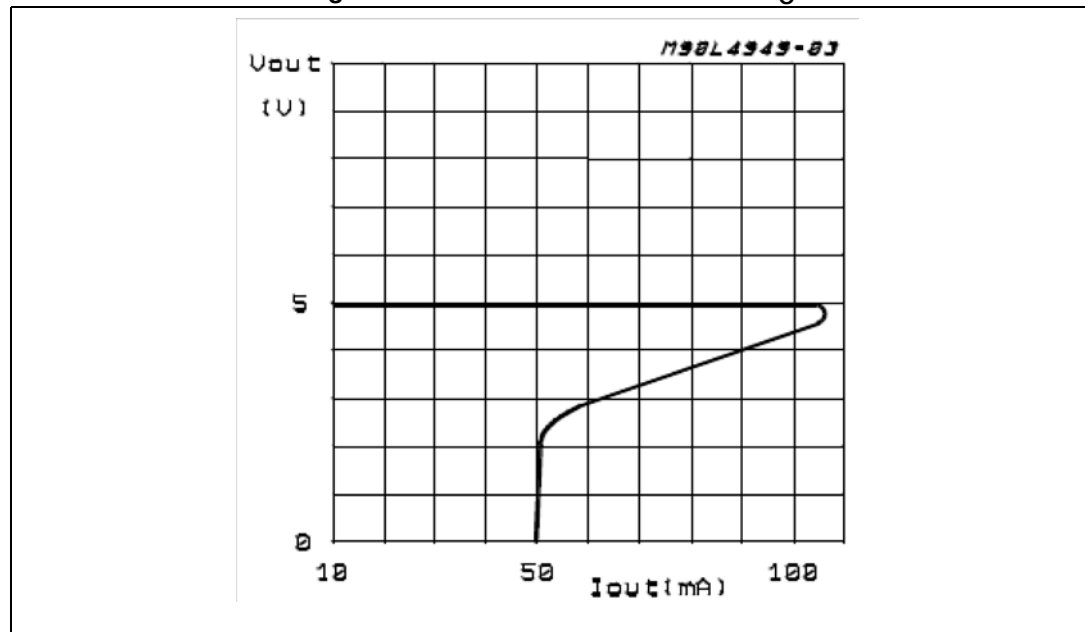
The L4949ED-E and L4949EP-E are monolithic integrated voltage regulator, based on the STM modular voltage regulator approach. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. Nevertheless, it is suitable also in other applications where the

present functions are required. The modular approach of this device allows to get easily also other features and functions when required.

3.3 Voltage regulator

The voltage regulator uses an Isolated Collector Vertical PNP transistor as a regulating element.

Figure 4. Foldback characteristic of V_O



With this structure very low dropout voltage at currents up to 100mA is obtained. The dropout operation of the standby regulator is maintained down to 3V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. With this feature no functional interruption due to overvoltage pulses is generated. The typical curve showing the standby output voltage as a function of the input supply voltage is shown in [Figure 5](#). The current consumption of the device (quiescent current) is less than 300 μ A.

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled, the quiescent current as a function of the supply input voltage is shown in [Figure 6](#).

Figure 5. Output voltage vs input voltage

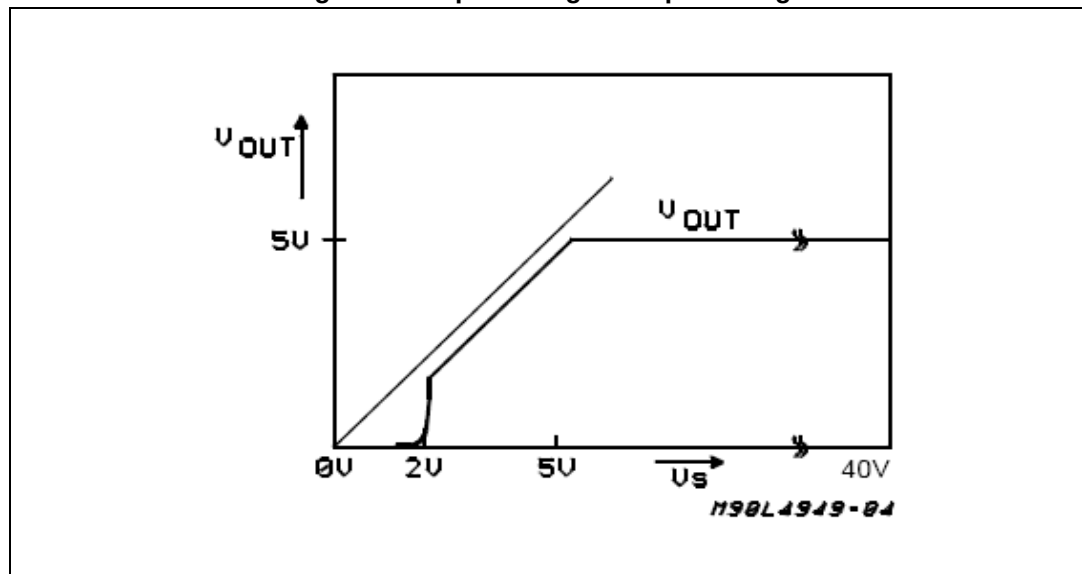
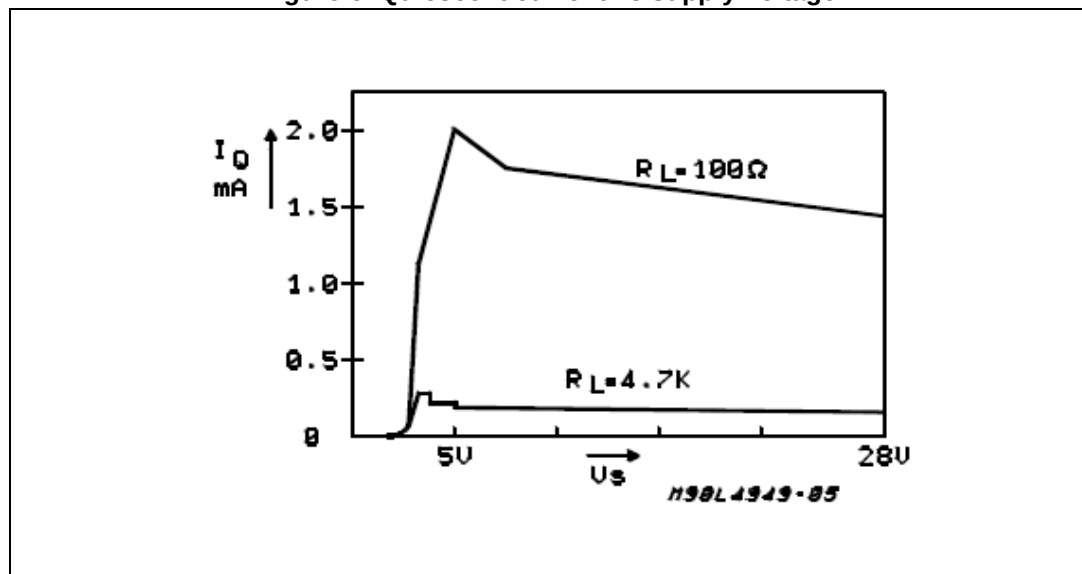


Figure 6. Quiescent current vs supply voltage



3.4 Preregulator

To improve the transient immunity a preregulator stabilizes the internal supply voltage to 5 V. This internal voltage is present at Pin 3 (V_Z). This voltage should not be used as an output because the output capability is very small ($\leq 10 \mu\text{A}$).

This output may be used as an option when a better transient behaviour for supply voltages less than 8 V is required (see also application note).

In this case a capacitor (100 nF - 1 μF) must be connected between pin V_Z and GND. If this feature is not used pin V_Z must be left open.

3.5 Reset circuit

The block circuit diagram of the reset circuit is shown in [Figure 7](#). The reset circuit supervises the output voltage.

The reset threshold of 4.5 V is defined with the internal reference voltage and standby output divider.

The reset pulse delay time t_{RD} , is defined with the charge time of an external capacitor C_T :

$$t_{RD} = \frac{C_T \cdot 2V}{2\mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T .

The reaction time of the reset circuit increases the noise immunity. Standby output voltage drops below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time.

The nominal reset delay time is generated for standby output voltage drops longer than approximately 50ms.

The typical reset output waveforms are shown in [Figure 8](#).

3.6 Sense comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23V. The use of an external voltage divider makes this comparator very flexible in the application.

It can be used to supervise the input voltage either before or after the protection diode and to give additional informations to the microprocessor like low voltage warnings.

Figure 7. Block circuit of reset circuit

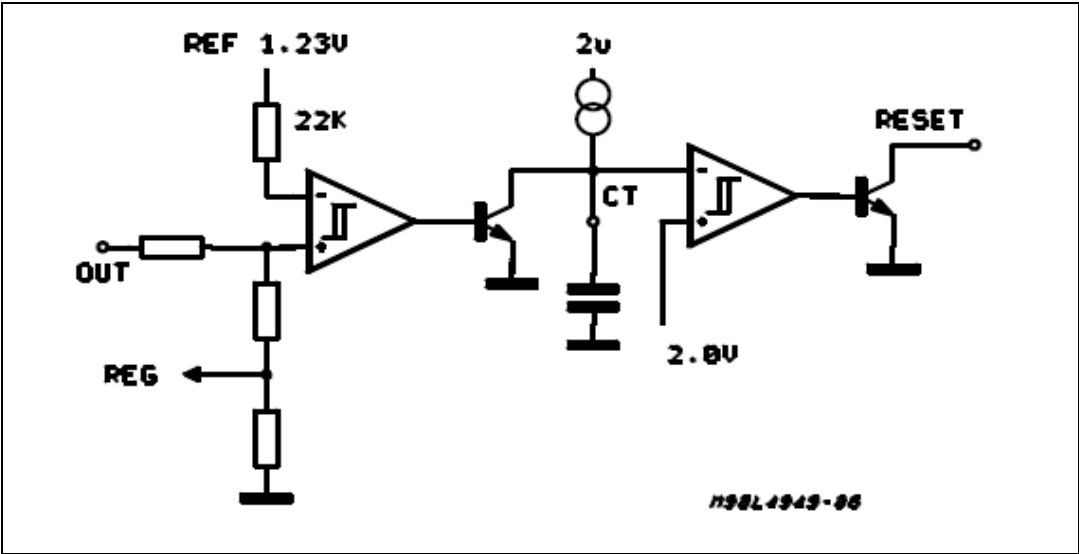
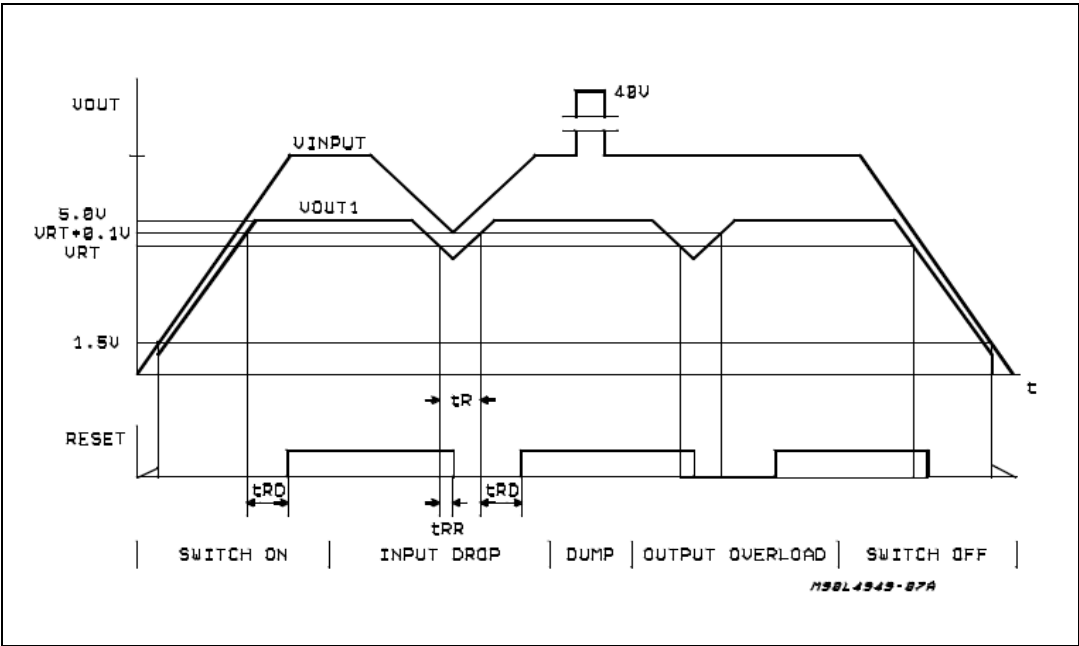


Figure 8. Waveforms



4 Package and packing information

4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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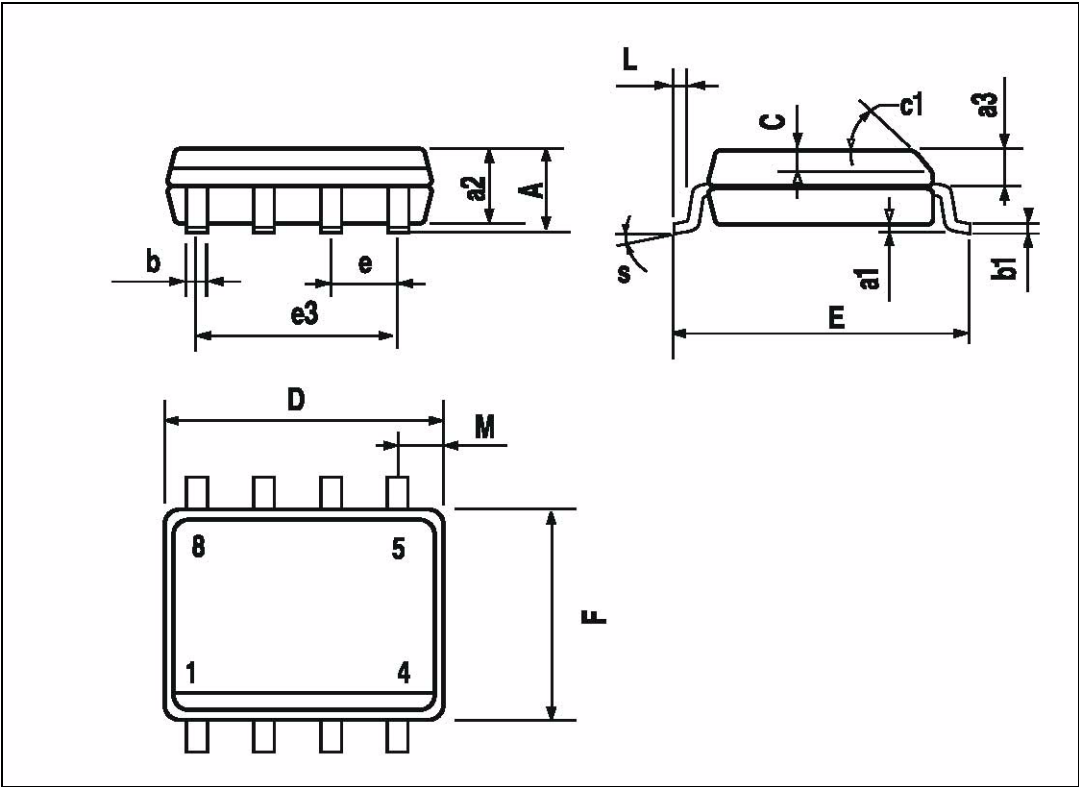
4.2 SO-8 TP package information

Table 9. SO-8 TP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45° (typ.)		
D ⁽¹⁾	4.8		5.0
E	5.8		6.2
e		1.27	
e3		3.81	
F ⁽¹⁾	3.8		4.0
L	0.4		1.27
M			0.6
S	8° (max.)		

1. D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).

Figure 9. SO-8 TP package dimensions



4.3 SO-20 TP package information

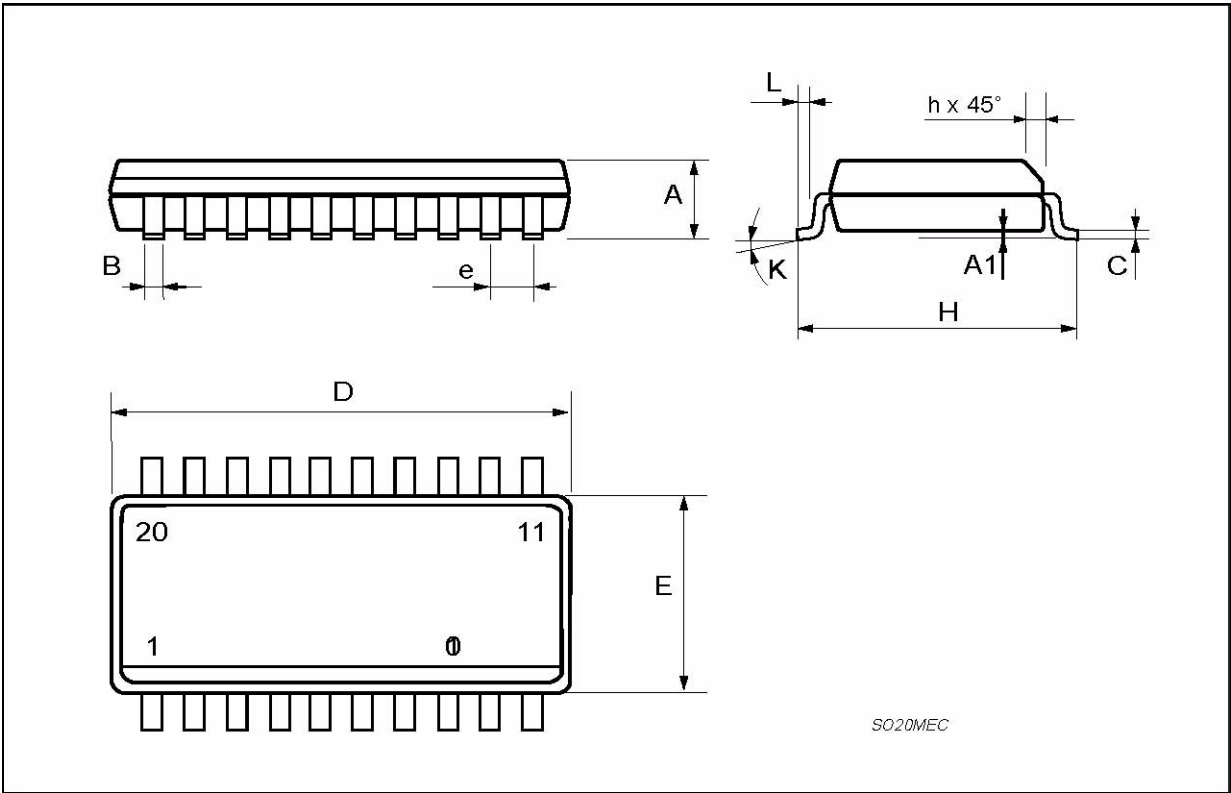
Table 10. SO-20 TP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.1		0.3
B	0.33		0.51
C	0.23		0.32
D	12.6		13
E	7.4		7.6
e		1.27	
H	10		10.65

Table 10. SO-20 TP mechanical data (continued)

Dim.	mm		
	Min.	Typ.	Max.
h	0.25		0.75
L	0.4		1.27
K	0 (min.)8 (max.)		

Figure 10. SO20 TP package dimensions



5 Revision history

Table 11. Document revision history

Date	Revision	Description of changes
24-Nov-2009	1	Initial release.
20-Sep-2013	2	Updated disclaimer.
28-Feb-2018	3	Removed tube version for SO-8 package.
24-Sep-2018	4	Updated : <i>Features</i>

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