

FIG.1- 8/20us pulse waveform according to IEC 61000-4-5

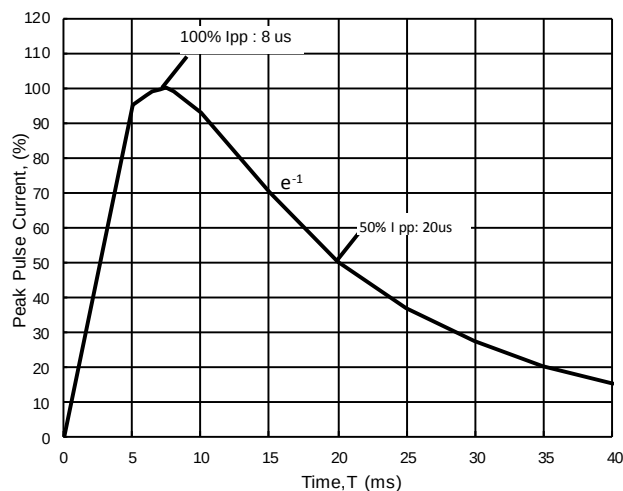


FIG.2- ESD pulse waveform according to IEC 61000-4-2

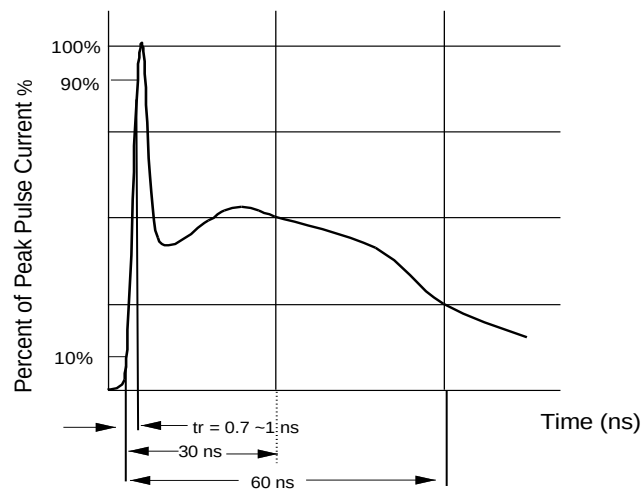


FIG3- Power dissipation versus pulse time

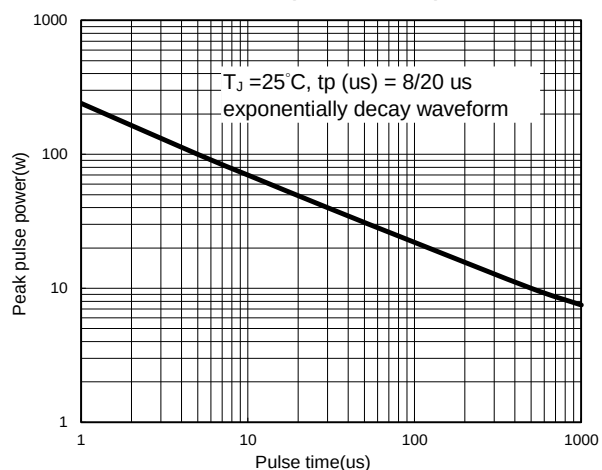


FIG4- Peak pulse power versus Tj

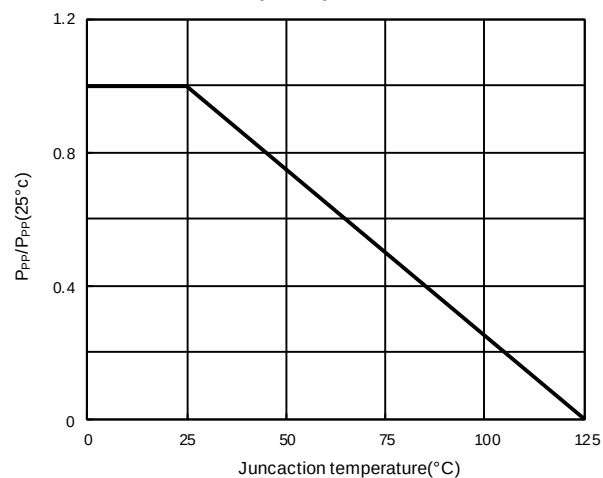


FIG.5- Typical junction capacitance

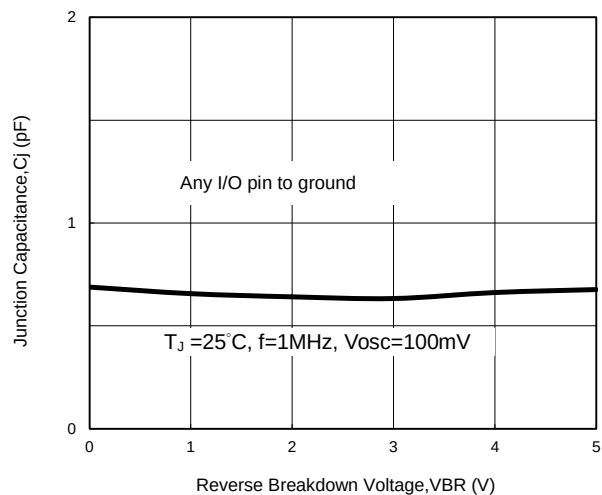
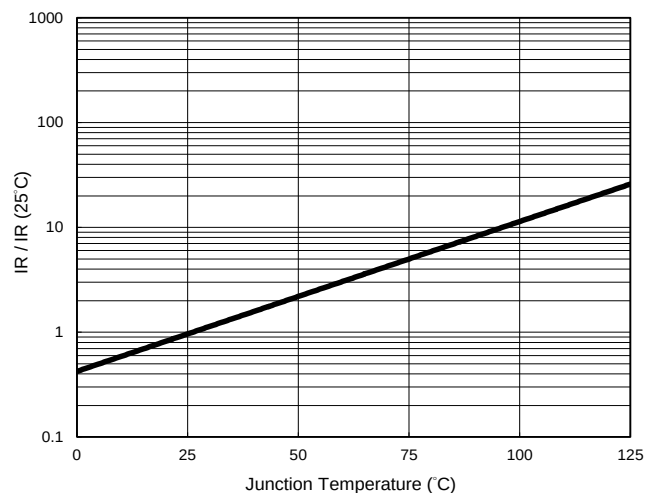


FIG.6- reverse leakage current versus Tj



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L05ESDL5V0NA-4

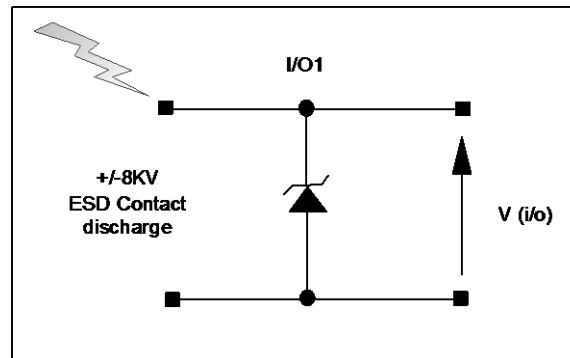


Figure 7. ESD Test Configuration

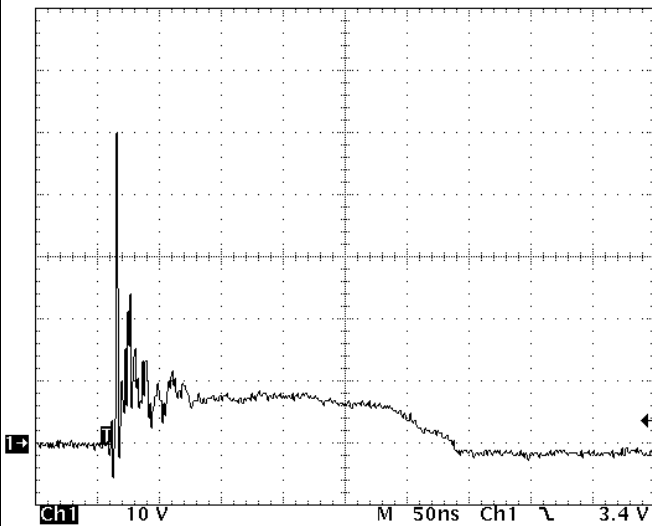


Figure 8. Clamped +8 kV ESD voltage waveform

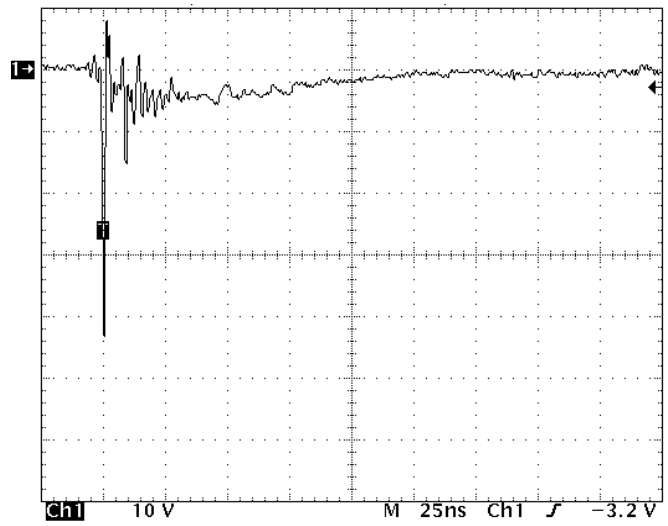


Figure 9. Clamped -8 kV ESD voltage waveform

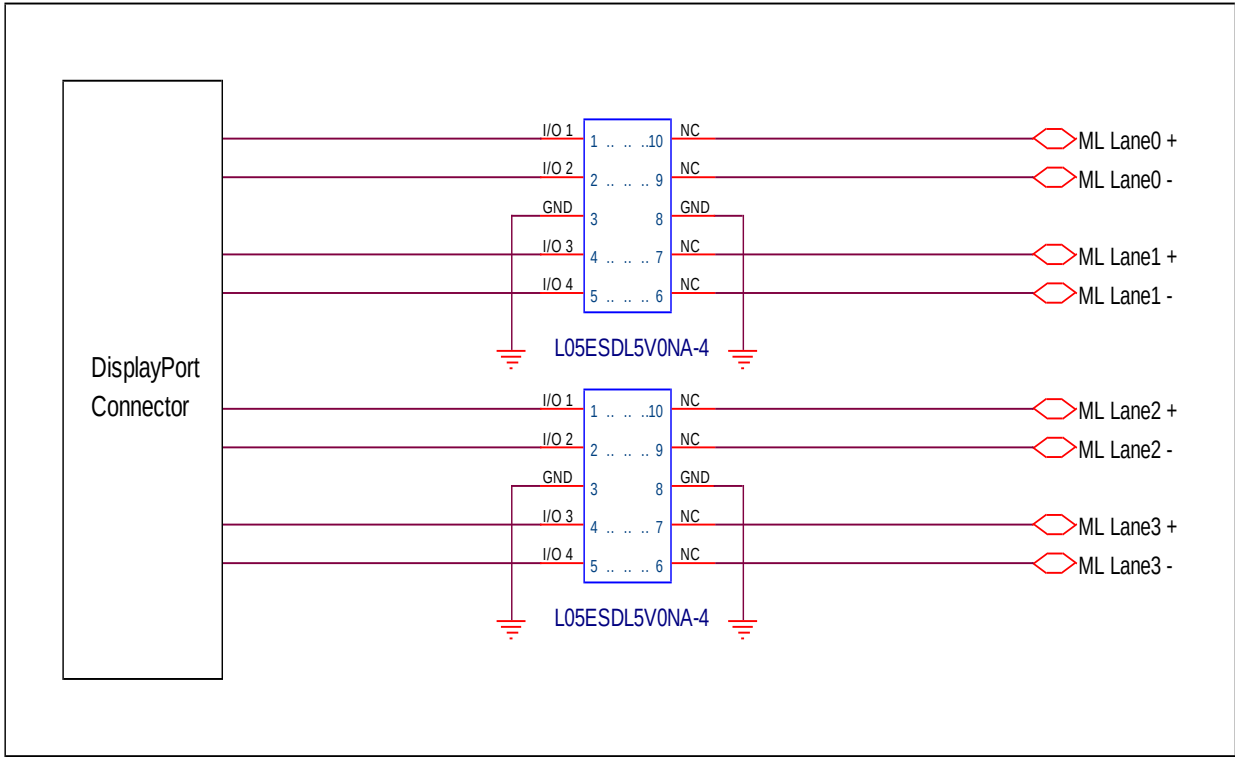


Figure 12. Display Port ESD Protection

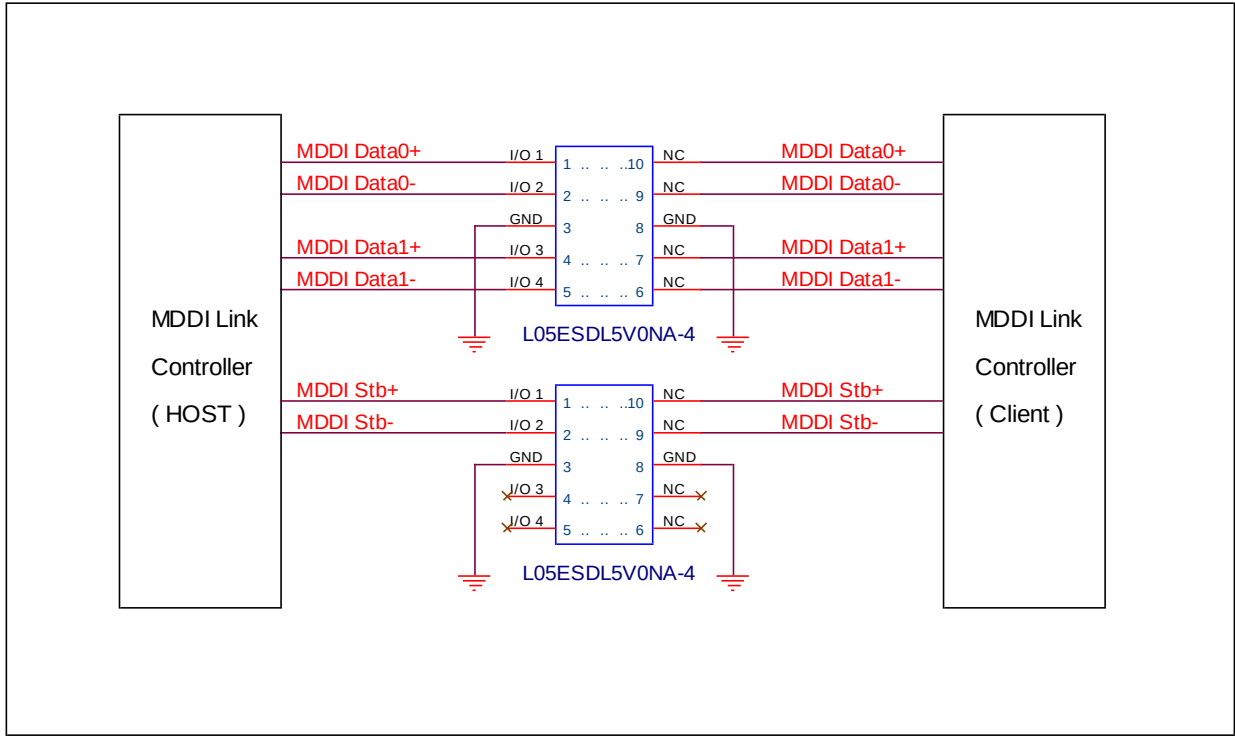


Figure 13. MDDI Interface ESD Protection

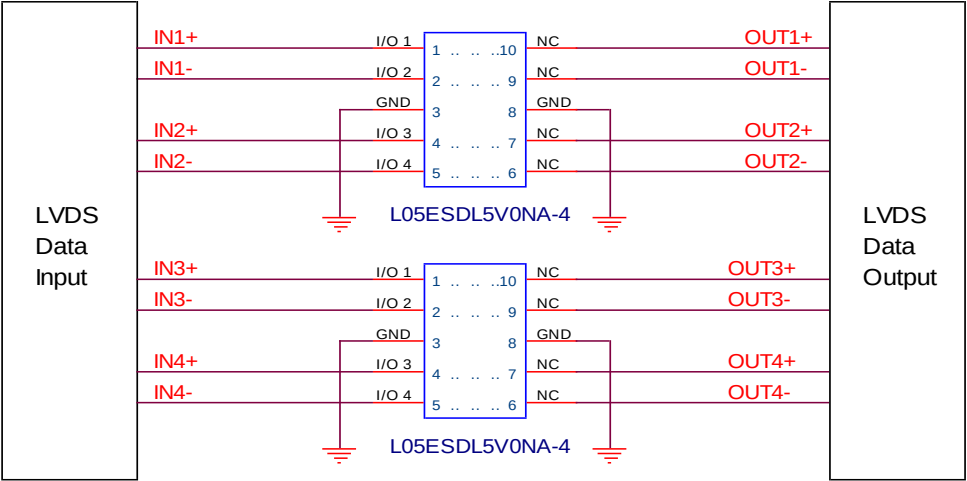


Figure 14. LVDS Interface ESD Protection

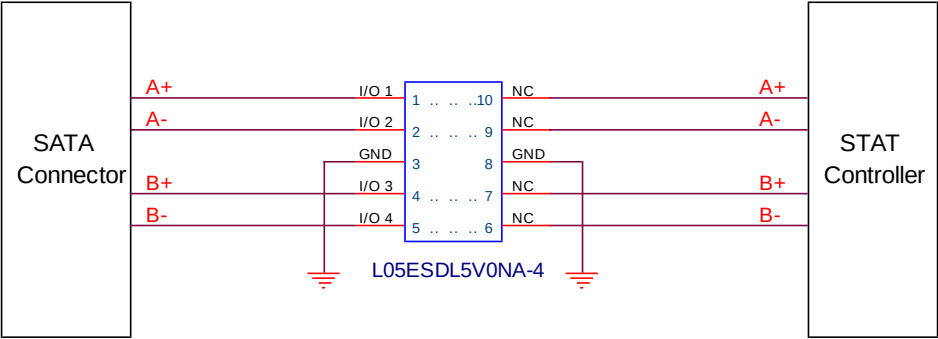
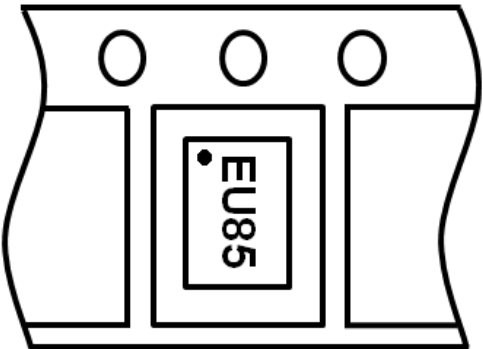


Figure 15. Serial ATA ESD Protection

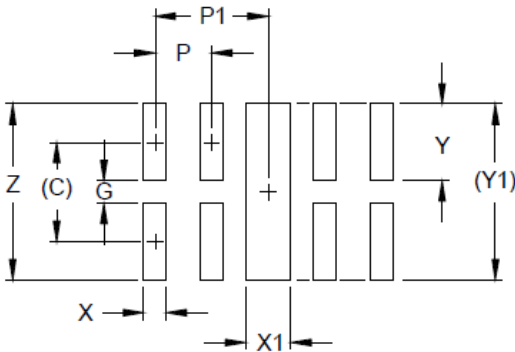
Marking and Orientation :



Packaging Information :

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L05ESDL5V0NA-4	3000	7	45000	90K/180K

SLP2510P8 Soldering Pad Layout :



DIM.	MILLIMETERS	INCHES
C	(0.875)	(0.034)
G	0.20	0.008
P	0.50	0.020
P1	1.00	0.039
X	0.20	0.008
X1	0.40	0.016
Y	0.68	0.027
Y1	(1.550)	(0.061)
Z	1.550	0.061

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