

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V, I_D = -1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.087	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.20	Ω	$V_{GS} = -10V, I_D = -11A$ ④
		—	—	0.22		$V_{GS} = -10V, I_D = -18A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
G_{fs}	Forward Transconductance	6.2	—	—	S	$V_{DS} = -15V, I_D = -11A$ ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	$V_{DS} = -80V, V_{GS} = 0V$
		—	—	-250		$V_{DS} = -80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Leakage Reverse	—	—	100		$V_{GS} = 20V$
Q_G	Total Gate Charge	—	—	60	nC	$I_D = -18A$
Q_{GS}	Gate-to-Source Charge	—	—	13		$V_{DS} = -50V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	35.2		$V_{GS} = -10V$
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	$V_{DD} = -50V$
t_r	Rise Time	—	—	85		$I_D = -11A$
$t_{d(off)}$	Turn-Off Delay Time	—	—	85		$R_G = 9.1\Omega$
t_f	Fall Time	—	—	65		$V_{GS} = -10V$
$L_S + L_D$	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	1400	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	600	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	200	—		$f = 1.0MHz$

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-18	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-72		
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	$T_J = 25^\circ\text{C}, I_S = -18A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	—	280	ns	$T_J = 25^\circ\text{C}, I_F = -18A, V_{DD} \leq -50V$
Q_{rr}	Reverse Recovery Charge	—	—	3.6	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	$^\circ\text{C}/W$
$R_{\theta CS}$	Case -to-Sink	—	0.21	—	
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	48	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -25V$, starting $T_J = 25^\circ\text{C}$, $L = 3.1mH$, Peak $I_L = -18A$, $V_{GS} = -10V$
- ③ $I_{SD} \leq -18A$, $di/dt \leq -100A/\mu s$, $V_{DD} \leq -100V$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$.

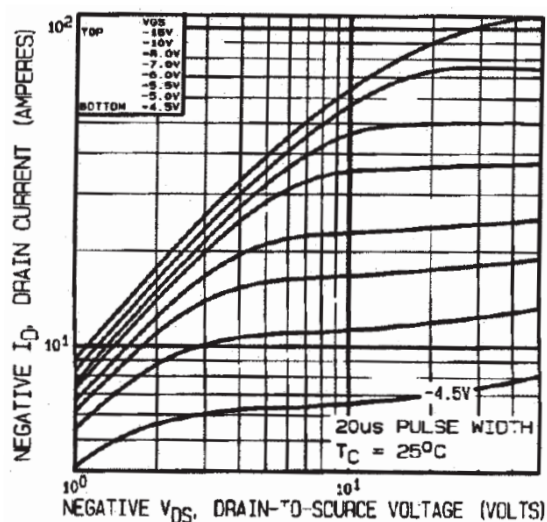


Fig 1. Typical Output Characteristics

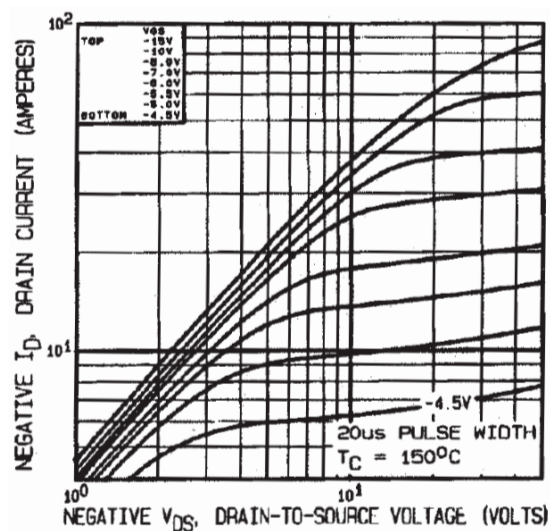


Fig 2. Typical Output Characteristics

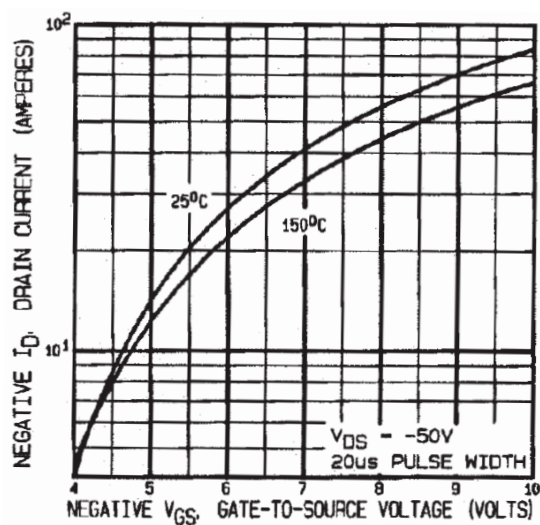


Fig 3. Typical Transfer Characteristics

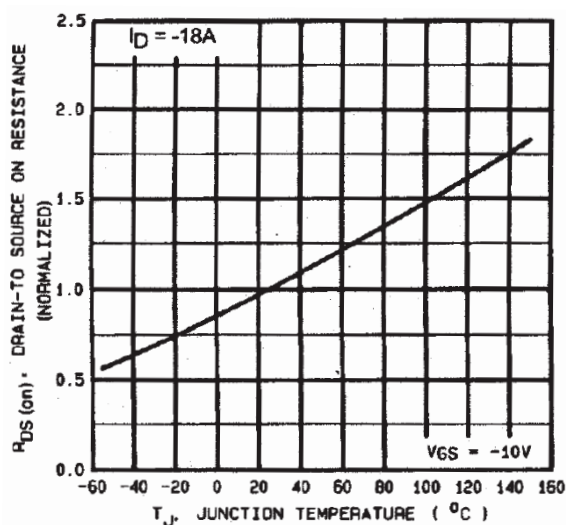


Fig 4. Normalized On-Resistance Vs. Temperature

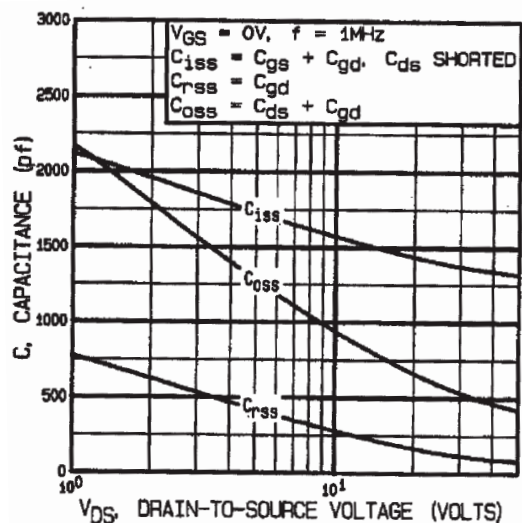


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

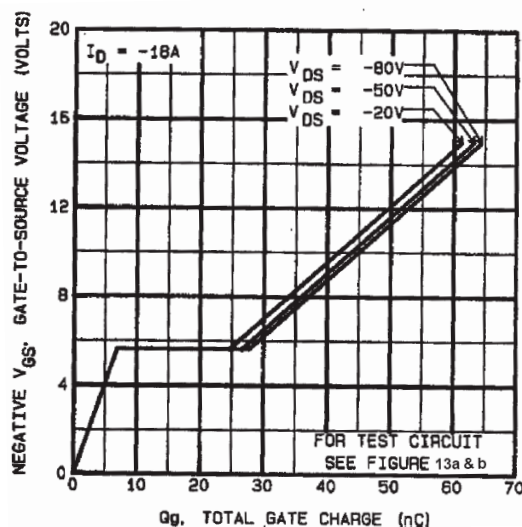


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

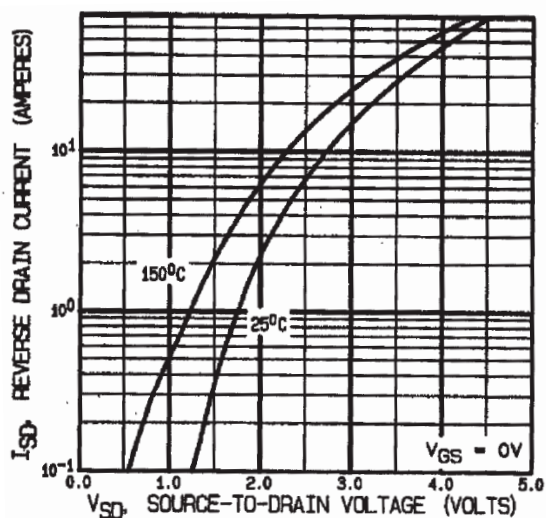


Fig 7. Typical Source-Drain Diode Forward Voltage

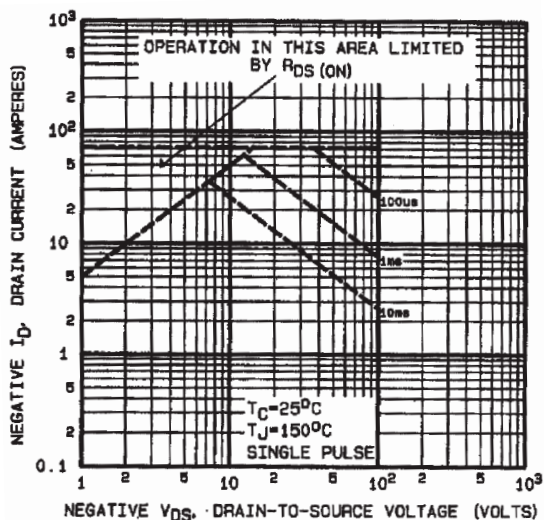


Fig 8. Maximum Safe Operating Area

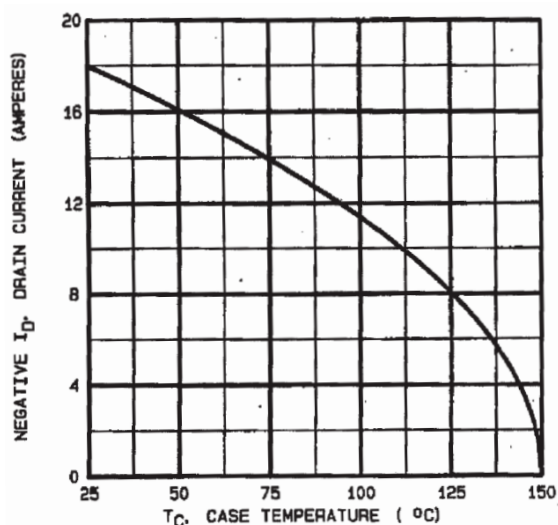


Fig 9. Maximum Drain Current Vs. Case Temperature

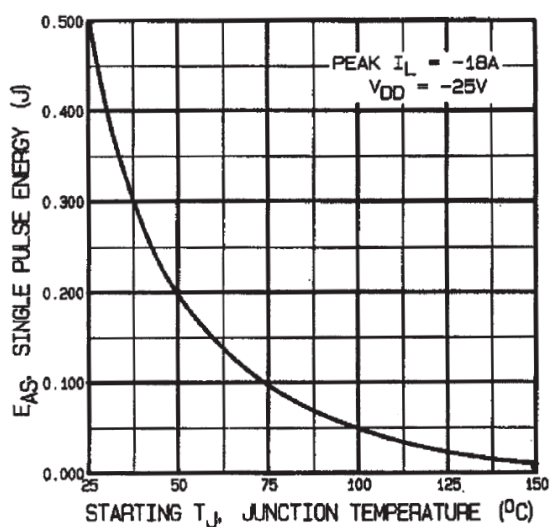


Fig 10. Maximum Avalanche Energy Vs. Drain Current

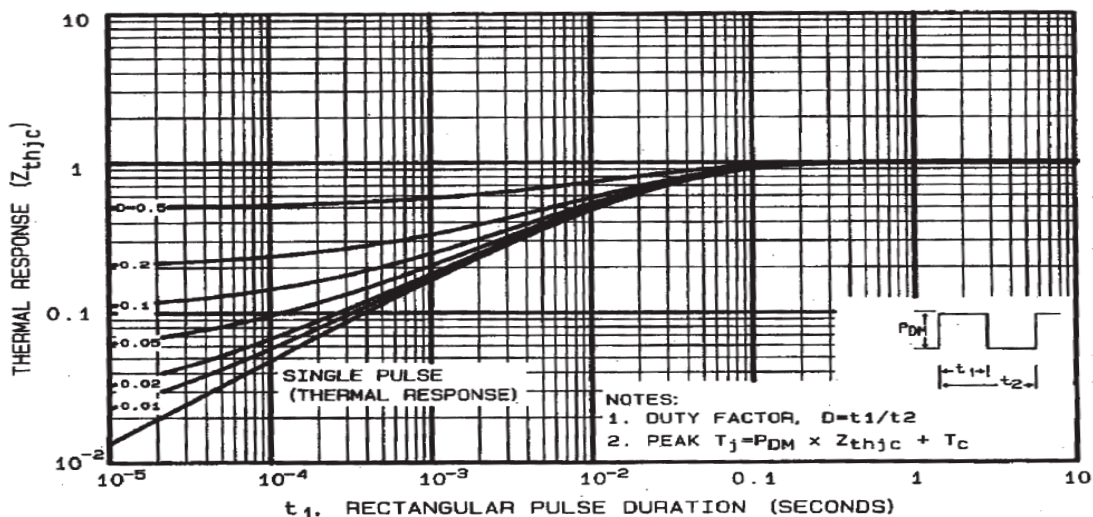


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

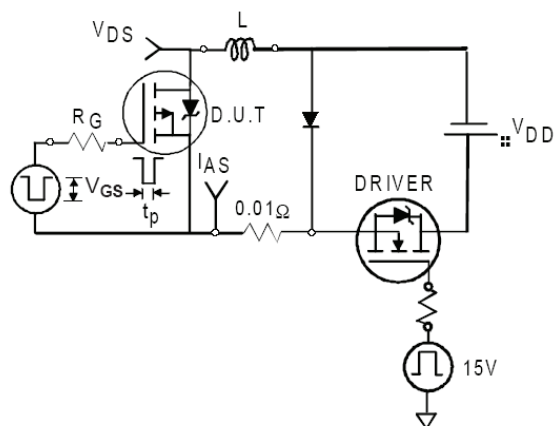


Fig 12a. Unclamped Inductive Test Circuit

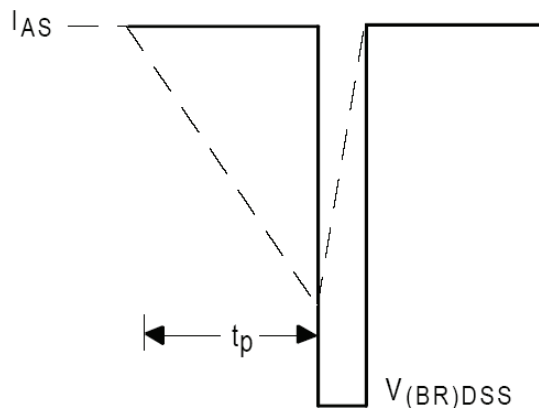


Fig 12b. Unclamped Inductive Waveforms

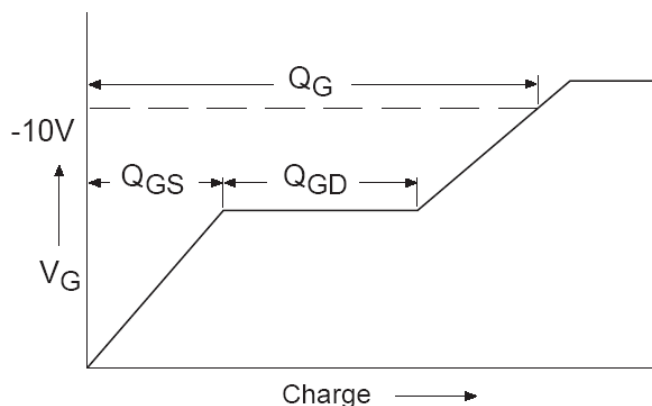


Fig 13a. Basic Gate Charge Waveform

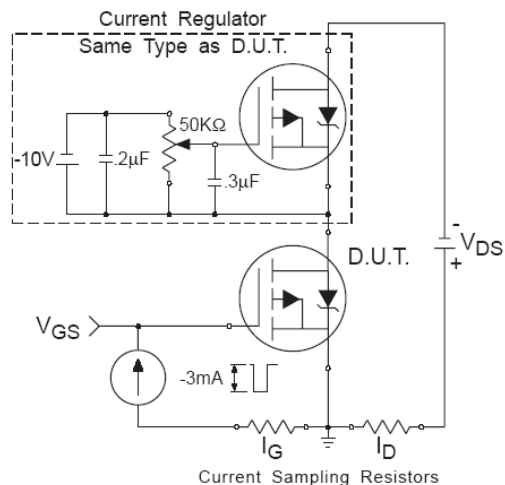


Fig 13b. Gate Charge Test Circuit

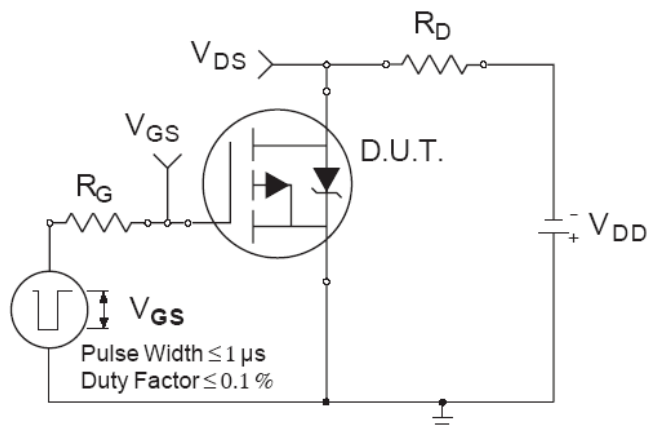


Fig 14a. Switching Time Test Circuit

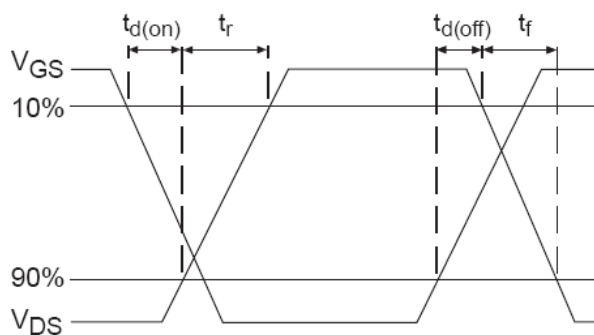
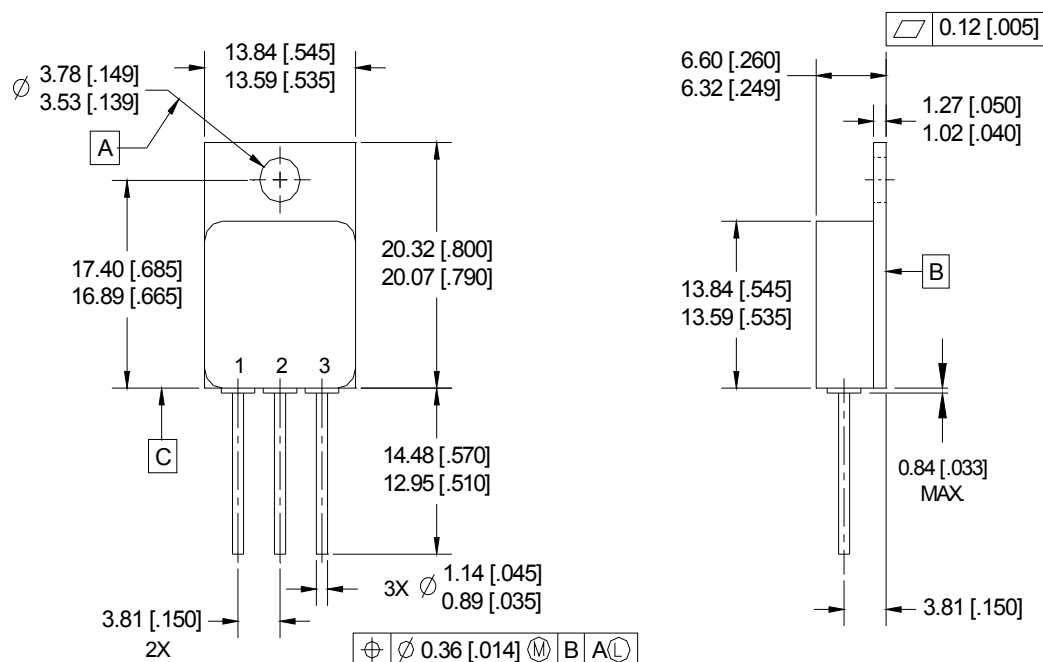


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions – TO-254AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

PIN ASSIGNMENTS

- 1 = DRAIN
2 = SOURCE
3 = GATE

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

IMPORTANT NOTICE

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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