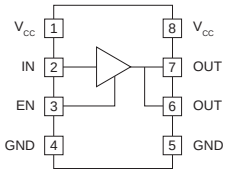
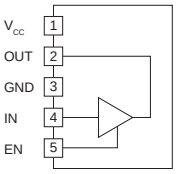
1 Specifications

1.1 Pin Configurations

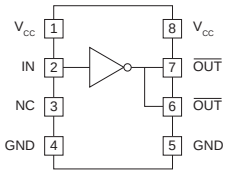
IXDD609 D2 / PI / SI / SIA



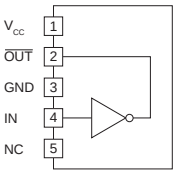
IXDD609 CI / YI



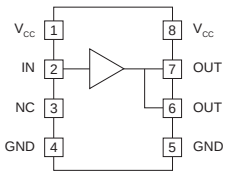
IXDI609 PI / SI / SIA



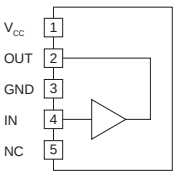
IXDI609 CI / YI



IXDN609 PI / SI / SIA



IXDN609 CI / YI



1.2 Pin Definitions

Pin Name	Description
IN	Logic Input
EN	Output Enable - Drive pin low to disable output, and force output to a high impedance state
OUT	Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
$\overline{OUT}$	Inverted Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
V_{CC}	Supply Voltage - Provides power to the device
GND	Ground - Common ground reference for the device
NC	Not connected

1.3 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V_{CC}	-0.3	40	V
Input Voltage	V_{IN}, V_{EN}	-5	V_{CC}+0.3	V
Output Current	I_{OUT}	-	±9	A
Junction Temperature	T_J	-55	+150	°C
Storage Temperature	T_{STG}	-65	+150	°C

Unless stated otherwise, absolute maximum electrical ratings are at 25°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Range	Units
Supply Voltage	V_{CC}	4.5 to 35	V
Operating Temperature Range	T_A	-40 to +125	°C

1.5 Electrical Characteristics: T_A = 25°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 35V (unless otherwise noted).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Voltage, High	4.5V ≤ V_{CC} ≤ 18V	V_{IH}	3.0	-	-	V
Input Voltage, Low	4.5V ≤ V_{CC} ≤ 18V	V_{IL}	-	-	0.8	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-	-	±10	µA
EN Input Voltage, High	IXDD609 only	V_{ENH}	2/3V_{CC}	-	-	V
EN Input Voltage, Low	IXDD609 only	V_{ENL}	-	-	1/3V_{CC}	
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	-	V
Output Voltage, Low	-	V_{OL}	-	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-100mA	R_{OH}	-	0.6	1	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=100mA	R_{OL}	-	0.4	0.8	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	-	±2	A
Rise Time	V_{CC}=18V, C_{LOAD}=10nF	t_r	-	22	35	ns
Fall Time	V_{CC}=18V, C_{LOAD}=10nF	t_f	-	15	25	
On-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{ondly}	-	40	60	
Off-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{offdly}	-	42	60	
Enable to Output-High Delay Time (IXDD609 Only)	V_{CC}=18V	t_{ENOH}	-	25	60	
Disable to High Impedance State Delay Time (IXDD609 Only)	V_{CC}=18V	t_{DOLD}	-	35	60	
Enable Pull-Up Resistor	-	R_{EN}	-	200	-	kΩ
Power Supply Current	V_{CC}=18V, V_{IN}=3.5V	I_{CC}	-	1	2	mA
	V_{CC}=18V, V_{IN}=0V		-	<1	10	µA
	V_{CC}=18V, V_{IN}=V_{CC}		-	<1	10	

1.6 Electrical Characteristics: T_A = - 40°C to +125°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 35V unless otherwise noted.

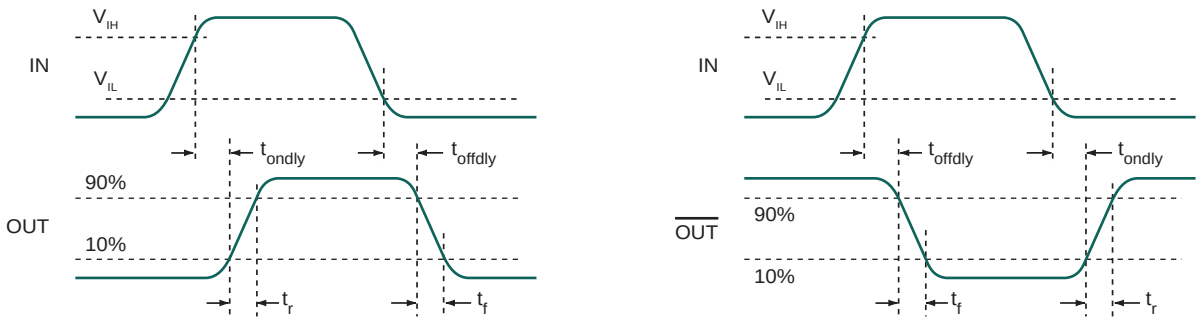
Parameter	Conditions	Symbol	Minimum	Maximum	Units
Input Voltage, High	4.5V ≤ V_{CC} ≤ 18V	V_{IH}	3.3	-	V
Input Voltage, Low	4.5V ≤ V_{CC} ≤ 18V	V_{IL}	-	0.65	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-	±10	µA
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	V
Output Voltage, Low	-	V_{OL}	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-100mA	R_{OH}	-	2	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=100mA	R_{OL}	-	1.5	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	±1	A
Rise Time	V_{CC}=18V, C_{LOAD}=10nF	t_r	-	40	ns
Fall Time	V_{CC}=18V, C_{LOAD}=10nF	t_f	-	30	
On-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{ondly}	-	75	
Off-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{offdly}	-	75	
Enable to Output-High Delay Time	IXDD609 only, V_{CC}=18V	t_{ENOH}	-	75	
Disable to High Impedance State Delay Time	IXDD609 only, V_{CC}=18V	t_{DOLD}	-	75	
Power Supply Current	V_{CC}=18V, V_{IN}=3.5V	I_{CC}	-	2.5	mA
	V_{CC}=18V, V_{IN}=0V		-	150	µA
	V_{CC}=18V, V_{IN}=V_{CC}		-	150	

1.7 Thermal Characteristics

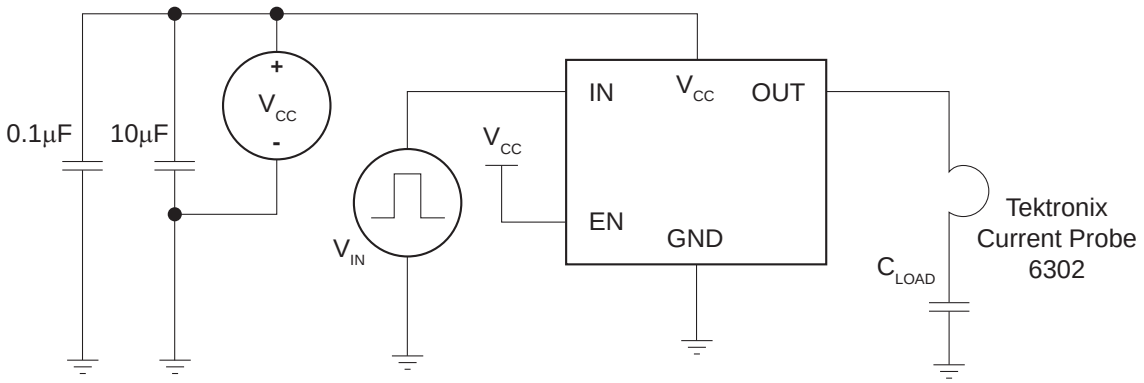
Package	Parameter	Symbol	Rating	Units
D2 (8-Pin DFN)	Thermal Impedance, Junction-to-Ambient	θ_{JA}	35	°C/W
CI (5-Pin TO-220)			36	
PI (8-Pin DIP)			125	
SI (8-Pin Power SOIC)			85	
SIA (8-Pin SOIC)			120	
YI (5-Pin TO-263)			46	
CI (5-Pin TO-220)	Thermal Impedance, Junction-to-Case	θ_{JC}	3	°C/W
SI (8-Pin Power SOIC)			10	
YI (5-Pin TO-263)			2	

2 IXD_609 Performance

2.1 Timing Diagrams

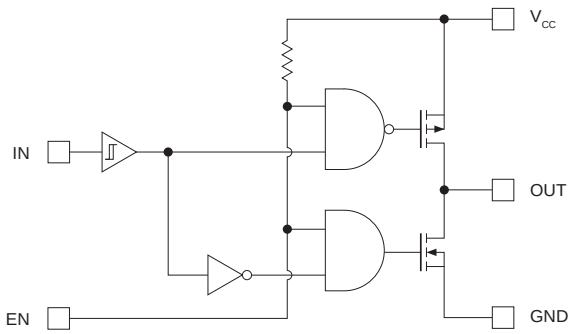


2.2 Characteristics Test Diagram



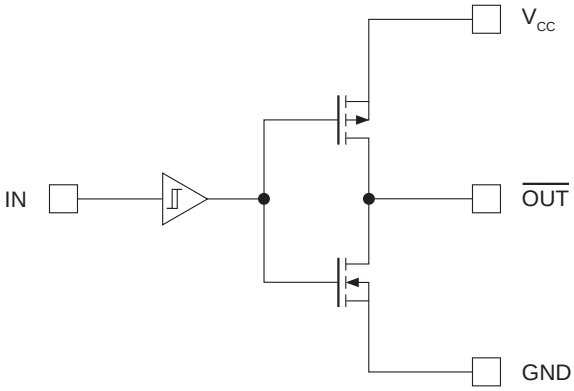
3 Block Diagrams & Truth Tables

3.1 IXDD609



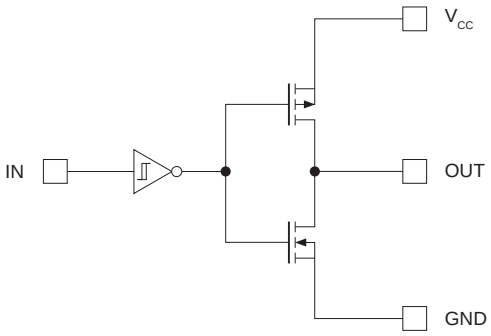
IN	EN	OUT
0	1 or open	0
1	1 or open	1
x	0	Z

3.2 IXDI609



IN	$\overline{OUT}$
0	1
1	0

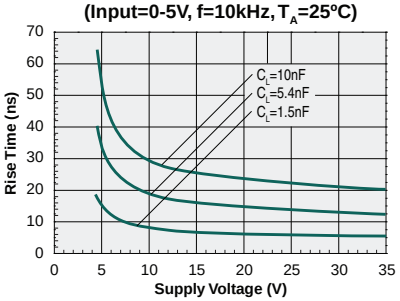
3.3 IXDN609



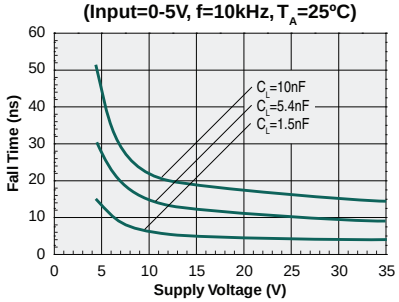
IN	OUT
0	0
1	1

4 Typical Performance Characteristics

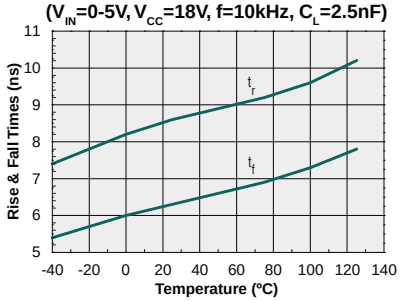
Rise Time vs. Supply Voltage
(Input=0-5V, f=10kHz, T_A=25ºC)



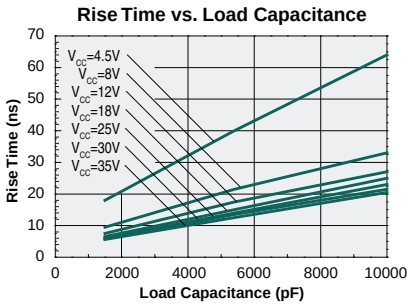
Fall Time vs. Supply Voltage
(Input=0-5V, f=10kHz, T_A=25ºC)



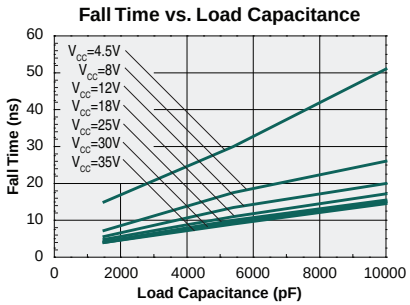
Rise and Fall Times vs. Temperature
(V_{IN}=0-5V, V_{CC}=18V, f=10kHz, C_L=2.5nF)



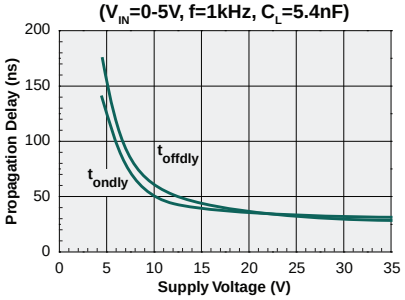
Rise Time vs. Load Capacitance



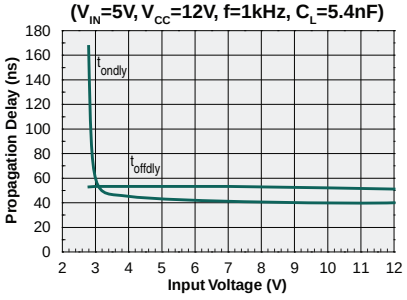
Fall Time vs. Load Capacitance



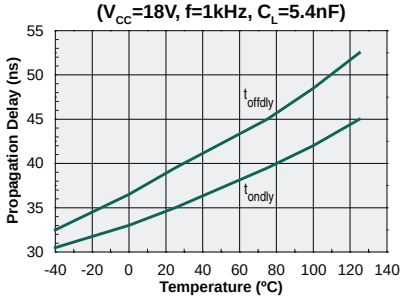
Propagation Delay vs. Supply Voltage
(V_{IN}=0-5V, f=1kHz, C_L=5.4nF)



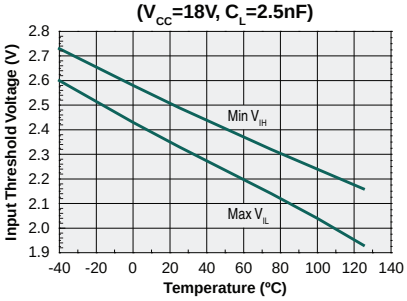
Propagation Delay vs. Input Voltage
(V_{IN}=5V, V_{CC}=12V, f=1kHz, C_L=5.4nF)



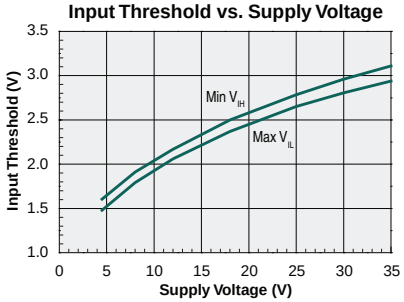
Propagation Delay
vs. Temperature
(V_{CC}=18V, f=1kHz, C_L=5.4nF)



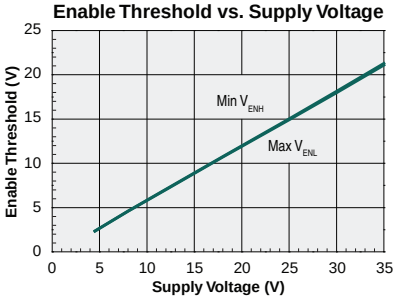
Input Threshold Voltage
vs. Temperature
(V_{CC}=18V, C_L=2.5nF)



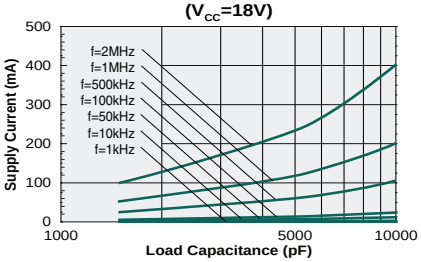
Input Threshold vs. Supply Voltage



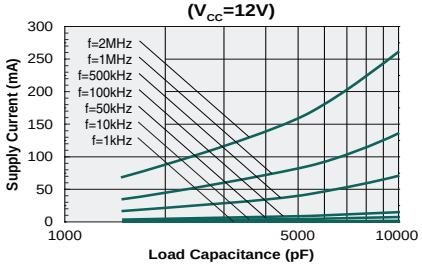
Enable Threshold vs. Supply Voltage



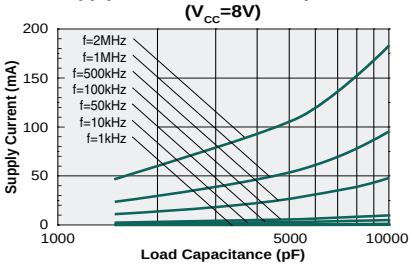
Supply Current vs. Load Capacitance (V_{CC}=18V)



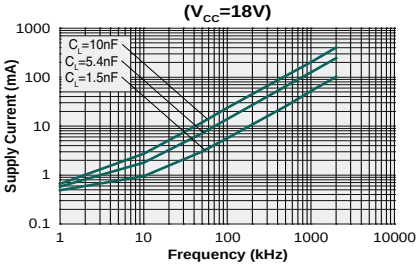
Supply Current vs. Load Capacitance (V_{CC}=12V)



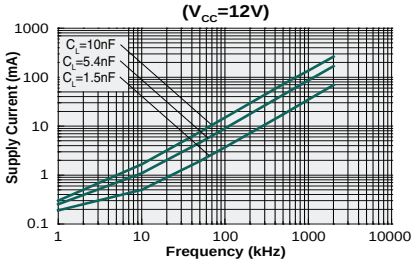
Supply Current vs. Load Capacitance (V_{CC}=8V)



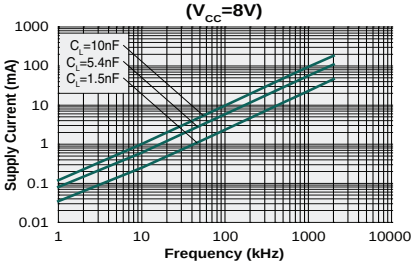
Supply Current vs. Frequency (V_{CC}=18V)



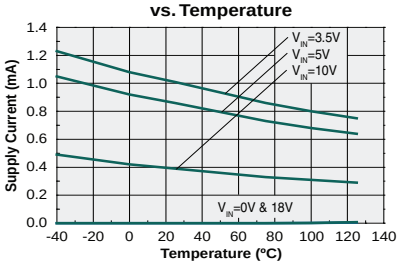
Supply Current vs. Frequency (V_{CC}=12V)



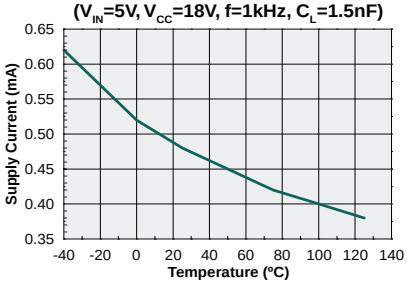
Supply Current vs. Frequency (V_{CC}=8V)



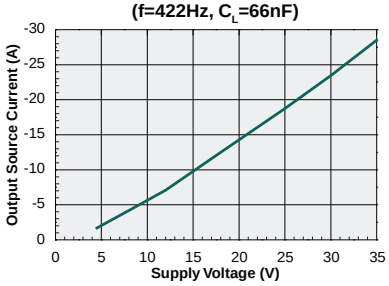
Quiescent Supply Current vs. Temperature



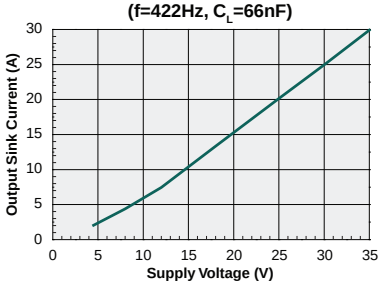
Dynamic Supply Current vs. Temperature (V_{IN}=5V, V_{CC}=18V, f=1kHz, C_L=1.5nF)



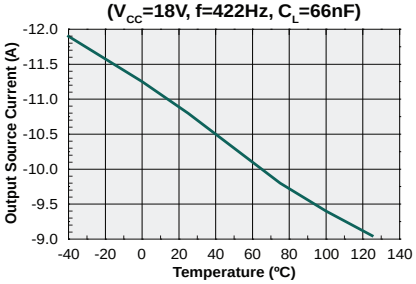
Output Source Current vs. Supply Voltage (f=422Hz, C_L=66nF)



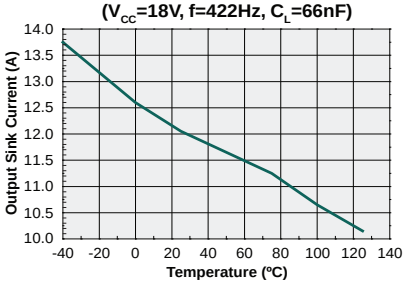
Output Sink Current vs. Supply Voltage (f=422Hz, C_L=66nF)



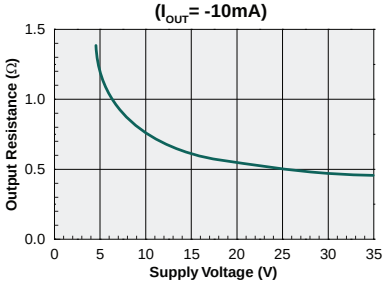
Output Source Current vs. Temperature (V_{CC}=18V, f=422Hz, C_L=66nF)



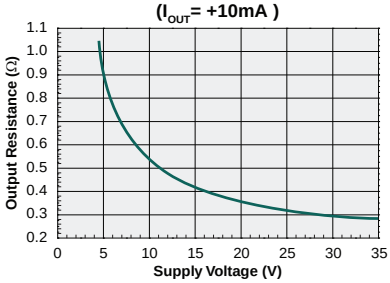
Output Sink Current vs. Temperature (V_{CC}=18V, f=422Hz, C_L=66nF)



High State Output Resistance vs. Supply Voltage (I_{OUT}= -10mA)



Low State Output Resistance vs. Supply Voltage (I_{OUT}= +10mA)



5 Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IXD_609 All Versions except IXD_609YI	MSL 1
IXD_609YI	MSL 3

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be (T_C - 5)ºC or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of J-STD-020 must be observed.

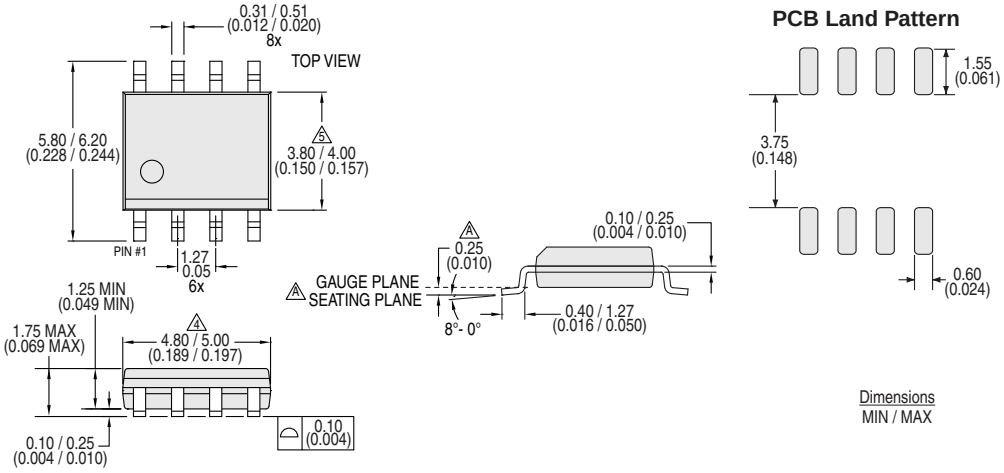
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Maximum Cycles
IXD_609CI	245°C for 30 seconds	30 seconds	1
IXD_609YI	245°C for 30 seconds	30 seconds	3
IXD_609PI	250°C for 30 seconds	30 seconds	3
IXD_609SI / IXD_609SIA / IXD_609D2	260°C for 30 seconds	30 seconds	3

5.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

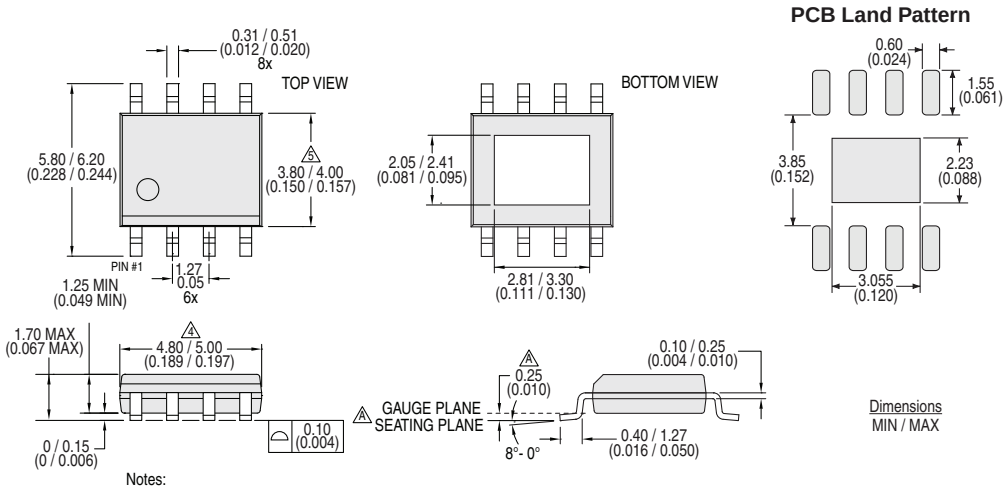
5.5 Mechanical Dimensions

5.5.1 SIA (8-Pin SOIC)



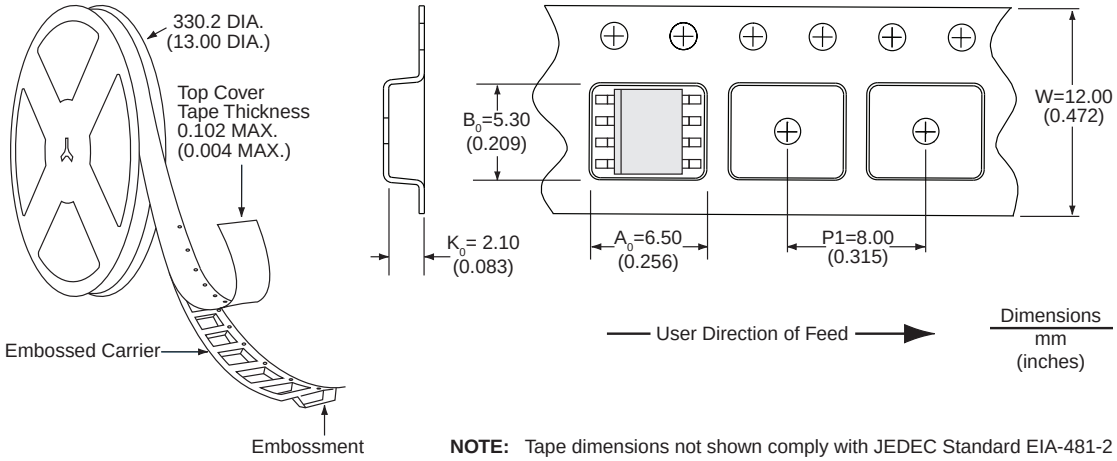
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation AA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. Lead thickness includes plating.

5.5.2 SI (8-Pin Power SOIC with Exposed Metal Back)



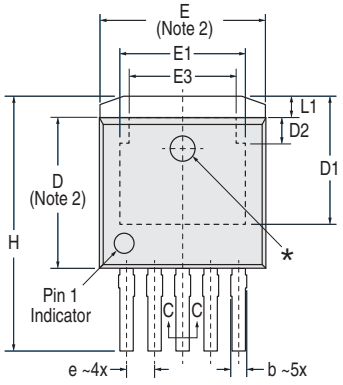
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation BA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. The exposed metal pad on the back of the package should be connected to GND. It is not suitable for carrying current.
7. Lead thickness includes plating.

5.5.3 Tape & Reel Information for SI and SIA Packages



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

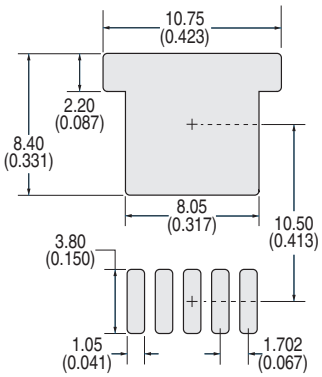
5.5.4 YI (5-Pin TO-263)

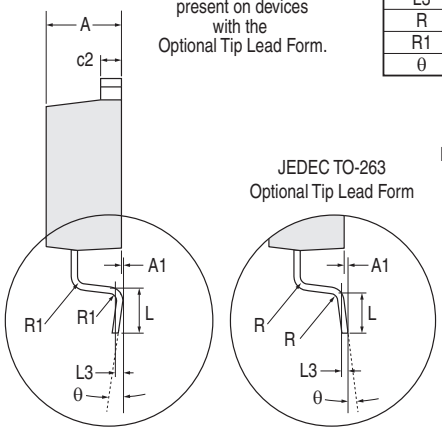


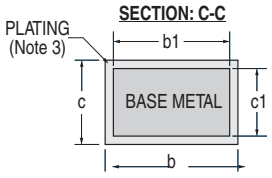
*Circular feature will be present on devices with the Optional Tip Lead Form.

SYMBOL	MM		INCH	
	MIN	MAX	MIN	MAX
A	4.064	4.826	0.160	0.190
A1	0.000	0.254	0.000	0.010
b	0.508	0.991	0.020	0.039
b1	0.508	0.889	0.020	0.035
c	0.381	0.737	0.015	0.029
c1	0.381	0.584	0.015	0.023
c2	1.143	1.651	0.045	0.065
D	8.382	9.652	0.330	0.380
D1	6.858	7.700	0.270	0.303
D2	1.358	1.562	0.053	0.062
E	9.652	10.668	0.380	0.420
E1	6.223	8.000	0.245	0.315
E3	5.092	6.869	0.200	0.270
e	1.702 BSC		0.067 BSC	
H	14.605	15.875	0.575	0.625
L	1.778	2.794	0.070	0.110
L1	1.000	1.676	0.039	0.066
L3	0.254 BSC		0.010 BSC	
R	0.460 TYP		0.018 TYP	
R1	0.506 TYP		0.02 TYP	
θ	-	8°	-	8°

Recommended PCB Pattern

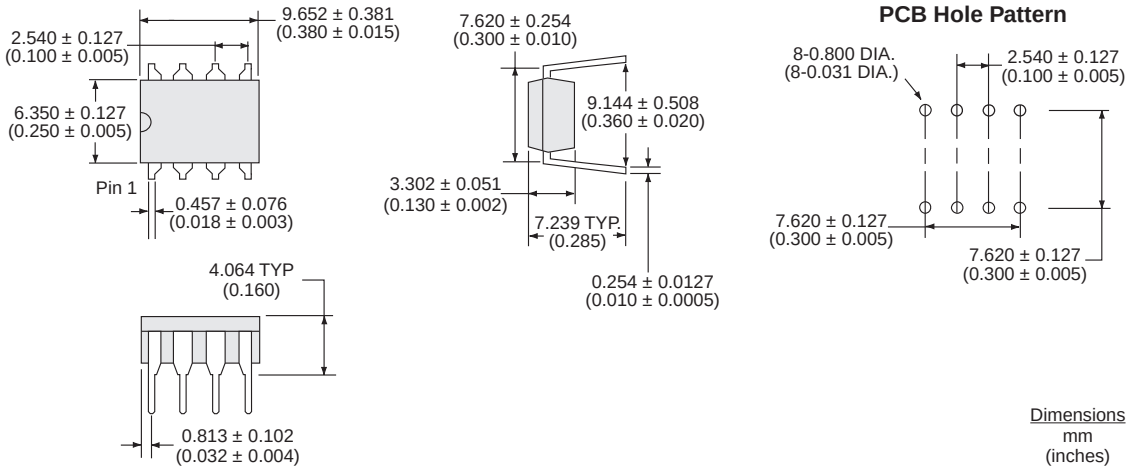




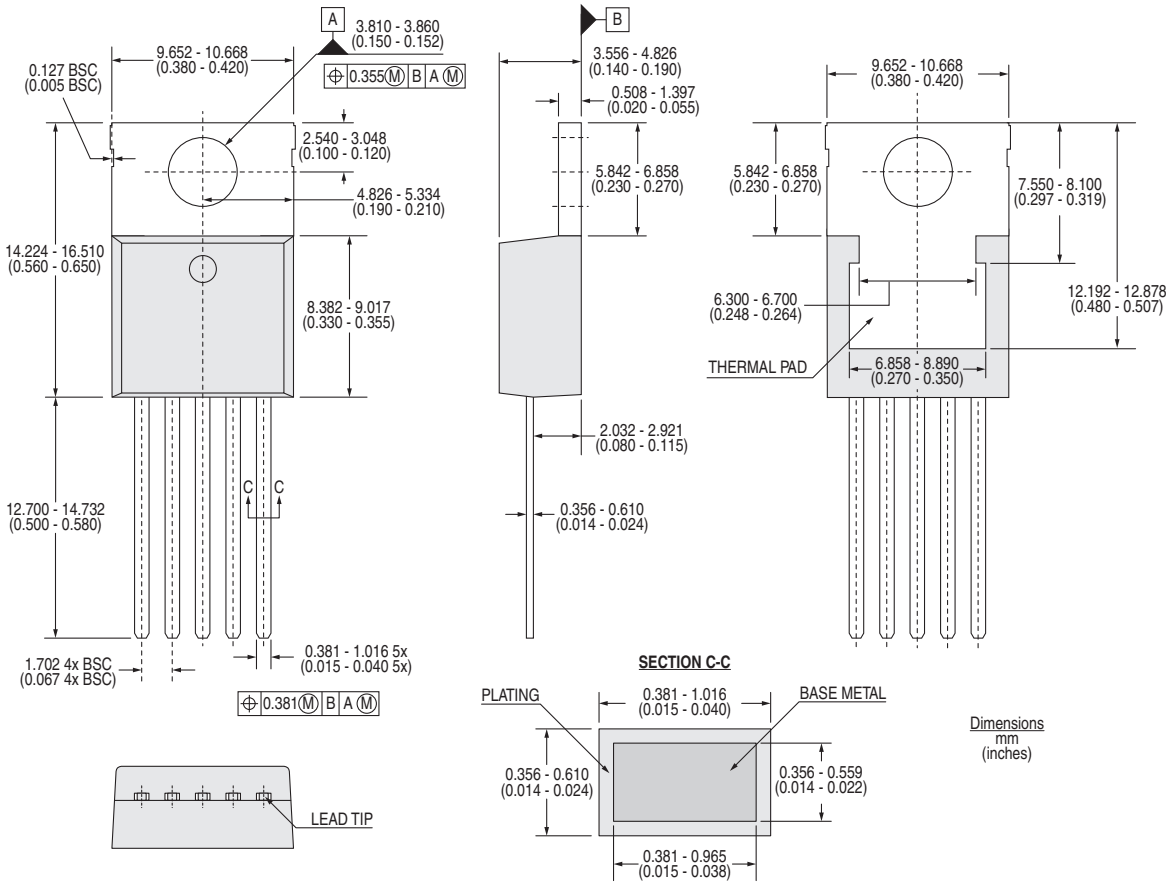


NOTES:
1. Reference JEDEC TO-263 Type "BA".
2. Dimension does not include mold flash; mold flash shall not exceed 0.127mm (0.005 inch) per side.
3. Minimum plating: 1000 microinches.
4. Controlling dimension: millimeters.

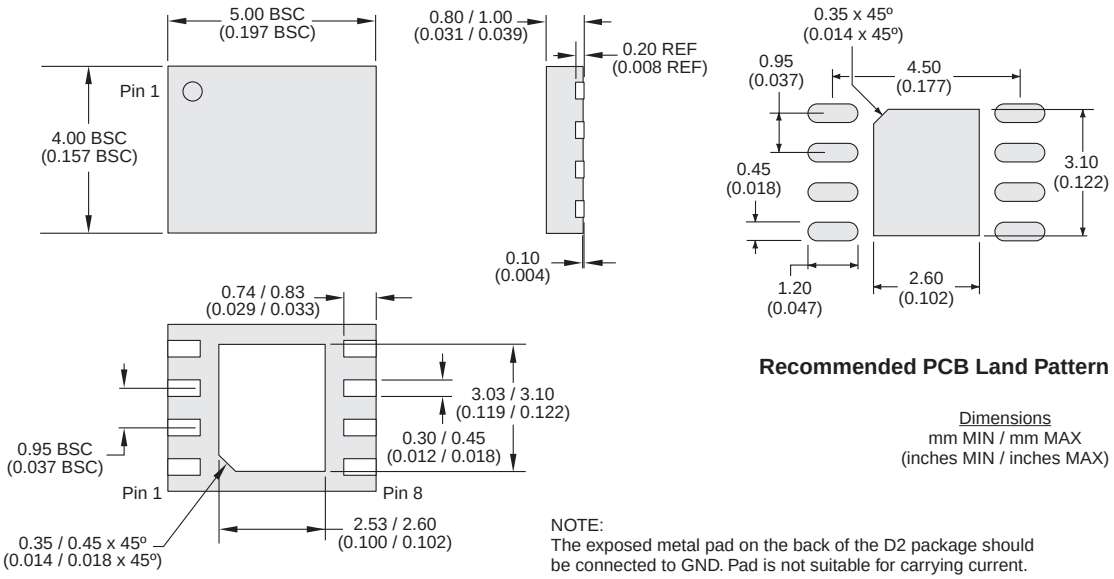
5.5.5 PI (8-Pin DIP)



5.5.6 CI (5-Pin TO-220)



5.5.7 D2 (8-Pin DFN)

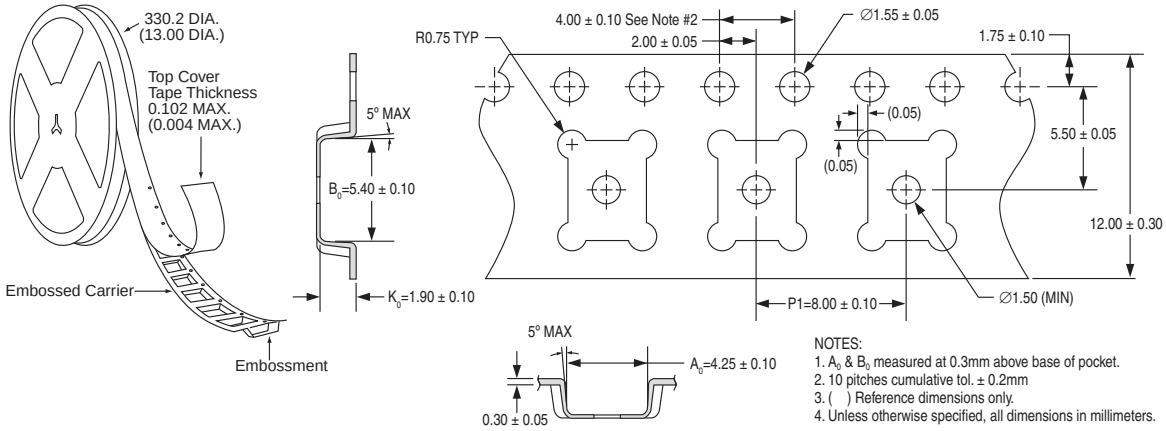


Recommended PCB Land Pattern

Dimensions
mm MIN / mm MAX
(inches MIN / inches MAX)

NOTE:
The exposed metal pad on the back of the D2 package should be connected to GND. Pad is not suitable for carrying current.

5.5.8 Tape & Reel Information for D2 Package



NOTES:
1. A_0 & B_0 measured at 0.3mm above base of pocket.
2. 10 pitches cumulative tol. ± 0.2mm
3. ( ) Reference dimensions only.
4. Unless otherwise specified, all dimensions in millimeters.

For additional information please visit our website at: www.ixysic.com

Specification: DS-IXD_609-R09

10/25/2017