

Revision History

Version	ECR	Date	Changes and/or Modifications
0	149329	February 2008	Update sections throughout.
A	147549	October 2007	New document.

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1. Pin Out

1.1 Pin Assignment

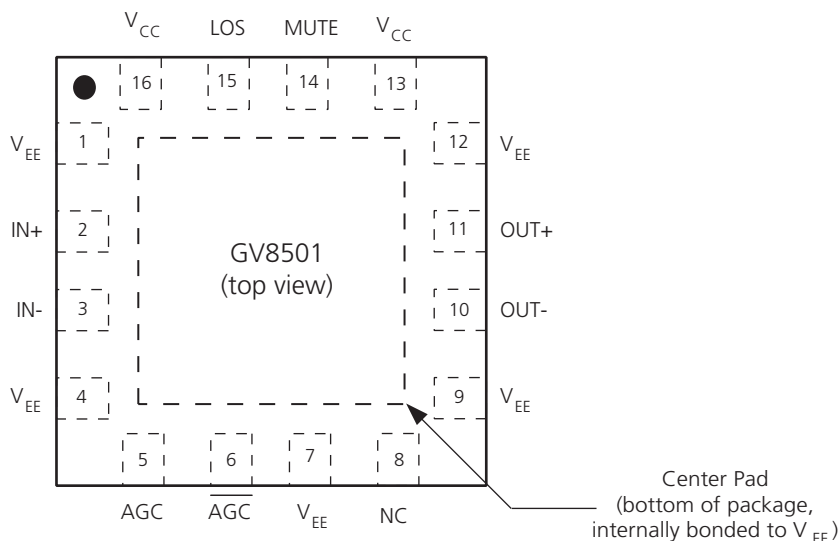


Figure 1-1: GV8501 16-Pin QFN

1.2 Pin Descriptions

Table 1-1: GV8501 Pin Descriptions

Pin Number	Name	Type	Description
1, 4, 7, 9, 12	V_{EE}	Power	Most negative power supply. Connect to GND.
2, 3	IN+, IN-	Input	Differential input.
5, 6	AGC, $\overline{AGC}$	–	External AGC capacitor.
8	NC	–	No connect.
10, 11	OUT+, OUT-	Output	Differential output.
13, 16	V_{CC}	Power	Most positive power supply. Connect to +3.3V DC.
14	MUTE	Input	Control Signal Input: Controls output behaviour on OUT+ and OUT-. Refer to 4.2 Mute and Loss of Signal .
15	LOS	Output	Loss Of Signal. Refer to 4.2 Mute and Loss of Signal .
–	Center Pad	Power	Internally bonded to V_{EE} .

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.3V to +3.6V DC
Input ESD Voltage	4kV
Storage Temperature Range	-50°C < T _s < 125°C
Input Voltage Range (any input)	-0.3 to (V _{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Solder Reflow Temperature	260°C

Note: Absolute Maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicate in AC/DC Electrical Characteristics sections, is not implied.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	V _{CC}	–	3.135	3.3	3.465	V	±5%
Power Consumption	P _D	T _A = 25°C	–	215	–	mW	
Supply Current	I _s	T _A = 25°C	–	65	–	mA	
Output Common Mode Voltage	V _{CMOUT}	T _A = 25°C	–	V _{CC} - ΔV _{OUT} /2	–	V	
Input Common Mode Voltage	V _{CMIN}	T _A = 25°C	–	1.75	–	V	
LOS Output Voltage	V _{LOS(OH)}	Carrier not present	2.4	–	–	V	
	V _{LOS(OL)}	Carrier present	–	–	0.4	V	
Mute Input Voltage Required to Force Outputs to Mute	V _{Mute}	Min to Mute	2.0	–	–	V	
Mute Input Voltage Required to Force Outputs Active	V _{Mute}	Max to Activate	–	–	0.8	V	

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

$V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$, PRBS2⁷-1, GV8500 as source, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	DR	–	0.25	–	3.4	Gb/s	
Serial Input Clock Rate	–	HDMI Clock, 1/10th Data Rate	25	–	340	MHz	
Input Voltage Swing	ΔV_{IN}	Measured prior to cable loss	700	800	900	mV _{p-p}	
Output Voltage Swing	ΔV_{OUT}	100 Ω load, $T_A = 25^\circ C$, differential	550	750	1050	mV _{p-p}	
Additive Jitter	–	1 - 40dB cable loss at 1.7GHz	–	0.3	–	UI	1
Output Rise/Fall Time	–	20% - 80%	40	80	220	ps	
Input Return Loss	–	–	TBD	TBD	–	dB	
Input Resistance	–	single ended	–	1.52	–	k Ω	
Input Capacitance	–	single ended	–	1	–	pF	
Output Resistance	–	single ended	–	50	–	Ω	

1. Based on characterization data using the recommended applications circuit.

3. Input / Output Circuits

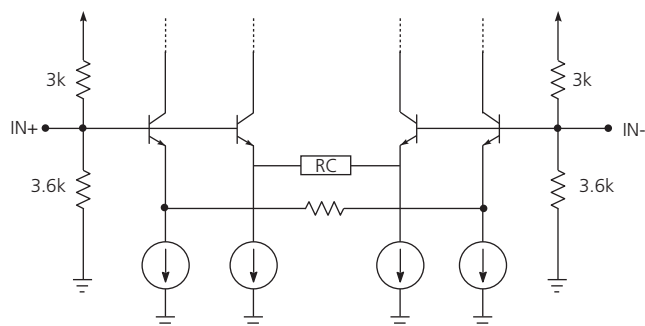


Figure 3-1: Differential Input Stage (IN+/IN-)

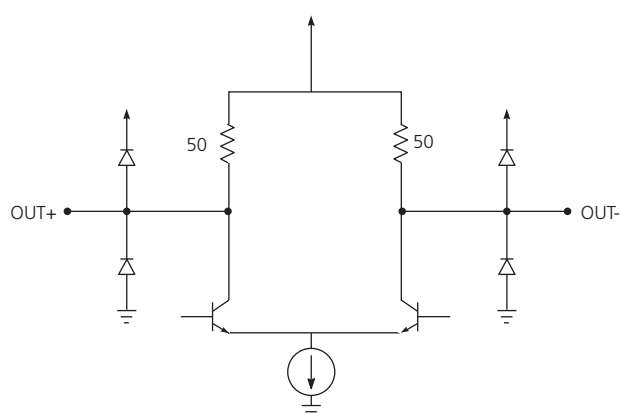


Figure 3-2: Differential Output Stage (OUT+/OUT-)

4. Detailed Description

The GV8501 is a high-speed BiCMOS IC designed to recover HDMI high-speed data and clock signals, and DisplayPort high-speed data signals after transmission over lossy media.

4.1 Serial Digital Inputs

AC coupling of the inputs is recommended, as the IN+ and IN- inputs are internally biased at approximately 1.8V.

4.2 Mute and Loss of Signal

The GV8501 has a MUTE input pin that allows the application interface to mute the serial digital output at any time. Set the MUTE pin HIGH to mute OUT+ and OUT-.

A Loss Of Signal output pin (LOS) indicates the absence of a valid signal at the input of the GV8501.

Note: This pin, MUTE, may be connected directly to the LOS pin to allow mute on loss of carrier.

Table 4-1: Mute Input Table

Mute	Function
0	OUT+ and OUT- operate normally
1	OUT+ and OUT- are forced to a steady state

Table 4-2: Loss of Signal Output Table

LOS	Input Status
0	Valid Input on IN+, IN- pins
1	Input is not valid

5. Application Information

This is a recommended circuit from one of Gennum's Reference Design Kits (RDKs).

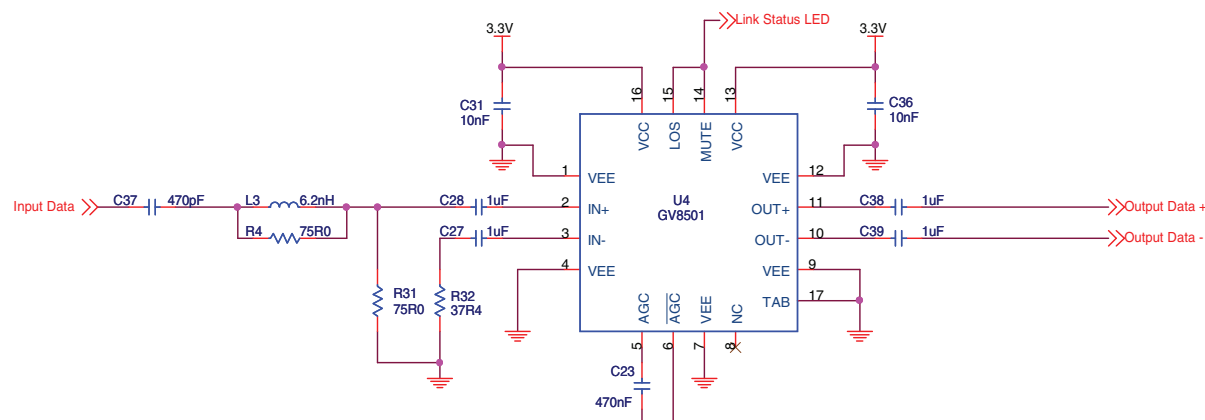


Figure 5-1: Recommended Circuit

See RDK documents for more information.

6. Package & Ordering Information

6.1 Package Dimensions

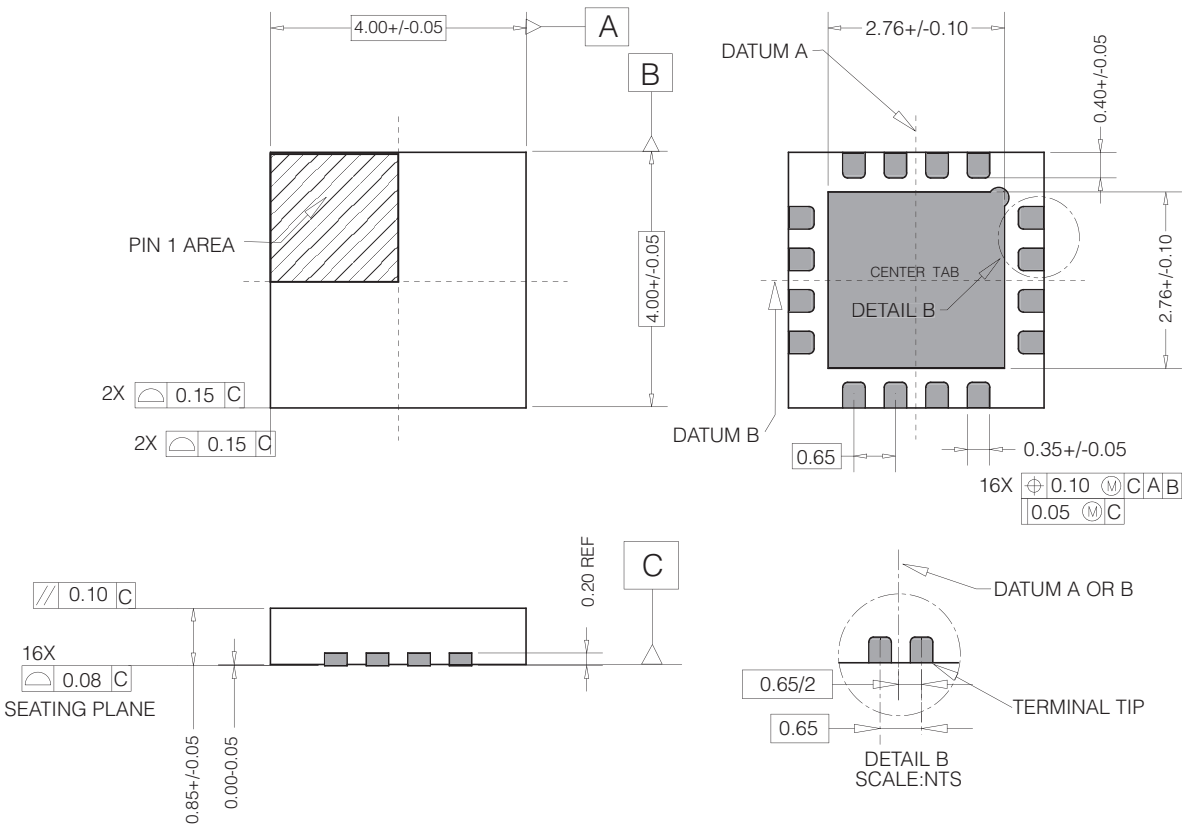


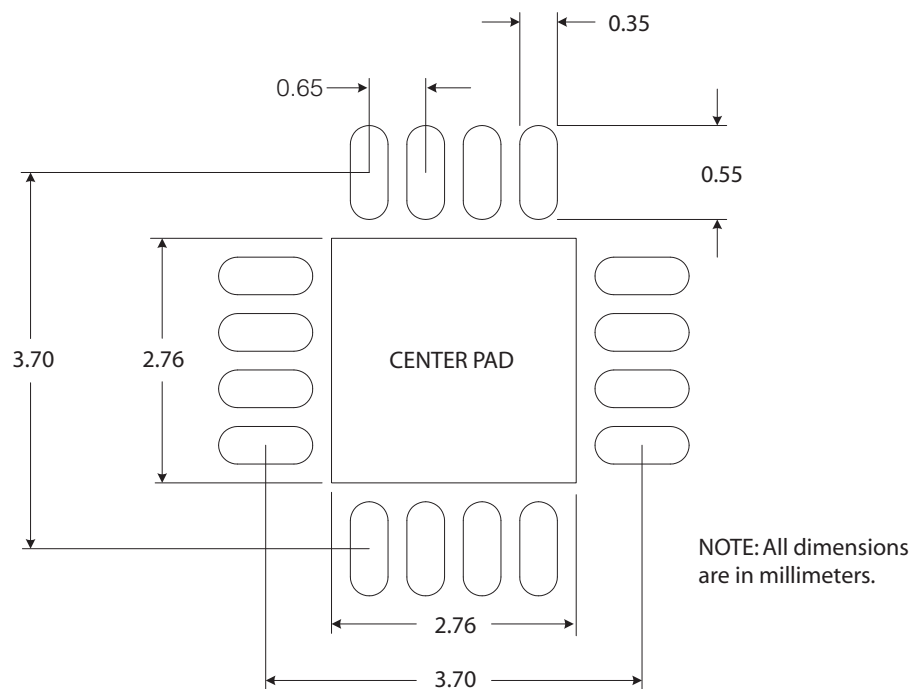
Figure 6-1: GV8501 Package Dimensions

6.2 Packaging Data

Table 6-1: Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, ψ	11.0°C/W
Pb-free and RoHS compliant	Yes

6.3 Recommended PCB Footprint



Note: Suggested dimensions only.
Final dimensions should conform to
customer design rules and process
optimizations.

Figure 6-2: GV8501 PCB Footprint

The Center Pad should be connected to the most negative power supply plane for analog circuitry in the device (V_{EE}) by a minimum of 5 vias.

6.4 Marking Diagram



Figure 6-3: GV8501 Marking Diagram

6.5 Solder Reflow Profile

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 6-4.

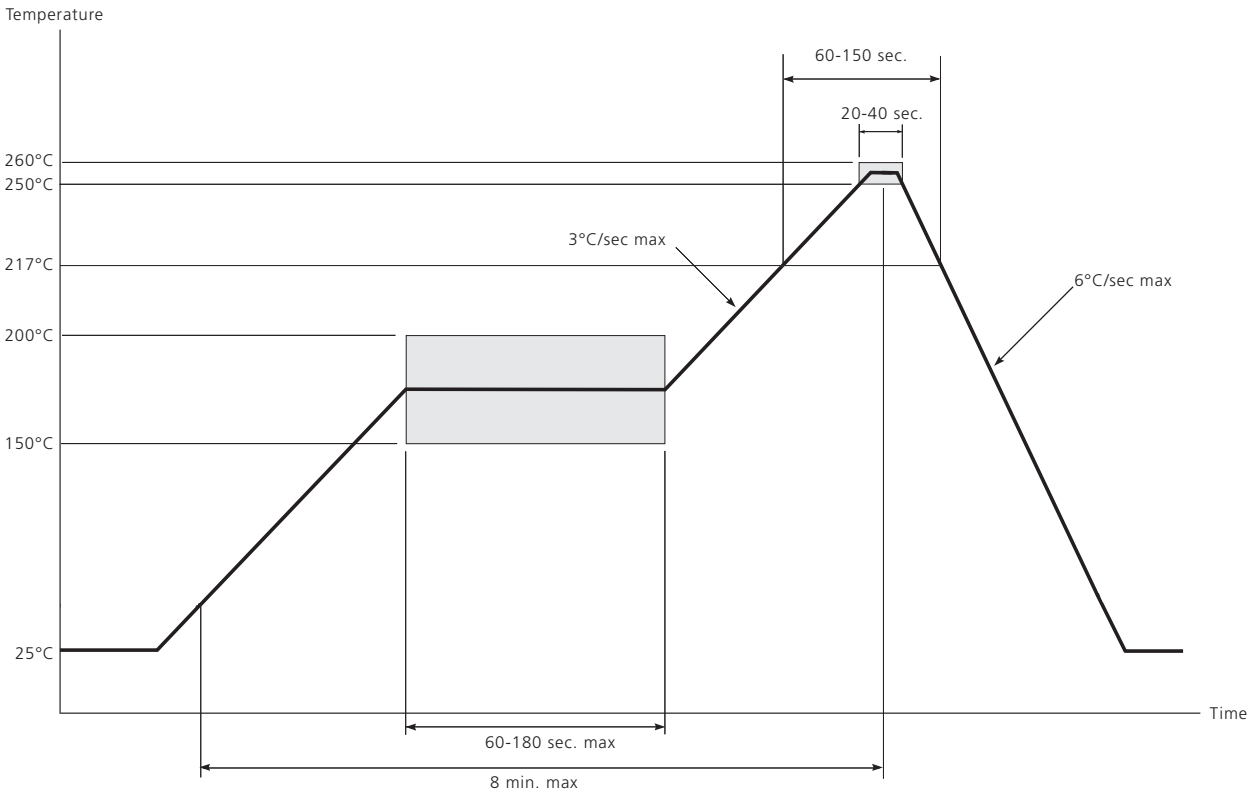


Figure 6-4: Maximum Pb-free Solder Reflow Profile (Preferred)

6.6 Ordering Information

Part Number	Package	Temperature Range
GV8501-CNE3	16-pin QFN	0°C to 70°C

CAUTION

ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

**DOCUMENT IDENTIFICATION
PRELIMINARY DATA SHEET**

The product is in a preproduction phase and specifications are subject to change without notice.

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