



November 2014

FDMC8588

N-Channel PowerTrench[®] MOSFET 25 V, 40 A, 5.7 mΩ

Features

- Max $r_{DS(on)}$ = 5.7 mΩ at $V_{GS} = 4.5$ V, $I_D = 16.5$ A
- State-of-the-art switching performance
- Lower output capacitance, gate resistance, and gate charge boost efficiency
- Shielded gate technology reduces switch node ringing and increases immunity to EMI and cross conduction
- RoHS Compliant

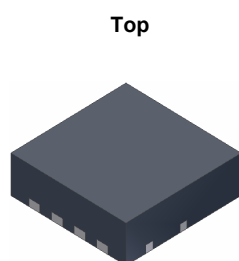


General Description

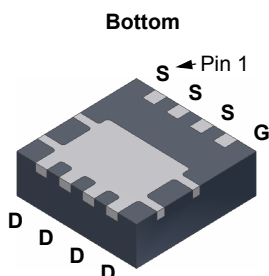
This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- High side switching for high end computing
- High power density DC-DC synchronous buck converter

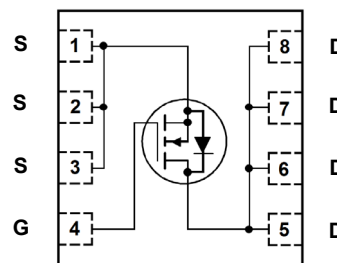


Top



Bottom

Power 33



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage (Note 5)	25	V
V_{GS}	Gate to Source Voltage (Note 4)	± 12	V
I_D	Drain Current - Continuous (Package limited) $T_C = 25^\circ\text{C}$	40	A
	- Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$	59	
	- Continuous (Note 1a)	16.5	
	- Pulsed	60	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	29	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	26	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	$T_C = 25^\circ\text{C}$	4.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	$T_A = 25^\circ\text{C}$ (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
08OD	FDMC8588	Power 33	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		17		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 12\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	0.8	1.4	1.8	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-4		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 17\text{ A}$		3.5	5.0	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 16.5\text{ A}$		4.3	5.7	
		$V_{GS} = 10\text{ V}$, $I_D = 17\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		4.8	6.9	
g_{FS}	Forward Transconductance	$V_{DD} = 5\text{ V}$, $I_D = 16.5\text{ A}$		85		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 13\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		1228	1720	pF
C_{oss}	Output Capacitance			441	620	pF
C_{rss}	Reverse Transfer Capacitance			69	100	pF
R_g	Gate Resistance		0.1	0.5	1.5	Ω

Switching Characteristics

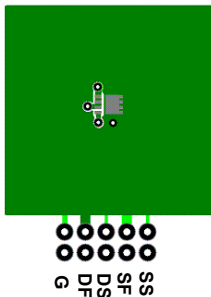
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13\text{ V}$, $I_D = 16.5\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		8	16	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			25	40	ns
t_f	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge at 4.5V	$V_{DD} = 13\text{ V}$, $I_D = 16.5\text{ A}$		12	17	nC
Q_{gs}	Total Gate Charge			3.0		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.3		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 16.5\text{ A}$ (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 16.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		25		ns
Q_{rr}	Reverse Recovery Charge			10		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. 125 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. E_{AS} of 29 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.2\text{ mH}$, $I_{AS} = 7\text{ A}$, $V_{DD} = 23\text{ V}$, $V_{GS} = 10\text{ V}$. 100% tested at $L = 0.1\text{ mH}$, $I_{AS} = 16\text{ A}$.

4. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

5. The continuous V_{ds} rating is 25V; however, a pulse of 28 V peak voltage for no longer than 3ns duration at 500KHz frequency can be applied.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

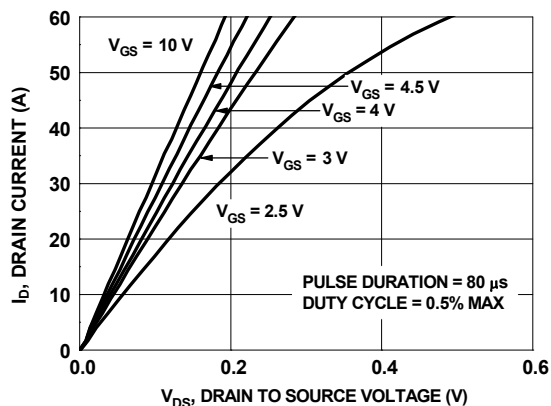


Figure 1. On Region Characteristics

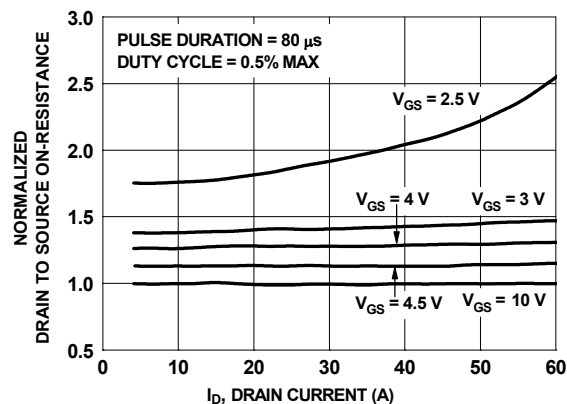


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

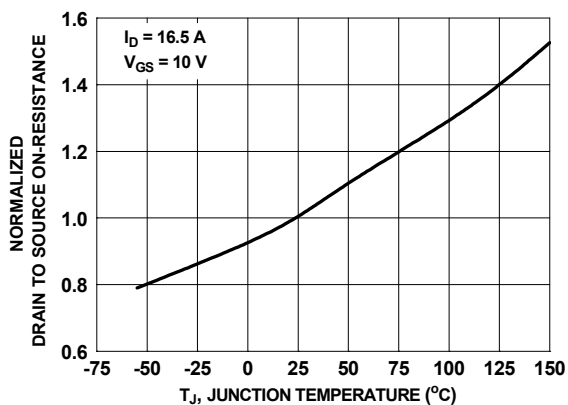


Figure 3. Normalized On Resistance vs. Junction Temperature

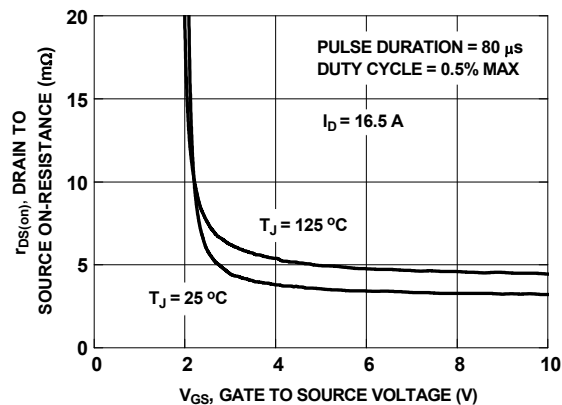


Figure 4. On-Resistance vs. Gate to Source Voltage

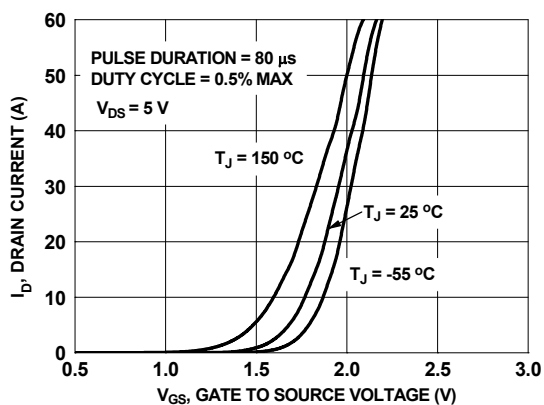


Figure 5. Transfer Characteristics

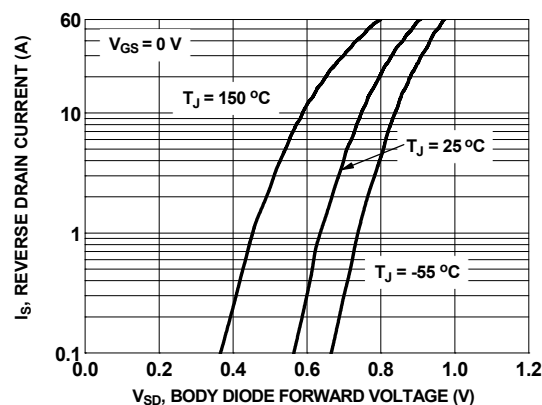


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

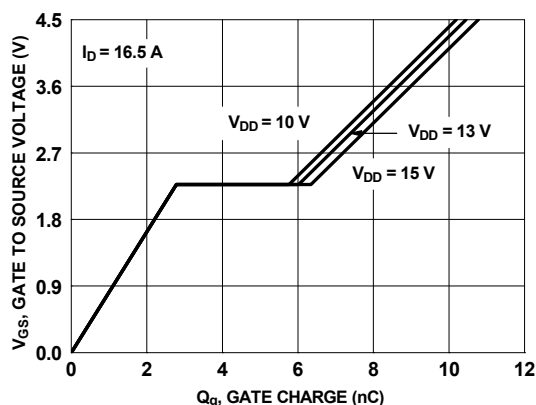


Figure 7. Gate Charge Characteristics

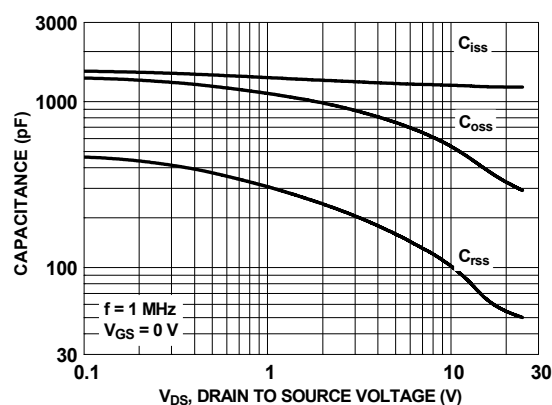


Figure 8. Capacitance vs. Drain to Source Voltage

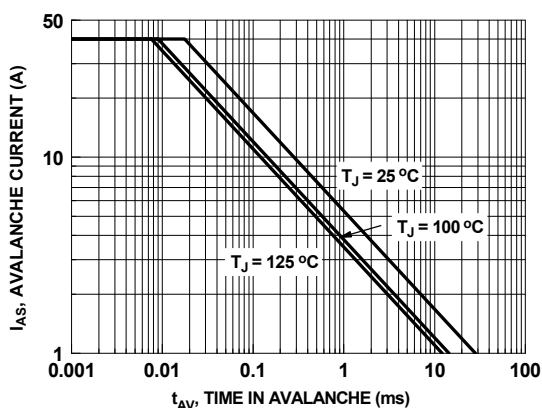


Figure 9. Unclamped Inductive Switching Capability

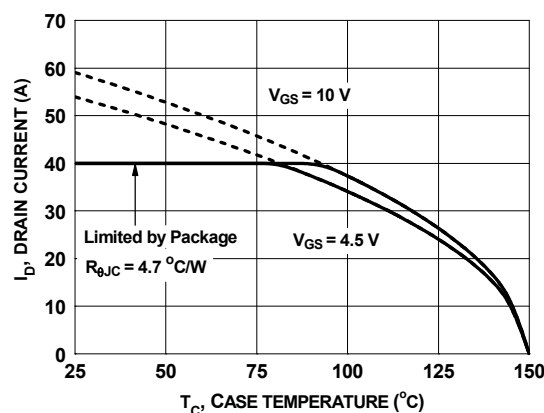


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

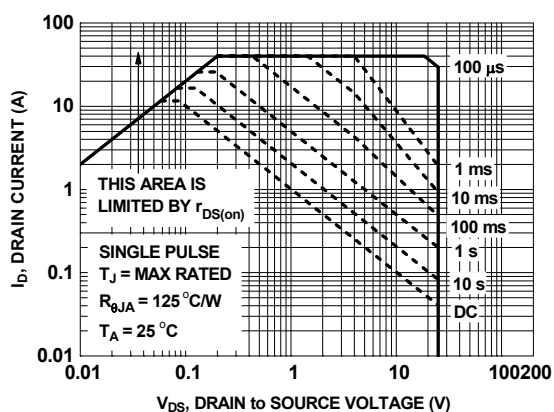


Figure 11. Forward Bias Safe Operating Area

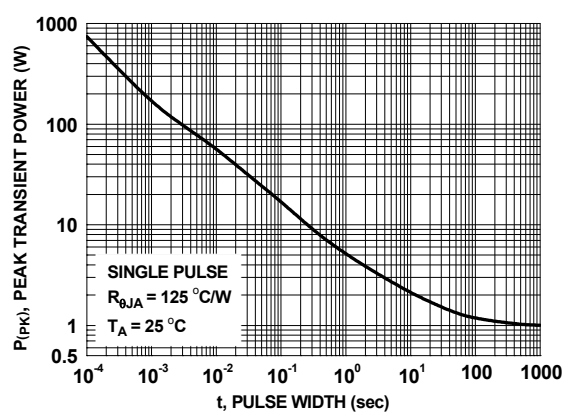


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

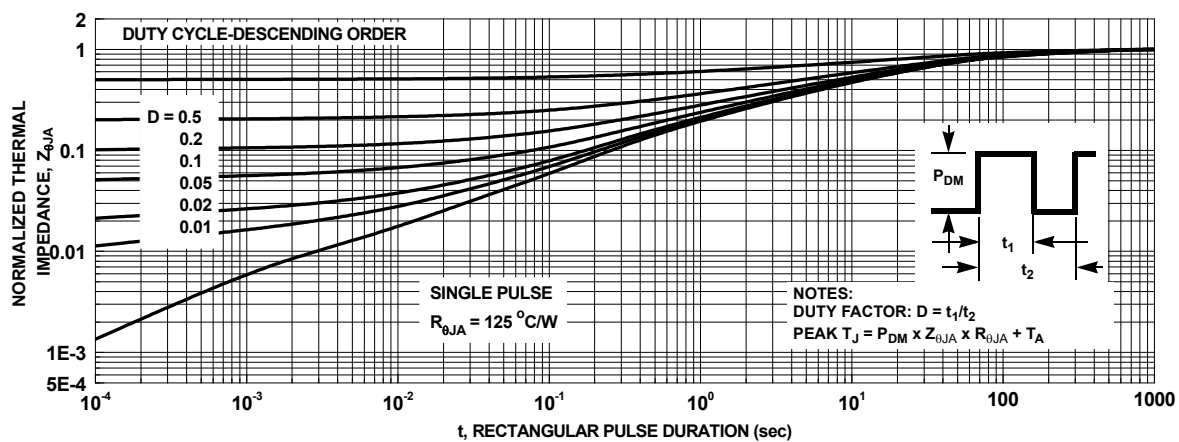
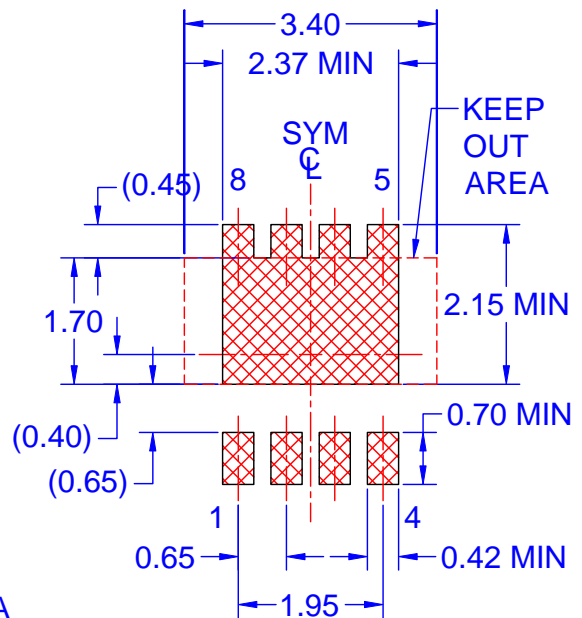
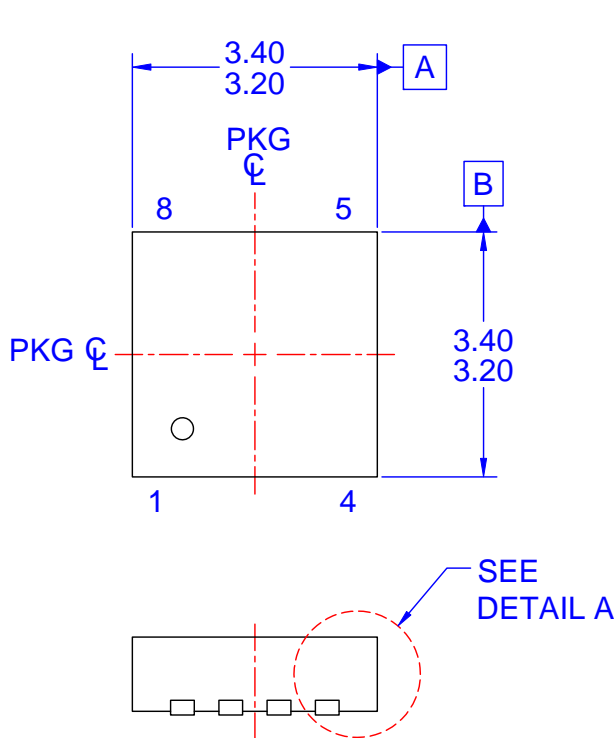
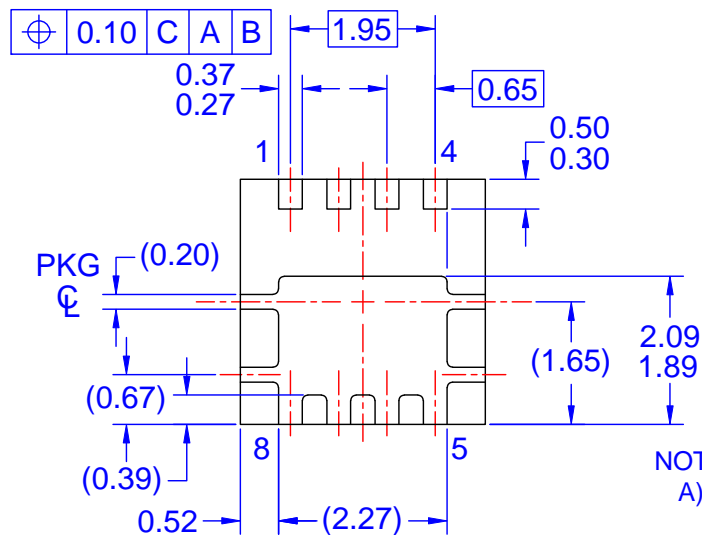


Figure 13. Junction-to-Ambient Transient Thermal Response Curve



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.

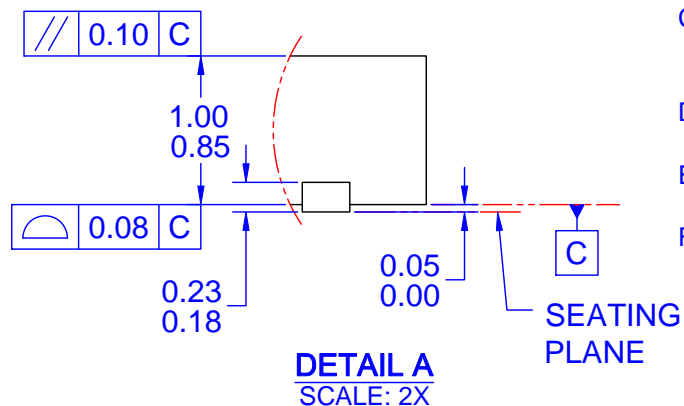
B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: PQFN08BREV2



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