

April 2015

# FDD86250

# N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET 150 V, 51 A, 22 m $\Omega$

#### **Features**

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 22 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 8 A
- Max  $r_{DS(on)}$  = 31 m $\Omega$  at  $V_{GS}$  = 6 V,  $I_D$  = 6.5 A
- 100% UIL tested
- RoHS Compliant

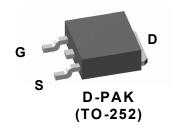


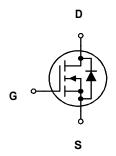
### **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

# **Application**

■ DC - DC Conversion





# **MOSFET Maximum Ratings** $T_C = 25$ °C unless otherwise noted.

Symbol	Parame	ter		Ratings	Units
$V_{DS}$	Drain to Source Voltage			150	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T <sub>C</sub> = 25 °C	(Note 5)	51	
	-Continuous	T <sub>C</sub> = 100 °C	(Note 5)	27	^
'D	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	8	A
	-Pulsed		(Note 4)	164	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	180	mJ
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25 °C		132	w
	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	3.1	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperat	ture Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.94	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a	40	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86250	FDD86250	D-PAK(TO-252)	13 "	16 mm	2500 units

# **Electrical Characteristics** T<sub>J</sub> = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		106		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA

#### On Characteristics

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	2.9	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		-10		mV/°C
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8 A		18.4	22	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 6 \text{ V}, I_D = 6.5 \text{ A}$		21.4	31	mΩ
, ,		$V_{GS}$ = 10 V, $I_{D}$ = 8 A, $T_{J}$ = 125 °C		35.8	45	1
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 8 A		28		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V - 75 V V - 0 V	1585	2110	pF
Coss	Output Capacitance	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V, ——f = 1 MHz	167	225	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1011 12	7	15	pF
$R_a$	Gate Resistance		0.6		Ω

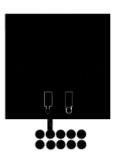
#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		1	1.2	20	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 75 V, I <sub>D</sub> = 8 A,	3	3.7	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$	2	20	32	ns
t <sub>f</sub>	Fall Time			4	10	ns
Qg	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	2	23	33	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to 5 V}$ $V_{DD} = 75 \text{ V},$	1:	2.8	18	nC
$Q_{gs}$	Gate to Source Charge	I <sub>D</sub> = 8 A	6	5.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		4	.7		nC

#### **Drain-Source Diode Characteristics**

V	Source-Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 8 \text{ A}$	(Note 2)	0.78	1.3	V
V SD	V <sub>SD</sub> Source-Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2.6 \text{ A}$	(Note 2)	0.73	1.2	
t <sub>rr</sub>	Reverse Recovery Time	$I_{\rm F}$ = 8 A, di/dt = 100 A/ $\mu$	c	71	113	ns
Q <sub>rr</sub>	Reverse Recovery Charge	1 <sub>F</sub> - δ A, αι/αι - 100 A/μS		104	166	nC

In R<sub>BJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>BJC</sub> is guaranteed by design while R<sub>BJA</sub> is determined by the user's board design.



a) 40 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 96 °C/W when mounted on a minimum pad

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.</li>
   Starting T<sub>J</sub> = 25 °C, L = 1.0 mH, I<sub>AS</sub> = 19 A, V<sub>DD</sub> = 135 V, V<sub>GS</sub> = 10 V.
   Pulsed Id please refer to Fig 11 SOA graph for more details.
   Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

## Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted.

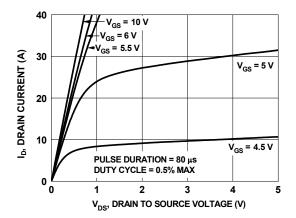


Figure 1. On-Region Characteristics

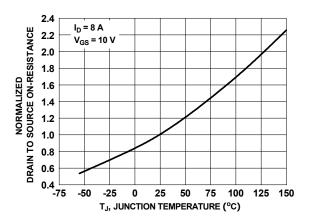


Figure 3. Normalized On-Resistance vs. Junction Temperature

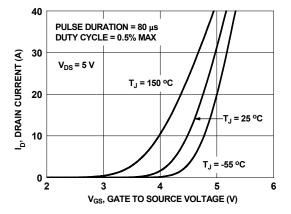


Figure 5. Transfer Characteristics

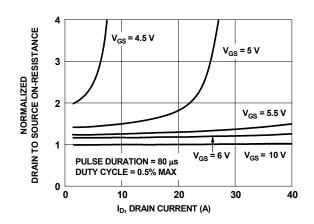


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

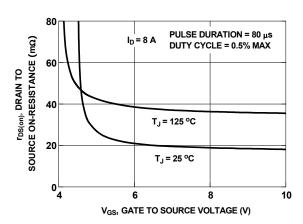


Figure 4. On-Resistance vs. Gate to Source Voltage

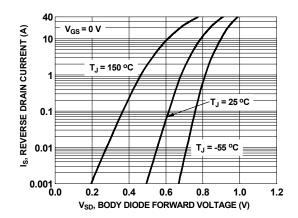


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# Typical Characteristics $T_J$ = 25 °C unless otherwise noted.

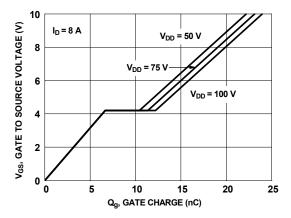


Figure 7. Gate Charge Characteristics

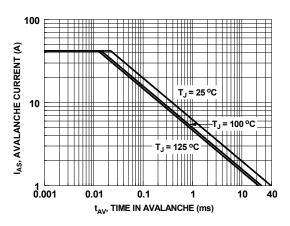


Figure 9. Unclamped Inductive Switching Capability

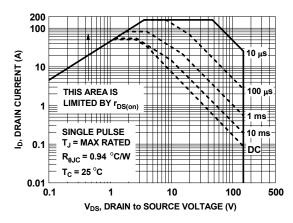


Figure 11. Forward BiasSafe Operating Area

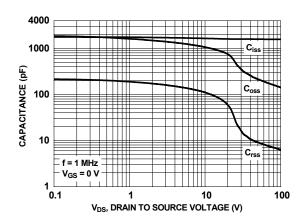


Figure 8. Capacitance vs. Drain to Source Voltage

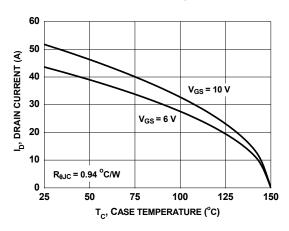


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

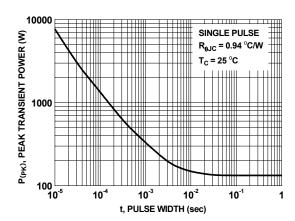


Figure 12. Single Pulse Maximum Power Dissipation



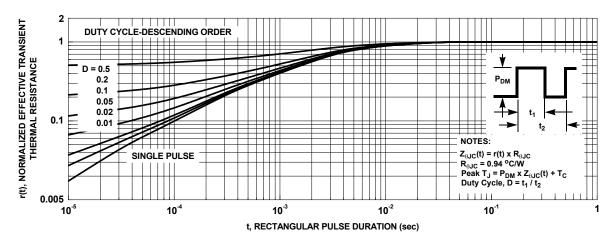
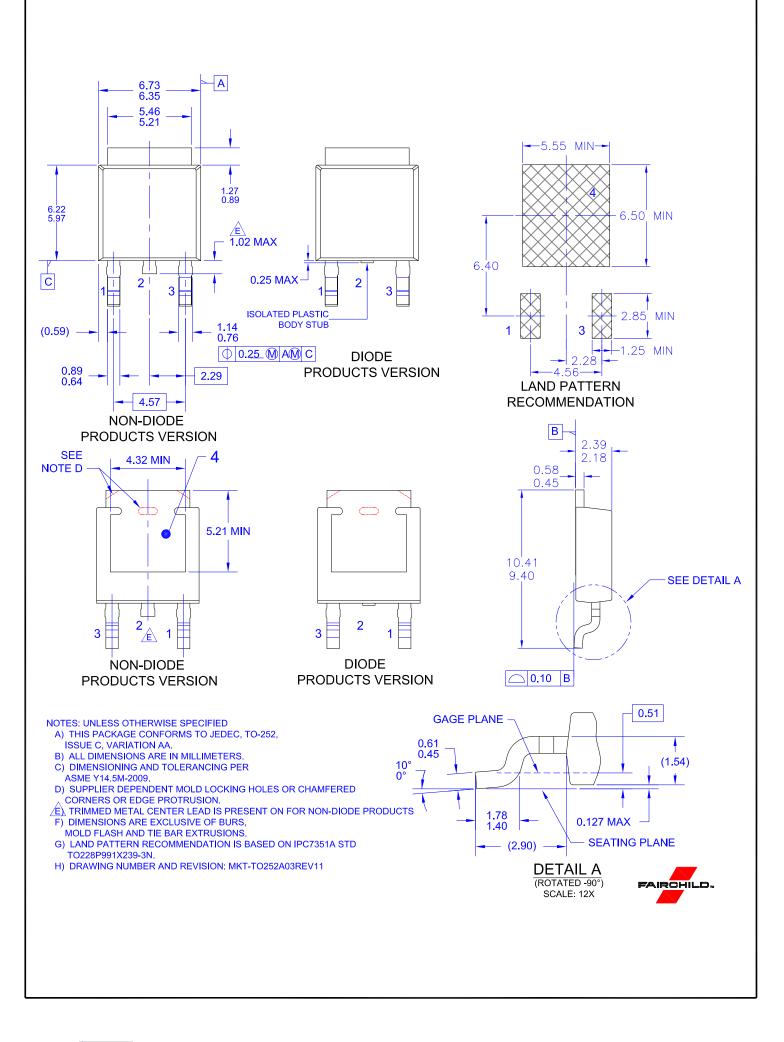


Figure 13. Junction-to-Case Transient Thermal Response Curve



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