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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2011-05-27	

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Last Trademarks Update 2010-06-09

Table of Contents

List of Figures

List of Tables

1 Uni-directional Ultra-Low Capacitance ESD / Transient Protection Diode

1.1 Features

- ESD / Transient protection of high speed data lines exceeding
  - IEC61000-4-2 (ESD): ±20 kV (air / contact)
  - IEC61000-4-4 (EFT): 2.5 kV / 50 A (5/50 ns)
  - IEC61000-4-5 (surge): 3 A (8/20 µs)
- Maximum working voltage: V_{RWM} = 5.3 V
- Ultra low capacitance: C_L = 0.4 pF (typical)
- Low clamping voltage, low dynamic resistance R_{DYN} = 0.6 Ω (typical)
- Very small form factor down to 0.62 x 0.32 x 0.31 mm^3
- Pb-free (RoHS compliant) and halogen free package

1.2 Application Examples

- USB 2.0, Mobile HDMI Link, MDDI, MIPI, etc.
- HDMI, DisplayPort, DVI, Ethernet, Firewire, S-ATA

2 Product Description

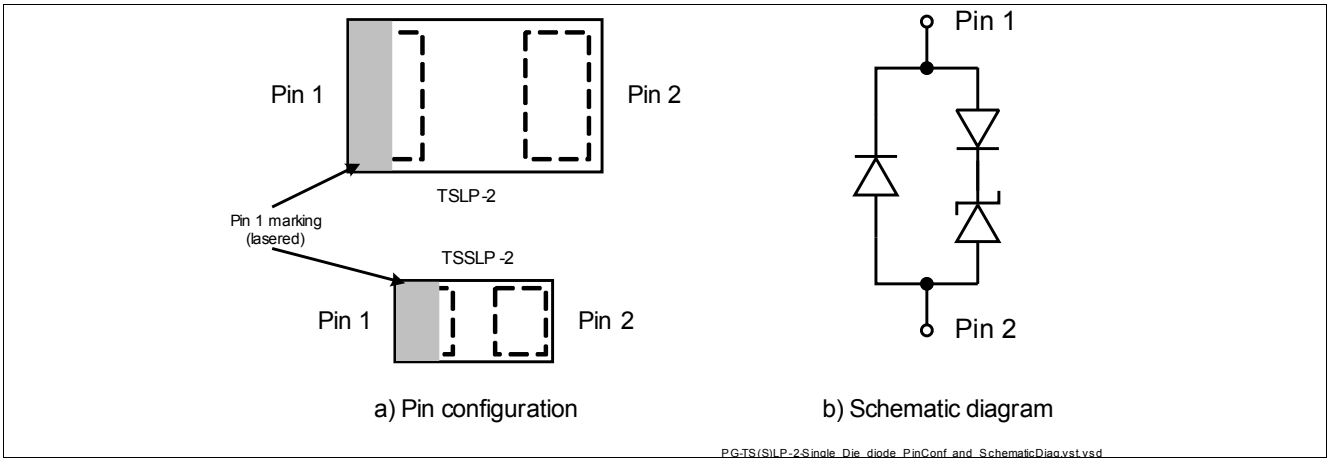

Figure 1 Pin Configuration and Schematic Diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD5V3U1U-02LS	PG-TSSLP-2-1	1 line, uni-directional	L
ESD5V3U1U--02LRH	PG-TSLP-2-7	1 line, uni-directional	E5

3 Characteristics

Table 2 Maximum Rating at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD (air / contact) discharge[1]	V_{ESD}	–	–	20	kV
Peak pulse current (t_p = 8/20 µs)[2]	I_{PP}	–	–	3	A
Operating temperature range	T_{OP}	-55	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2

2) I_{PP} according to IEC61000-4-5

3.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

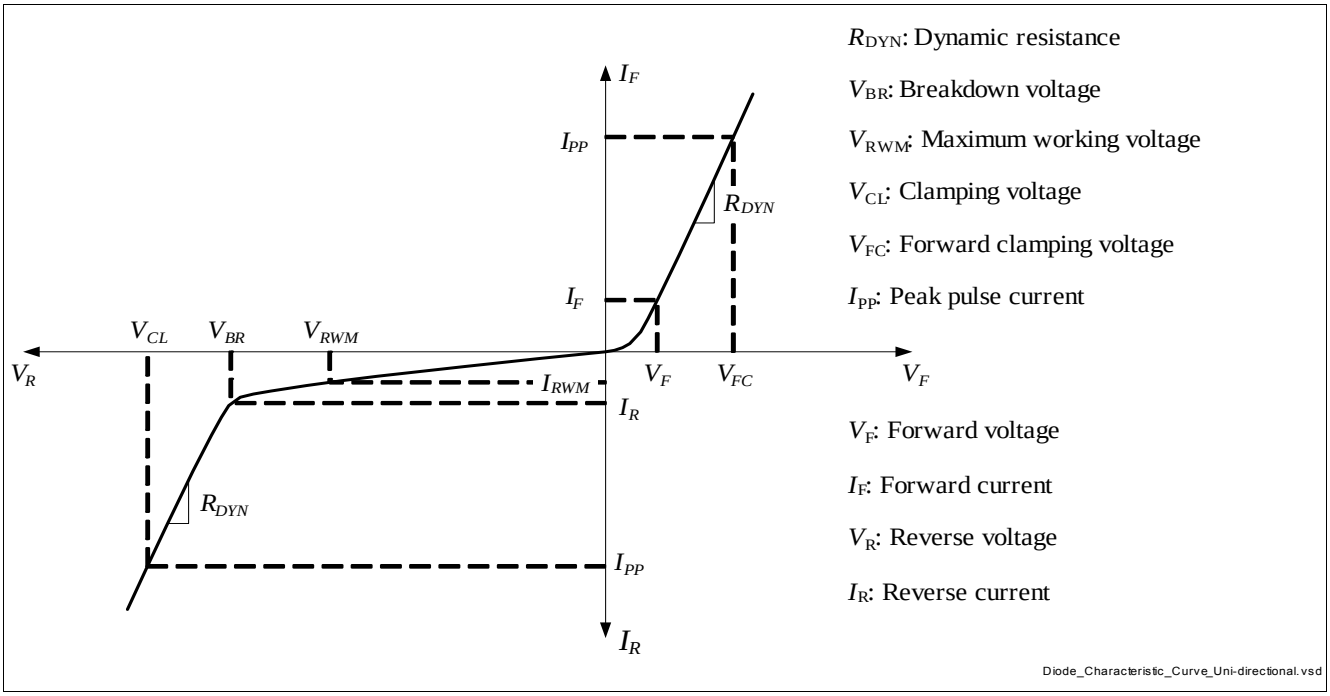

Figure 2 Definitions of Electrical Characteristics

Table 3 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	5.3	V	Pin 1 to Pin 2
Breakdown voltage	V_{BR}	6	–	–	V	I_{BR} = 1 mA, from Pin 1 to Pin 2
Reverse current	I_R	–	<10	100	nA	V_R = 5.3 V, from Pin 1 to Pin 2

Table 4 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance[1)]	C_L	–	0.4	0.6	pF	V_R = 0 V, f = 1 MHz
Serie inductance	L_S	–	0.2	–	nH	ESD5V3U1U-02LS
		–	0.4	–	nH	ESD5V3U1U-02LRH

1) Total capacitance line to ground

Table 5 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage	V_{CL}	–	19	–	V	I_{PP} = 16 A, from Pin 1 to Pin 2
		–	28	–	V	I_{PP} = 30 A, from Pin 1 to Pin 2
Forward clamping voltage	V_{FC}	–	10	–	V	I_{PP} = 16 A, from Pin 2 to Pin 1
		–	17	–	V	I_{PP} = 30 A, from Pin 2 to Pin 1
Dynamic resistance[1)]	R_{DYN}	–	0.6	–	V	Pin 1 to Pin 2
		–	0.5	–	V	Pin 2 to Pin 1

1)Please refer to Application Note AN210[1]. TLP parameter: Z_0 = 50 Ω, t_p = 100ns, t_r = 300ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP charactertistics between I_{PP1} = 10 A and I_{PP2} = 40 A.

3.2 Typical Characteristics at T_A=25°C, unless otherwise specified

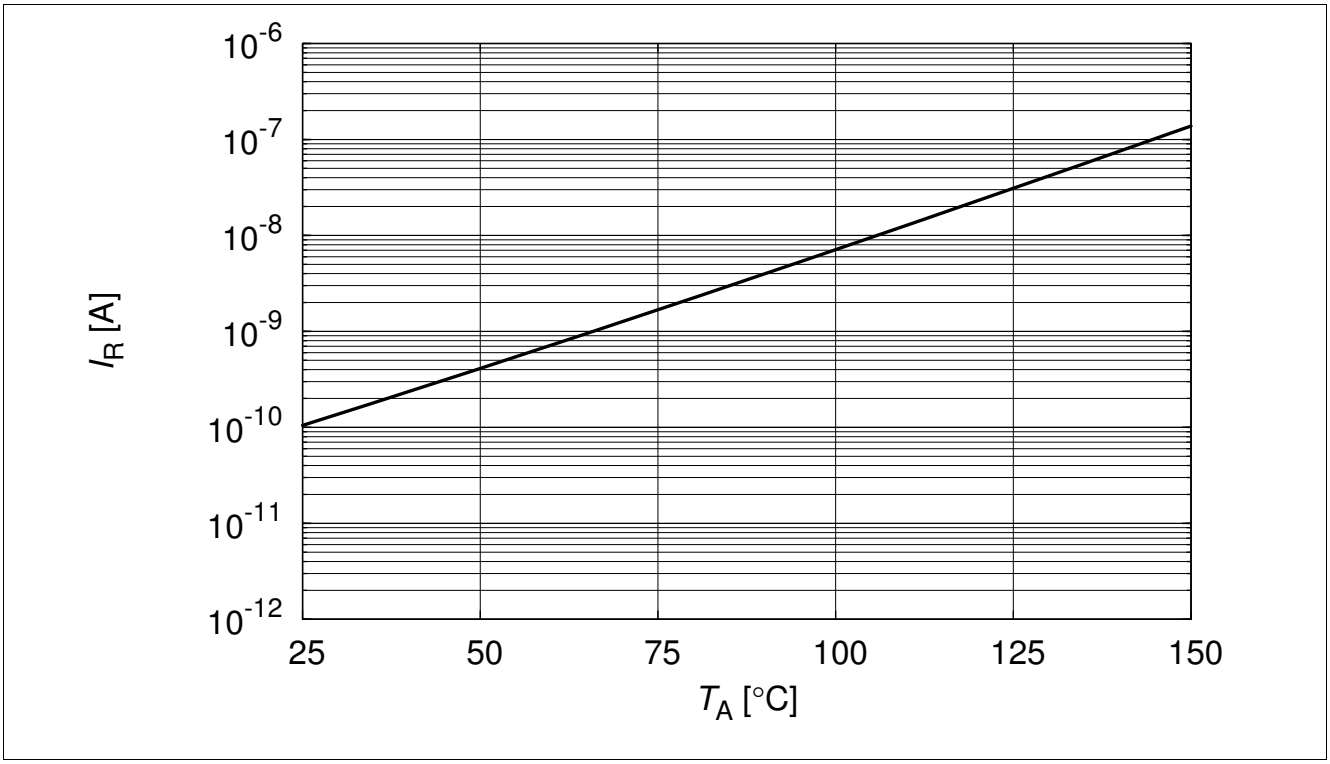

Figure 3 Reverse current $I_R = f(T_A)$, V_R = 5.3 V, from pin 1 to pin 2

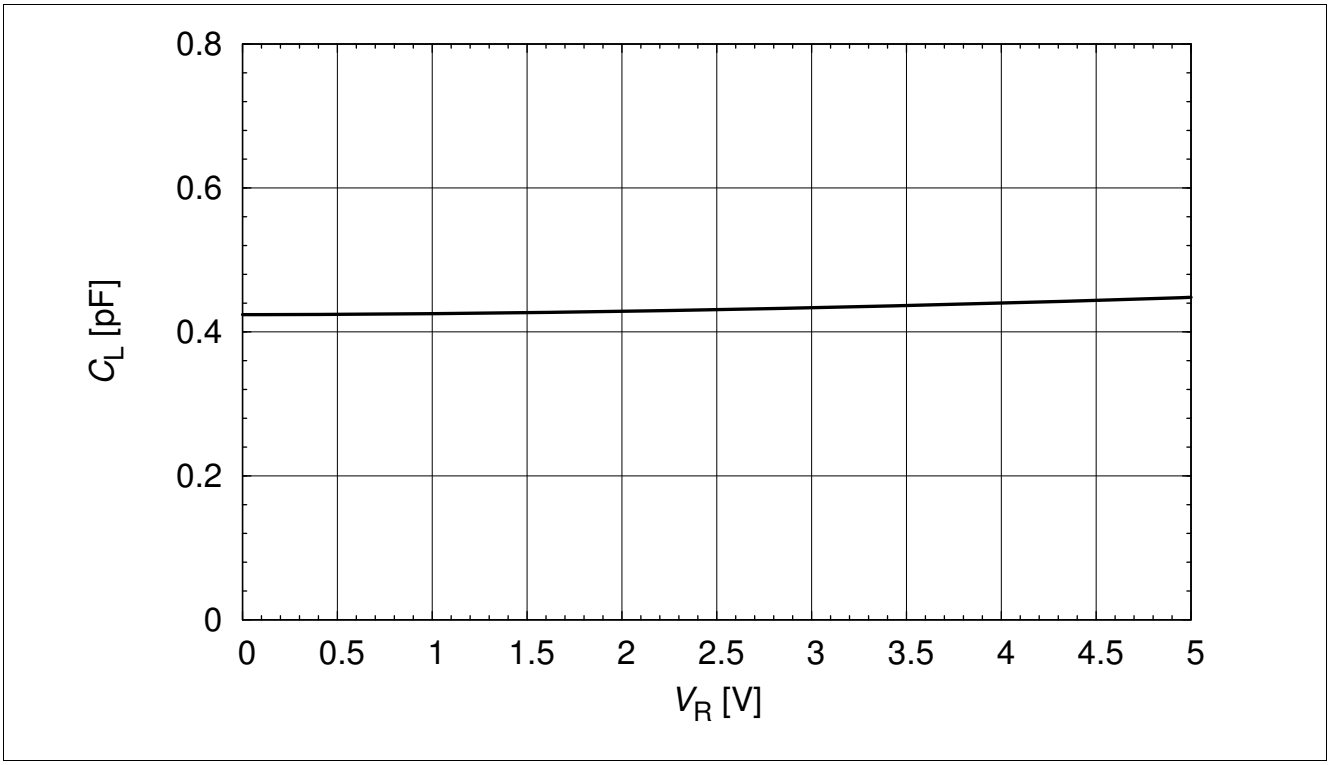

Figure 4 Line capacitance $C_L = f(V_R)$, f = 1MHz, from pin 1 to pin 2

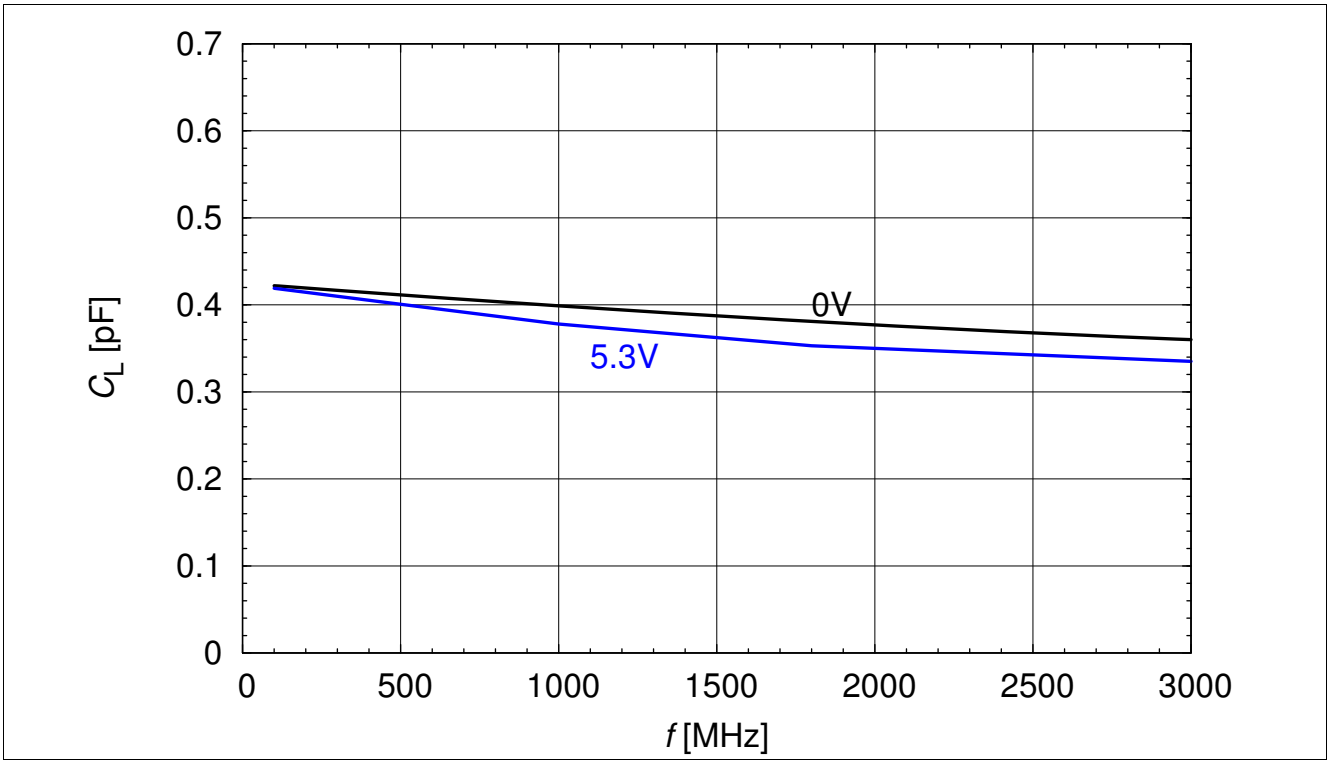

Figure 5 Line capacitance $C_L = f(f)$, from pin 1 to pin 2

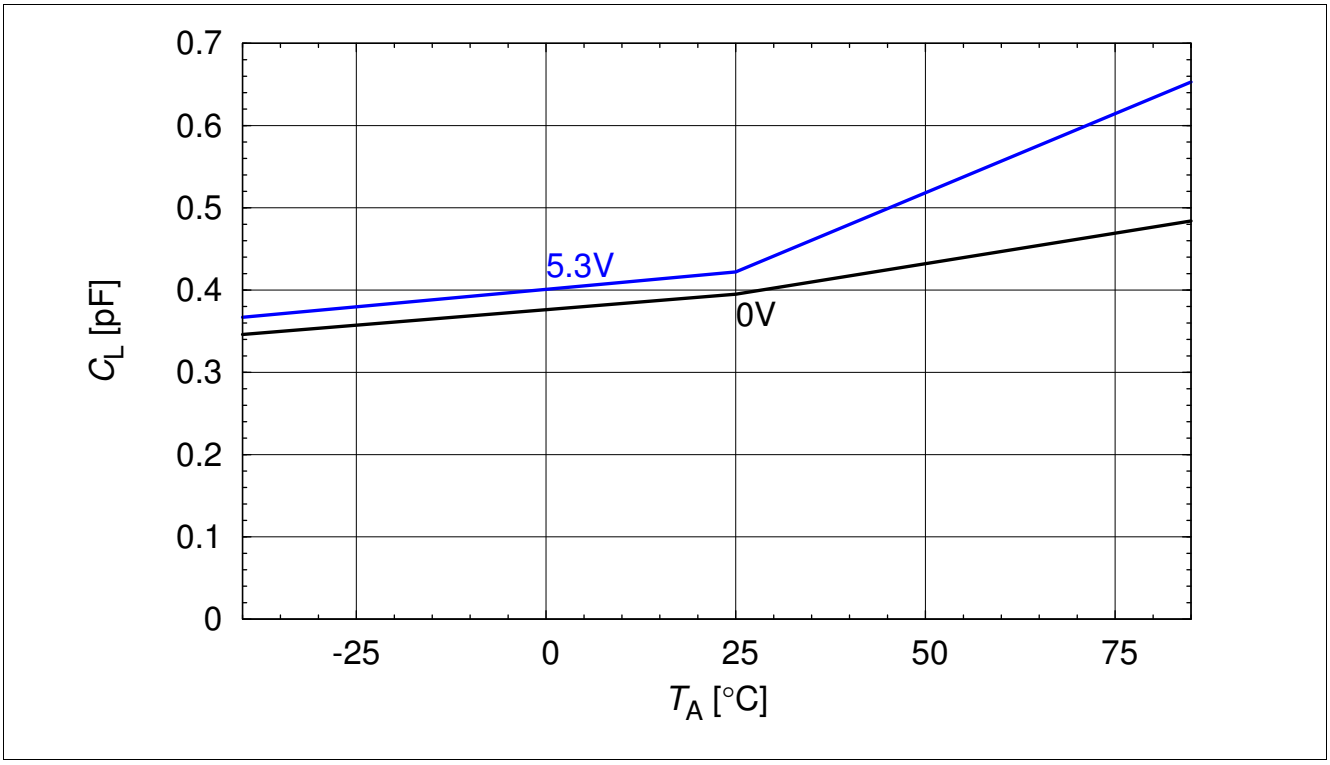

Figure 6 Line capacitance $C_L = f(T_A)$, from pin 1 to pin 2

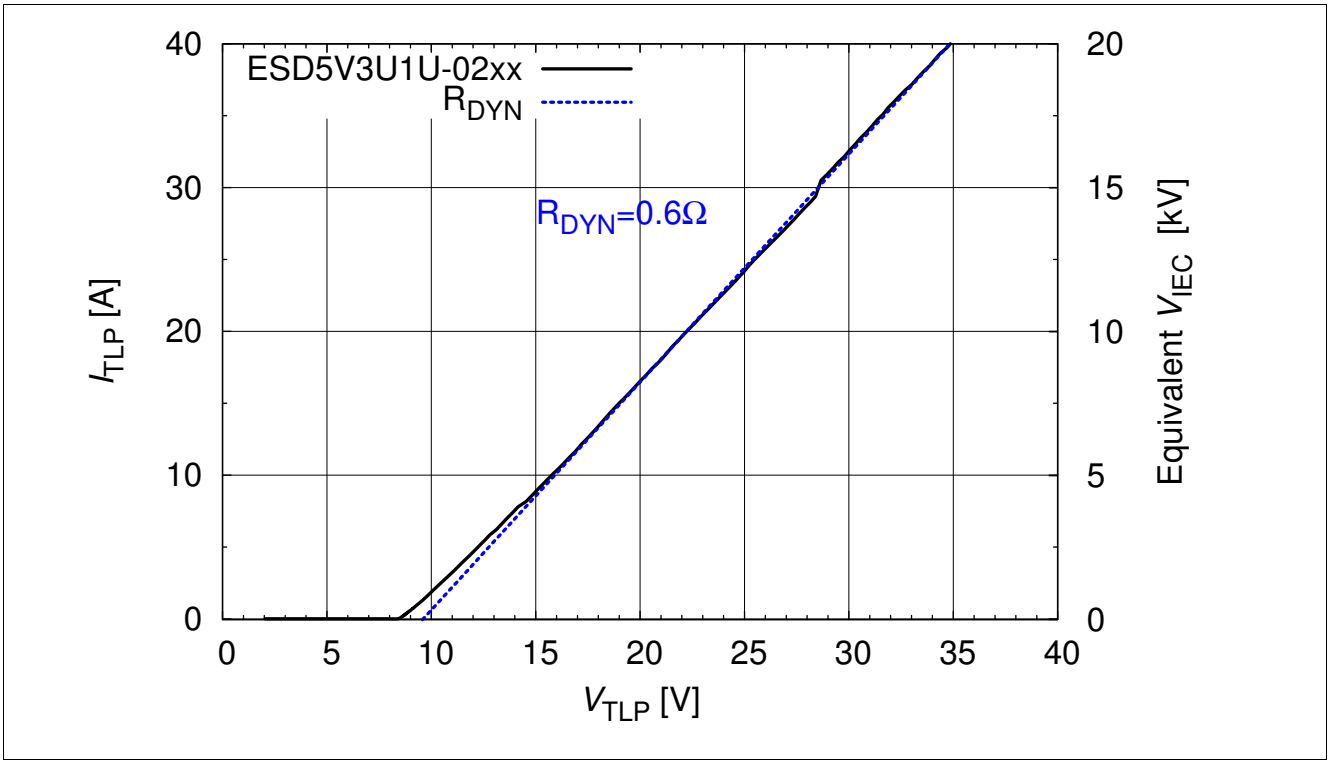

Figure 7 Clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 1 to pin 2[1]

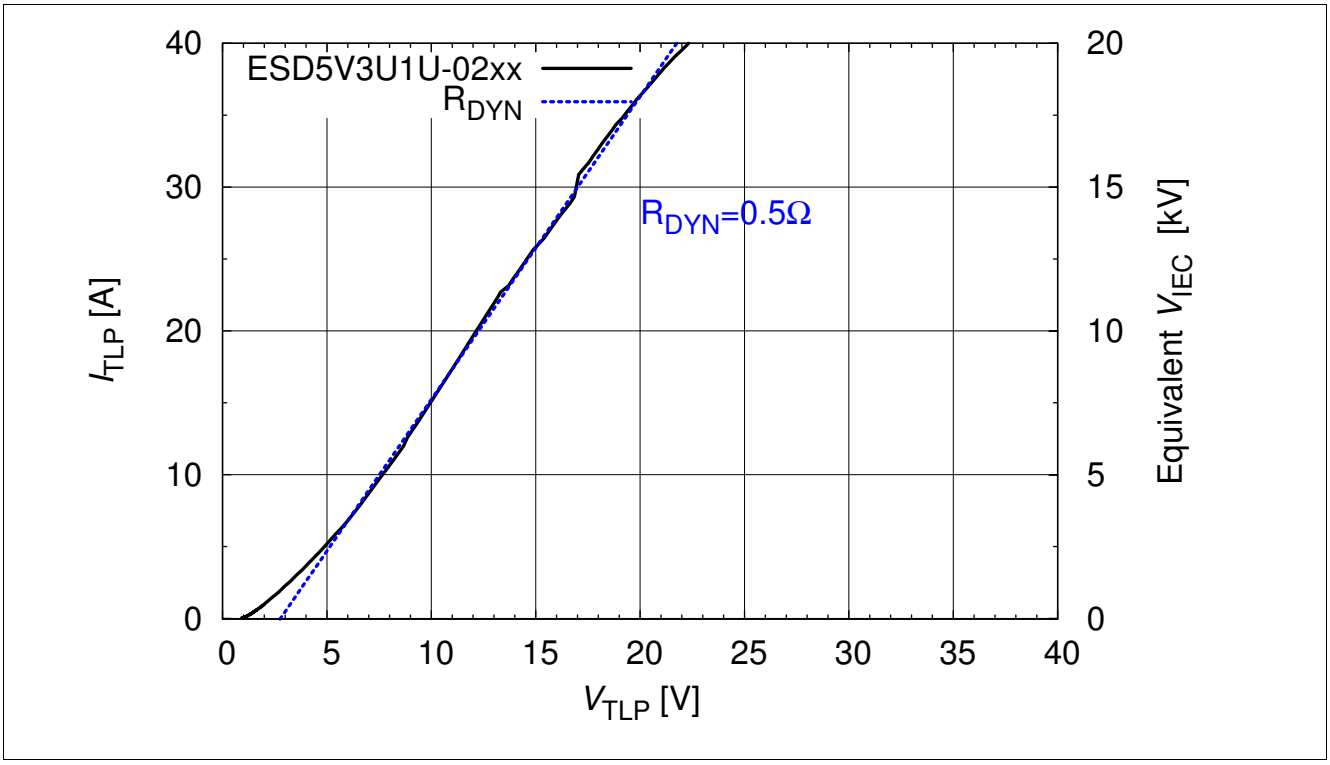

Figure 8 Forward clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 2 to pin 1[1]

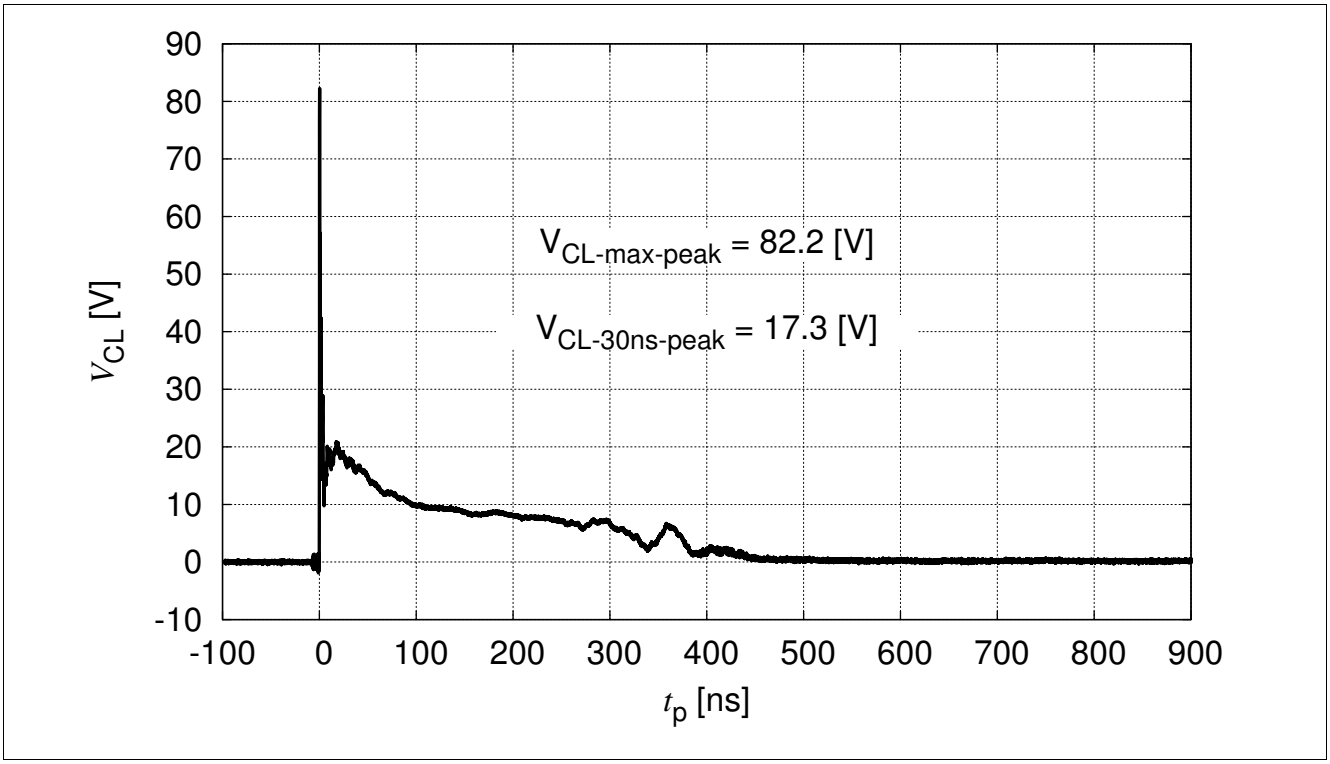

Figure 9 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2

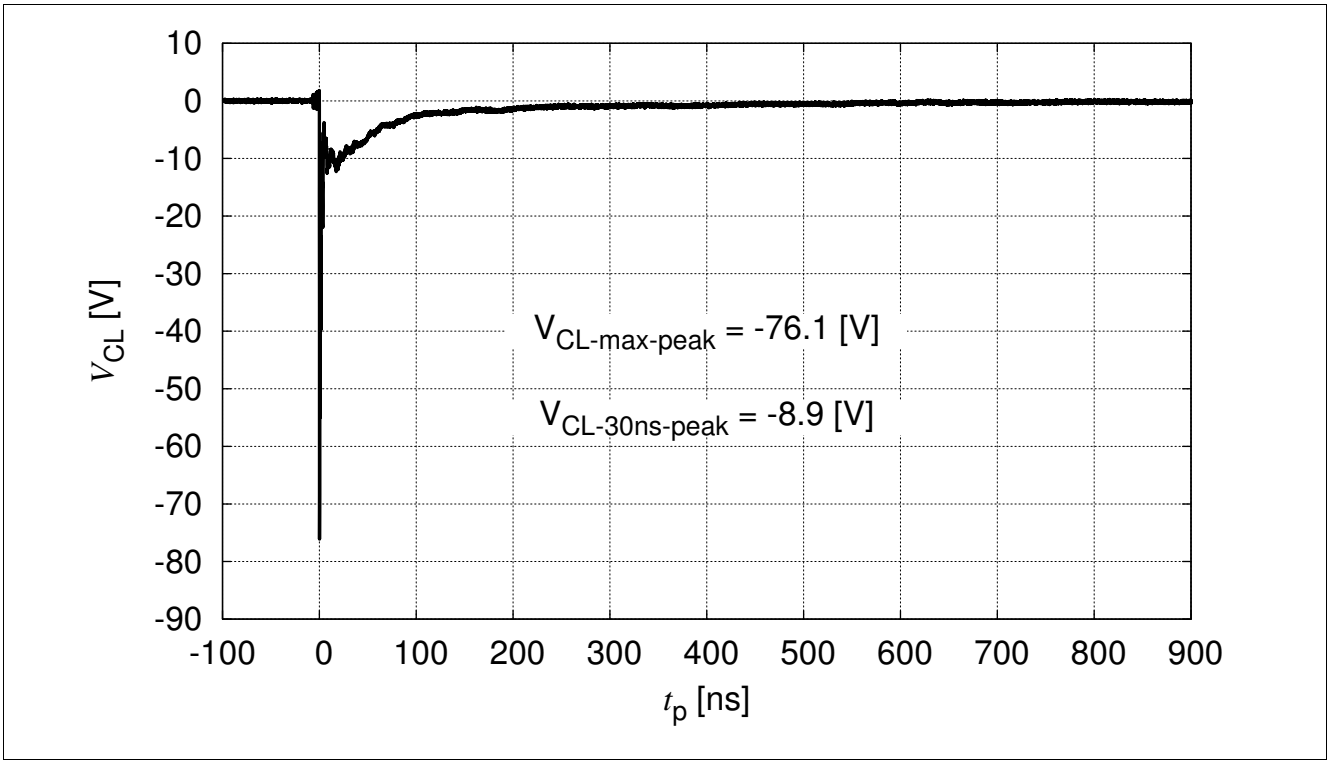

Figure 10 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2

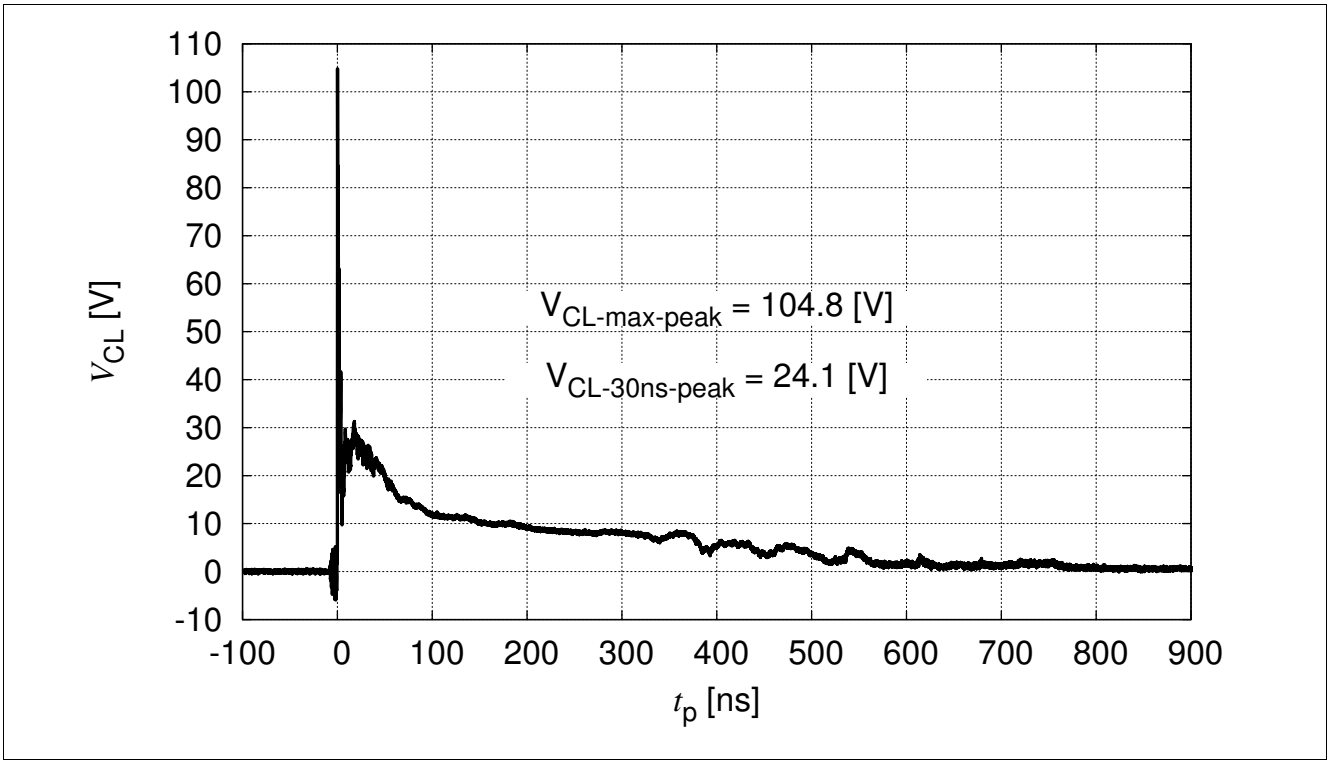

Figure 11 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2

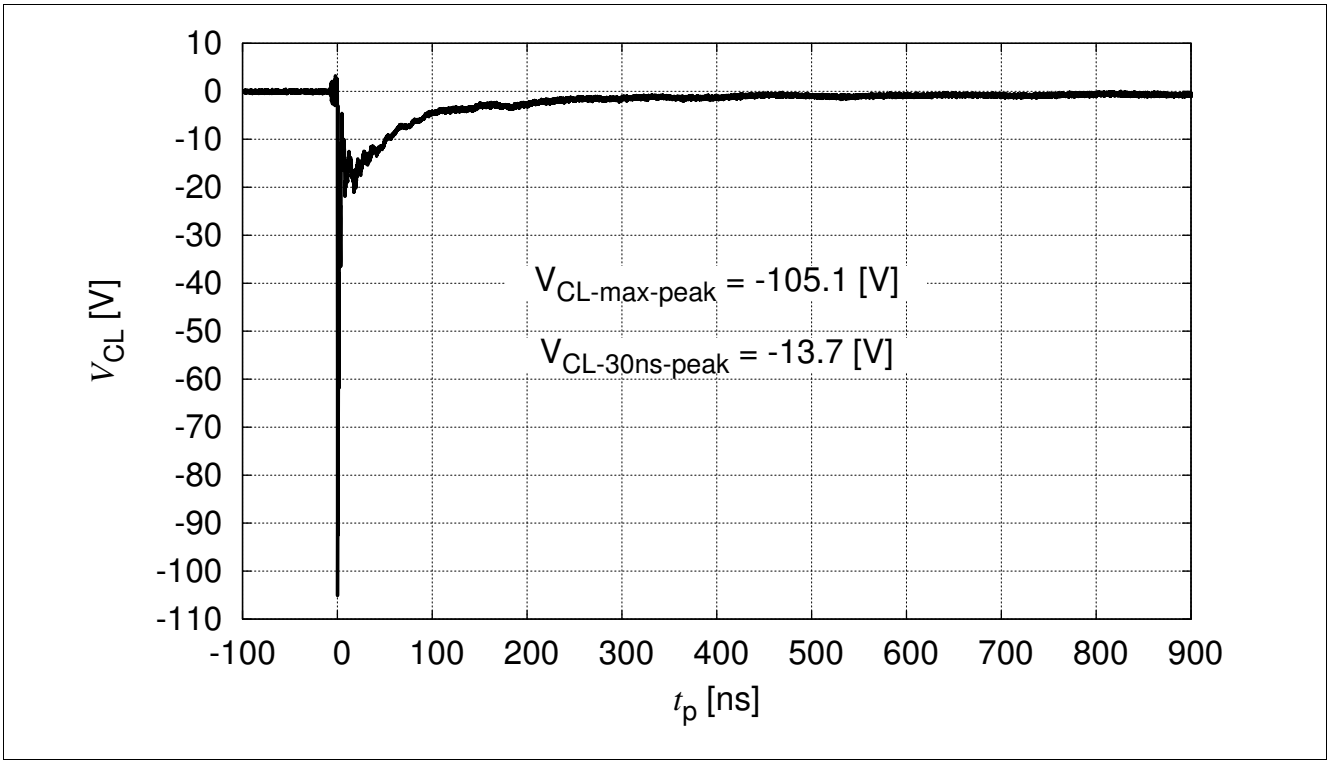

Figure 12 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2

4 Application Information

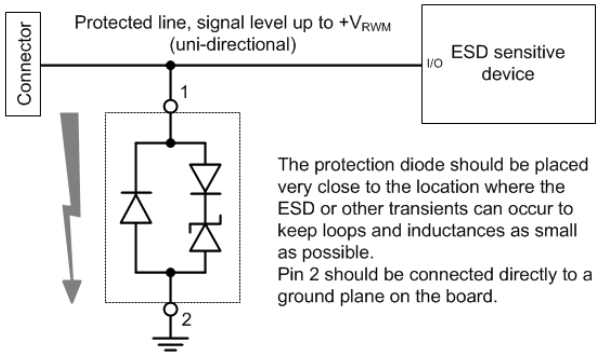

Figure 13 Single line, uni-directional ESD / Transient protection[2]

5 Ordering Information Scheme (Examples)

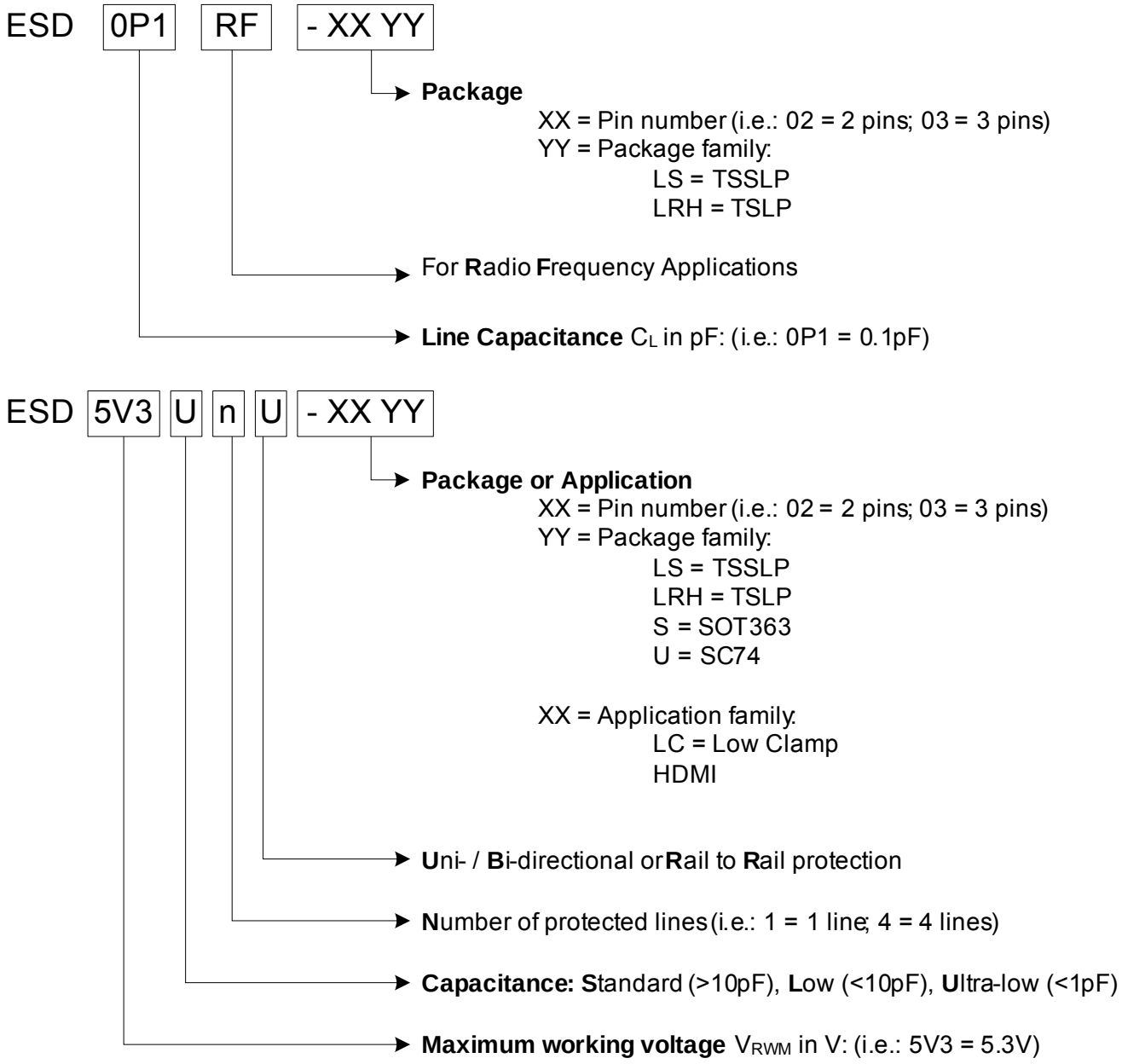

Figure 14 Ordering information scheme

6 Package Information

6.1 PG-TSSLP-2-1 (mm)[3]

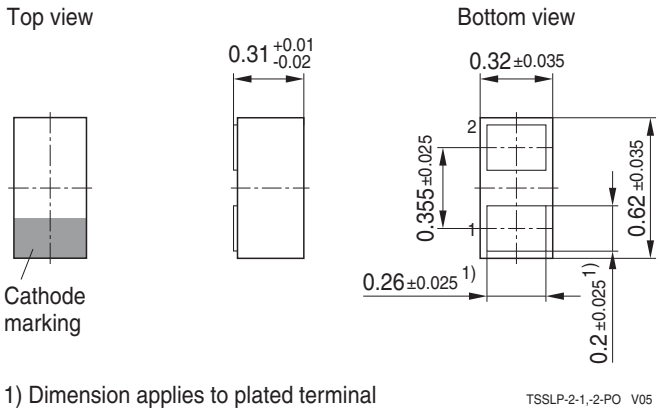

Figure 15 PG-TSSLP-2-1: Package overview

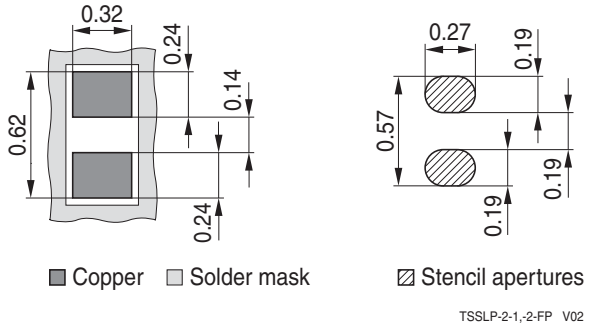

Figure 16 PG-TSSLP-2-1: Footprint

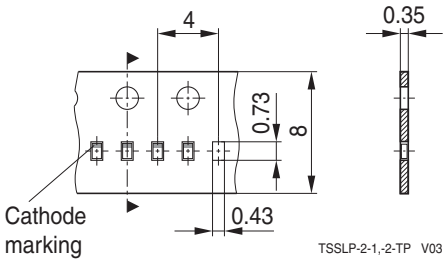

Figure 17 PG-TSSLP-2-1: Packing

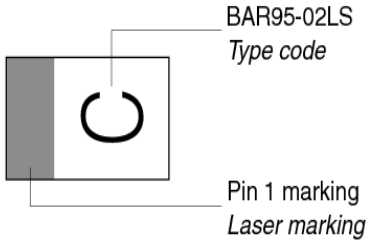

Figure 18 PG-TSSLP-2-1: Marking (example)

6.2 PG-TSLP-2-7 (mm)[3]

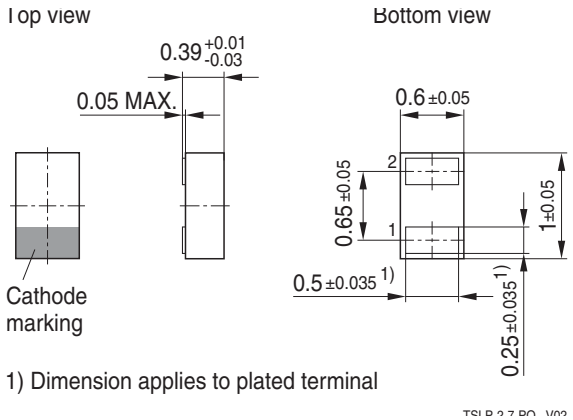

Figure 19 PG-TSLP-2-7: Package Overview

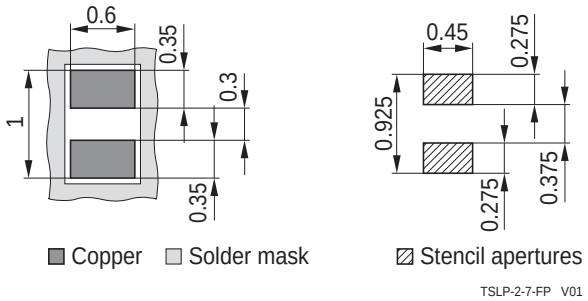

Figure 20 PG-TSLP-2-7: Footprint

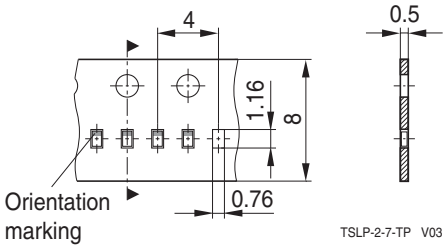

Figure 21 PG-TSLP-2-7: Packing

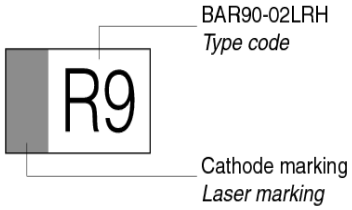

Figure 22 PG-TSLP-2-7: Marking (example)

Terminology

C_L	Line capacitance
DVI	Digital Visual Interface
EFT	Electrical Fast Transient
ESD	Electrostatic Discharge
HDMI	High Definition Multimedia Interface
IEC	International Electrotechnical Commission
I_{PP}	Peak pulse current
I_R	Reverse current
I_{RWM}	Maximum Reverse working Current
L_S	Serial inductance
MDDI	Mobile Display Digital Interface
MIPI	Mobile Industrial Processor Interface
RoHS	Restriction of Hazardous Substances Directive
S-ATA	Serial Advanced Technology Attachment
T_A	Ambient temperature
T_{OP}	Operation temperature
t_p	Pulse duration
T_{stg}	Storage temperature
USB	Universal Serial Bus
V_{BR}	Breakdown Voltage
V_{CL}	Reverse clamping voltage
V_{ESD}	Electrostatic discharge voltage
V_{FC}	Forward Clamping Voltage
V_R	Reverse voltage
V_{RWM}	Maximum Reverse Working Voltage

References

[1] Infineon AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP

[2] Infineon AG - **Application Note AN140**: ESD Protection for Digital High-Speed Interfaces (HDMI, FireWire, ...) using ESD5V3U1U)

[3] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Package

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