

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	30	V
Gate-Source Voltage	V <sub>GSS</sub>	+20 -16	V
Continuous Drain Current (Notes 6 & 9) V <sub>GS</sub> = 10V	I <sub>D</sub>	25 25	A
Continuous Drain Current (Note 5) V <sub>GS</sub> = 10V	I <sub>D</sub>	10.4 8.3	A
Maximum Continuous Body Diode Forward Current (Note 5)	I <sub>S</sub>	3	A
Pulsed Drain Current (10μs pulse, Duty Cycle = 1%)	I <sub>DM</sub>	95	A
Avalanche Current, L=0.3mH	I <sub>AS</sub>	27	A
Avalanche Energy, L=0.3mH	E <sub>AS</sub>	110	mJ

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 6)	P <sub>D</sub>	42	W
Thermal Resistance, Junction to Case (Note 6)	R <sub>θJC</sub>	3	°C/W
Total Power Dissipation (Note 5)	P <sub>D</sub>	2.1	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	60	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	30	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	-	-	1	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	-	-	100 -100	nA	V <sub>GS</sub> = +20V, V <sub>DS</sub> = 0V V <sub>GS</sub> = -16V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1	-	3	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	3.5	4.5	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 7A
Diode Forward Voltage	V <sub>SD</sub>	-	0.7	1	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	-	2370	-	pF	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1MHz
Output Capacitance	C <sub>oss</sub>	-	1360	-	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	-	240	-	pF	
Gate Resistance	R <sub>g</sub>	-	0.6	-	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	-	20	-	nC	V <sub>DS</sub> = 15V, I <sub>D</sub> = 20A
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	-	44	-	nC	
Gate-Source Charge	Q <sub>gs</sub>	-	7	-	nC	
Gate-Drain Charge	Q <sub>gd</sub>	-	8	-	nC	
Turn-On Delay Time	t <sub>D(ON)</sub>	-	6.2	-	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 10V, R <sub>L</sub> = 0.75Ω, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 20A
Turn-On Rise Time	t <sub>R</sub>	-	4.3	-	ns	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	-	21	-	ns	
Turn-Off Fall Time	t <sub>F</sub>	-	8	-	ns	
Body Diode Reverse Recovery Time	t <sub>RR</sub>	-	25	-	ns	I <sub>F</sub> = 15A, di/dt = 500A/μs
Body Diode Reverse Recovery Charge	Q <sub>RR</sub>	-	37	-	nC	

- Notes:
5. R<sub>θJA</sub> is determined with the device mounted on FR-4 substrate PC board, 2oz copper, with 1 inch square copper plate. R<sub>θJC</sub> is guaranteed by design while R<sub>θJA</sub> is determined by the user's board design.
  6. Thermal resistance from junction to soldering point (on the exposed drain pad).
  7. Short duration pulse test used to minimize self-heating effect.
  8. Guaranteed by design. Not subject to product testing.
  9. Package limited.

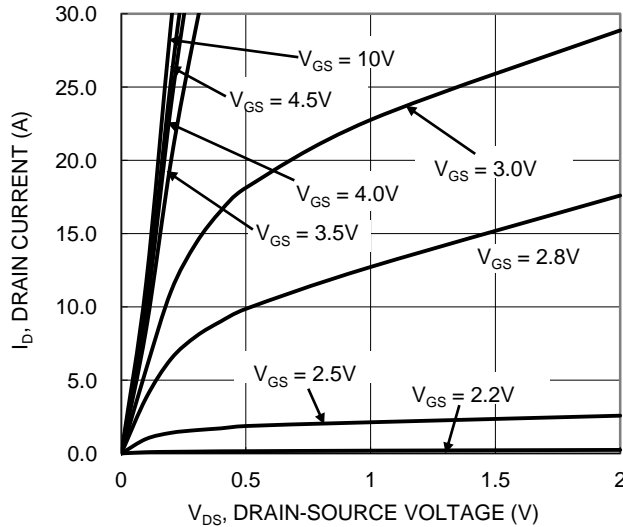


Figure 1. Typical Output Characteristic

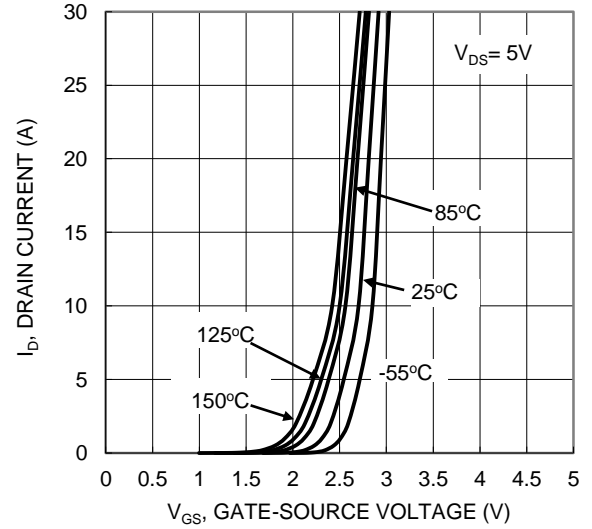


Figure 2. Typical Transfer Characteristic

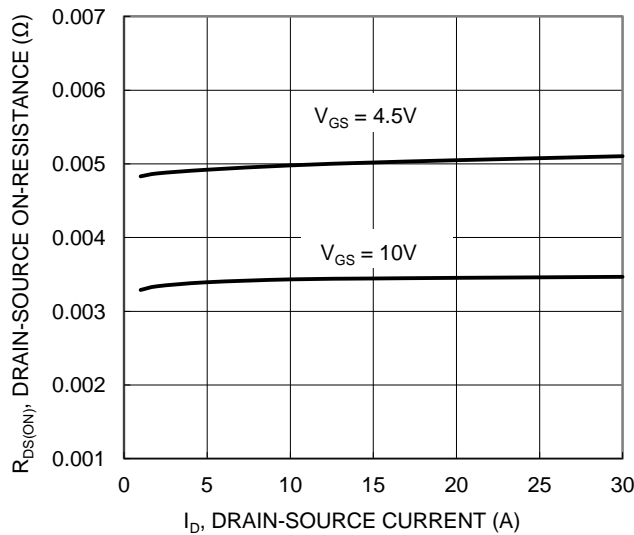


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

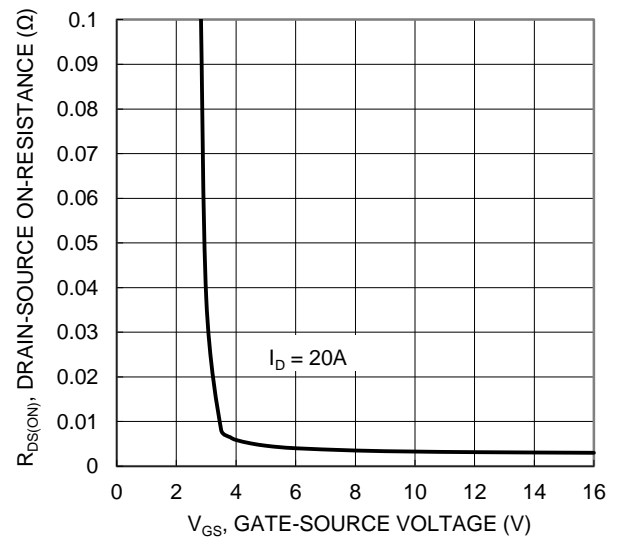


Figure 4. Typical Transfer Characteristic

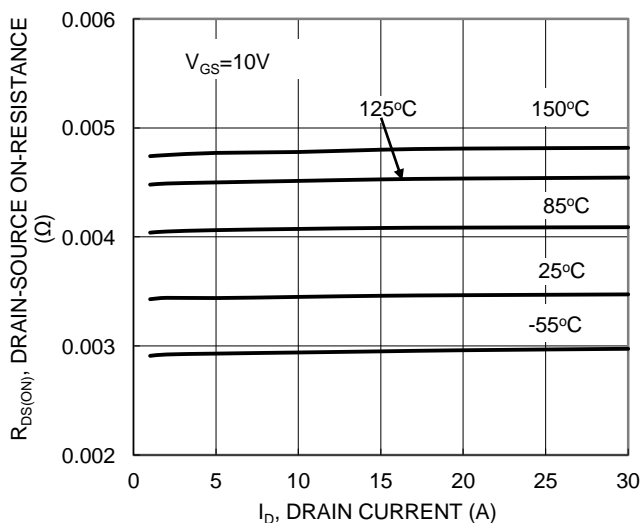


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

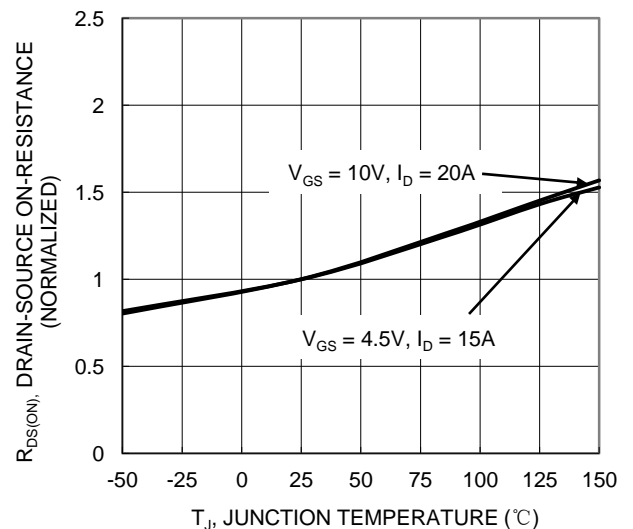


Figure 6. On-Resistance Variation with Junction Temperature

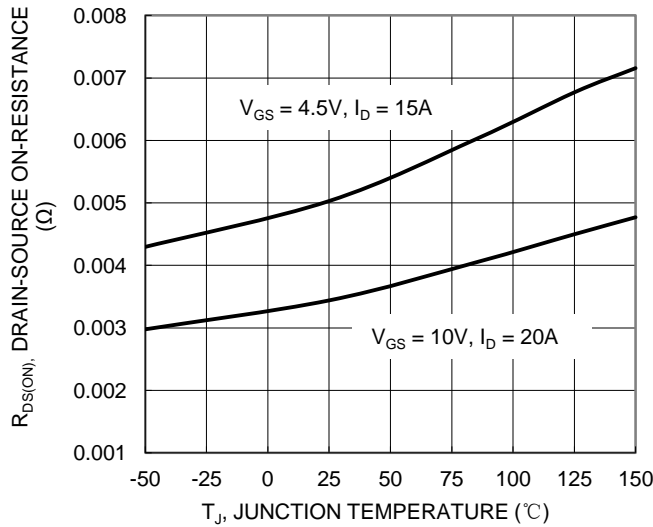


Figure 7. On-Resistance Variation with Junction Temperature

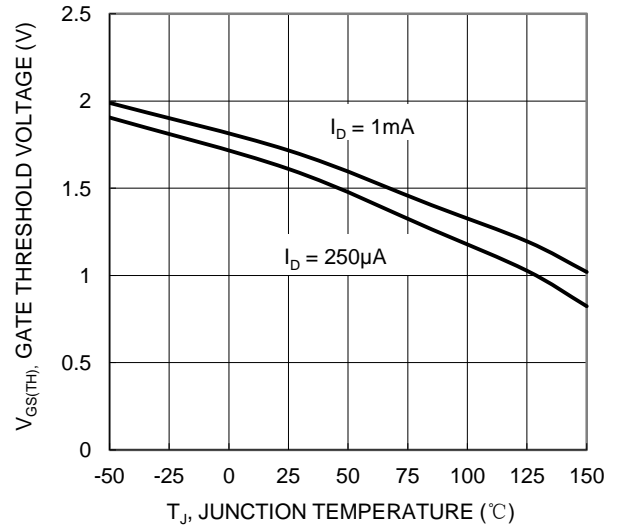


Figure 8. Gate Threshold Variation vs. Junction Temperature

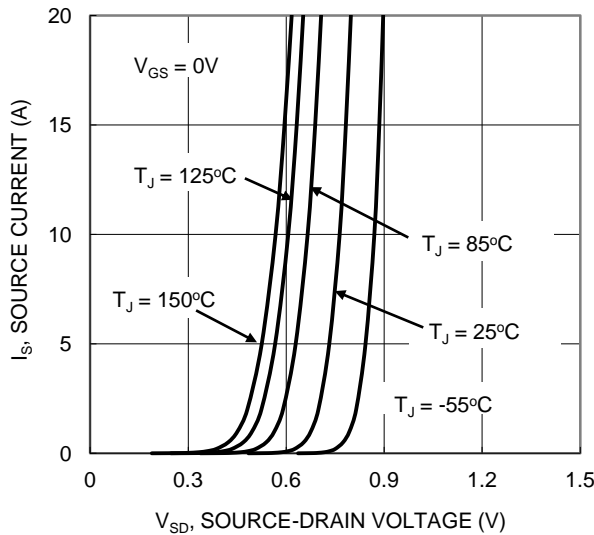


Figure 9. Diode Forward Voltage vs. Current

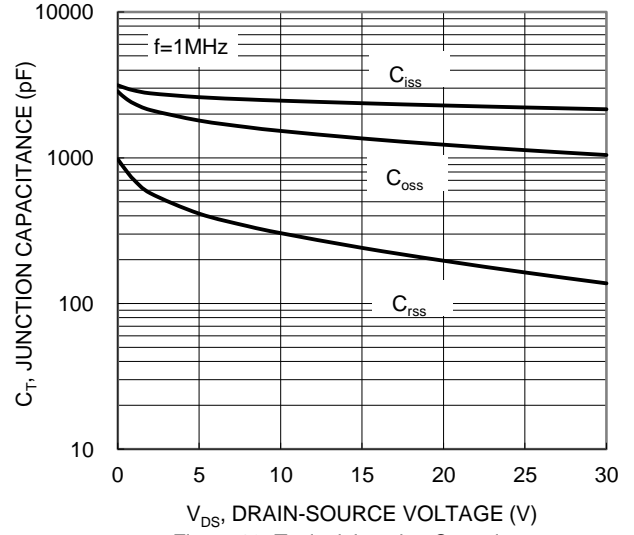


Figure 10. Typical Junction Capacitance

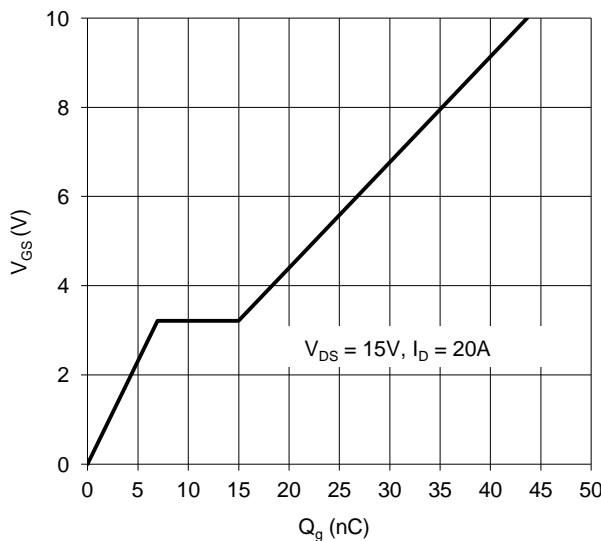


Figure 11. Gate Charge

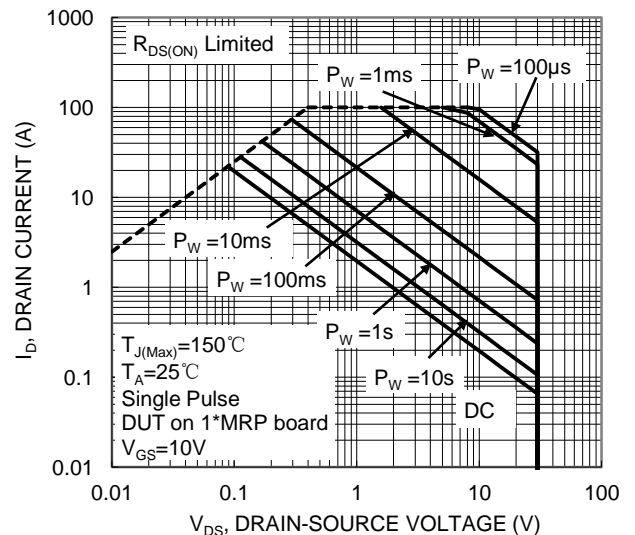


Figure 12. SOA, Safe Operation Area

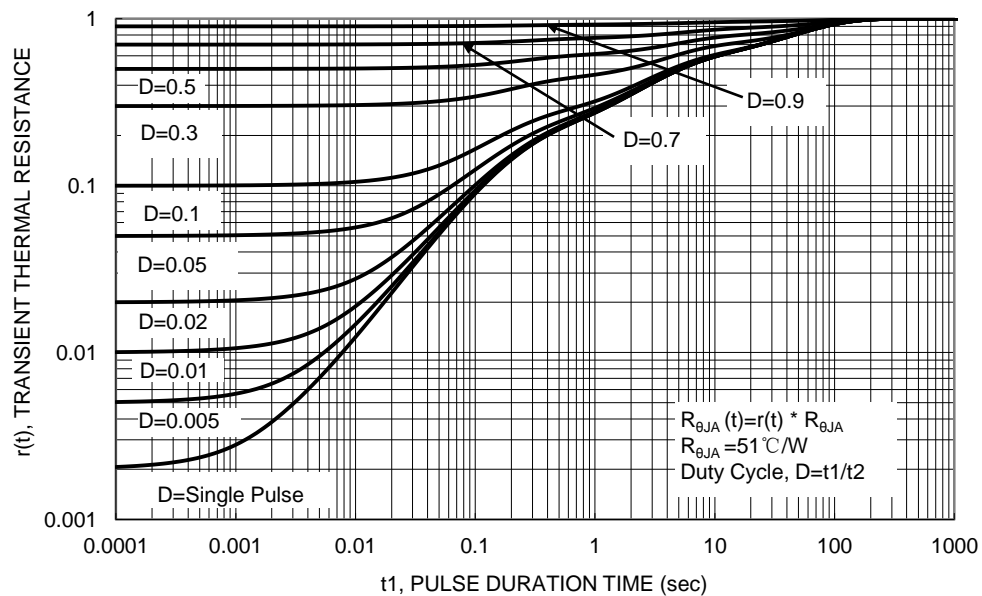
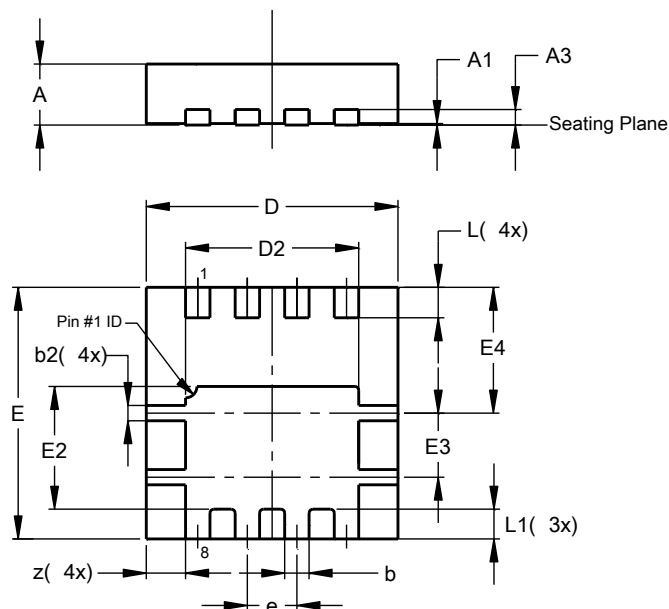


Figure 13. Transient Thermal Resistance

## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**PowerDI3333-8**

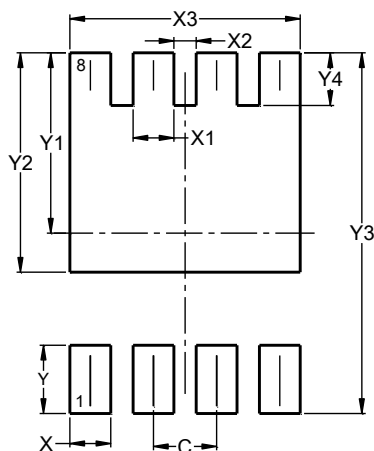


PowerDI3333-8			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	–	–	0.203
b	0.27	0.37	0.32
b2	0.15	0.25	0.20
D	3.25	3.35	3.30
D2	2.22	2.32	2.27
E	3.25	3.35	3.30
E2	1.56	1.66	1.61
E3	0.79	0.89	0.84
E4	1.60	1.70	1.65
e	–	–	0.65
L	0.35	0.45	0.40
L1	–	–	0.39
z	–	–	0.515
All Dimensions in mm			

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**PowerDI3333-8**



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	0.420
X2	0.230
X3	2.370
Y	0.700
Y1	1.850
Y2	2.250
Y3	3.700
Y4	0.540

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