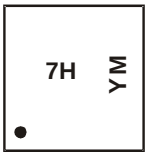
Marking Information

Site 1:



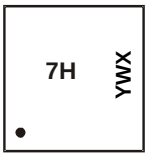
7H = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: H = 2020)
M = Month (ex: 9 = September)

Date Code Key

Year	2012	…	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	Z	…	H	I	J	K	L	M	N	O	P	R

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Site 2:



7H = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: H = 2020)
W = Week (ex: a = Week 27; z Represents Week 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2012	…	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	2	…	0	1	2	3	4	5	6	7	8	9

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	100	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +70°C	I_D	2.9 2.3	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	3.4 2.7	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	10	A
Maximum Body Diode Continuous Current			I_S	2.5	A
Avalanche Current (Note 7)			I_{AS}	4.7	A
Avalanche Energy (Note 7)			E_{AS}	16	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	0.66	W
	T_A = +70°C		0.42	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	189	°C/W
	t<10s		132	
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	2.03	W
	T_A = +70°C		1.31	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	61	°C/W
	t<10s		43	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	9.3	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	100	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1	µA	V_{DS} = 100V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.0	2.0	3.0	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	116	160	mΩ	V_{GS} = 10V, I_D = 5.0A
			126	200		V_{GS} = 4.5V, I_D =5.0A
Diode Forward Voltage	V_{SD}	—	0.9	1.0	V	V_{GS} = 0V, I_S = 10A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1167	—	pF	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	36	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	25	—	pF	
Gate Resistance	R_g	—	1.3	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	4.9	—	nC	V_{DS} = 80V, I_D = 12.8A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	9.7	—	nC	
Gate-Source Charge	Q_{gs}	—	2.0	—	nC	
Gate-Drain Charge	Q_{gd}	—	2.0	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	10.5	—	ns	V_{DS} = 50V, I_D = 12.8A V_{GS} = 10V, R_G = 25Ω
Turn-On Rise Time	t_R	—	11.1	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	42.6	—	ns	
Turn-Off Fall Time	t_F	—	12.8	—	ns	
Reverse Recovery Time	t_{RR}	—	30.3	—	ns	I_F = 12.8A, di/dt = 100A/µs
Reverse Recovery Charge	Q_{RR}	—	35.2	—	nC	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. UIS in production with L = 1.43mH, T_J = +25°C.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

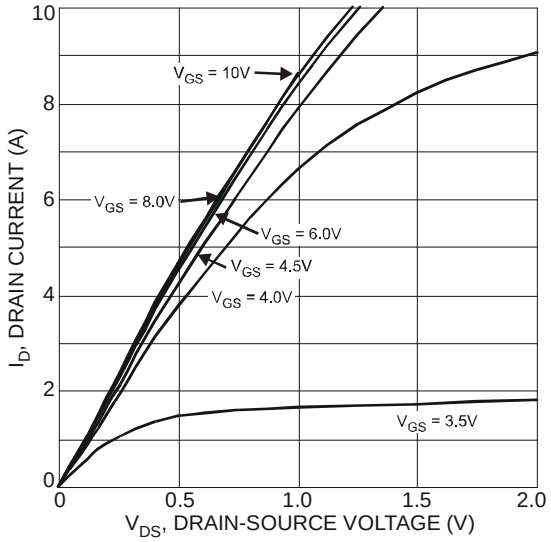


Fig.1 Typical Output Characteristic

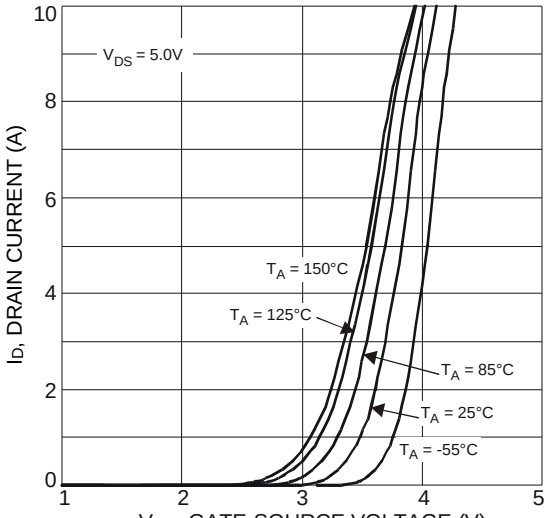


Fig. 2 Typical Transfer Characteristics

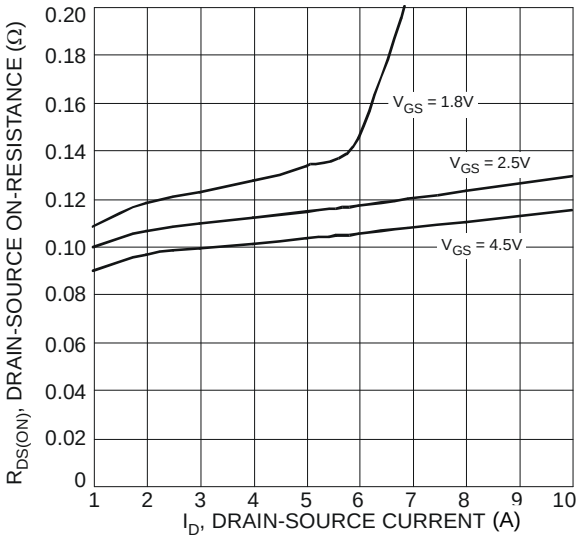


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

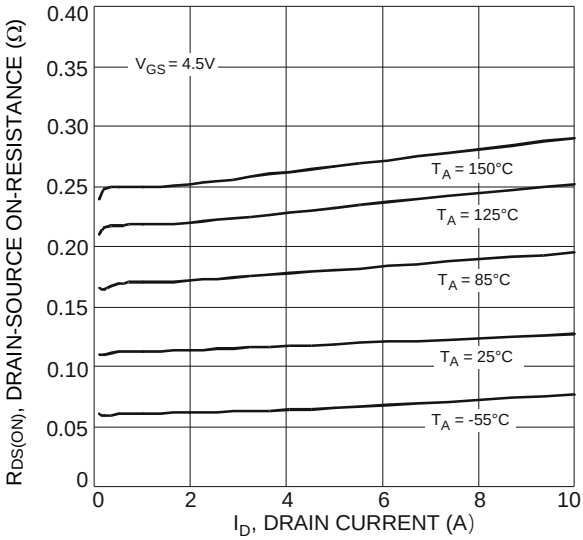


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

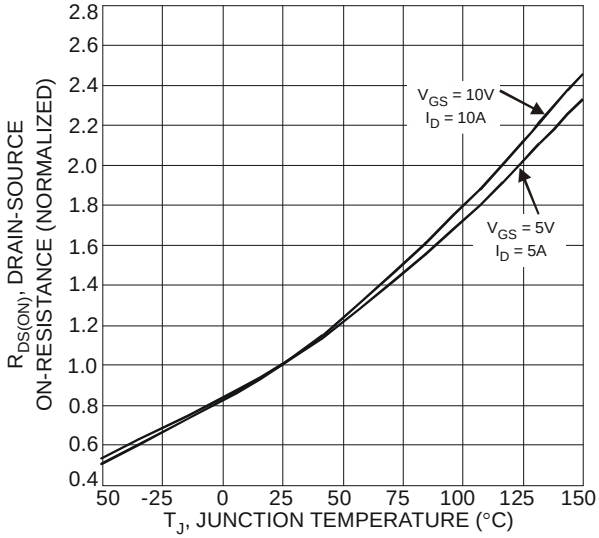


Fig. 5 On-Resistance Variation with Temperature

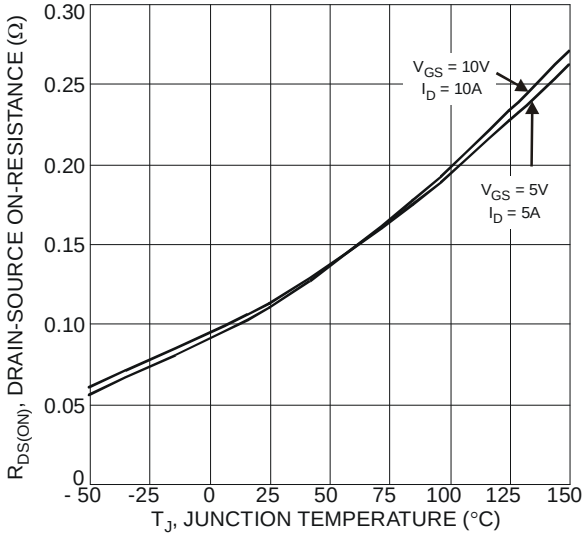


Fig. 6 On-Resistance Variation with Temperature

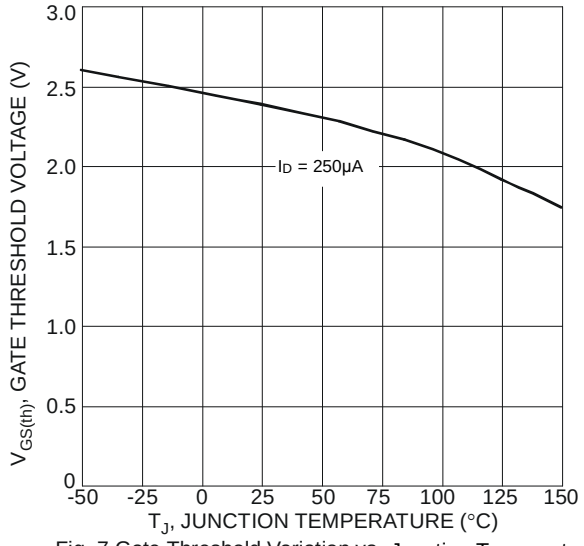


Fig. 7 Gate Threshold Variation vs. Junction Temperature

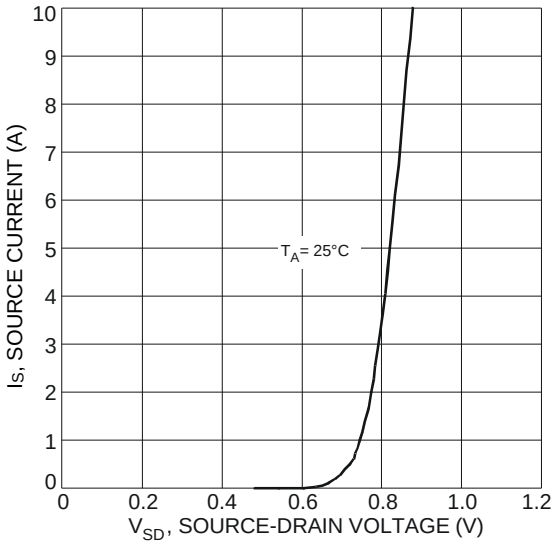


Fig. 8 Diode Forward Voltage vs. Current

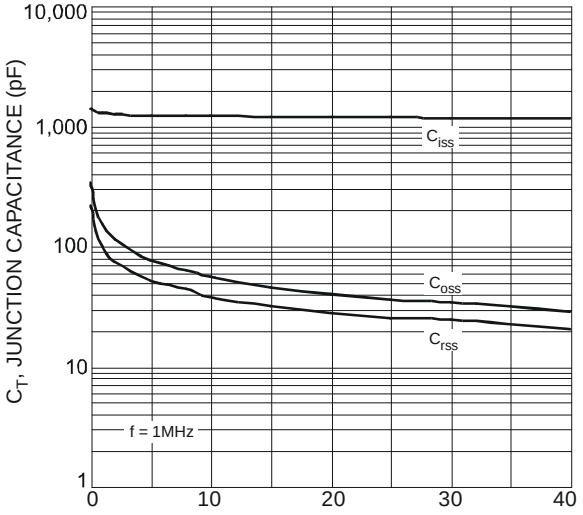


Fig. 9 Typical Junction Capacitance

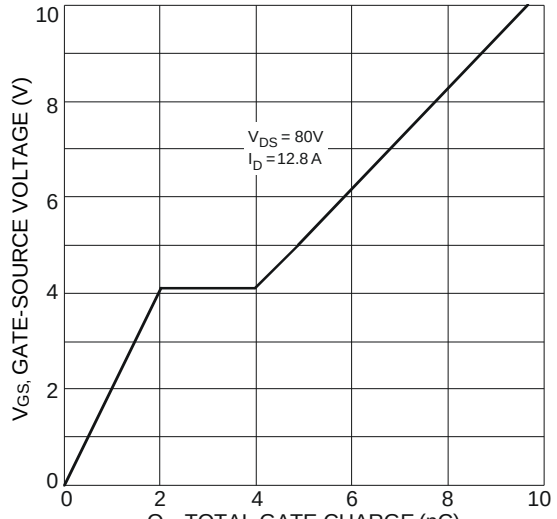


Fig. 10 Gate Charge

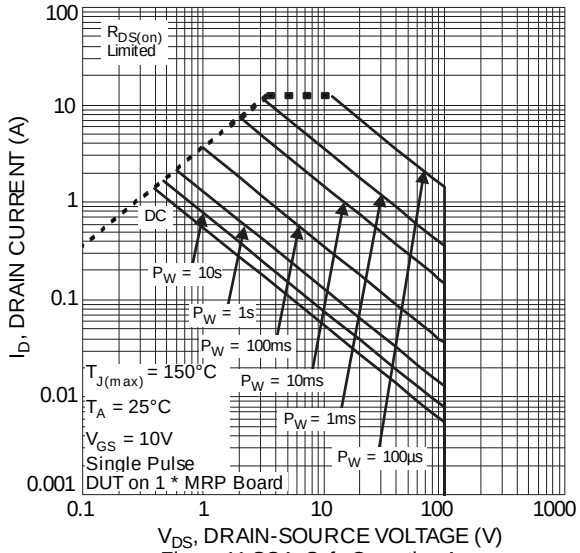


Figure 11 SOA, Safe Operation Area

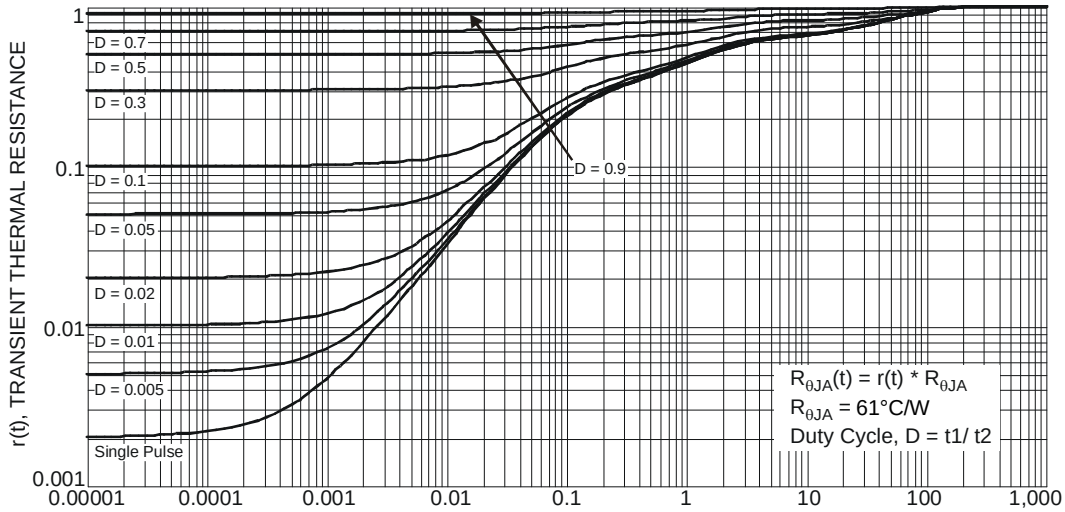
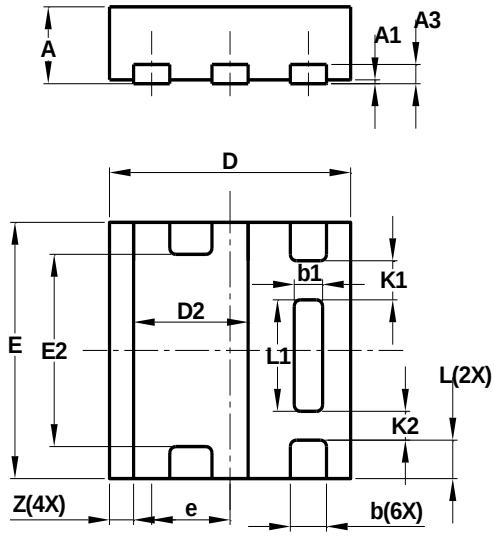


Figure 12 Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type E)

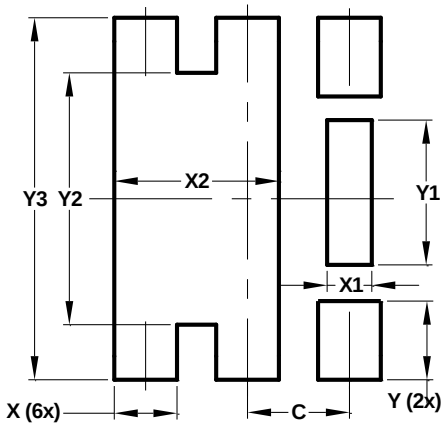


U-DFN2020-6 Type E			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.03
A3	—	—	0.15
b	0.25	0.35	0.30
b1	0.185	0.285	0.235
D	1.95	2.05	2.00
D2	0.85	1.05	0.95
E	1.95	2.05	2.00
E2	1.40	1.60	1.50
e	—	—	0.65
L	0.25	0.35	0.30
L1	0.82	0.92	0.87
K1	—	—	0.305
K2	—	—	0.225
Z	—	—	0.20
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type E)



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.285
X2	1.050
Y	0.500
Y1	0.920
Y2	1.600
Y3	2.300

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