Contents

Architecture Overview

The Block Diagram on page 1 shows the HX3C architecture. HX3C consists of two independent hub controllers (SS and USB 2.0), the Cortex-M0 CPU subsystem, two USB Type-C PD controllers, USB billboard, I^2C interface, and port controller blocks.

USB-PD Controller

HX3C has two USB-PD controllers consisting of a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as the 1.2-V front end. These controllers integrate the required termination resistors to identify the role of the EZ-PD solutions on two Type-C ports of the HX3C device. RD is used to identify a UFP in a dock or a dongle. When configured as a DFP, integrated current sources perform the role of RP or pull-up resistors. These current sources can be programmed to indicate the complete range of current capacity on VBUS defined in the Type-C spec. HX3C PD ports respond to all USB-PD communication.

The USB-PD controller contains a 8-bit Successive Approximation Register (SAR) ADC for analog-to-digital conversions (ADC). The ADC includes a 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses an internal bandgap voltage and an internal voltage proportional to the absolute temperature. All GPIO inputs can be connected to the global Analog Multiplex Busses through a switch at each GPIO that can enable that GPIO to be connected to the mux bus for ADC use. The CC1, and CC2 pins are not available to connect to the mux busses.

SS Hub Controller

This block supports the SS hub functionality based on the USB 3.1 Gen 1 specification. The SS hub controller supports the following:

- SS link power management (U0, U1, U2, U3 states)
- Full-duplex data transmission

USB 2.0 Hub Controller

This block supports the LS, FS, and HS hub functionalities. It includes the repeater, frame timer, and four transaction translators.

The USB 2.0 hub controller block supports the following:

- USB 2.0 link power management (L0, L1, L2, L3 states)
- Suspend, resume, and remote wake-up signaling
- Multi-TT (one TT for each DS port)

USB Billboard

HX3C has integrated USB Billboard controller. This is USB 2.0 certified Full-Speed (12 Mbps) controller, which supports native Billboard device class driver.

CPU

The Cortex-M0 CPUs in HX3C are part of the 32-bit MCU controller, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPUs also include a serial wire debug (SWD) interface, which is a two-wire form of JTAG.

Flash

HX3C has one flash module each for both USB-PD controllers and one for Billboard; with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

I^2C Interfaces

HX3C supports two I^2C interfaces, which supports I^2C slave, master and multi-master configurations. One of the I^2C interfaces is used for configuration of the hub during boot-up. Configuration can be from an external I^2C EEPROM or from an external I^2C master. Second I^2C interface shall be used to configure external I^2C slave device from HX3C.

Port Controller

The port controller block controls the DS port power to comply with the BC v1.2 and USB 3.1 Gen 1 specifications. Control signals for external power switches are implemented within the chip. HX3C controls the external power switches at power-on to reduce in-rush current.

Applications

- Docking stations for notebook PCs and tablets
- PC motherboards, servers
- Digital TV, monitors
- Retail hub boxes
- Printers, scanners
- Set-top boxes, home gateways, routers, game consoles
- Dongles and adapters

HX3C Product Options

Table 1. HX3C Product Options

Features	CYUSB3333 (Dongle-DRP)	CYUSB3343 (Dock-DFP)
Application	Dongles	Self-powered Docks, Monitors
Number of DS ports	3 (USB 3.0)	3 (USB 3.0)
Battery Charging on DS ports	Apple/BC v1.2	Apple/BC v1.2
External Power Switch Control	Individual or Ganged	Individual or Ganged
Number of I2C ports	2	2
Number of PD/Type-C ports	2	2
PD port-1 power role	DRP	DRP
PD port-2 power role	DRP	DFP
Termination Resistor on CC1 line of PD port-1	R_P[1], R_D[1]	R_P[1], R_D[1]
Termination Resistor on CC2 line of PD port-1	R_A[2]	R_P[1], R_D[1]
Termination Resistor on CC1 line of PD port-2	R_P[1], R_D[1]	R_p[3]
Termination Resistor on CC2 line of PD port-2	R_P[1], R_D[1]	R_p[3]
Billboard device	Yes	Yes
Package	121-ball BGA	121-ball BGA
Temperature range	Industrial and Commercial	Industrial and Commercial

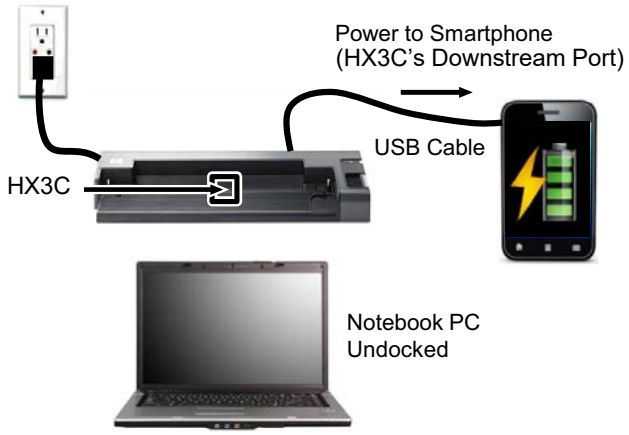
Notes
1. Termination resistor denoting the PD port as dual role port for power, power provider/consumer.
2. Termination resistor denoting the PD port as a VCONN powered accessory.
3. Termination resistor denoting the PD port as downstream facing port, power provider only.

Product Features

Ghost Charge in Type-A DS Port

Ghost Charge is a Cypress-proprietary feature for charging USB devices on the DS port when the US port is not connected to a host. For example, in a docking station with HX3C as shown in Figure 1, when the laptop is undocked, HX3C will emulate a dedicated charging port (DCP) to provide charge to a phone connected on a Type-A DS port.

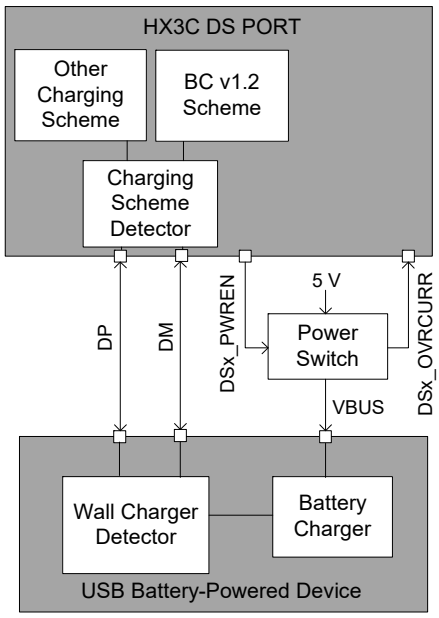
Figure 1. Ghost Charge



Charge a smartphone without docking the notebook

When the US port is disconnected from the host, HX3C detects if any of the DS ports are connected to a device requesting charging. It determines the charging method and then switches to the appropriate signaling based on the detected charging specification as shown in Figure 2. The hub either emulates a USB-compliant dedicated charging port by connecting DP and DM (see the BC v1.2 specification) or other supported proprietary charging schemes.

Figure 2. Ghost Charge Implementation in HX3C



Ghost Charge is enabled by default and can be disabled through configuration. Refer to Hub Configuration Options on page 11.

Vendor-Command Support

The hub supports vendor-specific requests and can also enumerate as a vendor-specific device. The vendor-specific request can be used to (a) bridge USB and I^2C and (b) configure HX3C. This feature can be used for the following applications:

- Firmware upgrade of an external ASSP connected to HX3C through USB
- In-System programming (ISP) of an EEPROM connected to HX3C through USB

Pin Information

Figure 3. HX3C 121-ball BGA Pinout for CYUSB3333/CYUSB3343

	1	2	3	4	5	6	7	8	9	10	11
A	DS4_DM	DS4_DP	AVDD33	DS2_DM	DS2_DP	AVDD33	DS1_DM	DS1_DP	VSS	US_DM	US_DP
B	DS2_OVRCURR	DVDD12	DS3_OVRCURR	VSS	AVDD12	VDDIO	AVDD33	VSS	XTAL_IN	VSS	DVDD12
C	US_TXM	DS4_OVRCURR	DS3_DP	DS3_DM	DS3_GREEN	DS1_PWREN	SWDCLK_BB	VCCD_BB	XTAL_OUT	GPIO2	DS1_RXP
D	US_TXP	MODE_SEL[1]	DS2_PWREN	RESET_N	AVDD12	DVDD12	XRES_BB	I2C_SDA2	VSS	SWDIO_BB	DS1_RXM
E	DVDD12	AVDD33	SWDCLK	USB2_RESREF	VSS	XRES_P1	I2C_SCL2	DS1_OVRCURR	GPIO1	GPIO6	VSS
F	US_RXM	SUSPEND	USB3_RESREF	MODE_SEL[0]	DS4_PWREN	DS4_GREEN	I2C_SDA	VDDIO_BB	GPIO5	DVDD12	DS1_TXM
G	US_RXP	SWDIO	VDD_EFUSE	VBUS_US	VBUS_DIS-CHARGE_P1	VBUS_DIS-CHARGE_P2	AVDD12	GPIO0	VSEL1_P2	VBUS_MON_P2	DS1_TXP
H	AVDD12	DS2_GREEN	VBUS_DS	CC2/VCONN1_P1	VSEL2_P1	HOTPLUG_-DET_P2	VBUS_MON_P1	GPIO7	VBUS_P_C-TRL_P1	VBUS_C_C-TRL_P2	DVDD12
J	DS4_TXP	VDDIO_P1	CC1_P1	SWDIO_P1	VBUS_C_C-TRL_P1	VSEL2_P2	CC1_P2	CC2_P2	XRES_P2	VBUS_P_C-TRL_P2	DS2_RXP
K	DS4_TXM	VSS	AVDD12	VDDD_P1	VSEL1_P1	SWDCLK_P1	SWDIO_P2	VDDIO_P2	VSS	VSS	DS2_RXM
L	DVDD12	DS4_RXM	DS4_RXP	VSS	VCCD_P1	HOTPLUG_-DET_P1	VCCD_P2	I2C_SCL	DS2_TXP	DS2_TXM	SWDCLK_P2

Pin Description

Table 2. 121-ball BGA Pinout for CYUSB3333/CYUSB3343

Pin Name	Type	Ball #	Description
USB 3.0 Upstream Port			
US_RXP	I	G1	Upstream port SuperSpeed receive plus
US_RXM	I	F1	Upstream port SuperSpeed receive minus
US_TXP	O	D1	Upstream port SuperSpeed transmit plus
US_TXM	O	C1	Upstream port SuperSpeed transmit minus
US_DP	I/O	A11	Upstream port USB 2.0 data plus
US_DM	I/O	A10	Upstream port USB 2.0 data minus
USB 3.0 Downstream Port 1			
DS1_RXP	I	C11	Downstream port 1 SuperSpeed receive plus
DS1_RXM	I	D11	Downstream port 1 SuperSpeed receive minus
DS1_TXP	O	G11	Downstream port 1 SuperSpeed transmit plus
DS1_TXM	O	F11	Downstream port 1 SuperSpeed transmit minus
DS1_DP	I/O	A8	Downstream port 1 USB 2.0 data plus
DS1_DM	I/O	A7	Downstream port 1 USB 2.0 data minus
DS1_OVRCURR	I	E8	Downstream port 1 Active low Over current detect
DS1_PWREN	O	C6	Downstream port 1 Active low VBUS Power enable
USB 3.0 Downstream Port 2			
DS2_RXP	I	J11	Downstream port 2 SuperSpeed receive plus
DS2_RXM	I	K11	Downstream port 2 SuperSpeed receive minus
DS2_TXP	O	L9	Downstream port 2 SuperSpeed transmit plus
DS2_TXM	O	L10	Downstream port 2 SuperSpeed transmit minus
DS2_DP	I/O	A5	Downstream port 2 USB 2.0 data plus
DS2_DM	I/O	A4	Downstream port 2 USB 2.0 data minus
DS2_OVRCURR	I	B1	Downstream port 2 Active low Over current detect
DS2_PWREN	O	D3	Downstream port 2 Active low VBUS Power enable
DS2_GREEN	O	H2	Downstream port 2 USB 2.0 Green LED indicator
USB 3.0 Downstream Port 3			
DS3_DP	I/O	C3	Downstream port 3 USB 2.0 data plus This pin is NC when Billboard function is used
DS3_DM	I/O	C4	Downstream port 3 USB 2.0 data minus This pin is NC when Billboard function is used
DS3_OVRCURR	I	B3	Downstream port 3 Active low Over current detect Pull-up this pin to 3.3 V when Billboard function is used
DS3_GREEN	O	C5	Downstream port3 USB 2.0 Green LED indicator
USB 3.0 Downstream Port 4			
DS4_RXP	I	L3	Downstream port 4 SuperSpeed receive plus
DS4_RXM	I	L2	Downstream port 4 SuperSpeed receive minus
DS4_TXP	O	J1	Downstream port 4 SuperSpeed transmit plus
DS4_TXM	O	K1	Downstream port 4 SuperSpeed transmit minus
DS4_DP	I/O	A2	Downstream port 4 USB 2.0 data plus
DS4_DM	I/O	A1	Downstream port 4 USB 2.0 data minus
DS4_OVRCURR	I	C2	Downstream port 4 Active low Over current detect

Table 2. 121-ball BGA Pinout for CYUSB3333/CYUSB3343 *(continued)*

Pin Name	Type	Ball #	Description
DS4_PWREN	O	F5	Downstream port 4 Active low VBUS Power enable
DS4_GREEN	O	F6	Downstream port 4 USB 2.0 Green LED indicator
Precision Resistors			
USB2_RESREF	A	E4	Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY.
USB3_RESREF	A	F3	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration.
PD Controller Port 1			
CC1_P1	A	J3	USB PD port 1 connector detect/Configuration Channel 1
CC2/VCONN1_P1	A	H4	CYUSB3333: USB PD port 1 VCONN1 input (4.0 V to 5.5 V) CYUSB3343: USB PD port 1 connector detect/Configuration Channel 2
VBUS_MON_P1	A	H7	VBUS monitor for PD port 1, connect PD port 1 VBUS through 100K:10K resistor divider network
VBUS_P_CTRL_P1	I/O	H9	GPIO, used for controlling provider power switch of PD port 1
VBUS_C_CTRL_P1	I/O	J5	GPIO, used for controlling consumer power switch of PD port 1
VBUS_DISCHARGE_P1	I/O	G5	GPIO, used for controlling VBUS discharge switch of PD port 1
VSEL1_P1	I/O	K5	GPIO, used for selecting VBUS voltage level of PD port 1
VSEL2_P1	I/O	H5	GPIO, used for selecting VBUS voltage level of PD port 1
HOTPLUG_DET_P1	I/O	L6	GPIO, used as Hot plug detect input from display port of PD port 1
PD Controller Port 2			
CC1_P2	A	J7	USB PD port 2 connector detect/Configuration Channel 2
CC2_P2	A	J8	USB PD port 2 connector detect/Configuration Channel 2
VBUS_MON_P2	A	G10	VBUS monitor for PD port 2, connect PD port 2 VBUS through 100K:10K resistor divider network
VBUS_P_CTRL_P2	I/O	J10	GPIO, used for controlling provider power switch of PD port 2
VBUS_C_CTRL_P2	I/O	H10	GPIO, used for controlling consumer power switch of PD port 2
VBUS_DISCHARGE_P2	I/O	G6	GPIO, used for controlling VBUS discharge switch of PD port 2
VSEL1_P2	I/O	G9	GPIO, used for selecting VBUS voltage level of PD port 2
VSEL2_P2	I/O	J6	GPIO, used for selecting VBUS voltage level of PD port 2
HOTPLUG_DET_P2	I/O	H6	GPIO, used as Hot plug detect input from display port of PD port 2
Mode select, Clock and Reset			
MODE_SEL[0]	I	F4	Hub firmware source MODE_SEL[1:0] = 11: Internal ROM firmware MODE_SEL[1:0] = 01: Firmware from external I2C EEPROM MODE_SEL[1:0] = 10: Firmware from external I2C Master MODE_SEL[1:0] = 00: Reserved, do not use this mode
MODE_SEL[1]	I	D2	
XTAL_OUT	A	C9	Crystal out
XTAL_IN	A	B9	Crystal In
RESET_N	I	D4	Active Low reset input of hub controller
XRES_P1	I	E6	Active Low reset input of port1 PD controller
XRES_P2	I	J9	Active Low reset input of port 2 PD controller
XRES_BB	I	D7	Active Low reset input of Billboard device
I2C, Debug, and GPIOs			
I2C_SCL	I/O	L8	I2C Clock, connect to I2C EEPROM to download hub firmware
I2C_SDA	I/O	F7	I2C Data, connect to I2C EEPROM to download hub firmware
I2C_SCL2	I/O	E7	GPIO, used as I2C clock for configuring DP/Flip MUX on Type-C ports
I2C_SDA2	I/O	D8	GPIO, used for I2C data for configuring DP/Flip MUX on Type-C ports

Table 2. 121-ball BGA Pinout for CYUSB3333/CYUSB3343 *(continued)*

Pin Name	Type	Ball #	Description
SWDCLK	I/O	E3	GPIO, used as SWD clock input for hub
SWDIO	I/O	G2	GPIO, used as SWD data I/O for hub
SWDCLK_P1	I/O	K6	GPIO, used as SWD clock input for port1 PD controller
SWDIO_P1	I/O	J4	GPIO, used as SWD data I/O for port1 PD controller
SWDCLK_P2	I/O	L11	GPIO, used as SWD clock input for port2 PD controller
SWDIO_P2	I/O	K7	GPIO, used as SWD data I/O for port2 PD controller
SWDCLK_BB	I/O	C7	GPIO, used as SWD clock input for Billboard device
SWDIO_BB	I/O	D10	GPIO, used as SWD data I/O for Billboard device
GPIO0	I/O	G8	GPIO
GPIO1	I/O	E9	GPIO
GPIO2	I/O	C10	GPIO
GPIO5	I/O	F9	GPIO
GPIO6	I/O	E10	GPIO
GPIO7	I/O	H8	GPIO
SUSPEND		F2	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state
Power Supply			
VBUS_US	PWR	G4	This pin must be connected to VBUS from Type-B port. For Type-C port this pin should be connected to 5 V on Type-C attach and to GND on deattach.
VBUS_DS	PWR	H3	This pin is used to power the Apple-charging circuit. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5-V supply.
VDD_EFUSE	PWR	G3	1.2 V for normal operation, 2.5 V for eFuse programming. Customers should connect this pin to 1.2 V
DVDD12	PWR	B2, B11, D6, E1, F10, H11, L1	1.2-V digital supply
AVDD12	PWR	B5, D5, G7, H1, K3	1.2-V analog supply
AVDD33	PWR	A3, A6, B7, E2	3.3-V analog supply
VDDIO	PWR	B6	3.3-V I/O supply
VDDIO_P1	PWR	J2	
VDDIO_P2	PWR	K8	
VDDIO_BB	PWR	F8	
VDDD_P1	PWR	K4	CYUSB3343: Connect to 3.3-V power supply CYUSB3333: Connect to VCONN1/5-V power supply
VCCD_P1	PWR	L5	1.8-V regulator output of port 1 PD controller. This pin should be decoupled to ground using a 1-µF
VCCD_P2	PWR	L7	1.8-V regulator output of port 2 PD controller. This pin should be decoupled to ground using a 1-µF
VCCD_BB	PWR	C8	1.8-V regulator output of Billboard device. This pin should be decoupled to ground using a 1-µF
VSS	PWR	A9, B4, B8, B10, D9, E11, E5, K10, K2, K9, L4	Supply ground

System Interfaces

Upstream Port (US)

The HX3C US port can function in Type-C or Type-B modes. This port includes an integrated 1.5-kΩ pull-up resistor and termination resistors.

Downstream Ports (DS1, 2, 3, 4)

One HX3C DS port works in Type-C mode and remaining ports work in Type-A mode. Selection of Type-C port is made by firmware at the time of device boot-up. The DS ports integrate 15-kΩ pull-down and termination resistors. Type-A DS ports can be disabled or enabled, and can be set to removable or non-removable options. BC v1.2 charging is enabled by default on Type-A DS ports and can be disabled using the configuration options (see Hub Configuration Options). DS3 is internally connected to Billboard device. This port can be used for external connection if Billboard device is disabled.

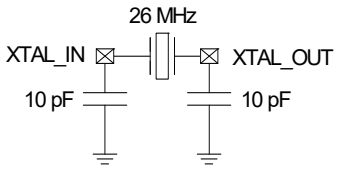
Communication Interfaces (I^2C)

There are two I^2C interfaces. The interfaces follow the Inter-IC Bus specification, version 3.0, with support for the standard mode (100 kHz) and the fast mode (400 kHz) frequencies. HX3C supports I^2C in the slave and master modes. The I^2C interface supports the multi-master mode of operation. Both the SCL and SDA signals require external pull-up resistors based on the specification. VDD_IO for HX3C is 3.3 V and I^2C pull-up resistors shall be connected to the same supply.

Oscillator

HX3C requires an external crystal with a frequency of 26 MHz and an accuracy of ±150 ppm in parallel resonant, fundamental mode. The crystal drive circuit is capable of a low-power drive level (<200 µW). The crystal connection to the XTAL_OUT and XTAL_IN pins is shown in Figure 4.

Figure 4. Crystal Connection



Power Control

The DS[1, 2 or 4]_PWREN and DS[1, 2, 3 or 4]_OVRCURR pins interface HX3C to external power switches. These pins are used to control power switches for DS port power and monitor overcurrent conditions. The power switch polarity and the power control mode can be changed using the configuration options.

Reset

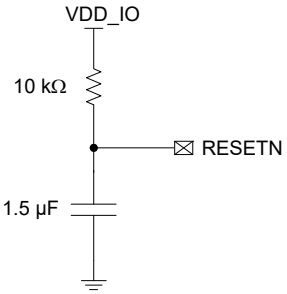
There are four reset pins for the HX3C device. These pins control independently reset operations for Hub controller, two USBPD controllers and Billboard section of the product. If any particular section of the device function not required, then that section alone can be kept in reset by asserting correspond reset pin to LOW.

HX3C operates with two external power supplies, 3.3 V and 1.2 V. There is no power sequencing requirement between these two supplies. However, all reset pins should be held LOW until both these supplies become stable.

The reset pins can be tied to VDD_IO through an external resistor and to ground (GND) through an external capacitor (minimum 5 ms time constant), as shown in Figure 5. This creates a clean reset signal for power-on reset (POR). If power-supply (VDD_IO supply) to RC circuit has a slow ramp-up, the ramp-up time of the power-supply has to be added to the Reset time-constant. For example, If power supply to VDD_IO has a ramp-up of 2 ms to reach valid range, then minimum time-constant should be higher than 7 ms (2 ms+5 ms).

HX3C does not support internal brown-out detection. If the system requires this feature, an external reset should be provided on the reset pins when supplies are below their valid operating ranges.

Figure 5. Reset Connection



Hub Configuration Mode Select

Configuration options are selected through the MODE_SEL pins. After power-up, these pins are sampled by an on-chip bootloader to determine the configuration options (see Table 3).

Table 3. Hub Boot Sequence

MODE SEL[1]	MODE SEL[0]	Hub Configuration Modes
0	0	Reserved. Do not use this mode.
1	1	Internal ROM configuration.
0	1	I^2C Master, read configuration from I^2C EEPROM.
1	0	I^2C Slave, configure from an external I^2C Master.

Hub Configuration Options

The Hub can be configured by using one of the following:

- External I²C slave such as an EEPROM
- External I²C master

I²C Configuration

When enabled for I²C configuration through the MODE_SEL pins (See Table 3 on page 10), HX3C can be configured as an I²C master or as an I²C slave using I2C_SCL and I2C_SDA pins. Hub's configuration data is a maximum of 197 bytes and Hub's firmware is 10 KB. Note that Hub's firmware also includes configuration settings.

HX3C as I²C Master

HX3C reads configurations from an external I²C EEPROM with sizes ranging from 16 to 64 KB using I2C_SCL and I2C_SDA pins. An example of a supported EEPROM is 24LC128. Based on the contents of the bSignature and bImageType fields in Table 4 on page 11, HX3C performs one of the following actions:

- Loads custom configuration settings from the EEPROM when bSignature is "CY" and bImageType is 0xD4.
- Loads the Cypress-provided firmware from the EEPROM when bSignature is "CY" and bImageType is 0xB0. This firmware also includes configuration settings.
- If bSignature ≠ "CY", the Hub enumerates in the vendor-specific mode.

The contents of the EEPROM can be updated with the easy-to-use Cypress Blaster Plus tool. Blaster Plus is a GUI-based tool to configure HX3C. This tool allows to do the following:

- Download the Cypress-provided firmware from a PC via HX3C's US port and store it on an EEPROM connected to HX3C's I²C port.
- Read the configuration settings from the EEPROM. These settings are displayed in the Blaster Plus GUI. Modify settings as required.
- Write back the updated settings on to the EEPROM. In addition, an image file can be created for external use.

The Blaster Plus tool, user guide, and the Cypress-provided firmware are available at www.cypress.com/hx3.

HX3C as I²C Slave

An external I²C master can program the configuration settings into the Hub according to the EEPROM map in Table 4 on page 11. Alternatively, the Hub firmware (<10 KB), which includes configuration settings, can also be programmed. It is recommended to use the Blaster Plus tool to create the HX3C firmware or configuration image file. Hub's I²C slave address needs to be provided while creating the image file.

Table 4. EEPROM Map

I²C Offset	Bits	Name	Default	Description
0	7:0	bSignature LSB ("C")	0x43	The first byte of the 2-byte signature initialized with "CY" ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device.
1	7:0	bSignature MSB ("Y")	0x59	The second byte of the 2-byte signature initialized with "CY" ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device.
2	7:6	bImageCTL	b'00	Reserved
	5:4	I²C Speed	b'11	b'01: 400 kHz b'11: 100 kHz
	3:1	bImageCTL	b'000	Reserved
	0	bImageCTL	0	0: Execution binary file 1: Data file
3	7:0	bImageType	0xD4	0xD4: Load only configuration 0xB0: Load firmware boot image All other bImageType will return an error code.
4	7:0	bD4Length	40	bD4Length is defined in bytes as the length from offset 5. I²C offset bytes 0–4 are the header bytes. bD4Length = 6: Only update VID, PID, and DID bD4Length = 18: Configuration options (no PHY trim) bD4Length = 40: Configuration options with PHY trim options bD4Length > 40: User must provide valid string descriptors bD4Length > 192: Error
5	7:0	VID [7:0]	0xB4	Custom Vendor ID - LSB
6	7:0	VID [15:8]	0x04	Custom Vendor ID - MSB

Table 4. EEPROM Map *(continued)*

I²C Offset	Bits	Name	Default	Description
7	7:0	PID [7:0]	0x04	Custom Product ID (PID) Default: 0x6504 If separate PID is used for USB 2.0, the USB 2.0 PID will be read from offset 35 and 36. Else, USB 2.0 PID = PID+2; Default: 0x6506
8	7:0	PID [15:8]	0x65	
9	7:0	DID [7:0]	00	Custom Device ID - revision - LSB
10	7:0	DID [15:8]	50	Custom Device ID - revision - MSB
11	7:0	Reserved	0	Reserved
12	7:4	Reserved	b'0000	Reserved
	3:0	SHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a SuperSpeed port is active. bit[3:0] = DS4, Reserved, DS2, DS1 0: Not active 1: Active
13	7:0	POWER_ON_TIME	0x32	Time (in 2-ms intervals) from the time the power-on sequence begins on a port until power is good on that port (bPwron2PwrGood)
14	7:4	REMOVABLE_PORTS [3:0]	b'1011	Indicates if the port is removable. bit[7:4] = DS4, DS3, DS2, DS1 0: Non-removable 1: Removable
	3:0	UHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a USB 2.0 port is active. bit[3:0] = DS4, DS3, DS2, DS1 0: Not active 1: Active
15	7:4	Reserved	0	Reserved
	3	COMPOUND_HUB	1	Identifies a compound device. 0: Hub is not part of a compound device. 1: Hub is part of a compound device.
	2:1	Reserved	0	Reserved
	0	GANG	0	1: Ganged power switch enable for all DS ports 0: Individual port power switch enable for each DS port
16	7	SUSPEND_INDICATOR_DISABLE	0	0: Suspend indicator enabled 1: Suspend indicator disabled
	6	SS_US_DISABLE	0	Hub mode of operation (USB 3.0 or USB 2.0) 0: USB 3.0 hub and USB 2.0 hub enabled 1: USB 3.0 hub disabled and USB 2.0 hub enabled
	5	PWR_EN_POLARITY	0	Power switch control output polarity 0: Active LOW 1: Active HIGH
	4:0	PORT_POLARITY	b'00000	USB 2.0 DP and DM swapped bit[4:0] = DS4, DS3, DS2, DS1, US 1: Port polarity swapped 0: Port polarity not swapped
17	7:5	Reserved	0	Reserved
	4	BC_ENABLE	1	0: BC v1.2 disabled 1: BC v1.2 enabled
	3	ACA_DOCK	0	If this bit is set, enable ACA-Dock on the US port
	2	APPLE_XA	0	0: Max limit for Apple charging 2.1 A 1: Max limit for Apple charging 1 A
	1	Reserved	0	Reserved
	0	GHOST_CHARGE_EN	1	0: Ghost Charging disabled 1: Ghost Charging enabled
18	7:4	CDP_EN[3:0]	b'1111	Per-port charging setting bit[7:4] = DS4, DS3, DS2, DS1 0: CDP disabled 1: CDP enabled
	3:0	DCP_EN[3:0]	b'0000	Per-port charging setting bit[3:0] = DS4, DS3, DS2, DS1 0: DCP disabled 1: DCP enabled

Table 4. EEPROM Map *(continued)*

I²C Offset	Bits	Name	Default	Description
19	7	EMBEDDED_HUB	0	If this bit is set, the US is as an embedded port and VBUS connected to VBUS_US pin is ignored.
	6	ILLEGAL_DESCRIPTOR	1	If this bit is set, the USB 2.0 hub controller will accept both 0x00 and 0x29 as valid descriptor types. If '0', only 0x29 will be accepted as a valid descriptor type.
	5	Reserved	1	Reserved
	4	OC_POLARITY	0	Overcurrent input polarity 0: Active LOW 1: Active HIGH
	3:0	OC_TIMER	b'1000	Time in milliseconds for which the overcurrent inputs will be filtered
20	7:0	Reserved	0	Reserved
21	7:4	Reserved	0	Reserved
	3	STRING_DESCRIPTOR_ENABLE[4]	0	0: String descriptor support is disabled 1: String descriptor support is enabled When string descriptors are not supported, the hub controller returns a non-zero index (compile-time programmable) for each string which is supported, and 0x00 for each string not supported, as indicated by this field.
	2:0	Reserved	0	Reserved
22	7:0	Reserved	0	Reserved
23	7:6	HS_AMPLITUDE_DS4	b'00	HS driver amplitude control; HS driver current: +0% to +7.5% b'00: Default b'01: +2.5% b'10: +5% b'11: +7.5%
	5:4	HS_AMPLITUDE_DS3	b'00	
	3:2	HS_AMPLITUDE_DS2	b'00	
	1:0	HS_AMPLITUDE_DS2	b'00	
24	7:6	HS_AMPLITUDE_US	b'00	
	5:2	HS_SLOPE	b'0100	HS driver slope control for all ports b'0000: +15% b'0001: +5% b'0100: Default b'0101: -5% b'1111: -7.5%
	1:0	HS_TX_VREF	b'10	Reference voltage for HS squelch (transmission envelope detector) for all ports b'00: 96 mV b'01: 108 mV b'10: 120 mV b'11: 132 mV
25	7:3	HS_PREEMP_EN[4:0]	b'00000	HS driver pre-emphasis enable – for ports DS4, DS3, DS2, DS1, and US 0: pre-emphasis is disabled 1: pre-emphasis is enabled
	2	HS_PREEMP_DEPTH_DS4[5]	0	HS driver pre-emphasis depth 0: +10% 1: +20%
	1	HS_PREEMP_DEPTH_DS3[5]	0	
	0	HS_PREEMP_DEPTH_DS2[5]	0	
26	7	HS_PREEMP_DEPTH_DS1[5]	0	
	6	HS_PREEMP_DEPTH_US[5]	0	
	5	Reserved	1	Reserved
	4:1	PCS_TX_DEEMPH_DS4	0x6	USB 3.0 Tx driver de-emphasis value 0x3: –2.75 dB 0x6: –3.4 dB (Default) 0x9: –4.0 dB
	0	Reserved	0	Reserved

Notes
4. When the string descriptor supports LangID, Manufacturer, Product and Serial Number, the serial number must be unique for each device.
5. HS_PREEMP_DEPTH is valid only when corresponding HS_PREEMP_EN is set for that port.

Table 4. EEPROM Map *(continued)*

I²C Offset	Bits	Name	Default	Description
27	7:4	Reserved	0x6	USB 3.0 Tx driver de-emphasis value 0x3: –2.75 dB 0x6: –3.4 dB (Default) 0x9: –4.0 dB
	3:0	PCS_TX_DEEMPH_DS2	0x6	
28	7:4	PCS_TX_DEEMPH_DS1	0x6	
	3:0	PCS_TX_DEEMPH_US	0x6	
29	7	Reserved	0	Reserved
	6	Reserved	1	Reserved
	5:0	PCS_TX_SWING_FULL_DS4	0x29	Adjust launch amplitude of the transmitter 0x1F - 0.9 V 0x29 - 1.0 V (Default) 0x35 - 1.1 V 0x3F - 1.2 V
30	7:6	Reserved	0	Reserved
	5:0	Reserved	0x29	Reserved
31	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS2	0x29	Adjust launch amplitude of the transmitter 0x1F - 0.9 V 0x29 - 1.0 V (Default) 0x35 - 1.1 V 0x3F - 1.2 V
32	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS1	0x29	Adjust launch amplitude of the transmitter 0x1F - 0.9 V 0x29 - 1.0 V (Default) 0x35 - 1.1 V 0x3F - 1.2 V
33	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_US	0x29	Adjust launch amplitude of the transmitter 0x1F - 0.9 V 0x29 - 1.0 V (Default) 0x35 - 1.1 V 0x3F - 1.2 V
34	7:0	Reserved	0	Reserved
35	7:0	UHC_PID [7:0]_LSB	0x06	USB 2.0 PID. If bD4Length ≥ 40, USB 2.0 PID will be read from this location.
36	7:0	UHC_PID [15:8]_MSB	0x65	
37–44	7:0	Reserved	0	Eight bytes reserved for future expansion
45	7:0	bLength: LangID	4	Size of LangID (defined by spec as N + 2)
46	7:0	DescType	3	String descriptor type (constant value)
47	7:0	LangID - MSB	9	String language ID - MSB of wLangID
48	7:0	LangID - LSB	4	String language ID - MSB of wLangID
49	7:0	bLength: Manufacturer (X)	54	Manufacturer string length (“bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number” should be less than or equal to 152 bytes). X ≤ 66.
50	7:0	DescType	3	String descriptor type (constant value)
51	7:0	bString: Manufacturer	‘2’, 0, ‘0’, 0, ‘1’, 0, ‘4’, 0, ‘ ‘, 0, ‘C’, 0, ‘y’, 0, ‘p’, 0, ‘r’, 0, ‘e’, 0, ‘s’, 0, ‘s’, 0, ‘ ‘, 0, ‘S’, 0, ‘e’, 0, ‘m’, 0, ‘i’, 0, ‘c’, 0, ‘o’, 0, ‘n’, 0, ‘d’, 0, ‘u’, 0, ‘c’, 0, ‘t’, 0, ‘o’, 0, ‘r’, 0	Manufacturer string: UNICODE UTF-16LE per USB 2.0 specification: “2014 Cypress Semiconductor”
49 + X	7:0	bLength: Product (Y)	22	Product string length (“bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number” should be less than or equal to 152 bytes). Y ≤ 66.
50 + X	7:0	DescType	3	String descriptor type (constant value)
51 + X	7:0	bString: Product	‘C’, 0, ‘Y’, 0, ‘-’, 0, ‘H’, 0, ‘X’, 0, ‘3’, 0, ‘ ‘, 0, ‘H’, 0, ‘U’, 0, ‘B’, 0	Product string: UNICODE UTF-16LE per USB 2.0 specification: “CY-HX3 HUB”

Table 4. EEPROM Map *(continued)*

I²C Offset	Bits	Name	Default	Description
49 + X + Y	7:0	bLength: Serial Number (Z)	22	Serial number string length (“bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number” should be less than or equal to 152 bytes). Z ≤ 66.
50 + X + Y	7:0	DescType	3	String descriptor type (constant value)
51 + X + Y	7:0	bString: Serial Number	‘1’, 0, ‘2’, 0, ‘3’, 0, ‘4’, 0, ‘5’, 0, ‘6’, 0, ‘7’, 0, ‘8’, 0, ‘9’, 0, ‘A’, 0	Serial number string: UNICODE UTF-16LE per USB 2.0 specification: “123456789A”

EMI

HX3C meets the EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. HX3C tolerates EMI conducted by aggressors outlined by the above specifications and continues to function as expected.

ESD

HX3C has a built-in ESD protection on all pins. The ESD protection level provided on these ports is 2.2 kV Human Body Model (HBM) based on the JESD22-A114 specification.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature..... –65 °C to +150 °C

Operating temperature ..... –40 °C to +85 °C

Electrostatic discharge voltage ..... 2200 V

Oscillator or crystal frequency ..... 26 MHz ±150 ppm

I/O voltage supply .....3 V to 3.6 V

Maximum input sink current per I/O ..... 4 mA

Electrical Specifications

HX3C meets all USB-IF Electrical Compliance specifications.

DC Electrical Characteristics

Table 5. DC Electrical Characteristics

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Power supply Voltage Specs						
VDD_EFUSE	eFuse supply	1.14	1.2	1.26	V	Normal operation
		2.5	2.6	2.7	V	Programming
VBUS	VBUS supply voltage	4.35	5.0	5.5	V	–
DVDD12	1.2 V core supply	1.14	1.2	1.26	V	–
AVDD12	1.2 V analog supply	1.14	1.2	1.26	V	–
AVDD33	3.3 V analog supply	3.0	3.3	3.6	V	–
VDDIO VDDIO_P1 VDDIO_P2 VDDIO_BB	3.3 V I/O supply	3	3.3	3.6	V	–
VDDD_P1	PD Port-1 power supply	2.7	–	5.5	V	UFP Applications
		3.0	–	5.5	V	DFP/DRP Applications
VCCD_P1	Output voltage (for core logic)	–	1.8	–	V	Connect a 1-µF capacitor between this pin and ground
VCCD_P2	Output voltage (for core logic)	–	1.8	–	V	Connect a 1-µF capacitor between this pin and ground
VCCD_BB	Output voltage (for core logic)	–	1.8	–	V	Connect a 1-µF capacitor between this pin and ground
VCONN1	VCONN supply voltage	4	5.0	5.5	V	–
V_{RAMP}	Voltage ramp rate on core and I/O supplies	0.2	–	50	V/ms	Voltage ramp must be monotonic
V_N	Noise level permitted on core and I/O supplies	–	–	100	mV	Max p-p noise level permitted on all supplies except AVDD
V_{N_USB}	Noise level permitted on AVDD12 and AVDD33 supply	–	–	20	mV	Max p-p noise level permitted USB supplies
Power Supply Current Specs						
I_{CC12}	1.2 V supplies combined operating current	–	320	420	mA	Upstream connected to Super-Speed Host and DS connected to Hubs (both SS and USB 2.0 in active state)
I_{CC33}	3.3 V supplies combined operating current	–	230	300	mA	All USB ports active, PD ports and BB device in active state

Table 5. DC Electrical Characteristics *(continued)*

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{CCVBUS}	VBUS supply operating current	–	3	5	mA	Current consumed through VBUS supply pin when USB is in Active state
I_{SB12}	1.2 V supplies combined suspend current	–	12	–	mA	USB in suspend state, CPUs are in SLEEP mode, CC I/O ON, no I/O sourcing current
I_{SB33}	3.3 V supplies combined suspend current	–	13	–	mA	
I_{SBVBUS}	VBUS supply suspend current	–	5	–	µA	
I/O Specs						
V_{IH}[6]	Input voltage HIGH threshold	0.7 × VDDIO	–	–	V	CMOS input
V_{IL}	Input voltage LOW threshold	–	–	0.3 × VDDIO	V	CMOS input
V_{OH}	Output voltage HIGH level	2.4	–	–	V	Output HIGH voltage at IOH ≤ +4 mA
V_{OL}	Output voltage LOW level	–	–	0.6	V	Output LOW voltage at IOL ≥ –4 mA
I_{IL}	Input leakage current	–1	–	1	µA	I/O signals held at VDDIO or GND

Note
6. V_{IH} should not exceed VDDIO + 0.2 V.

Power Consumption

Table 6 provides the power consumption estimates for HX3C under different conditions. Table 7 summarizes the power consumption for various combinations of devices connected to DS ports.

For example, to calculate the HX3C power consumption for three SS devices connected to DS ports (and no device connected to one DS port), and a US port connected to a USB 3.1 Gen 1 host:

Power consumption = [a] + (2 × [g]) = 492.5 + (2 × 76) = 644 mW

[a] is the active power consumption for the US port connected to a USB 3.0 host and the SS device connected to the DS port.

[g] is the incremental power consumption for an additional SS device connected to the DS port.

Table 6. Power Consumption Estimates for Various Usage Scenarios

Device Condition	Number and Speed of DS Ports Connected	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
Suspend[7]	–	12.0	13.0	57	–
Active with USB 3.0 host upstream[8]	1 SS	204.0	75.0	492	[a]
	1 HS	52.0	46.0	214	[b]
	1 FS	51.0	34.0	173	[c]
	1 SS + 1 HS	218.0	104.0	605	[d]
Active with USB 2.0 host upstream[8, 9]	1 HS	52.0	46.0	214	[e]
	1 FS	51.0	34.0	173	[f]
Incremental active power for every DS port connected	SS	40.0	9.0	78	[g]
	HS	7.0	20.0	74	[h]
	FS	7.0	14.0	55	[i]
Active power for each PD port	–	–	7.5	25	[j]
Active power for Bill board function	–	–	20.0	66	[k]

Table 7. Power Consumption Under Various Configurations

Configuration	Number of DS Devices Connected With Data Transfer	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
US connected to USB 3.0 Type-C host	3 SS Type-A devices	284.0	100.5	673	a + (2 × g) + j
	2 SS + 1 HS Type-A devices	258.0	120.5	707	d + g + j
	2 HS Type-A devices	59.0	73.5	313	b + h + j
	1 SS Type-C + 1 SS Type-A + 1 HS Type-A devices	258.0	128	732	d + g + (2 × j)
	1 SS Type-C + 1 SS Type-A + 1 HS Type-A devices + Billboard enumerated	265.0	162	853	d + g + i + (2 × j) + k
US connected to USB 2.0 Type-C host	3 HS Type-A devices	66.0	93.5	388	e + (2 × h) + j
	1 HS Type-C + 1 HS Type-A + 1 FS Type-A devices	66.0	95	393	e + h + i + (2 × j)
	1 HS Type-C + 1 HS Type-A + 1 FS Type-A devices + Billboard enumerated	80.0	149	588	e + h + (2 × i) + (2 × j)

Notes
7. Suspend means US port SS in U3 state, USB2.0 in L2 power states, no PD activity and no I/O sourcing current.
8. All DS ports are enabled.
9. US SuperSpeed disabled.

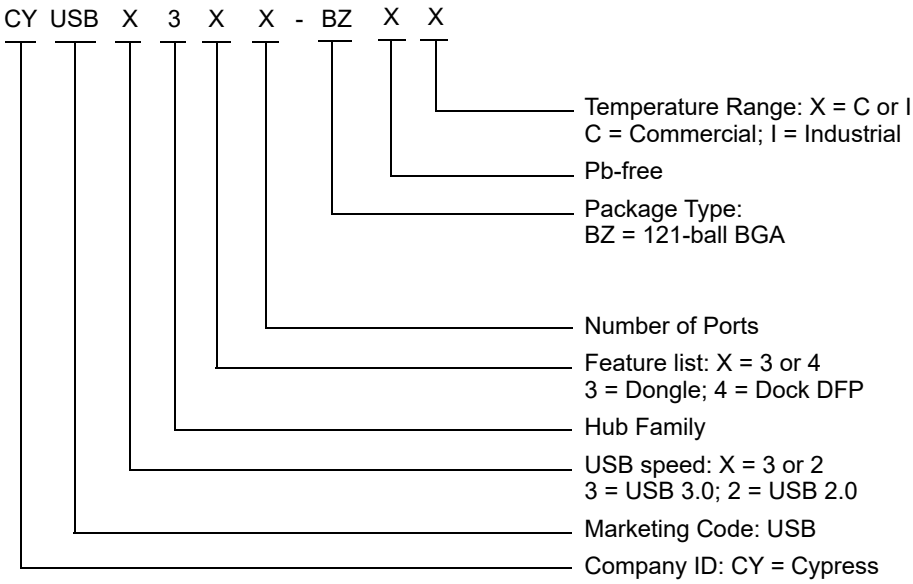
Ordering Information

Table 8 lists HX3C's ordering information. The table contains only the part numbers that are currently available for order. Additional part numbers with customized configurations can be made available on request. For more information, visit the Cypress website or contact the local sales representative.

Table 8. Ordering Information

Serial No.	Ordering Part Number	Application	PD Port-2 Power Roles	Type-C Ports	Package
1	CYUSB3333-BZXI	Dongles	DRP	US and 1 DS	121-ball BGA
2	CYUSB3343-BZXI	Self-Powered Docks, Monitors	DFP	US and 1 DS	121-ball BGA

Ordering Code Definitions



Packaging

Table 9. Package Characteristics

Parameter	Description	Min	Typ	Max	Units
T_A	Operating ambient temperature	–40	–	85	°C
T_J	Operating junction temperature	–40	–	125	°C
T_{JA}	Package J_A (121-ball BGA)	–	44.05	–	°C/W
T_{JC}	Package J_C (121-ball BGA)	–	19.65	–	°C/W

Table 10. Solder Reflow Peak Temperature

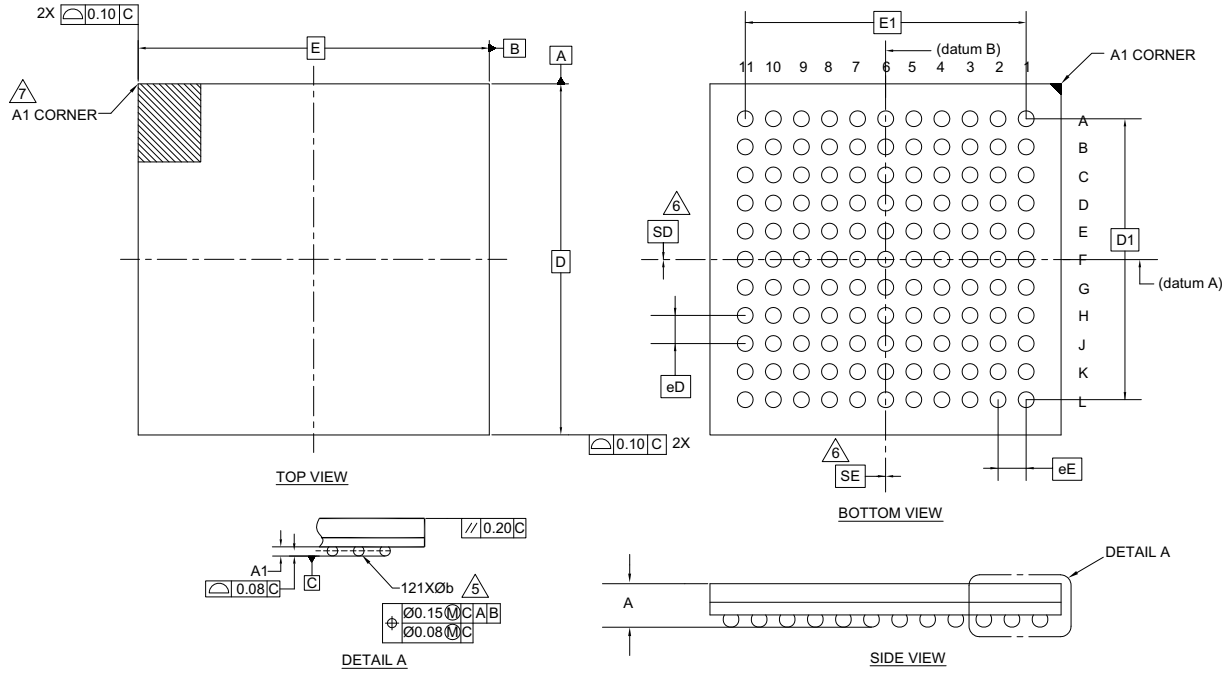
Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
121-ball BGA	260 °C	30 seconds

Table 11. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
121-ball BGA	MSL 3

Package Diagram

Figure 6. 121-ball FBGA (10.0 × 10.0 × 1.20 mm (0.30 Ball Diameter)) Package Outline, 001-54471



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.15	-	-
D	10.00 BSC		
E	10.00 BSC		
D1	8.00 BSC		
E1	8.00 BSC		
MD	11		
ME	11		
N	121		
∅ b	0.25	0.30	0.35
eD	0.80 BSC		
eE	0.80 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

001-54471 *F

Acronyms

Table 12. Acronyms Used in this Document

Acronym	Description
ACA	Accessory Charging Adapter
ASSP	Application-Specific Standard Product
BC	Battery Charging
CDP	Charging Downstream Port
DS	DownStream
DCP	Dedicated Charging Port
DNU	Do Not Use
DWG	Device Working Group
EEPROM	Electrically Erasable Programmable Read-Only Memory
FBGA	Fine-Pitch Ball Grid Array
FS	Full-Speed
FW	FirmWare
GND	GrouND
GPIO	General-Purpose Input/Output
HS	Hi-Speed
ISP	In-System Programming
I/O	Input/Output
LS	Low-Speed
NC	No Connect
OTG	On-The-Go
PID	Product ID
POR	Power-On Reset
ROM	Read-Only Memory
SCL	Serial CLock
SDA	Serial DAta
SS	SuperSpeed
TT	Transaction Translator
US	UpStream
VID	Vendor ID

Reference Documents

USB 2.0 Specification

USB 3.1 Specification

Battery Charging Specification

Document Conventions

Units of Measure

Table 13. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Ω	ohm
Gbps	gigabit per second
KB	kilobyte
kHz	kilohertz
kΩ	kiloohm
Mbps	megabit per second
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
ppm	parts per million
V	volt

Document History

Document Title: CYUSB3333/CYUSB3343, HX3C USB Type-C Hub with PD Document Number: 002-10462				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5147085	HBM	03/30/2016	New datasheet.
*A	5312423	HBM	06/17/2016	Corrected typo in 121-ball BGA Pinout for CYUSB3333/CYUSB3343.
*B	5766271	AESATMP9	06/07/2017	Updated logo and copyright.
*C	5846705	HBM	08/16/2017	Updated subsections SS Hub Controller and Reset. Updated Figure 6 in Package Diagram (spec 001-54471 *E to *F). Removed Preliminary document status.

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