## Contents

**Features** ..... **1**
**Functional Description** ..... **1**
**Logic Block Diagram** ..... **1**
**Contents** ..... **2**
**Selection Guide** ..... **3**
**Pin Configuration** ..... **3**
**Functional Description** ..... **5**
**Architecture** ..... **5**
**Resetting the FIFO** ..... **5**
**FIFO Operation** ..... **5**
**Programming** ..... **5**
Programmable Flag ($\overline{PAE}$, $\overline{PAF}$) Operation ..... 7
**Width Expansion Configuration** ..... **8**
**Flag Operation** ..... **8**
Full Flag ..... 8
Empty Flag ..... 8
**Maximum Ratings**[4] ..... 9
**Operating Range** ..... **9**
**Electrical Characteristics** Over the Operating Range ..... 9
**Capacitance[9]** ..... **9**
**Switching Characteristics Over the Operating Range** ..... **10**
**Switching Waveforms** ..... **11**
**Typical AC and DC Characteristics** ..... **17**
256 x 9 Synchronous FIFO ..... 18
1K x 9 Synchronous FIFO ..... 18
2K x 9 Synchronous FIFO ..... 18
4K x 9 Synchronous FIFO ..... 18
8K x 9 Synchronous FIFO ..... 18
**Package Diagrams** ..... **19**
**Document History Page** ..... **20**
**Sales, Solutions, and Legal Information** ..... **20**
Worldwide Sales and Design Support ..... 20
Products ..... 20
PSoC Solutions ..... 20

## Selection Guide

| Description | | -10 | -15 | -25 | Unit |
|---|---|---|---|---|---|
| Maximum Frequency | | 100 | 66.7 | 40 | MHz |
| Maximum Access Time | | 8 | 10 | 15 | ns |
| Minimum Cycle Time | | 10 | 15 | 25 | ns |
| Minimum Data or Enable Setup | | 3 | 4 | 6 | ns |
| Minimum Data or Enable Hold | | 0.5 | 1 | 1 | ns |
| Maximum Flag Delay | | 8 | 10 | 15 | ns |
| Active Power Supply Current | Commercial | 35 | 35 | 35 | **ICC1** |
| | Industrial | 40 | 40 | 40 | |

| | CY7C4421 | CY7C4201 | CY7C4211 | CY7C4221 | CY7C4231 | CY7C4241 | CY7C4251 |
|---|---|---|---|---|---|---|---|
| Density | 64 × 9 | 256 × 9 | 512 × 9 | 1K × 9 | 2K × 9 | 4K × 9 | 8K × 9 |

## Pin Configuration

**Figure 1. Pin Diagram**

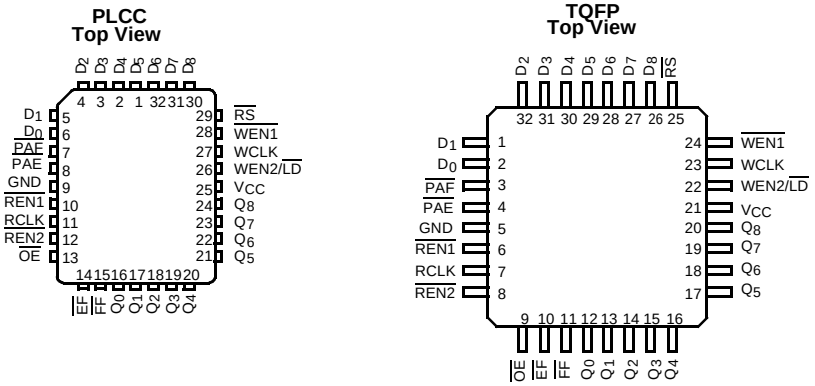



**Table 1. Pin Definitions**

| Pin | Name | I/O | Description |
|---|---|---|---|
| $D_{0–8}$ | Data Inputs | I | Data inputs for 9-bit bus. |
| $Q_{0–8}$ | Data Outputs | O | Data outputs for 9-bit bus. |
| WEN1 | Write Enable 1 | I | The only write enable to have programmable flags when device is configured. Data is written on a LOW-to-HIGH transition of WCLK when WEN1 is asserted and FF is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when WEN1 is LOW and WEN2/LD and FF are HIGH. |
| WEN2/LD Dual Mode Pin | Write Enable 2 | I | If HIGH at reset, this pin operates as a second write enable. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. WEN1 must be LOW and WEN2 must be HIGH to write data into the FIFO. Data is not written into the FIFO if the FF is LOW. If the FIFO is configured to have programmable flags, WEN2/LD is held LOW to write or read the programmable flag offsets. |
| | Load | I | |
| REN1, REN2 | Read Enable Inputs | I | Enables device for read operation. |
| WCLK | Write Clock | I | The rising edge clocks data into the FIFO when WEN1 is LOW, WEN2/LD is HIGH, and the FIFO is not Full. When LD is asserted, WCLK writes data into the programmable flag-offset register. |

**Table 1. Pin Definitions** (continued)

| Pin | Name | I/O | Description |
|---|---|---|---|
| RCLK | Read Clock | I | The rising edge clocks data out of the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are LOW and the FIFO is not Empty. When WEN2/$\overline{LD}$ is LOW, RCLK reads data out of the programmable flag-offset register. |
| $\overline{EF}$ | Empty Flag | O | When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK. |
| $\overline{FF}$ | Full Flag | O | When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK. |
| $\overline{PAE}$ | Programmable Almost Empty | O | When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO. |
| $\overline{PAF}$ | Programmable Almost Full | O | When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. |
| $\overline{RS}$ | Reset | I | Resets device to empty condition. A reset is required before an initial read or write operation after power up. |
| $\overline{OE}$ | Output Enable | I | When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High-Z (high-impedance) state. |

## Functional Description

The CY7C42X1 provides four status pins: Empty, Full, Almost Empty, Almost Full. The Almost Empty/Almost Full flags are programmable to single word granularity. The programmable flags default to Empty – 7 and Full – 7.

The flags are synchronous - they change state relative to either the Read clock (RCLK) or the Write clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle.

All configurations are fabricated using advanced 0.65µ N-Well CMOS technology. Input ESD protection is greater than 2001V, and latch up is prevented by the use of guard rings.

## Architecture

The CY7C42X1 consists of an array of 64 to 8K words of 9 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, REN1, REN2, WEN1, WEN2, RS), and flags (EF, PAE, PAF, FF).

## Resetting the FIFO

During power up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs ($Q_{0–8}$) go LOW $t_{RSF}$ after the rising edge of $\overline{RS}$. For the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or write while $\overline{RS}$ is LOW. All flags are guaranteed to be valid $t_{RSF}$ after $\overline{RS}$ is taken LOW.

## FIFO Operation

When the $\overline{WEN1}$ signal is active LOW and WEN2 is active HIGH, data present on the $D_{0–8}$ pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN1}$ and REN2 signals are active LOW, data in the FIFO memory is presented on the $Q_{0–8}$ outputs. New data is presented on each rising edge of RCLK while $\overline{REN1}$ and $\overline{REN2}$ must set up $t_{ENS}$ before RCLK for it to be a valid read function. $\overline{WEN1}$ and WEN2 must occur $t_{ENS}$ before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the $Q_{0–8}$ outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (LOW), data in the output register is available to the $Q_{0–8}$ outputs after $t_{OE}$.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its $Q_{0–8}$ outputs even after additional reads occur.

**Write Enable 1 ($\overline{WEN1}$)**. If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only write enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every Write clock (WCLK). Data is stored is the RAM array sequentially and independently of any on-going read operation.

**Write Enable 2/Load ($\overline{WEN2/LD}$)**. This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If Write Enable 2/Load ($\overline{WEN2/LD}$) is set active HIGH at Reset ($\overline{RS}$ = LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2/Load ($\overline{WEN2/LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every Write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

## Programming

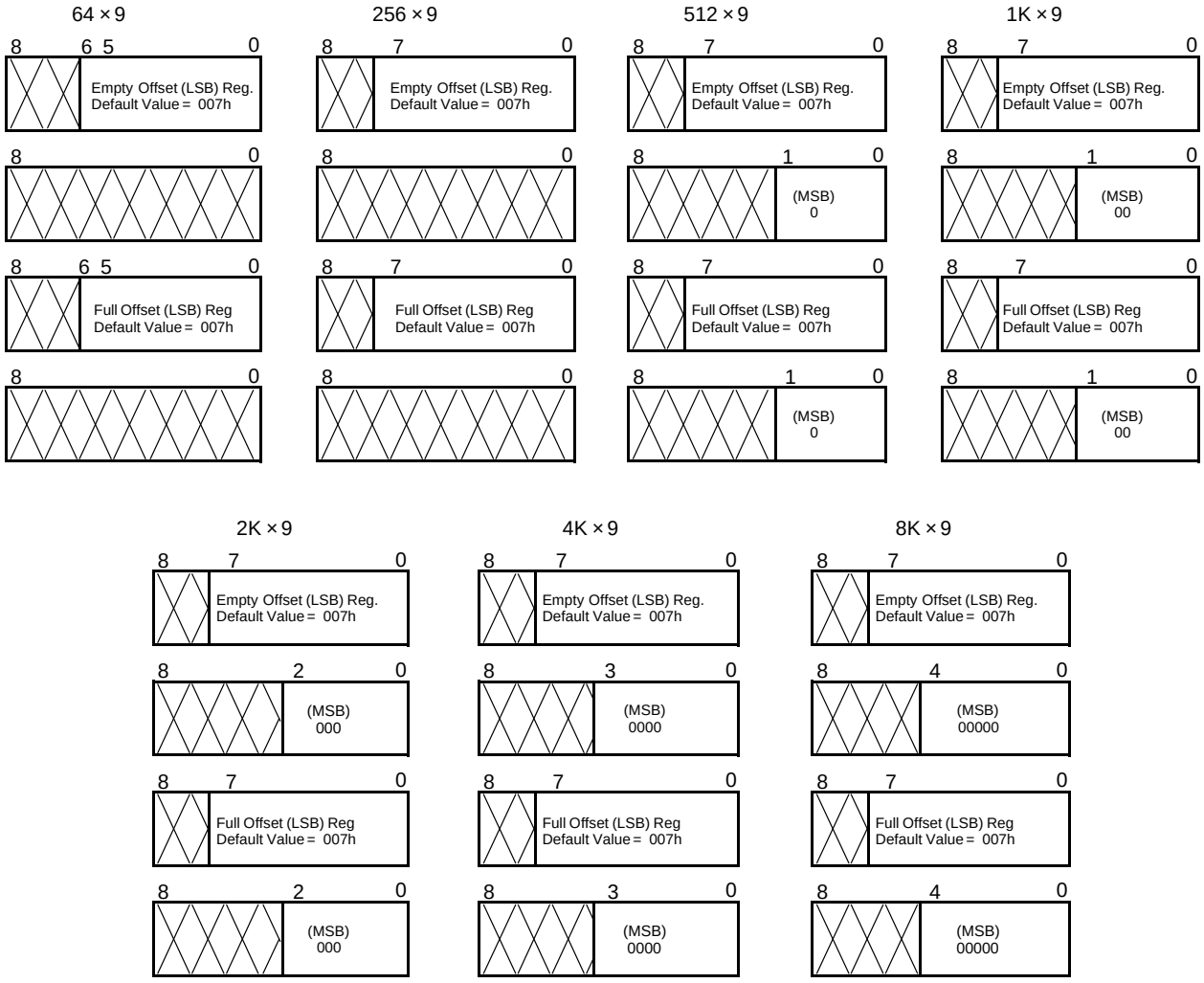
When $\overline{WEN2/LD}$ is held LOW during Reset, this pin is the load ($\overline{LD}$) enable for flag offset programming. In this configuration, $\overline{WEN2/LD}$ can be used to access the four 8-bit offset registers contained in the CY7C42X1 for writing or reading data to these registers.

When the device is configured for programmable flags and both $\overline{WEN2/LD}$ and $\overline{WEN1}$ are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when $\overline{WEN2/LD}$ and $\overline{WEN1}$ are LOW. The fifth LOW-to-HIGH transition of WCLK while $\overline{WEN2/LD}$ and $\overline{WEN1}$ are LOW writes data to the empty LSB register again. Figure 2 shows the registers sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the $\overline{WEN2/LD}$ input HIGH, the FIFO is returned to normal read and write operation. The next time $\overline{WEN2/LD}$ is brought LOW, a write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when $\overline{WEN2/LD}$ is LOW and both $\overline{REN1}$ and $\overline{REN2}$ are LOW. LOW-to-HIGH transitions of RCLK Read register contents to the data outputs. Writes and reads should not be preformed simultaneously on the offset registers.

**Figure 2. Offset Register Location and Default Values**



## Programmable Flag ($\overline{PAE}$, $\overline{PAF}$) Operation

Whether the flag offset registers are programmed as described in Table 2 or the default values are used, the programmable almost-empty flag ($\overline{PAE}$) and programmable almost-full flag ($\overline{PAF}$) states are determined by their corresponding offset registers and the difference between the read and write pointers.

The number formed by the empty offset least significant bit register and empty offset most significant register is referred to as *n* and determines the operation of $\overline{PAE}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words. $\overline{PAE}$ is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n + 1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of $\overline{PAF}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4421. (64 – m), CY7C4201 (256 – m), CY7C4211 (512 – m), CY7C4221 (1K – m), CY7C4231 (2K – m), CY7C4241 (4K – m), and CY7C4251 (8K – m). $\overline{PAF}$ is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than m.

**Table 2. Writing the Offset Registers**

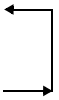
| LD | WEN | WCLK[1] | Selection |
|---|---|---|---|
| 0 | 0 |  | Empty Offset (LSB)<br>Empty Offset (MSB)<br>Full Offset (LSB)<br>Full Offset (MSB)  |
| 0 | 1 |  | No Operation |
| 1 | 0 |  | Write Into FIFO |
| 1 | 1 |  | No Operation |

**Table 3. Status Flags**

| Number of Words in FIFO | | | $\overline{FF}$ | $\overline{PAF}$ | $\overline{PAE}$ | $\overline{EF}$ |
|---|---|---|---|---|---|---|
| CY7C4421 | CY7C4201 | CY7C4211 | | | | |
| 0 | 0 | 0 | H | H | L | L |
| 1 to n[2] | 1 to n[2] | 1 to n[2] | H | H | L | H |
| (n + 1) to 32 | (n + 1) to 128 | (n + 1) to 256 | H | H | H | H |
| 33 to (64 – (m + 1)) | 129 to (256 – (m + 1)) | 257 to (512 – (m + 1)) | H | H | H | H |
| (64 – m)[3] to 63 | (256 – m)[3] to 255 | (512 – m)[3] to 511 | H | L | H | H |
| 64 | 256 | 512 | L | L | H | H |

| Number of Words in FIFO | | | | $\overline{FF}$ | $\overline{PAF}$ | $\overline{PAE}$ | $\overline{EF}$ |
|---|---|---|---|---|---|---|---|
| CY7C4221 | CY7C4231 | CY7C4241 | CY7C4251 | | | | |
| 0 | 0 | 0 | 0 | H | H | L | L |
| 1 to n[2] | 1 to n[2] | 1 to n[2] | 1 to n[2] | H | H | L | H |
| (n + 1) to 512 | (n + 1) to 1024 | (n + 1) to 2048 | (n + 1) to 4096 | H | H | H | H |
| 513 to (1024 – (m + 1)) | 1025 to (2048 – (m + 1)) | 2049 to (4096 – (m + 1)) | 4097 to (8192 – (m + 1)) | H | H | H | H |
| (1024 – m)[3] to 1023 | (2048 – m)[3] to 2047 | (4096 – m)[3] to 4095 | (8192 – m)[3] to 8191 | H | L | H | H |
| 1024 | 2048 | 4096 | 8192 | L | L | H | H |

**Notes**
1. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and a read is performed on the LOW-to-HIGH transition of RCLK.
2. n = Empty Offset (n = 7 default value).
3. m = Full Offset (m = 7 default value).

## Width Expansion Configuration

Word width may be increased by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{PAE}$ and $\overline{PAF}$) can be detected from any one device. Figure 3 demonstrates a 18-bit word width by using two CY7C42X1s. Any word width can be attained by adding additional CY7C42X1s.

When the CY7C42X1 is in a Width Expansion Configuration, the Read Enable ($\overline{REN2}$) control input can be grounded (See Figure 3). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

## Flag Operation

The CY7C42X1 devices provide four flag pins to indicate the condition of the FIFO contents. Empty, Full, PAE, and PAF are synchronous.

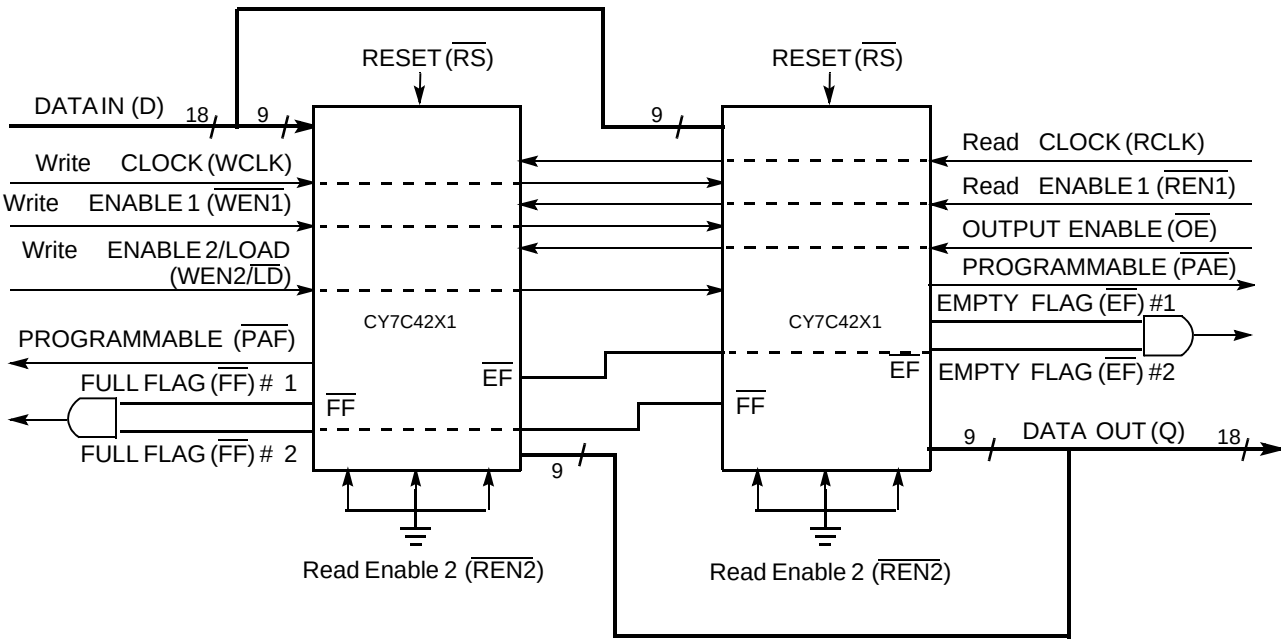
### Full Flag

The Full Flag ($\overline{FF}$) goes LOW when device is full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of WEN1 and WEN2/$\overline{LD}$. $\overline{FF}$ is synchronized to WCLK - it is exclusively updated by each rising edge of WCLK.

### Empty Flag

The Empty Flag ($\overline{EF}$) goes LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN1}$ and $\overline{REN2}$. $\overline{EF}$ is synchronized to RCLK - it is exclusively updated by each rising edge of RCLK.

**Figure 3. Block Diagram of 64 x 9, 256 x 9, 512 x 9, 1024 x 9, 2048 x 9, 4096 x 9, 8192 x 9 Synchronous FIFO Memory Used in a Width Expansion Configuration**



## Maximum Ratings[4]

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied .....–55°C to +125°C

Supply Voltage to Ground Potential.....–0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State.....–0.5V to +7.0V

DC Input Voltage .....–3.0V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....> 2001V (per MIL-STD-883, Method 3015)

Latch up Current.....> 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ±10% |
| Industrial[5] | –40°C to +85°C | 5V ±10% |

## Electrical Characteristics Over the Operating Range

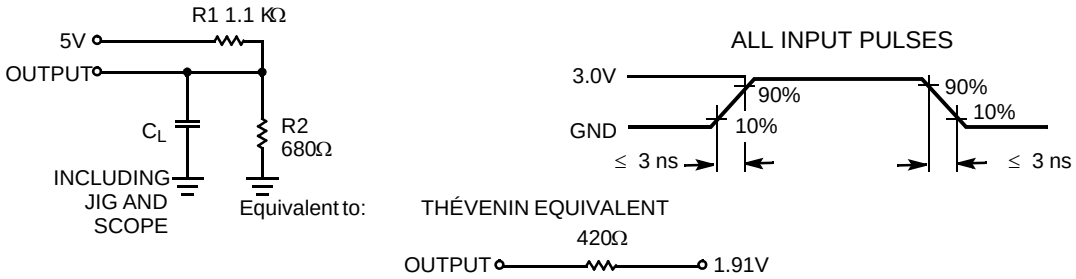
| Parameter | Description | Test Conditions | | -10 | | -15 | | -25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –2.0 mA | | 2.4 | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | | 0.4 | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.2 | $V_{CC}$ | 2.2 | $V_{CC}$ | 2.2 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | –3.0 | 0.8 | –3.0 | 0.8 | –3.0 | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | $V_{CC}$ = Max. | | –10 | +10 | –10 | +10 | –10 | +10 | µA |
| $I_{OS}$[6] | Output Short Circuit Current | $V_{CC}$ = Max., $V_{OUT}$ = GND | | –90 | | –90 | | –90 | | mA |
| $I_{OZL}$ $I_{OZH}$ | Output OFF, High-Z Current | $\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$ | | –10 | +10 | –10 | +10 | –10 | +10 | mA |
| $I_{CC1}$[7] | Active Power Supply Current | | Commercial | | 35 | | 35 | | 35 | mA |
| | | | Industrial | | 40 | | 40 | | 40 | mA |
| $I_{CC2}$[8] | Average Standby Current | | Commercial | | 10 | | 10 | | 10 | mA |
| | | | Industrial | | 15 | | 15 | | 15 | mA |

## Capacitance[9]

| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 5 | pF |
| $C_{OUT}$ | Output Capacitance | | 7 | pF |

**Notes**
4. The voltage on any input or I/O pin cannot exceed the power pin during power up.
5. $T_A$ is the "instant on" case temperature.
6. Test no more than one output at a time for not more than one second.
7. Outputs open. Tested at frequency = 20 MHz.
8. All inputs = $V_{CC}$ – 0.2V, except WCLK and RCLK, which are switching at 20 MHz.
9. Tested initially and after any design or process changes that may affect these parameters.

**Figure 4. AC Test Loads and Waveforms**[10, 11]




## Switching Characteristics Over the Operating Range

| Parameter | Description | -10 | | -15 | | -25 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_S$ | Clock Cycle Frequency | | 100 | | 66.7 | | 40 | MHz |
| $t_A$ | Data Access Time | 2 | 8 | 2 | 10 | 2 | 15 | ns |
| $t_{CLK}$ | Clock Cycle Time | 10 | | 15 | | 25 | | ns |
| $t_{CLKH}$ | Clock HIGH Time | 4.5 | | 6 | | 10 | | ns |
| $t_{CLKL}$ | Clock LOW Time | 4.5 | | 6 | | 10 | | ns |
| $t_{DS}$ | Data Setup Time | 3 | | 4 | | 6 | | ns |
| $t_{DH}$ | Data Hold Time | 0.5 | | 1 | | 1 | | ns |
| $t_{ENS}$ | Enable Setup Time | 3 | | 4 | | 6 | | ns |
| $t_{ENH}$ | Enable Hold Time | 0.5 | | 1 | | 1 | | ns |
| $t_{RS}$ | Reset Pulse Width[12] | 10 | | 15 | | 25 | | ns |
| $t_{RSS}$ | Reset Setup Time | 8 | | 10 | | 15 | | ns |
| $t_{RSR}$ | Reset Recovery Time | 8 | | 10 | | 15 | | ns |
| $t_{RSF}$ | Reset to Flag and Output Time | | 10 | | 15 | | 25 | ns |
| $t_{OLZ}$ | Output Enable to Output in Low-Z[13] | 0 | | 0 | | 0 | | ns |
| $t_{OE}$ | Output Enable to Output Valid | 3 | 7 | 3 | 8 | 3 | 12 | ns |
| $t_{OHZ}$ | Output Enable to Output in High-Z[13] | 3 | 7 | 3 | 8 | 3 | 12 | ns |
| $t_{WFF}$ | Write Clock to Full Flag | | 8 | | 10 | | 15 | ns |
| $t_{REF}$ | Read Clock to Empty Flag | | 8 | | 10 | | 15 | ns |
| $t_{PAF}$ | Clock to Programmable Almost-Full Flag | | 8 | | 10 | | 15 | ns |
| $t_{PAE}$ | Clock to Programmable Almost-Full Flag | | 8 | | 10 | | 15 | ns |
| $t_{SKEW1}$ | Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag | 5 | | 6 | | 10 | | ns |
| $t_{SKEW2}$ | Skew Time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag | 10 | | 15 | | 18 | | ns |

**Notes**
10. $C_L$ = 30 pF for all AC parameters except for $t_{OHZ}$.
11. $C_L$ = 5 pF for $t_{OHZ}$.
12. Pulse widths less than minimum values are not allowed.
13. Values guaranteed by design, not currently tested.

## Switching Waveforms

**Figure 5. Write Cycle Timing**

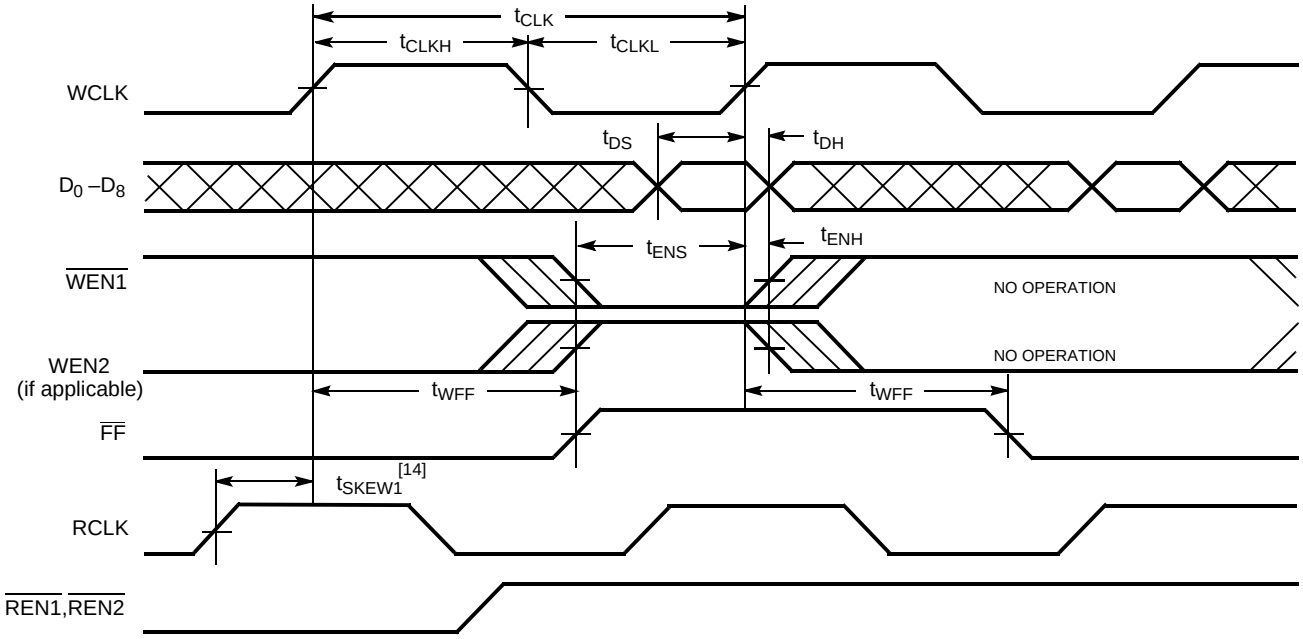
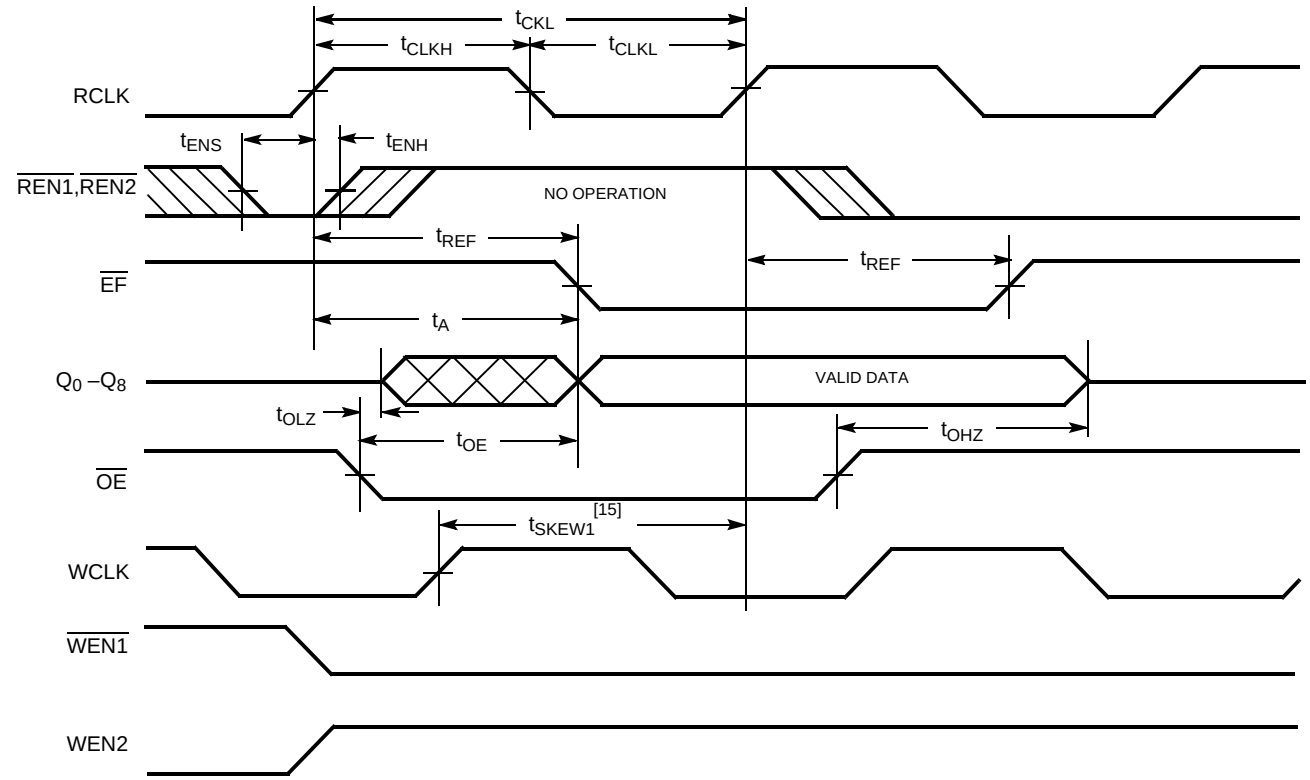



**Figure 6. Read Cycle Timing**




**Notes**

14. $t_{SKEW1}$ is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ goes HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than $t_{SKEW1}$, then $\overline{FF}$ may not change state until the next WCLK rising edge.
15. $t_{SKEW1}$ is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ goes HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than $t_{SKEW1}$, then $\overline{EF}$ may not change state until the next RCLK rising edge.

**Figure 7. Reset Timing**[16]

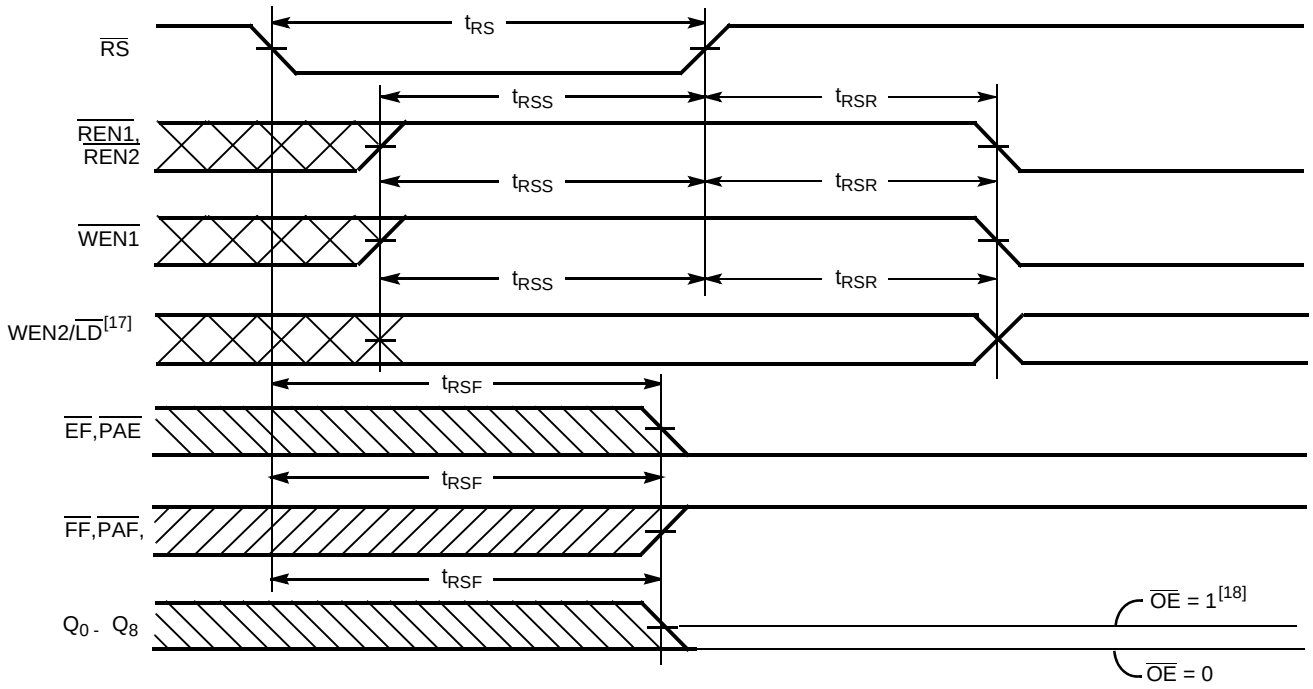
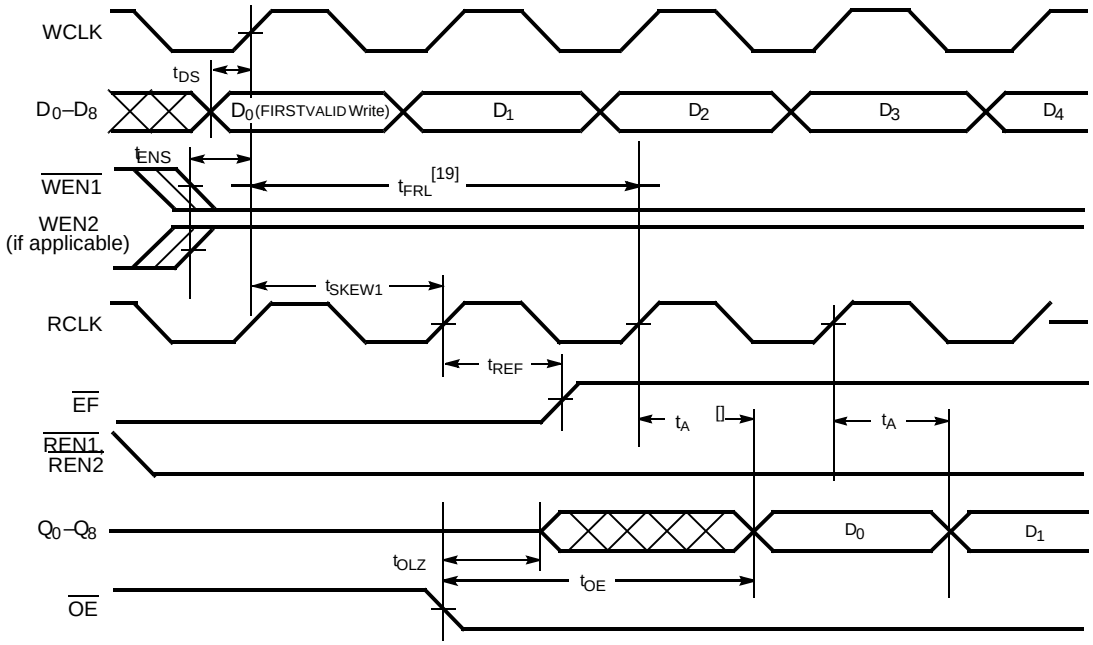



**Figure 8. First Data Word Latency after Reset with Simultaneous Read and Write**




**Notes**

16. The clocks (RCLK, WCLK) can be free-running during reset.
17. Holding WEN2/LD HIGH during reset makes the pin act as a second enable pin. Holding WEN2/LD LOW during reset makes the pin act as a load enable for the programmable flag offset registers.
18. After reset, the outputs are LOW if OE = 0 and three-state if OE = 1.
19. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL}$ (maximum) = $t_{CLK} + t_{SKEW1}$. When $t_{SKEW1}$ < minimum specification, $t_{FRL}$ (maximum) = either $2*t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$. The Latency Timing applies only at the Empty Boundary (EF = LOW).
20. The first word is available the cycle after EF goes HIGH, always.

**Figure 9. Empty Flag Timing**

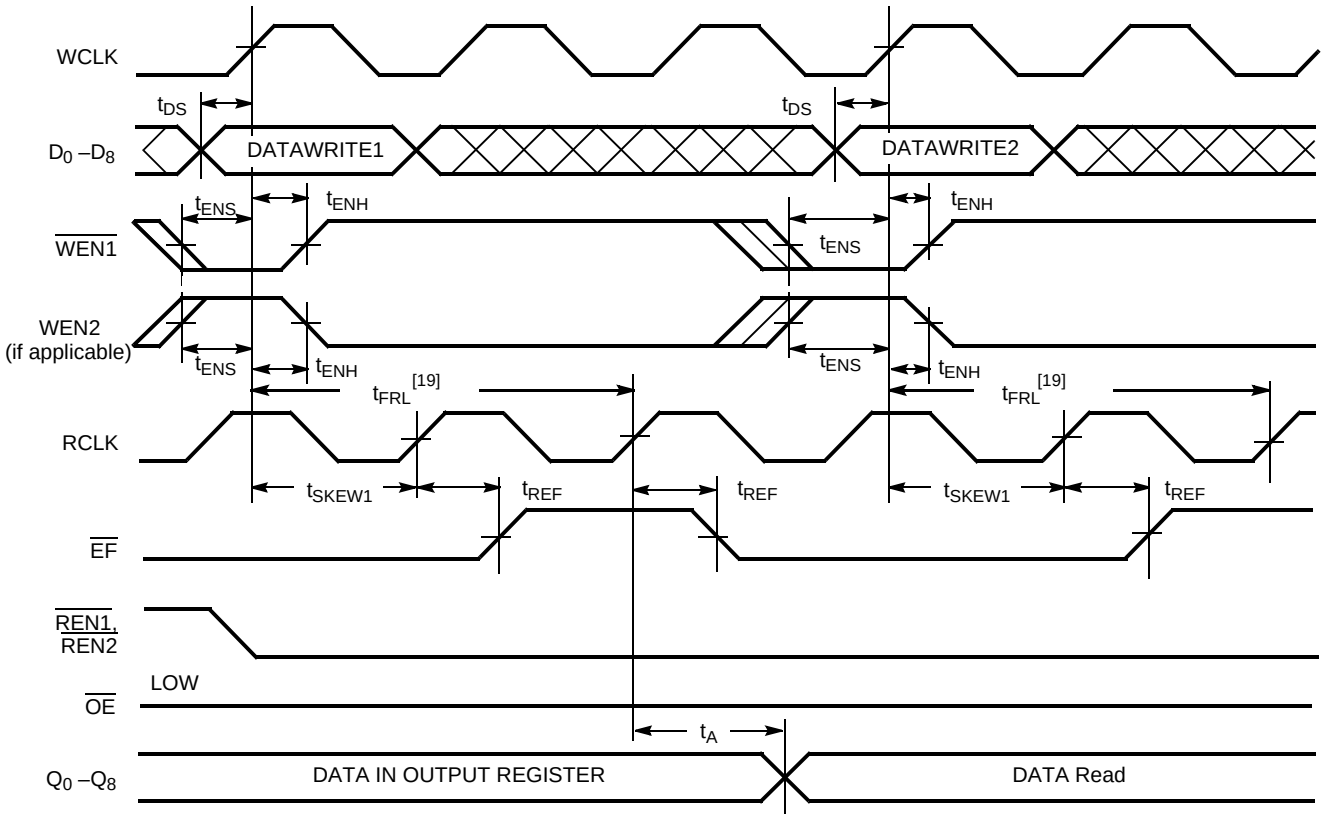


**Figure 10. Full Flag Timing**

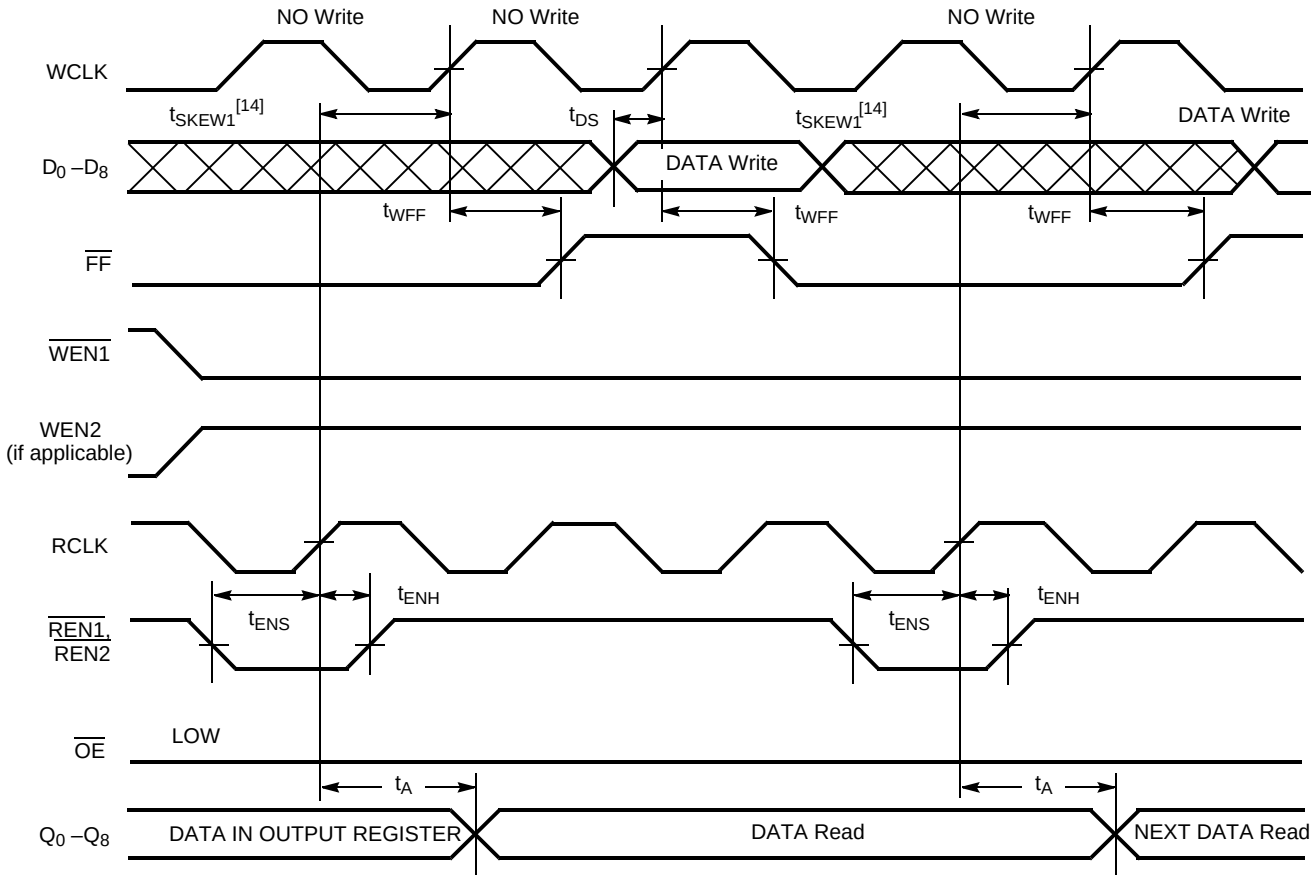
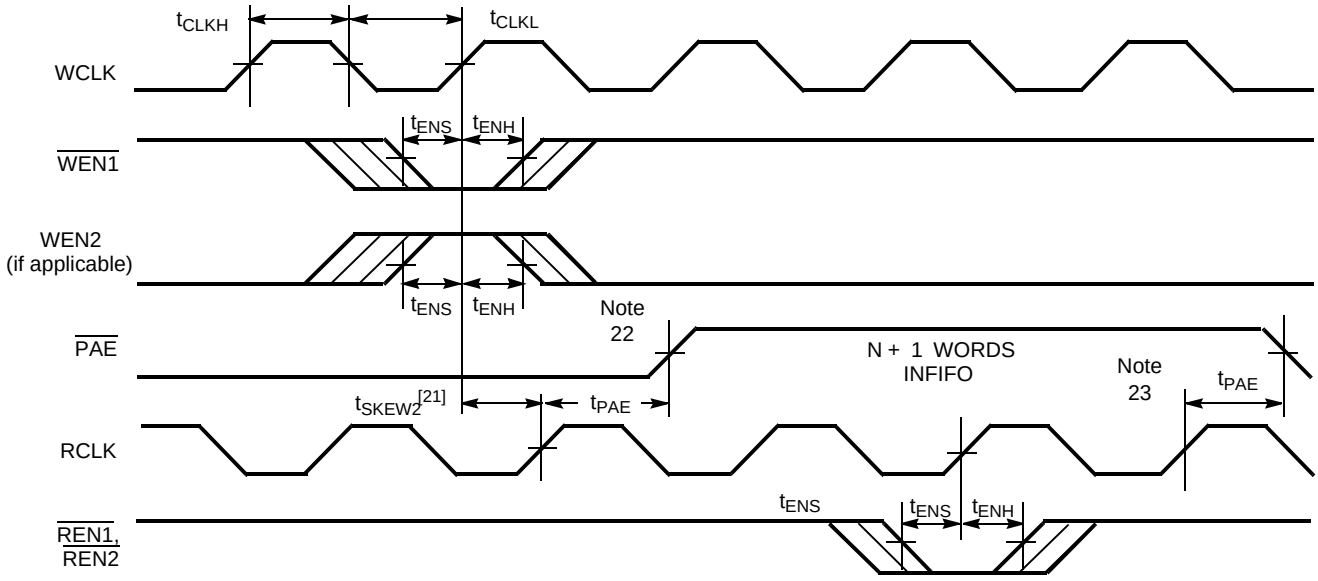



**Figure 11. Programmable Almost Empty Flag Timing**




**Notes**

21. $t_{SKEW2}$ is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than $t_{SKEW2}$, then $\overline{PAE}$ may not change state until the next RCLK.
22. PAE offset = n.
23. If a read is performed on this rising edge of the read clock, there are Empty + (n – 1) words in the FIFO when $\overline{PAE}$ goes LOW.

**Figure 12. Programmable Almost Full Flag Timing**

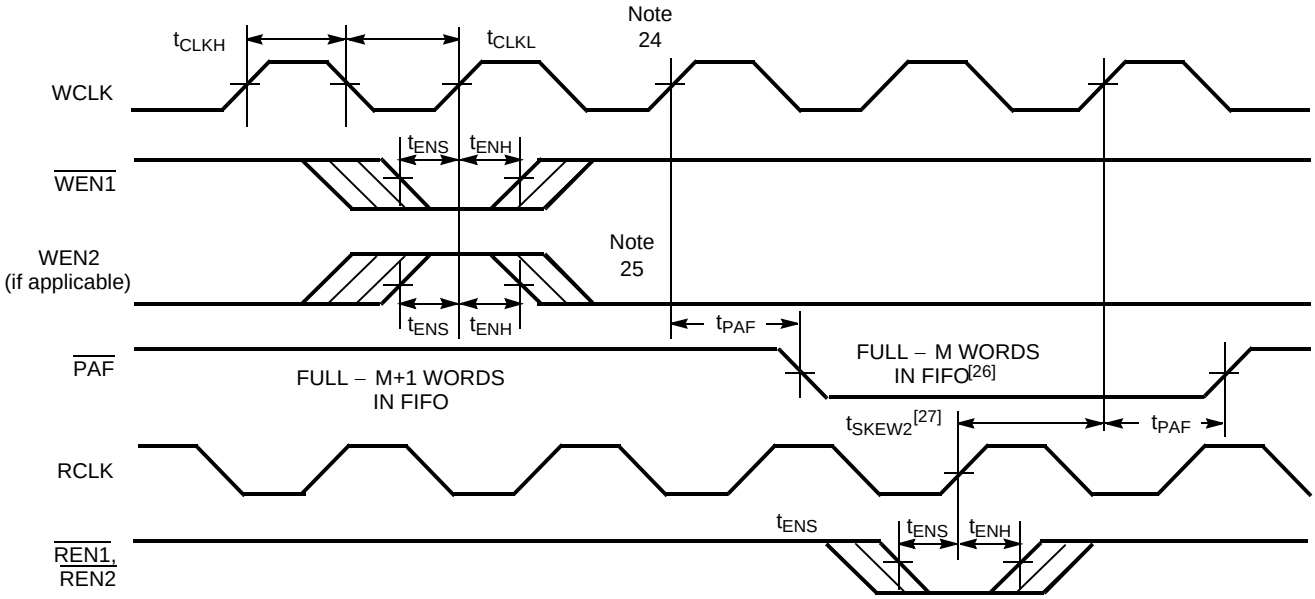
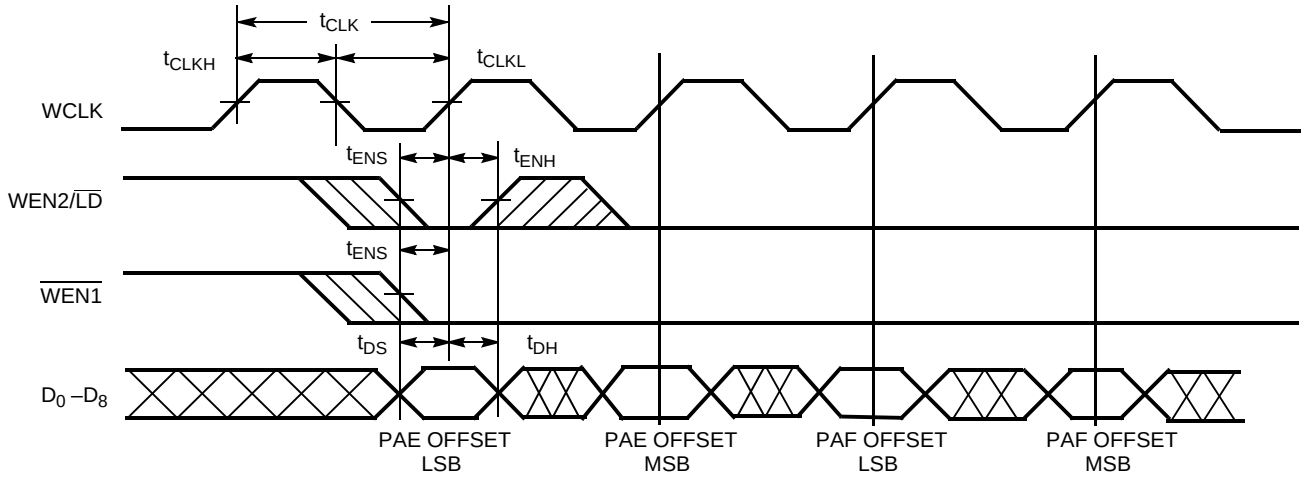


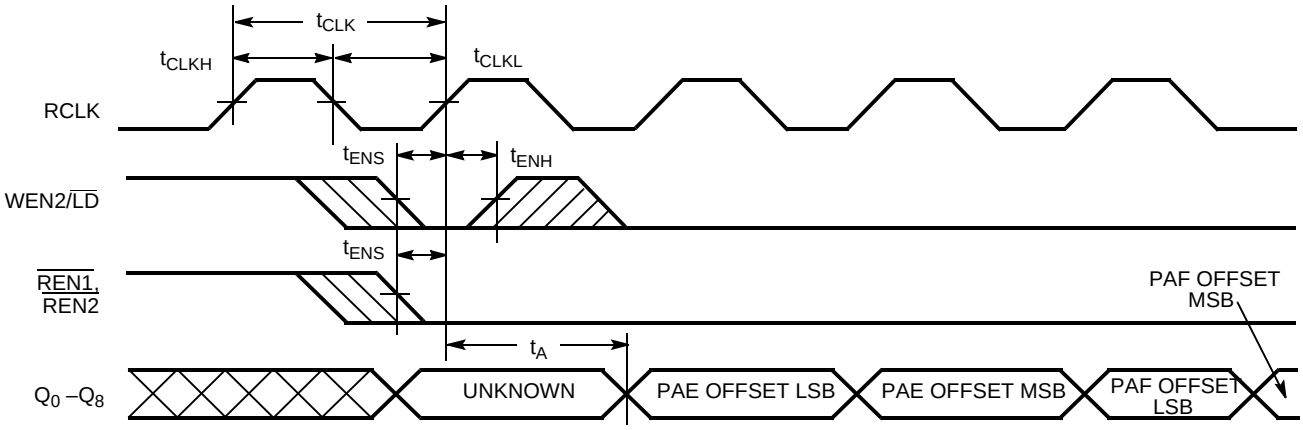

**Figure 13. Write Programmable Registers**




**Notes**

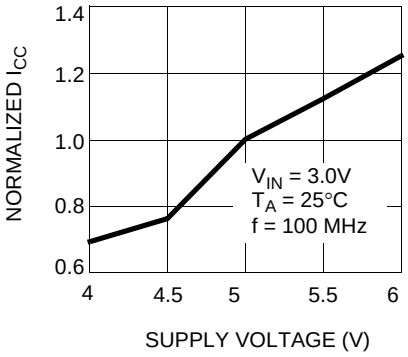
24. If a write is performed on this rising edge of the write clock, there are Full – (m – 1) words of the FIFO when $\overline{PAF}$ goes LOW.
25. PAF offset = m.
26. 64-m words for CY7C4421, 256 – m words in FIFO for CY7C4201, 512 – m words for CY7C4211, 1024 – m words for CY7C4221, 2048 – m words for CY7C4231, 4096 – m words for CY7C4241, 8192 – m words for CY7C4251.
27. $t_{SKEW2}$ is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than $t_{SKEW2}$, then PAF may not change state until the next WCLK.

**Figure 14. Read Programmable Registers**

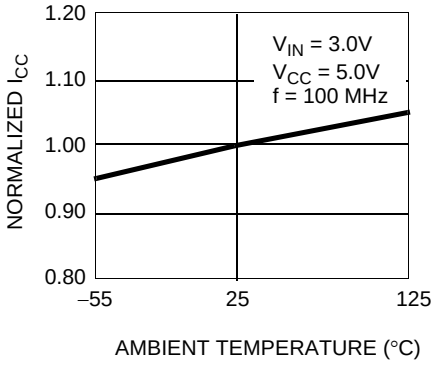


## Typical AC and DC Characteristics

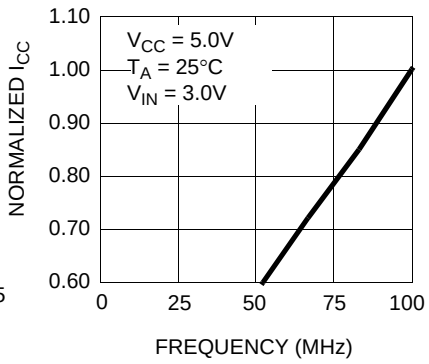
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



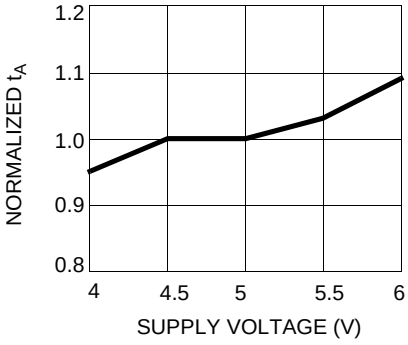

**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



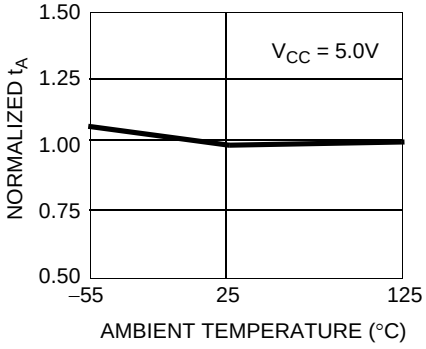

**NORMALIZED SUPPLY CURRENT vs. FREQUENCY**



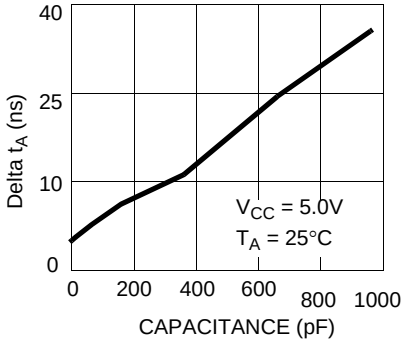

**NORMALIZED $t_A$ vs. SUPPLY VOLTAGE**



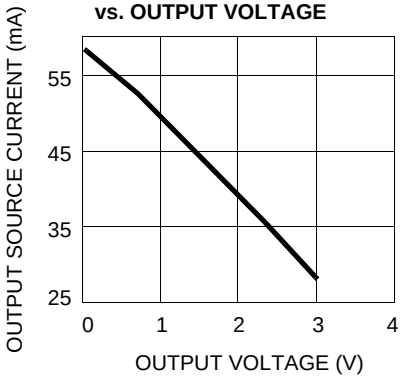

**NORMALIZED $t_A$ vs. AMBIENT TEMPERATURE**



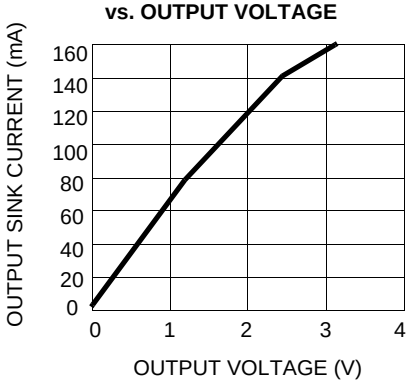

**TYPICAL $t_A$ CHANGE vs. OUTPUT LOADING**




**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**




**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**



### 256 x 9 Synchronous FIFO

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C4201-15JC | J65 | 32-Pin Plastic Leaded Chip Carrier | Commercial |
| | CY7C4201-15JXC | J65 | 32-Pin Pb-free Plastic Leaded Chip Carrier | |

### 1K x 9 Synchronous FIFO

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C4221-15AXC | A32 | 32-Pin Pb-free Thin Quad Flatpack | Commercial |
| | CY7C4221-15JXC | J65 | 32-Pin Pb-free Plastic Leaded Chip Carrier | |

### 2K x 9 Synchronous FIFO

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C4231-15AXC | A32 | 32-Pin Pb-free Thin Quad Flatpack | Commercial |
| | CY7C4231-15JXC | J65 | 32-Pin Pb-free Plastic Leaded Chip Carrier | |

### 4K x 9 Synchronous FIFO

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 10 | CY7C4241-10AC | A32 | 32-Pin Thin Quad Flatpack | Commercial |
| | CY7C4241-10AXC | A32 | 32-Pin Pb-free Thin Quad Flatpack | |
| | CY7C4241-10JI | J65 | 32-Pin Plastic Leaded Chip Carrier | Industrial |
| 15 | CY7C4241-15AC | A32 | 32-Pin Thin Quad Flatpack | Commercial |
| | CY7C4241-15JC | J65 | 32-Pin Plastic Leaded Chip Carrier | |
| | CY7C4241-15JXC | J65 | 32-Pin Pb-free Plastic Leaded Chip Carrier | |

### 8K x 9 Synchronous FIFO

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 10 | CY7C4251-10AC | A32 | 32-Pin Thin Quad Flatpack | Commercial |
| | CY7C4251-10JC | J65 | 32-Pin Plastic Leaded Chip Carrier | |
| | CY7C4251-10JXC | J65 | 32-Pin Pb-free Plastic Leaded Chip Carrier | |
| | CY7C4251-10AI | A32 | 32-Pin Thin Quad Flatpack | Industrial |
| | CY7C4251-10AXI | A32 | 32-Pin Pb-free Thin Quad Flatpack | |
| 15 | CY7C4251-15AC | A32 | 32-Pin Thin Quad Flatpack | Commercial |
| | CY7C4251-15AXC | A32 | 32-Pin Pb-free Thin Quad Flatpack | |
| | CY7C4251-15JC | J65 | 32-Pin Plastic Leaded Chip Carrier | |
| | CY7C4251-15JXC | J65 | 32-Pin Pb-free Plastic Leaded Chip Carrier | |

## Package Diagrams

**Figure 15. 32-Pin Pb-free Thin Plastic Quad Flatpack 7 × 7 × 1.0 mm A32, 51-85063**

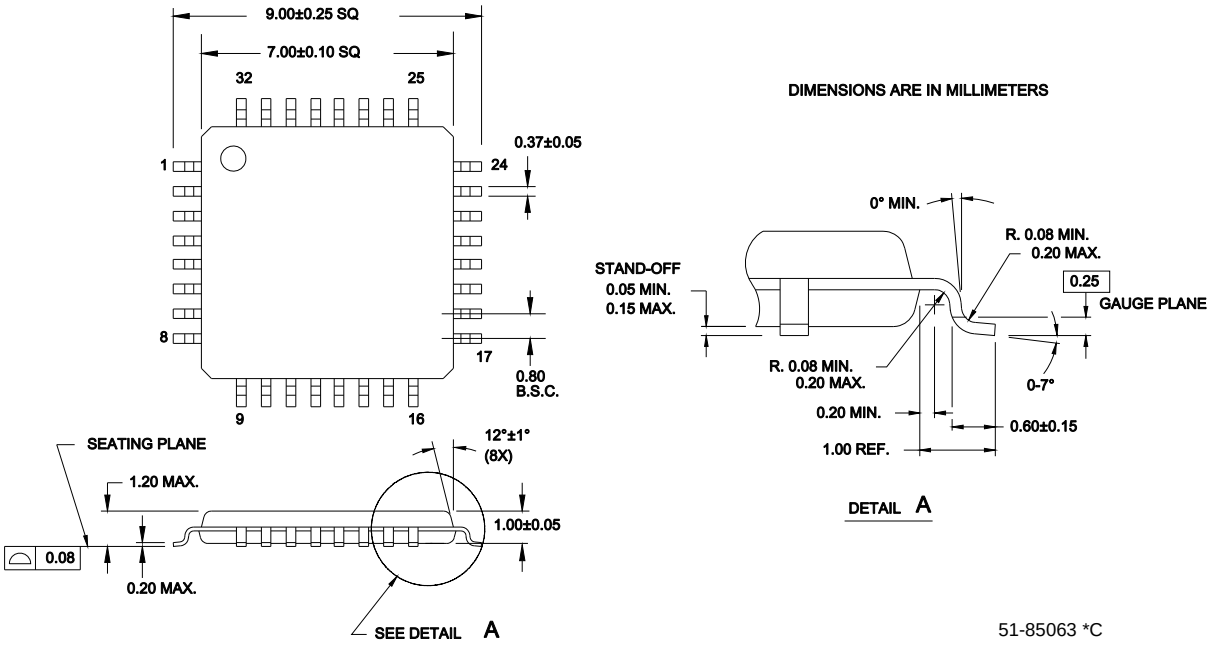
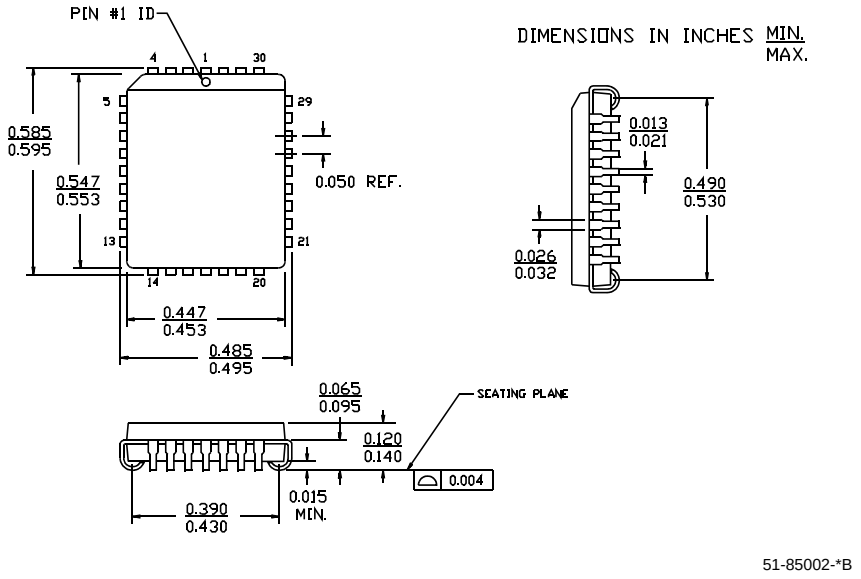



**Figure 16. 32-Pin Pb-free Plastic Leaded Chip Carrier J65, 51-85002**



## Document History Page

| Document Title: CY7C4421/4201/4211/4221, CY7C4231/4241/4251 64/256/512/1K/2K/4K/8K x 9 Synchronous FIFOs<br>Document Number: 38-06016 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 106477 | 09/10/01 | SZV | Change from Spec number: 38-00419 to 38-06016 |
| *A | 110725 | 03/20/02 | FSG | Change Input Leakage current $I_{IX}$ unit from mA to μA (typo) |
| *B | 122268 | 12/26/02 | RBI | Power up requirements added to Maximum Ratings Information |
| *C | 386306 | See ECN | ESH | Added Pb-free logo to top of front page<br>Added CY7C4421-10JXC, CY7C4201-15AXC. CY7C4201-15JXC, CY7C4211-10AXI, CY7C4211-15AXC, CY7C4211-15JXC, CY7C4221-15AXC, CY7C4221-15JXC, CY7C4231-15JXC, CY7C4231-15AXC, CY7C4241-10AXC, CY7C4241-15AXC, CY7C4241-15JXC, CY7C4251-10JXC, CY7C4251-10AXI, CY7C4251-15AXC, CY7C4251-15JXC |
| *D | 2863896 | 01/22/10 | VKN/PYRS | Removed inactive/pruned parts from the Ordering Information table<br>Added Table of Contents<br>Updated TQFP package diagram |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

### Products

| | |
|---|---|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc<br>cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| Optical & Image Sensing | cypress.com/go/image |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

### PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5