

## Contents

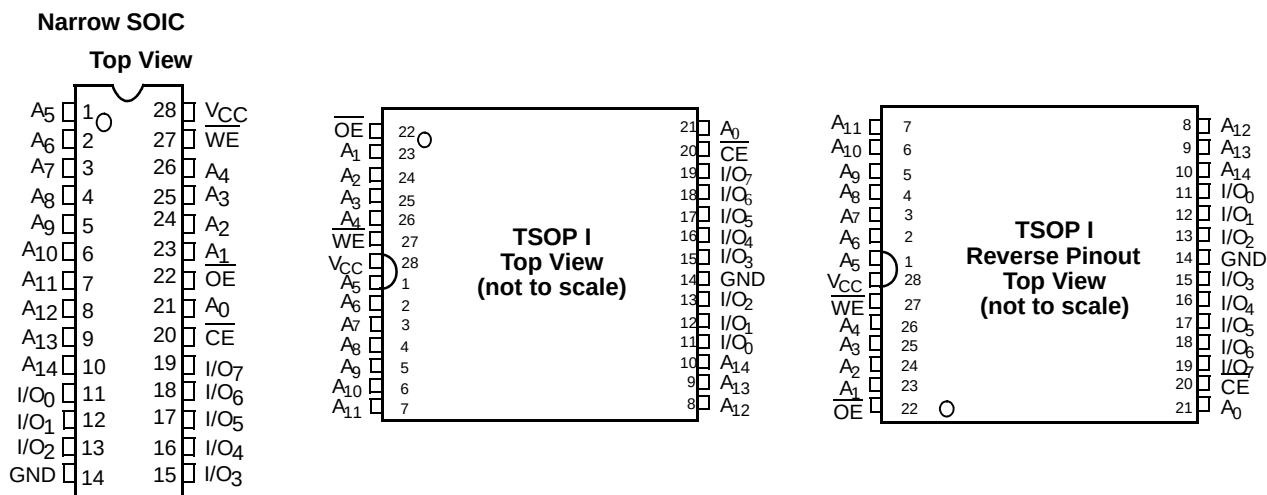
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## Product Portfolio

| Product     | Range        | V <sub>CC</sub> Range (V) |                    |     | Power Dissipation               |     |                                |     |
|-------------|--------------|---------------------------|--------------------|-----|---------------------------------|-----|--------------------------------|-----|
|             |              |                           |                    |     | Operating, I <sub>CC</sub> (mA) |     | Standby, I <sub>SB2</sub> (μA) |     |
|             |              | Min                       | Typ <sup>[1]</sup> | Max | Typ <sup>[1]</sup>              | Max | Typ <sup>[1]</sup>             | Max |
| CY62256VNLL | Commercial   | 2.7                       | 3.0                | 3.6 | 11                              | 30  | 0.1                            | 5   |
| CY62256VNLL | Industrial   | 2.7                       | 3.0                | 3.6 | 11                              | 30  | 0.1                            | 10  |
| CY62256VNLL | Automotive-A | 2.7                       | 3.0                | 3.6 | 11                              | 30  | 0.1                            | 10  |
| CY62256VNLL | Automotive-E | 2.7                       | 3.0                | 3.6 | 11                              | 30  | 0.1                            | 130 |

## Pin Configurations

Figure 1. 28-pin SOIC and 28-pin TSOP I pinouts



## Pin Definitions

| Pin Number      | Type          | Description                                                                                                                                                                            |
|-----------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1–10, 21, 23–26 | Input         | <b>A<sub>0</sub>–A<sub>14</sub></b> . Address inputs                                                                                                                                   |
| 11–13, 15–19    | Input/Output  | <b>I/O<sub>0</sub>–I/O<sub>7</sub></b> . Data lines. Used as input or output lines depending on operation.                                                                             |
| 27              | Input/Control | <b>WE</b> . When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.                                                                                          |
| 20              | Input/Control | <b>CE</b> . When LOW, selects the chip. When HIGH, deselects the chip.                                                                                                                 |
| 22              | Input/Control | <b>OE</b> . Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. |
| 14              | Ground        | <b>GND</b> . Ground for the device                                                                                                                                                     |
| 28              | Power Supply  | <b>V<sub>CC</sub></b> . Power supply for the device                                                                                                                                    |

### Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> Typ, T<sub>A</sub> = 25 °C, and t<sub>AA</sub> = 70 ns.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage to ground potential (pin 28 to pin 14) <sup>[2]</sup> ..... -0.5 V to +4.6 V

DC voltage applied to outputs in high Z State <sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage <sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage

(per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

| Device    | Range        | Ambient Temperature ( $T_A$ ) <sup>[3]</sup> | $V_{CC}$       |
|-----------|--------------|----------------------------------------------|----------------|
| CY62256VN | Commercial   | 0 °C to +70 °C                               | 2.7 V to 3.6 V |
|           | Industrial   | -40 °C to +85 °C                             |                |
|           | Automotive-A | -40 °C to +85 °C                             |                |
|           | Automotive-E | -40 °C to +125 °C                            |                |

## Electrical Characteristics

Over the Operating Range

| Parameter        | Description                                      | Test Conditions                                                                                                                                           |                                            | -70  |                    |                       | Unit |
|------------------|--------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|------|--------------------|-----------------------|------|
|                  |                                                  |                                                                                                                                                           |                                            | Min  | Typ <sup>[4]</sup> | Max                   |      |
| V <sub>OH</sub>  | Output HIGH voltage                              | I <sub>OH</sub> = −1.0 mA                                                                                                                                 | V <sub>CC</sub> = 2.7 V                    | 2.4  | –                  | –                     | V    |
| V <sub>OL</sub>  | Output LOW voltage                               | I <sub>OL</sub> = 2.1 mA                                                                                                                                  | V <sub>CC</sub> = 2.7 V                    | –    | –                  | 0.4                   | V    |
| V <sub>IH</sub>  | Input HIGH voltage                               |                                                                                                                                                           |                                            | 2.2  | –                  | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub>  | Input LOW voltage                                |                                                                                                                                                           |                                            | −0.5 | –                  | 0.8                   | V    |
| I <sub>IX</sub>  | Input leakage current                            | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                                                                                                                   | Commercial/<br>Industrial/<br>Automotive-A | −1   | –                  | +1                    | μA   |
|                  |                                                  |                                                                                                                                                           | Automotive-E                               | −10  | –                  | +10                   | μA   |
| I <sub>OZ</sub>  | Output leakage current                           | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> ,<br>Output Disabled                                                                                              | Commercial/<br>Industrial/<br>Automotive-A | −1   | –                  | +1                    | μA   |
|                  |                                                  |                                                                                                                                                           | Automotive-E                               | −10  | –                  | +10                   | μA   |
| I <sub>CC</sub>  | V <sub>CC</sub> operating supply current         | V <sub>CC</sub> = 3.6 V,<br>I <sub>OUT</sub> = 0 mA,<br>f = f <sub>MAX</sub> = 1/t <sub>RC</sub>                                                          | All ranges                                 | –    | 11                 | 30                    | mA   |
| I <sub>SB1</sub> | Automatic CE power-down<br>current - TTL inputs  | V <sub>CC</sub> = 3.6 V,<br>CE ≥ V <sub>IH</sub> ,<br>V <sub>IN</sub> ≥ V <sub>IH</sub> or<br>V <sub>IN</sub> ≤ V <sub>IL</sub> ,<br>f = f <sub>MAX</sub> | All ranges                                 | –    | 100                | 300                   | μA   |
| I <sub>SB2</sub> | Automatic CE power-down<br>current - CMOS inputs | V <sub>CC</sub> = 3.6 V,<br>CE ≥ V <sub>CC</sub> − 0.3 V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3 V or<br>V <sub>IN</sub> ≤ 0.3 V, f = 0               | Commercial                                 | –    | 0.1                | 5                     | μA   |
|                  |                                                  |                                                                                                                                                           | Industrial/<br>Automotive-A                | –    |                    | 10                    |      |
|                  |                                                  |                                                                                                                                                           | Automotive-E                               | –    |                    | 130                   |      |

### Notes

2.  $V_{IL}$  (min) = -2.0 V for pulse durations of less than 20 ns.

3.  $T_A$  is the "Instant-On" case temperature.

4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC}$  Typ,  $T_A = 25$  °C, and  $t_{AA} = 70$  ns.

## Capacitance

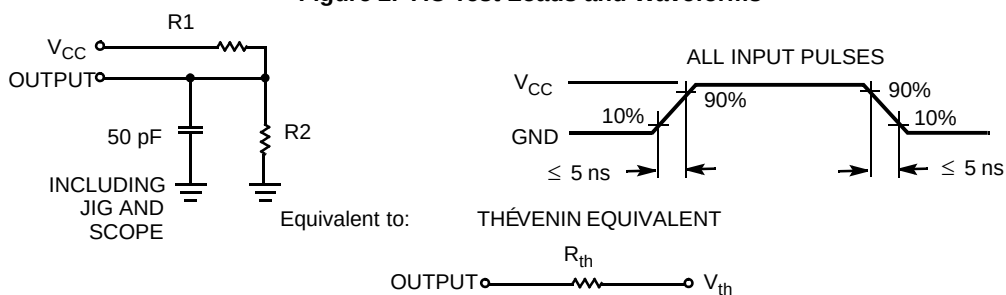
| Parameter <sup>[5]</sup> | Description        | Test Conditions                                                         | Max | Unit |
|--------------------------|--------------------|-------------------------------------------------------------------------|-----|------|
| $C_{IN}$                 | Input capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.0\text{ V}$ | 6   | pF   |
| $C_{OUT}$                | Output capacitance |                                                                         | 8   | pF   |

## Thermal Resistance

| Parameter <sup>[5]</sup> | Description                              | Test Conditions                                                               | SOIC  | TSOPI | RTSOPI | Unit               |
|--------------------------|------------------------------------------|-------------------------------------------------------------------------------|-------|-------|--------|--------------------|
| $\theta_{JA}$            | Thermal resistance (junction to ambient) | Still air, soldered on a $3 \times 4.5$ inch, two-layer printed circuit board | 68.45 | 87.62 | 87.62  | $^\circ\text{C/W}$ |
| $\theta_{JC}$            | Thermal resistance (junction to case)    |                                                                               | 26.94 | 23.73 | 23.73  | $^\circ\text{C/W}$ |

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



| Parameter | Value | Units |
|-----------|-------|-------|
| R1        | 1100  | Ohms  |
| R2        | 1500  | Ohms  |
| RTH       | 645   | Ohms  |
| VTH       | 1.750 | Volts |

### Note

5. Tested initially and after any design or process changes that may affect these parameters.

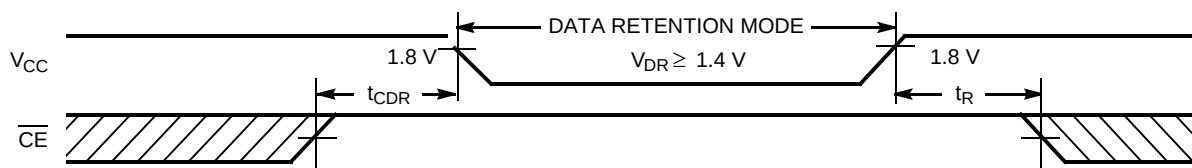
## Data Retention Characteristics

Over the Operating Range

| Parameter       | Description                          | Conditions <sup>[6]</sup>                                                                                                                         | Min                                                                      | Typ <sup>[7]</sup> | Max          | Unit          |
|-----------------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|--------------------|--------------|---------------|
| $V_{DR}$        | $V_{CC}$ for data retention          |                                                                                                                                                   | 1.4                                                                      | –                  | –            | V             |
| $I_{CCDR}$      | Data retention current               | $V_{CC} = 1.4\text{ V}$ ,<br>$\overline{CE} \geq V_{CC} - 0.3\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.3\text{ V}$<br>or $V_{IN} \leq 0.3\text{ V}$ | Commercial<br>–<br>Industrial/<br>Automotive-A<br>–<br>Automotive-E<br>– | 0.1                | 3<br>6<br>50 | $\mu\text{A}$ |
| $t_{CDR}^{[6]}$ | Chip deselect to data retention time |                                                                                                                                                   | 0                                                                        | –                  | –            | ns            |
| $t_R^{[8]}$     | Operation recovery time              |                                                                                                                                                   | 70                                                                       | –                  | –            | ns            |

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

6. No input may exceed  $V_{CC} + 0.3\text{ V}$ .
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC}\text{ Typ}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , and  $t_{AA} = 70\text{ ns}$ .
8. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics

Over the Operating Range

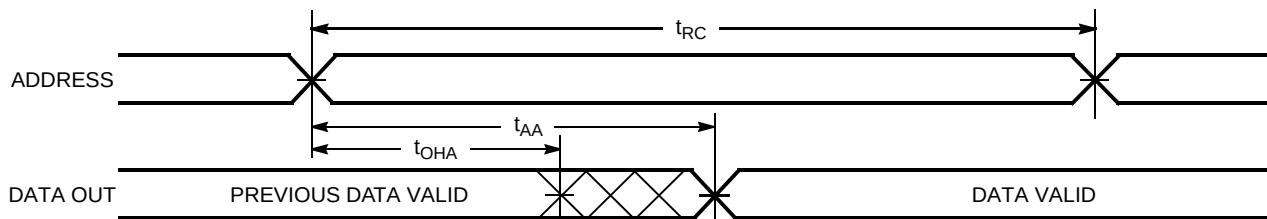
| Parameter <sup>[9]</sup>        | Description                                        | CY62256VN-70 |     | Unit |
|---------------------------------|----------------------------------------------------|--------------|-----|------|
|                                 |                                                    | Min          | Max |      |
| Read Cycle                      |                                                    |              |     |      |
| t <sub>RC</sub>                 | Read cycle time                                    | 70           | –   | ns   |
| t <sub>AA</sub>                 | Address to data valid                              | –            | 70  | ns   |
| t <sub>OHA</sub>                | Data hold from address change                      | 10           | –   | ns   |
| t <sub>ACE</sub>                | $\overline{CE}$ LOW to data valid                  | –            | 70  | ns   |
| t <sub>DOE</sub>                | $\overline{OE}$ LOW to data valid                  | –            | 35  | ns   |
| t <sub>LZOE</sub>               | $\overline{OE}$ LOW to low Z <sup>[10]</sup>       | 5            | –   | ns   |
| t <sub>HZOE</sub>               | $\overline{OE}$ HIGH to high Z <sup>[10, 11]</sup> | –            | 25  | ns   |
| t <sub>LZCE</sub>               | $\overline{CE}$ LOW to low Z <sup>[10]</sup>       | 10           | –   | ns   |
| t <sub>HZCE</sub>               | $\overline{CE}$ HIGH to high Z <sup>[10, 11]</sup> | –            | 25  | ns   |
| t <sub>PU</sub>                 | $\overline{CE}$ LOW to power-up                    | 0            | –   | ns   |
| t <sub>PD</sub>                 | $\overline{CE}$ HIGH to power-down                 | –            | 70  | ns   |
| Write Cycle <sup>[12, 13]</sup> |                                                    |              |     |      |
| t <sub>WC</sub>                 | Write cycle time                                   | 70           | –   | ns   |
| t <sub>SCE</sub>                | $\overline{CE}$ LOW to write end                   | 60           | –   | ns   |
| t <sub>AW</sub>                 | Address setup to write end                         | 60           | –   | ns   |
| t <sub>HA</sub>                 | Address hold from write end                        | 0            | –   | ns   |
| t <sub>SA</sub>                 | Address setup to write start                       | 0            | –   | ns   |
| t <sub>PWE</sub>                | $\overline{WE}$ pulse width                        | 50           | –   | ns   |
| t <sub>SD</sub>                 | Data setup to write end                            | 30           | –   | ns   |
| t <sub>HD</sub>                 | Data hold from write end                           | 0            | –   | ns   |
| t <sub>HZWE</sub>               | $\overline{WE}$ LOW to high Z <sup>[10, 11]</sup>  | –            | 25  | ns   |
| t <sub>LZWE</sub>               | $\overline{WE}$ HIGH to low Z <sup>[10]</sup>      | 10           | –   | ns   |

### Notes

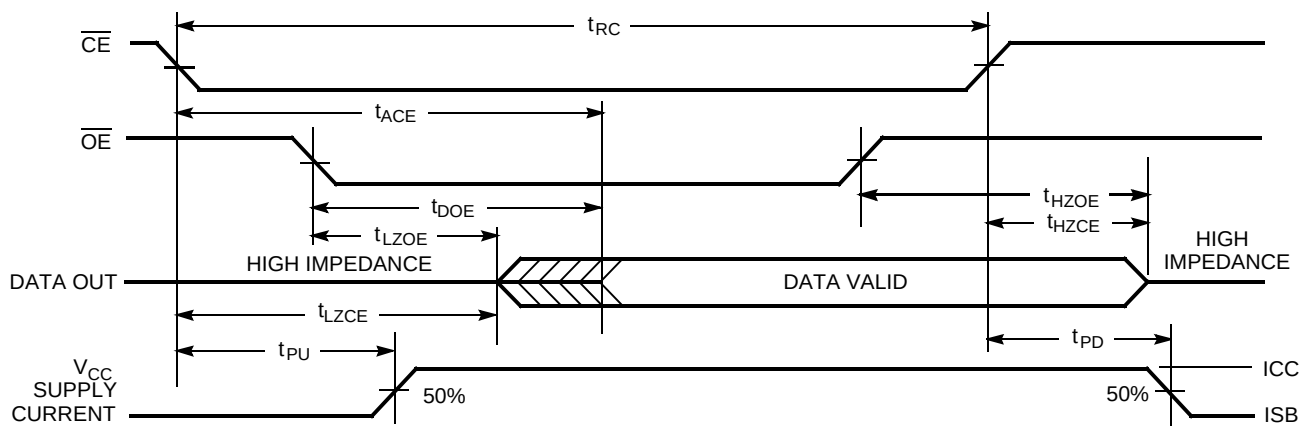
9. Test conditions assume signal transition time of 5 ns or less timing reference levels of  $V_{CC}/2$ , input pulse levels of 0 to  $V_{CC}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 100-pF load capacitance.
10. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
11.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
12. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
13. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

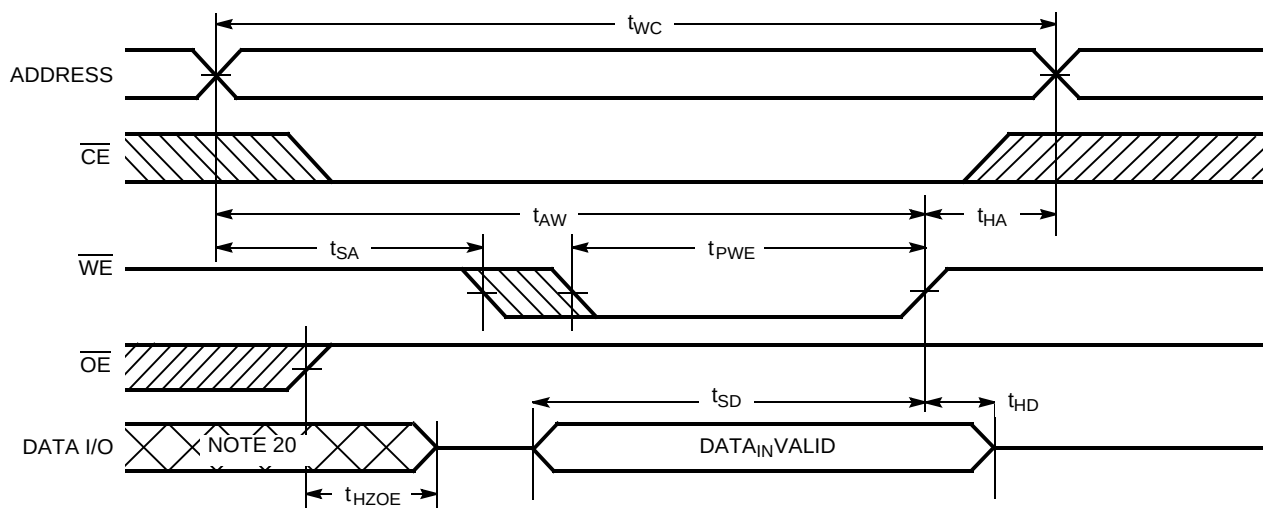
**Figure 4. Read Cycle No. 1** [14, 15]



**Figure 5. Read Cycle No. 2** [15, 16]

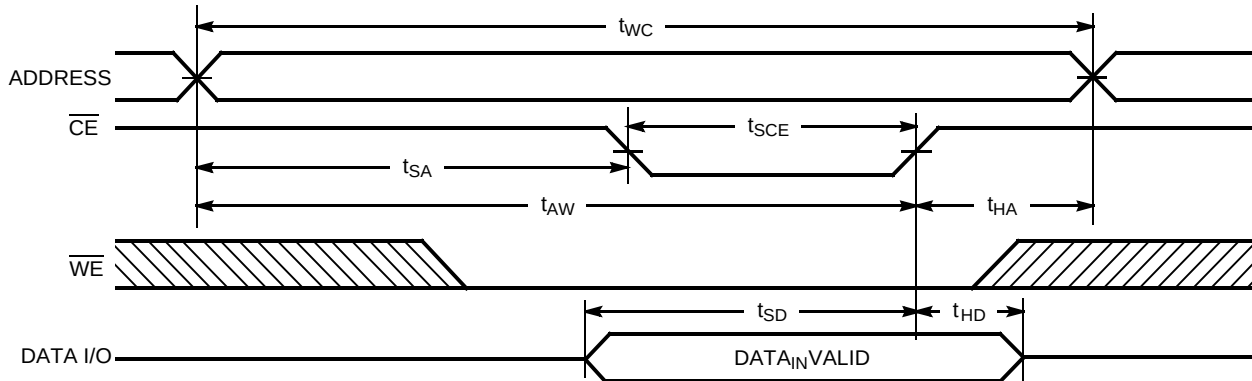
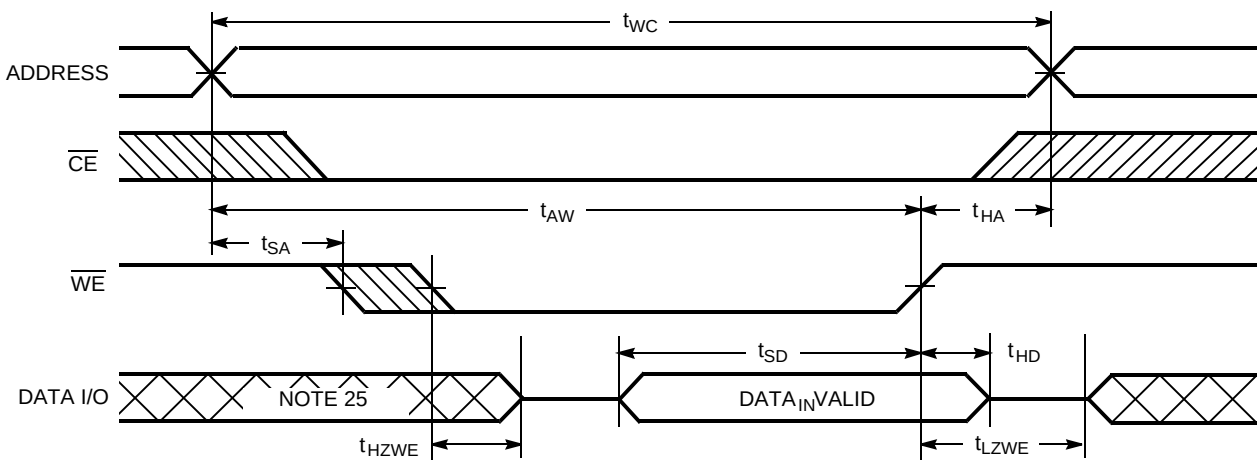


**Figure 6. Write Cycle No. 1 (WE Controlled)** [17, 18, 19]



### Notes

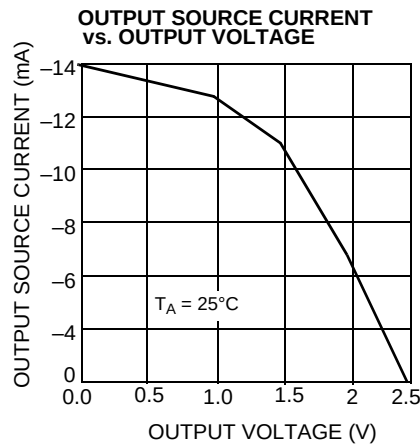
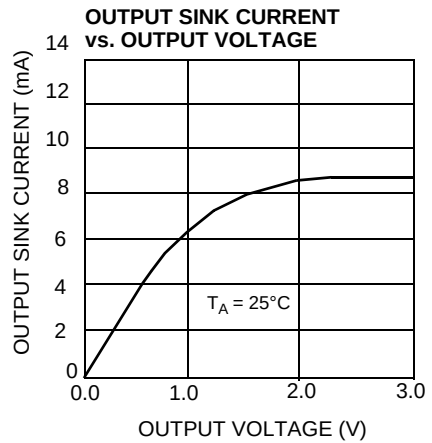
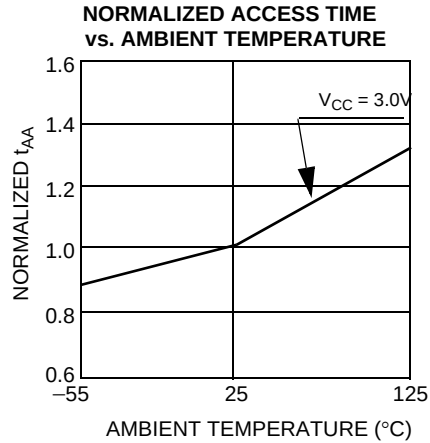
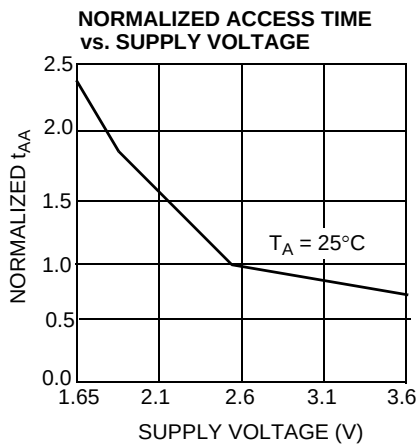
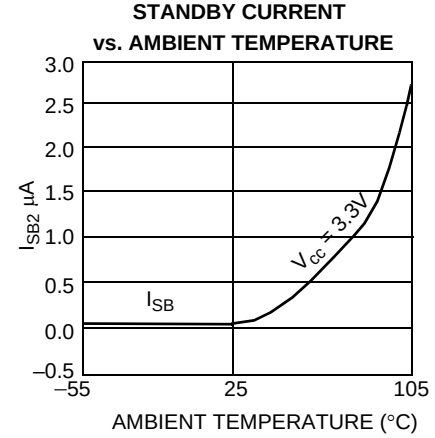
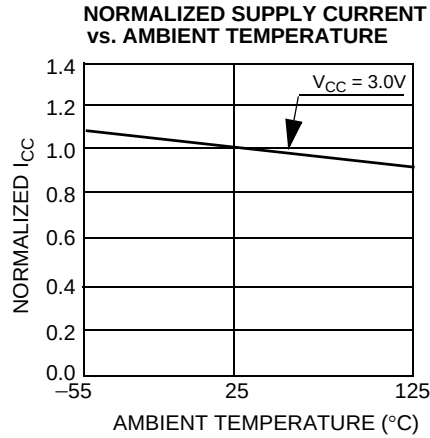
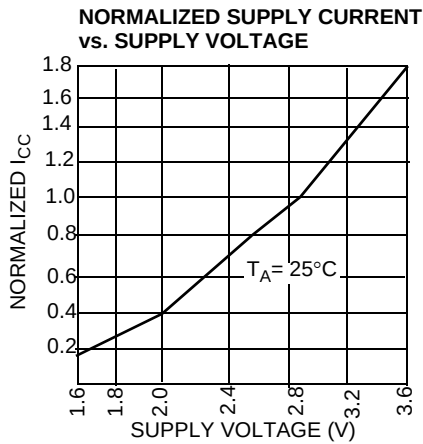
14. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
15. WE is HIGH for read cycle.
16. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
17. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
18. Data I/O is high impedance if  $OE = V_{IH}$ .
19. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.
20. During this period, the I/Os are in output state and input signals should not be applied.

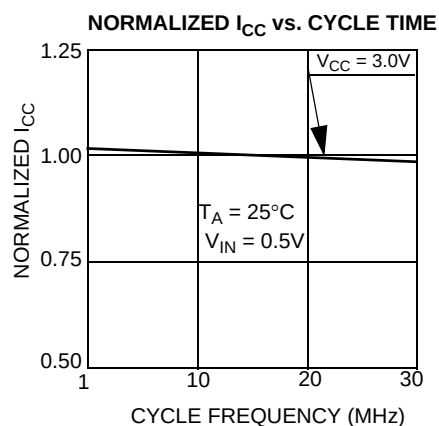
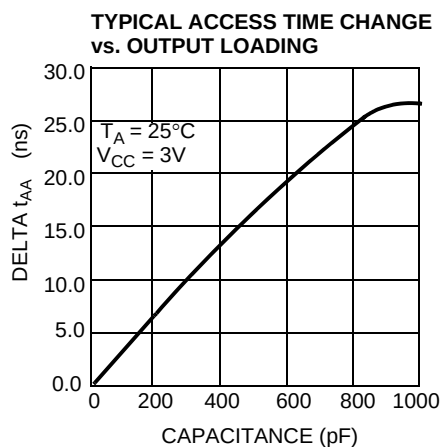
**Switching Waveforms (continued)**
**Figure 7. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled) [21, 22, 23]**

**Figure 8. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [23, 24]**

**Notes**

21. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
22. Data I/O is high impedance if  $\text{OE} = V_{\text{IH}}$ .
23. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state.
24. The minimum write cycle time for write cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .
25. During this period, the I/Os are in output state and input signals should not be applied.



## Typical DC and AC Characteristics



**Typical DC and AC Characteristics** *(continued)*

**Truth Table**

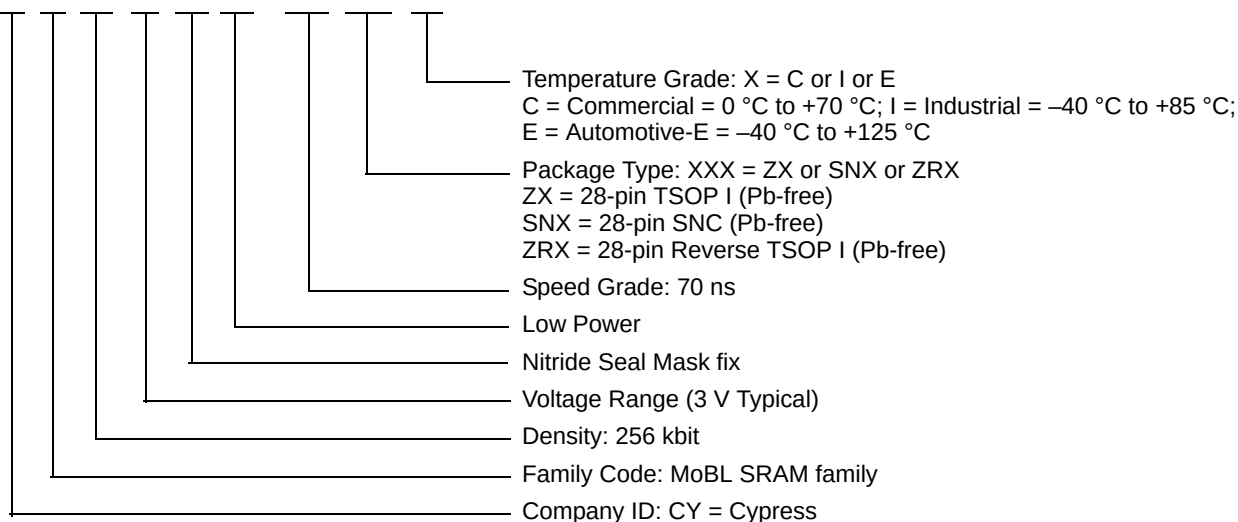
| $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | Inputs/Outputs | Mode                      | Power                |
|------------------------|------------------------|------------------------|----------------|---------------------------|----------------------|
| H                      | X                      | X                      | High Z         | Deselect/power-down       | Standby ( $I_{SB}$ ) |
| L                      | H                      | L                      | Data out       | Read                      | Active ( $I_{CC}$ )  |
| L                      | L                      | X                      | Data in        | Write                     | Active ( $I_{CC}$ )  |
| L                      | H                      | H                      | High Z         | Deselect, output disabled | Active ( $I_{CC}$ )  |

## Ordering Information

| Speed (ns) | Ordering Code      | Package Diagram | Package Type                                | Operating Range |
|------------|--------------------|-----------------|---------------------------------------------|-----------------|
| 70         | CY62256VNLL-70ZXC  | 51-85071        | 28-pin TSOP I (Pb-free)                     | Commercial      |
|            | CY62256VNLL-70SNXI | 51-85092        | 28-pin SNC (300 Mils) Narrow Body (Pb-free) | Industrial      |
|            | CY62256VNLL-70ZXI  | 51-85071        | 28-pin TSOP I (Pb-free)                     |                 |
|            | CY62256VNLL-70ZRXI | 51-85074        | 28-pin Reverse TSOP I (Pb-free)             |                 |
|            | CY62256VNLL-70SNXE | 51-85092        | 28-pin SNC (300 Mils) Narrow Body (Pb-free) | Automotive-E    |
|            | CY62256VNLL-70ZXE  | 51-85071        | 28-pin TSOP I (Pb-free)                     |                 |

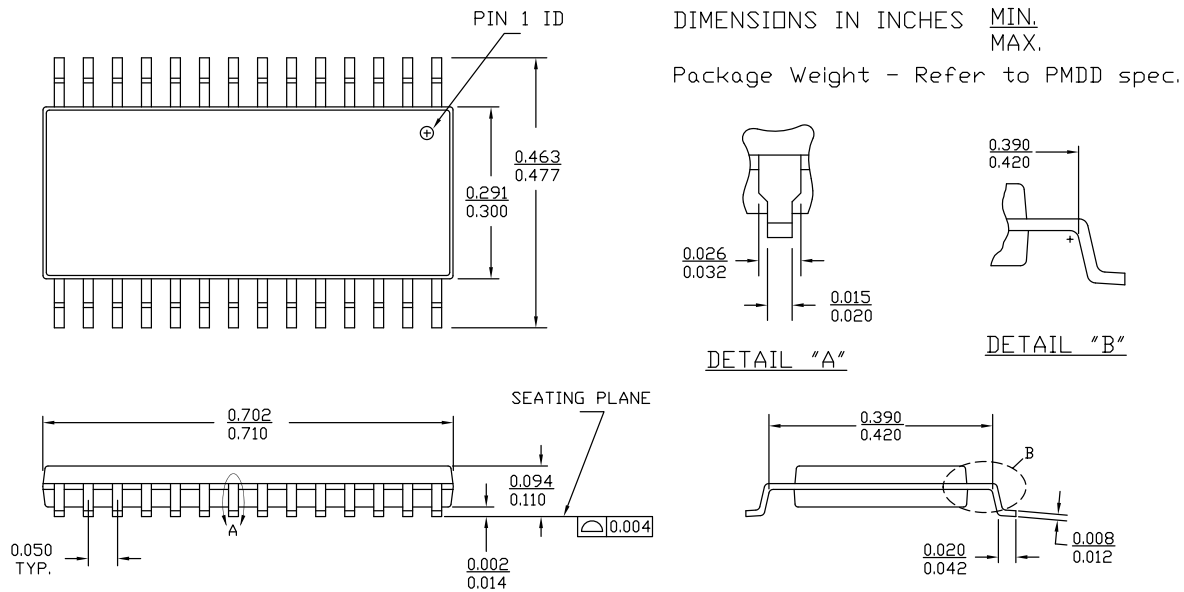
## Ordering Code Definitions

CY 62 256 V N LL - 70 XXX X



## Package Diagrams

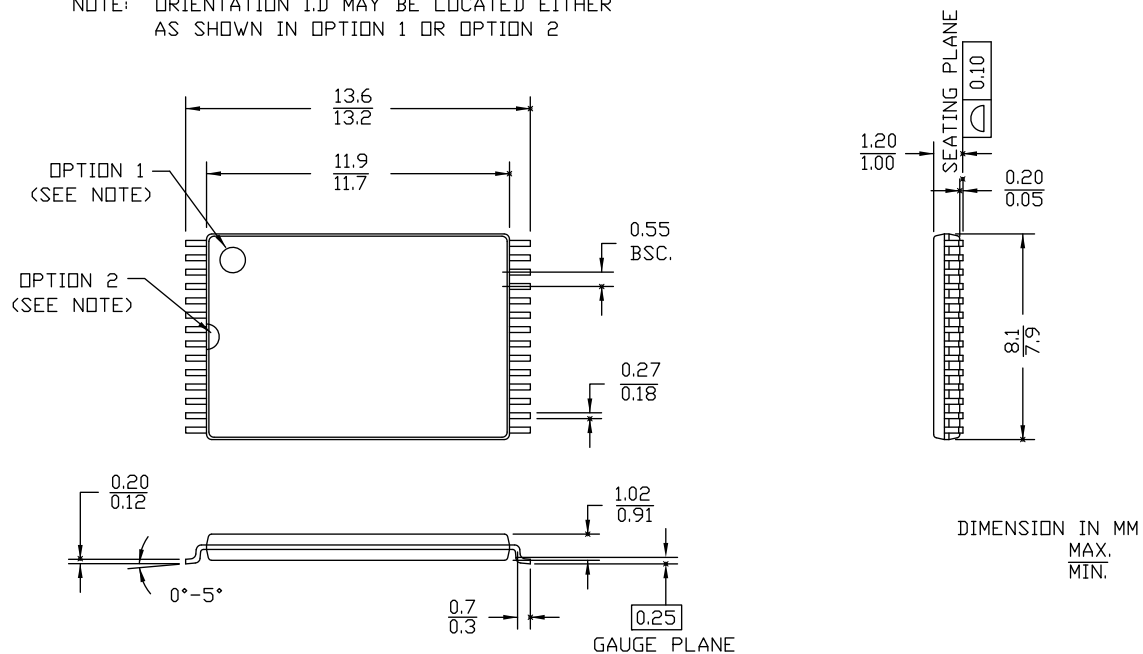
Figure 9. 28-pin SNC (300 Mils) SN28.3 (Narrow Body) Package Outline, 51-85092



51-85092 \*E

Figure 10. 28-pin TSOP 1 (8 × 13.4 × 1.2 mm) Z28 (Standard) Package Outline, 51-85071

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

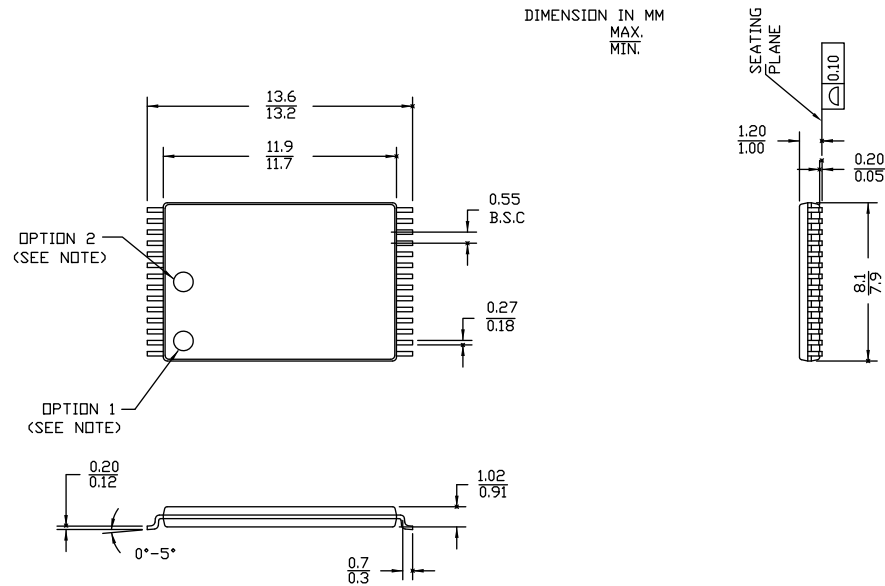


51-85071 \*J

## Package Diagrams

**Figure 11. 28-pin TSOP I (8 × 13.4 mm) Package Outline - Reverse, 51-85074**

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



51-85074 \*H

## Acronyms

| Acronym | Description                             |
|---------|-----------------------------------------|
| CMOS    | Complementary Metal Oxide Semiconductor |
| I/O     | Input/Output                            |
| SRAM    | Static Random Access Memory             |
| TSOP    | Thin Small Outline Package              |
| VFBGA   | Very Fine-Pitch Ball Grid Array         |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| μA     | microampere     |
| mA     | milliampere     |
| MHz    | megahertz       |
| ns     | nanosecond      |
| Ω      | ohm             |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

## Document History Page

| Document Title: CY62256VN, 256-Kbit (32 K × 8) Static RAM<br>Document Number: 001-06512 |         |                 |                 |                                                                                                                                                                                                                                                                                                           |
|-----------------------------------------------------------------------------------------|---------|-----------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                     |
| **                                                                                      | 426504  | NXR             | See ECN         | New data sheet                                                                                                                                                                                                                                                                                            |
| *A                                                                                      | 488954  | NXR             | See ECN         | Added Automotive product<br>Updated ordering Information table                                                                                                                                                                                                                                            |
| *B                                                                                      | 2769239 | VKN / AESA      | 09/25/09        | Corrected V <sub>IL</sub> description in the Electrical Characteristics table                                                                                                                                                                                                                             |
| *C                                                                                      | 2901521 | AJU             | 03/30/2010      | Removed inactive parts from Ordering Information.<br>Updated Package Diagram.                                                                                                                                                                                                                             |
| *D                                                                                      | 3119519 | AJU             | 01/04/2011      | Updated <a href="#">Ordering Information</a> .<br>Added <a href="#">Ordering Code Definitions</a> .                                                                                                                                                                                                       |
| *E                                                                                      | 3329873 | RAME            | 07/27/11        | Updated template and styles according to current Cypress standards.<br>Added acronyms and units.<br>Removed reference to AN1064 SRAM system guidelines.<br>Updated operation recovery time parameter under <a href="#">Data Retention Characteristics on page 6</a> .                                     |
| *F                                                                                      | 4122787 | VINI            | 09/13/2013      | Updated <a href="#">Package Diagrams</a> :<br>spec 51-85092 – Changed revision from *C to *E.<br>Updated in new template.<br>Completing Sunset Review.                                                                                                                                                    |
| *G                                                                                      | 4525875 | VINI            | 10/06/2014      | Updated <a href="#">Maximum Ratings</a> :<br>Referred Note 2 in “Supply voltage to ground potential (pin 28 to pin 14)”.<br>Updated <a href="#">Package Diagrams</a> :<br>spec 51-85071 – Changed revision from *I to *J.<br>spec 51-85074 – Changed revision from *G to *H.<br>Completing Sunset Review. |
| *H                                                                                      | 4576406 | VINI            | 01/16/2015      | Added related documentation hyperlink in page 1.<br>Added Note <a href="#">13</a> in <a href="#">Switching Characteristics</a> .<br>Added note reference <a href="#">13</a> in the <a href="#">Switching Characteristics</a> table.                                                                       |

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