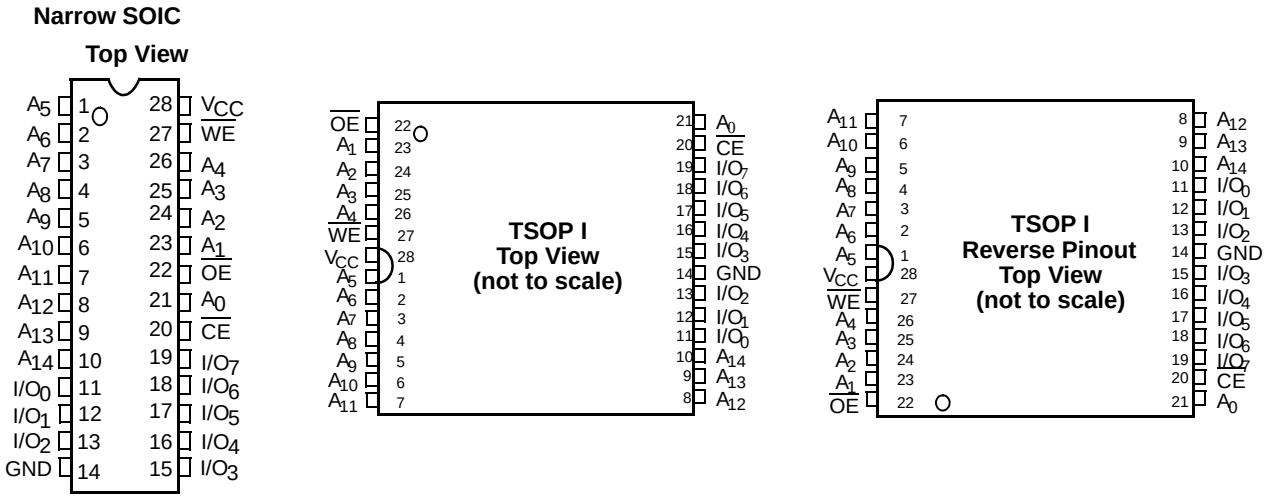
## Contents

## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) | | | Power Dissipation | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | Operating, $I_{CC}$ (mA) | | Standby, $I_{SB2}$ (µA) | |
| | | Min | Typ[1] | Max | Typ[1] | Max | Typ[1] | Max |
| CY62256VNLL | Commercial | 2.7 | 3.0 | 3.6 | 11 | 30 | 0.1 | 5 |
| CY62256VNLL | Industrial | 2.7 | 3.0 | 3.6 | 11 | 30 | 0.1 | 10 |
| CY62256VNLL | Automotive-A | 2.7 | 3.0 | 3.6 | 11 | 30 | 0.1 | 10 |
| CY62256VNLL | Automotive-E | 2.7 | 3.0 | 3.6 | 11 | 30 | 0.1 | 130 |

## Pin Configurations

**Figure 1. 28-pin SOIC and 28-pin TSOP I pinouts**




## Pin Definitions

| Pin Number | Type | Description |
|---|---|---|
| 1–10, 21, 23–26 | Input | **$A_0$–$A_{14}$**. Address inputs |
| 11–13, 15–19 | Input/Output | **$I/O_0$–$I/O_7$**. Data lines. Used as input or output lines depending on operation. |
| 27 | Input/Control | **$\overline{WE}$**. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted. |
| 20 | Input/Control | **$\overline{CE}$**. When LOW, selects the chip. When HIGH, deselects the chip. |
| 22 | Input/Control | **$\overline{OE}$**. Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. |
| 14 | Ground | **GND**. Ground for the device |
| 28 | Power Supply | **$V_{CC}$**. Power supply for the device |

**Note**
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC}$ Typ, $T_A$ = 25 °C, and $t_{AA}$ = 70 ns.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential (pin 28 to pin 14) [2] .....–0.5 V to +4.6 V

DC voltage applied to outputs in high Z State [2] .....–0.5 V to $V_{CC}$ + 0.5 V

DC input voltage [2] .....–0.5 V to $V_{CC}$ + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

| Device | Range | Ambient Temperature ($T_A$) [3] | $V_{CC}$ |
|---|---|---|---|
| CY62256VN | Commercial | 0 °C to +70 °C | 2.7 V to 3.6 V |
| | Industrial | –40 °C to +85 °C | |
| | Automotive-A | –40 °C to +85 °C | |
| | Automotive-E | –40 °C to +125 °C | |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | -70 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [4] | Max | |
| $V_{OH}$ | Output HIGH voltage | $I_{OH}$ = –1.0 mA | $V_{CC}$ = 2.7 V | 2.4 | – | – | V |
| $V_{OL}$ | Output LOW voltage | $I_{OL}$ = 2.1 mA | $V_{CC}$ = 2.7 V | – | – | 0.4 | V |
| $V_{IH}$ | Input HIGH voltage | | | 2.2 | – | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage | | | –0.5 | – | 0.8 | V |
| $I_{IX}$ | Input leakage current | GND ≤ $V_{IN}$ ≤ $V_{CC}$ | Commercial/ Industrial/ Automotive-A | –1 | – | +1 | µA |
| | | | Automotive-E | –10 | – | +10 | µA |
| $I_{OZ}$ | Output leakage current | GND ≤ $V_{IN}$ ≤ $V_{CC}$, Output Disabled | Commercial/ Industrial/ Automotive-A | –1 | – | +1 | µA |
| | | | Automotive-E | –10 | – | +10 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | $V_{CC}$ = 3.6 V, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ | All ranges | – | 11 | 30 | mA |
| $I_{SB1}$ | Automatic CE power-down current - TTL inputs | $V_{CC}$ = 3.6 V, CE ≥ $V_{IH}$, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | All ranges | – | 100 | 300 | µA |
| $I_{SB2}$ | Automatic CE power-down current - CMOS inputs | $V_{CC}$ = 3.6 V, CE ≥ $V_{CC}$ – 0.3 V, $V_{IN}$ ≥ $V_{CC}$ – 0.3 V or $V_{IN}$ ≤ 0.3 V, f = 0 | Commercial | – | 0.1 | 5 | µA |
| | | | Industrial/ Automotive-A | – | | 10 | |
| | | | Automotive-E | – | | 130 | |

**Notes**
2. $V_{IL}$ (min) = –2.0 V for pulse durations of less than 20 ns.
3. $T_A$ is the “Instant-On” case temperature.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC}$ Typ, $T_A$ = 25 °C, and $t_{AA}$ = 70 ns.

## Capacitance

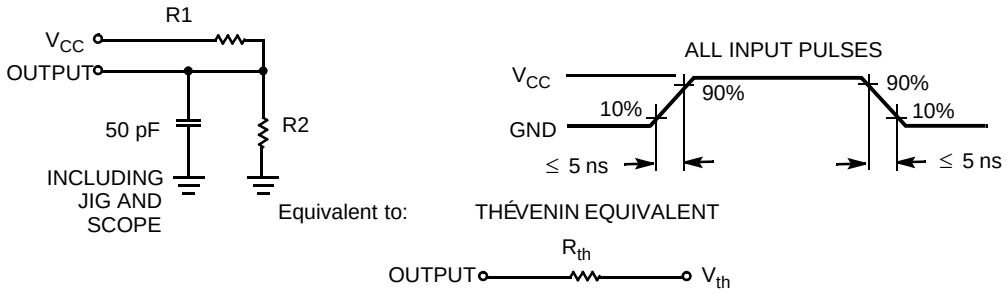
| Parameter [5] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = 3.0 V | 6 | pF |
| $C_{OUT}$ | Output capacitance | | 8 | pF |

## Thermal Resistance

| Parameter [5] | Description | Test Conditions | SOIC | TSOPI | RTSOPI | Unit |
|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 68.45 | 87.62 | 87.62 | °C/W |
| $\theta_{JC}$ | Thermal resistance (junction to case) | | 26.94 | 23.73 | 23.73 | °C/W |

## AC Test Loads and Waveforms

**Figure 2. AC Test Loads and Waveforms**




| Parameter | Value | Units |
|---|---|---|
| R1 | 1100 | Ohms |
| R2 | 1500 | Ohms |
| RTH | 645 | Ohms |
| VTH | 1.750 | Volts |

**Note**
5. Tested initially and after any design or process changes that may affect these parameters.

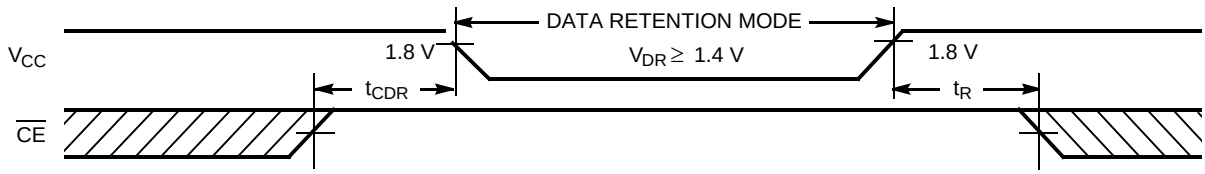
## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions[6] | | Min | Typ [7] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | | | 1.4 | – | – | V |
| $I_{CCDR}$ | Data retention current | $V_{CC}$ = 1.4 V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V | Commercial | – | 0.1 | 3 | µA |
| | | | Industrial/ Automotive-A | – | | 6 | |
| | | | Automotive-E | – | | 50 | |
| $t_{CDR}$[6] | Chip deselect to data retention time | | | 0 | – | – | ns |
| $t_R$[8] | Operation recovery time | | | 70 | – | – | ns |

## Data Retention Waveform

**Figure 3. Data Retention Waveform**




**Notes**
6. No input may exceed $V_{CC}$ + 0.3 V.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC}$ Typ, $T_A$ = 25 °C, and $t_{AA}$ = 70 ns.
8. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics

Over the Operating Range

| Parameter [9] | Description | CY62256VN-70 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read cycle time | 70 | – | ns |
| $t_{AA}$ | Address to data valid | – | 70 | ns |
| $t_{OHA}$ | Data hold from address change | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to data valid | – | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to low Z[10] | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to high Z[10, 11] | – | 25 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to low Z[10] | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to high Z[10, 11] | – | 25 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to power-up | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to power-down | – | 70 | ns |
| **Write Cycle** [12, 13] | | | | |
| $t_{WC}$ | Write cycle time | 70 | – | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to write end | 60 | – | ns |
| $t_{AW}$ | Address setup to write end | 60 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 50 | – | ns |
| $t_{SD}$ | Data setup to write end | 30 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to high Z[10, 11] | – | 25 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to low Z[10] | 10 | – | ns |

**Notes**

9. Test conditions assume signal transition time of 5 ns or less timing reference levels of $V_{CC}/2$, input pulse levels of 0 to $V_{CC}$, and output loading of the specified $I_{OL}/I_{OH}$ and 100-pF load capacitance.
10. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
11. $t_{HZOE}$, $t_{HZCE}$, and $t_{HZWE}$ are specified with $C_L$ = 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
12. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
13. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of $t_{HZWE}$ and $t_{SD}$.

## Switching Waveforms

**Figure 4. Read Cycle No. 1** [14, 15]

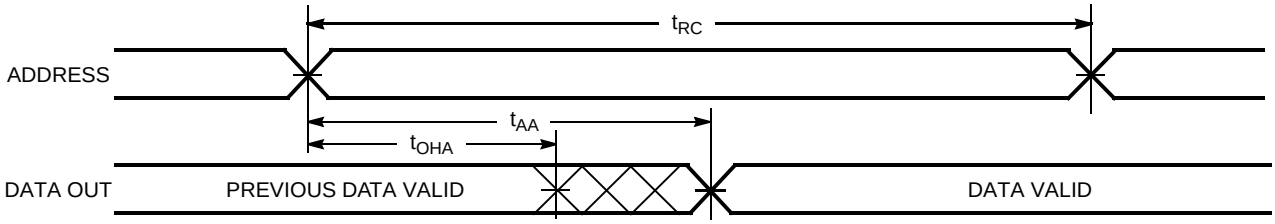



**Figure 5. Read Cycle No. 2** [15, 16]

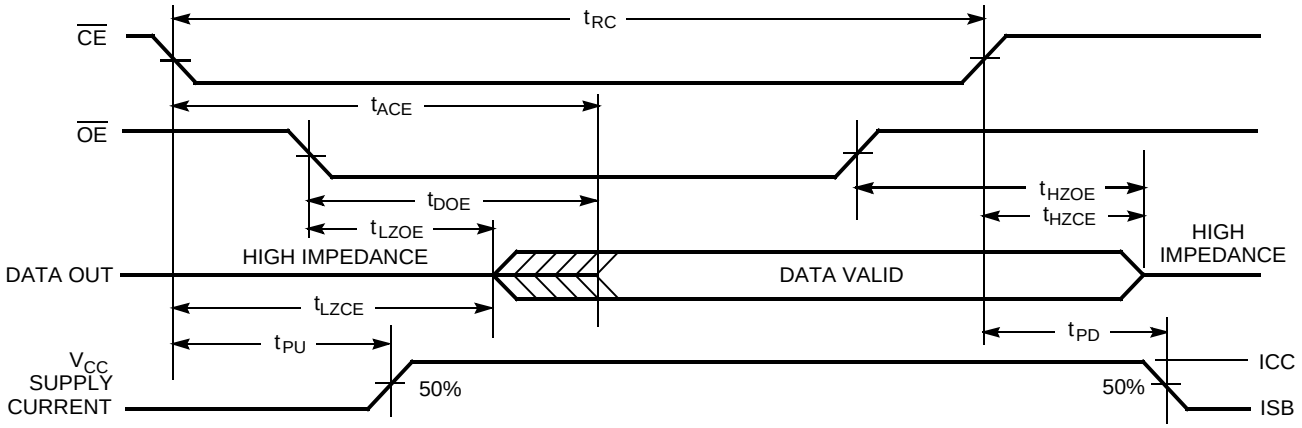
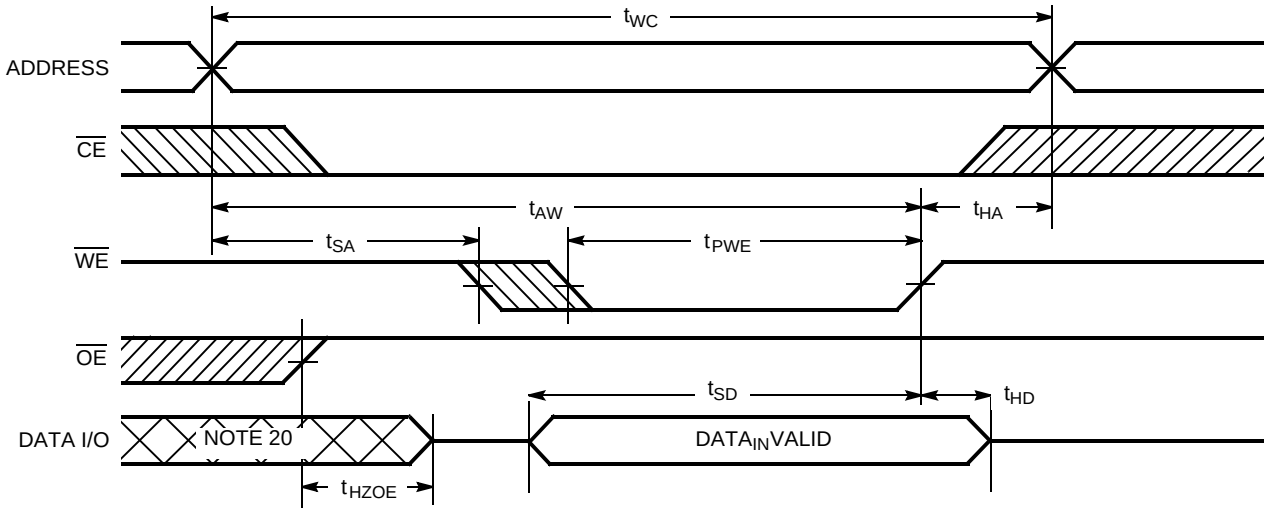



**Figure 6. Write Cycle No. 1 (WE Controlled)** [17, 18, 19]




**Notes**

14. Device is continuously selected. OE, CE = $V_{IL}$.
15. WE is HIGH for read cycle.
16. Address valid prior to or coincident with CE transition LOW.
17. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
18. Data I/O is high impedance if OE = $V_{IH}$.
19. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state.
20. During this period, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms *(continued)*

**Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled)** [21, 22, 23]

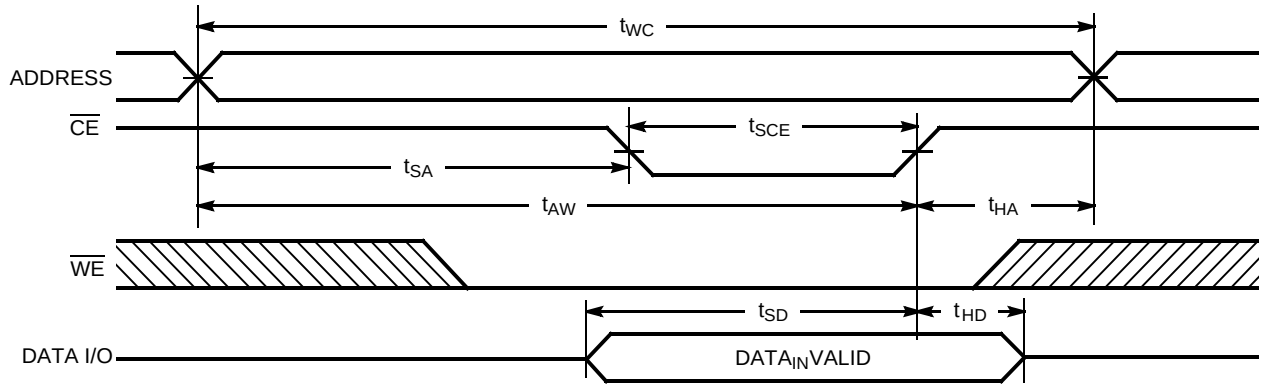
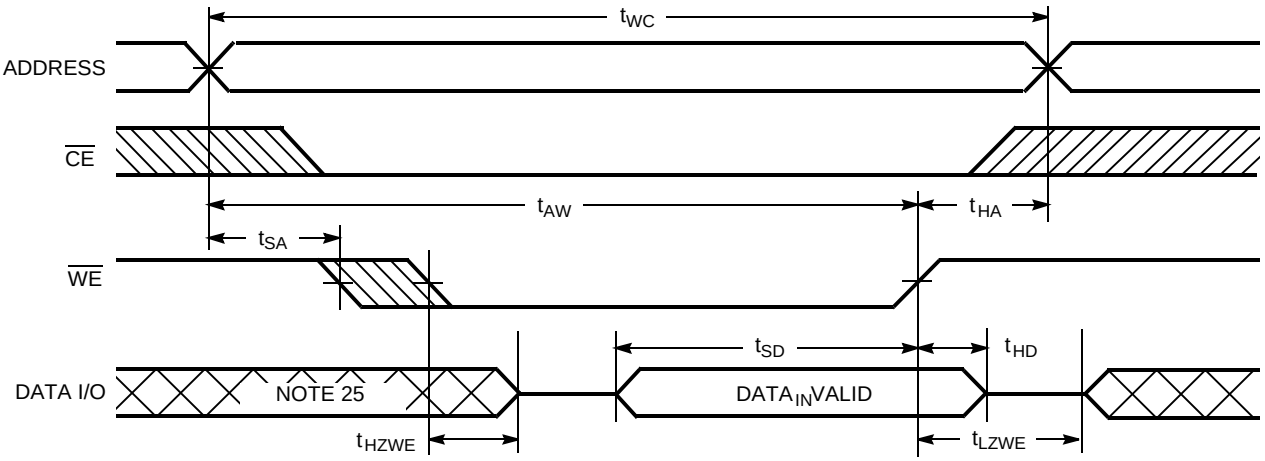



**Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)** [23, 24]

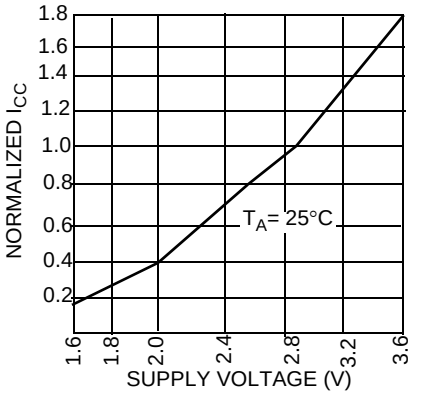



**Notes**

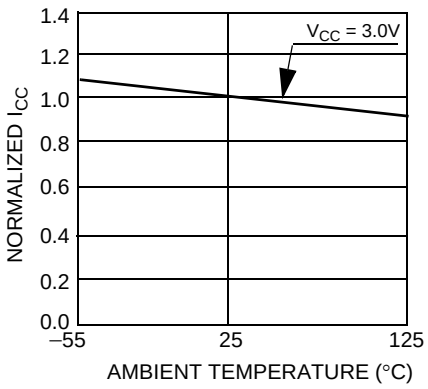
21. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
22. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
23. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
24. The minimum write cycle time for write cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of $t_{HZWE}$ and $t_{SD}$.
25. During this period, the I/Os are in output state and input signals should not be applied.

## Typical DC and AC Characteristics

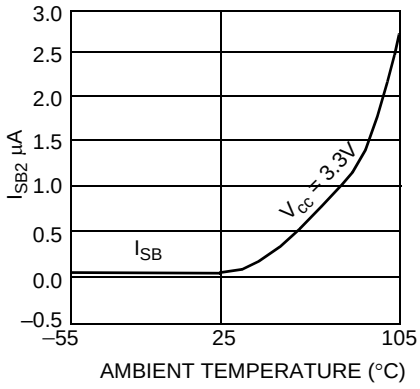
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



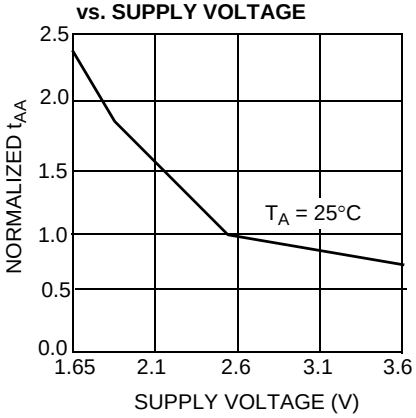

**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



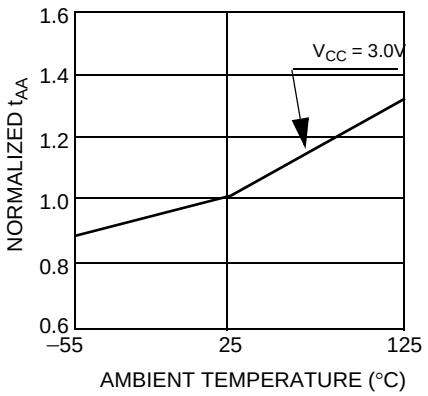

**STANDBY CURRENT vs. AMBIENT TEMPERATURE**



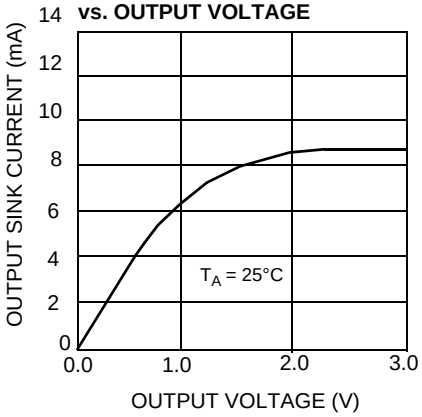

**NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**



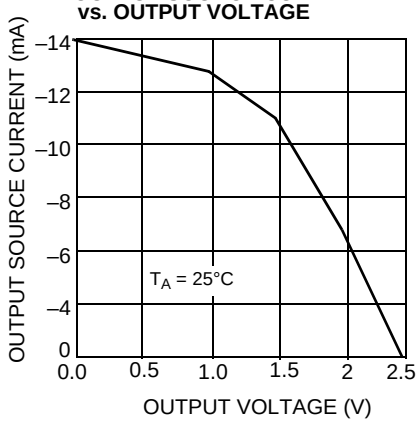

**NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE**




**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**

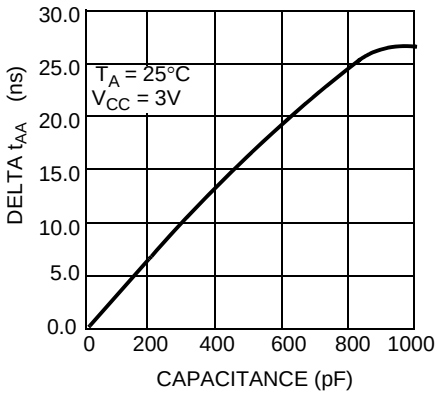



**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**

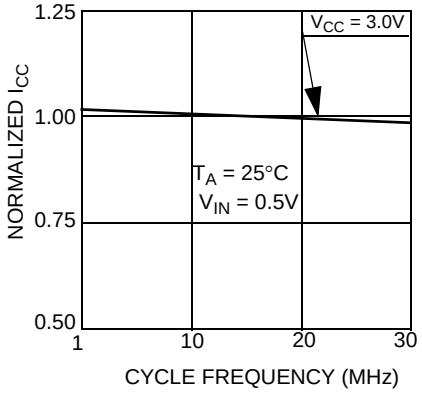


## Typical DC and AC Characteristics *(continued)*

**TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING**




**NORMALIZED $I_{CC}$ vs. CYCLE TIME**



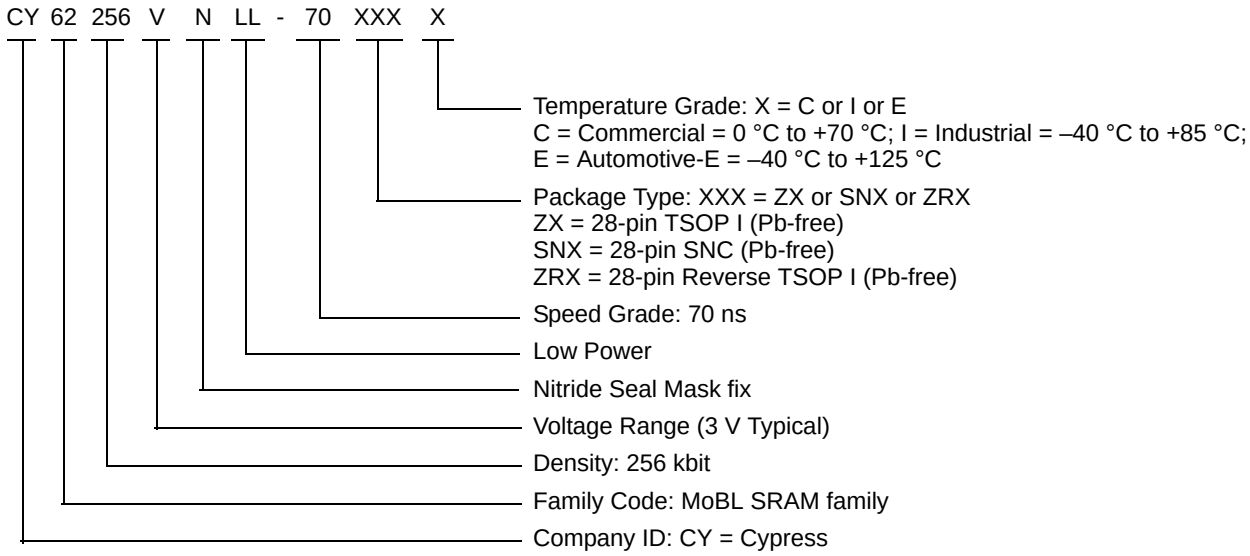

## Truth Table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|
| H | X | X | High Z | Deselect/power-down | Standby ($I_{SB}$) |
| L | H | L | Data out | Read | Active ($I_{CC}$) |
| L | L | X | Data in | Write | Active ($I_{CC}$) |
| L | H | H | High Z | Deselect, output disabled | Active ($I_{CC}$) |

## Ordering Information

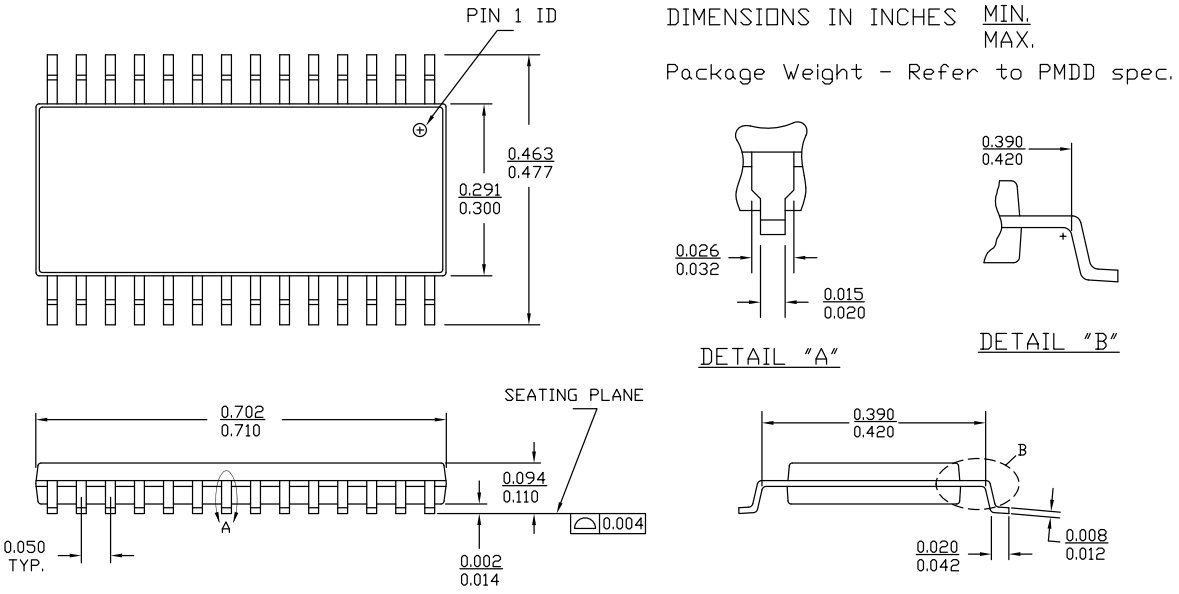
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 70 | CY62256VNLL-70ZXC | 51-85071 | 28-pin TSOP I (Pb-free) | Commercial |
| | CY62256VNLL-70SNXI | 51-85092 | 28-pin SNC (300 Mils) Narrow Body (Pb-free) | Industrial |
| | CY62256VNLL-70ZXI | 51-85071 | 28-pin TSOP I (Pb-free) | |
| | CY62256VNLL-70ZRXI | 51-85074 | 28-pin Reverse TSOP I (Pb-free) | |
| | CY62256VNLL-70SNXE | 51-85092 | 28-pin SNC (300 Mils) Narrow Body (Pb-free) | Automotive-E |
| | CY62256VNLL-70ZXE | 51-85071 | 28-pin TSOP I (Pb-free) | |

### Ordering Code Definitions



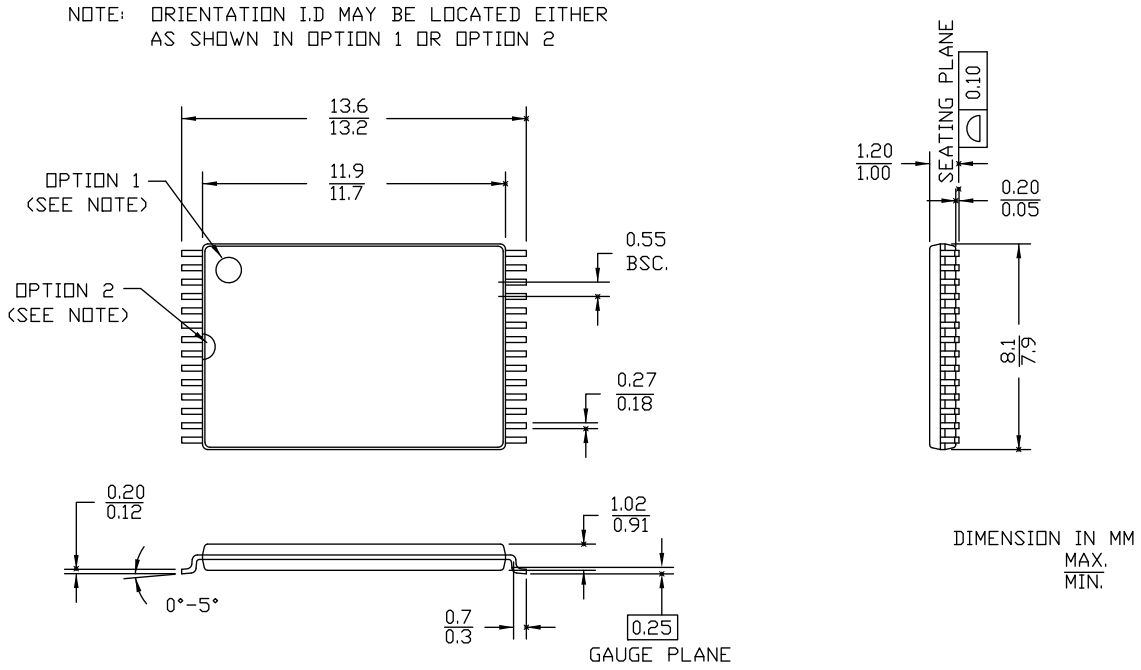
## Package Diagrams

**Figure 9. 28-pin SNC (300 Mils) SN28.3 (Narrow Body) Package Outline, 51-85092**




51-85092 *E

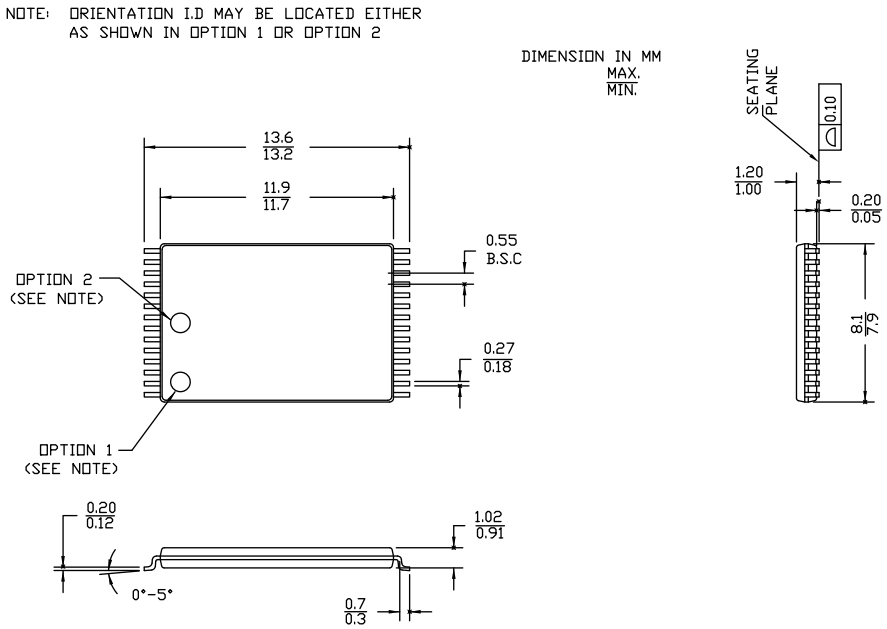
**Figure 10. 28-pin TSOP 1 (8 × 13.4 × 1.2 mm) Z28 (Standard) Package Outline, 51-85071**




51-85071 *J

## Package Diagrams

**Figure 11. 28-pin TSOP I (8 × 13.4 mm) Package Outline - Reverse, 51-85074**




51-85074 *H

## Acronyms

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| VFBGA | Very Fine-Pitch Ball Grid Array |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| µA | microampere |
| mA | milliampere |
| MHz | megahertz |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY62256VN, 256-Kbit (32 K × 8) Static RAM<br>Document Number: 001-06512 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 426504 | NXR | See ECN | New data sheet |
| *A | 488954 | NXR | See ECN | Added Automotive product<br>Updated ordering Information table |
| *B | 2769239 | VKN / AESA | 09/25/09 | Corrected $V_{IL}$ description in the Electrical Characteristics table |
| *C | 2901521 | AJU | 03/30/2010 | Removed inactive parts from Ordering Information.<br>Updated Package Diagram. |
| *D | 3119519 | AJU | 01/04/2011 | Updated Ordering Information.<br>Added Ordering Code Definitions. |
| *E | 3329873 | RAME | 07/27/11 | Updated template and styles according to current Cypress standards.<br>Added acronyms and units.<br>Removed reference to AN1064 SRAM system guidelines.<br>Updated operation recovery time parameter under Data Retention Characteristics on page 6. |
| *F | 4122787 | VINI | 09/13/2013 | Updated Package Diagrams:<br>spec 51-85092 – Changed revision from *C to *E.<br>Updated in new template.<br>Completing Sunset Review. |
| *G | 4525875 | VINI | 10/06/2014 | Updated Maximum Ratings:<br>Referred Note 2 in “Supply voltage to ground potential (pin 28 to pin 14)”.<br>Updated Package Diagrams:<br>spec 51-85071 – Changed revision from *I to *J.<br>spec 51-85074 – Changed revision from *G to *H.<br>Completing Sunset Review. |
| *H | 4576406 | VINI | 01/16/2015 | Added related documentation hyperlink in page 1.<br>Added Note 13 in Switching Characteristics.<br>Added note reference 13 in the Switching Characteristics table. |

## Sales, Solutions, and Legal Information

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| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc |
| Memory | cypress.com/go/memory |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

### PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

### Cypress Developer Community

Community | Forums | Blogs | Video | Training

### Technical Support

cypress.com/go/support