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## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage to ground potential ..... -0.3 V to 3.9 V

DC voltage applied to outputs in High Z State <sup>[3, 4]</sup> ..... -0.3 V to 3.9 V

DC input voltage <sup>[3, 4]</sup> ..... -0.3 V to 3.9 V

Output current into outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

| Product       | Range                     | Ambient Temperature | V <sub>CC</sub> <sup>[5]</sup> |
|---------------|---------------------------|---------------------|--------------------------------|
| CY62138FV30LL | Industrial / Automotive-A | -40 °C to +85 °C    | 2.2 V to 3.6 V                 |

## Electrical Characteristics

Over the Operating Range

| Parameter                       | Description                                 | Test Conditions                                                                                                                                                                                                                      | 45 ns (Industrial / Automotive-A) |                    |                         | Unit |
|---------------------------------|---------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|--------------------|-------------------------|------|
|                                 |                                             |                                                                                                                                                                                                                                      | Min                               | Typ <sup>[6]</sup> | Max                     |      |
| V <sub>OH</sub>                 | Output HIGH voltage                         | I <sub>OH</sub> = -0.1 mA                                                                                                                                                                                                            | 2.0                               | —                  | —                       | V    |
|                                 |                                             | I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> ≥ 2.70 V                                                                                                                                                                                  | 2.4                               | —                  | —                       | V    |
| V <sub>OL</sub>                 | Output LOW voltage                          | I <sub>OL</sub> = 0.1 mA                                                                                                                                                                                                             | —                                 | —                  | 0.4                     | V    |
|                                 |                                             | I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> ≥ 2.70 V                                                                                                                                                                                   | —                                 | —                  | 0.4                     | V    |
| V <sub>IH</sub>                 | Input HIGH voltage                          | V <sub>CC</sub> = 2.2 V to 2.7 V                                                                                                                                                                                                     | 1.8                               | —                  | V <sub>CC</sub> + 0.3 V | V    |
|                                 |                                             | V <sub>CC</sub> = 2.7 V to 3.6 V                                                                                                                                                                                                     | 2.2                               | —                  | V <sub>CC</sub> + 0.3 V | V    |
| V <sub>IL</sub>                 | Input LOW voltage                           | V <sub>CC</sub> = 2.2 V to 2.7 V For BGA package                                                                                                                                                                                     | -0.3                              | —                  | 0.6                     | V    |
|                                 |                                             | V <sub>CC</sub> = 2.7 V to 3.6 V                                                                                                                                                                                                     | -0.3                              | —                  | 0.8                     | V    |
|                                 |                                             | V <sub>CC</sub> = 2.2 V to 3.6 V For other packages                                                                                                                                                                                  | -0.3                              | —                  | 0.6                     | V    |
| I <sub>IX</sub>                 | Input leakage current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                                                                                                                                                                               | -1                                | —                  | +1                      | μA   |
| I <sub>OZ</sub>                 | Output leakage current                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , output disabled                                                                                                                                                                             | -1                                | —                  | +1                      | μA   |
| I <sub>CC</sub>                 | V <sub>CC</sub> Operating supply current    | f = f <sub>max</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = V <sub>CCmax</sub> , I <sub>OUT</sub> = 0 mA, CMOS levels                                                                                                                 | —                                 | 13                 | 18                      | mA   |
|                                 |                                             | f = 1 MHz                                                                                                                                                                                                                            | —                                 | 1.6                | 2.5                     |      |
| I <sub>SB1</sub> <sup>[7]</sup> | Automatic CE Power-down current—CMOS inputs | CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2 V or CE <sub>2</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≤ 0.2 V, f = f <sub>max</sub> (address and data only), f = 0 (OE, and WE), V <sub>CC</sub> = 3.60 V | —                                 | 1                  | 5                       | μA   |
| I <sub>SB2</sub> <sup>[7]</sup> | Automatic CE Power-down current—CMOS inputs | CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2 V or CE <sub>2</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0, V <sub>CC</sub> = 3.60 V                                                          | —                                 | 1                  | 5                       | μA   |

### Notes

- V<sub>IL(min)</sub> = -2.0 V for pulse durations less than 20 ns.
- V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
- Chip enables (CE<sub>1</sub> and CE<sub>2</sub>) must be at CMOS level to meet the I<sub>SB1</sub> / I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

## Capacitance

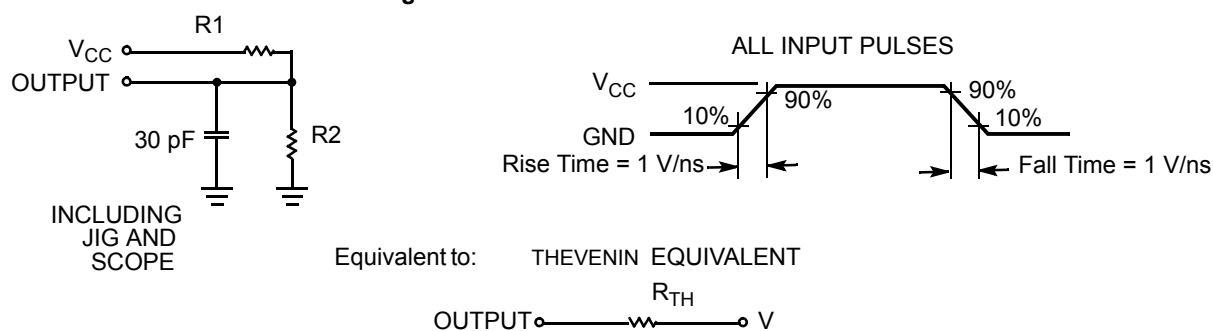
| Parameter <sup>[8]</sup> | Description        | Test Conditions                                                            | Max | Unit |
|--------------------------|--------------------|----------------------------------------------------------------------------|-----|------|
| C <sub>IN</sub>          | Input Capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ.)</sub> | 10  | pF   |
| C <sub>OUT</sub>         | Output Capacitance |                                                                            | 10  | pF   |

## Thermal Resistance

| Parameter <sup>[8]</sup> | Description                              | Test Conditions                                                        | 32-pin SOIC | 36-ball VFBGA | 32-pin TSOP II | 32-pin STSOP | 32-pin TSOP I | Unit |
|--------------------------|------------------------------------------|------------------------------------------------------------------------|-------------|---------------|----------------|--------------|---------------|------|
| Θ <sub>JA</sub>          | Thermal resistance (Junction to Ambient) | Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board | 44.53       | 38.49         | 44.16          | 59.72        | 50.19         | °C/W |
| Θ <sub>JC</sub>          | Thermal resistance (Junction to Case)    |                                                                        | 24.05       | 17.66         | 11.97          | 15.38        | 14.59         | °C/W |

## AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms



| Parameter       | 2.5 V (2.2 V to 2.7 V) | 3.0 V (2.7 V to 3.6 V) | Unit |
|-----------------|------------------------|------------------------|------|
| R1              | 16667                  | 1103                   | Ω    |
| R2              | 15385                  | 1554                   | Ω    |
| R <sub>TH</sub> | 8000                   | 645                    | Ω    |
| V <sub>TH</sub> | 1.20                   | 1.75                   | V    |

### Note

8. Tested initially and after any design or process changes that may affect these parameters.

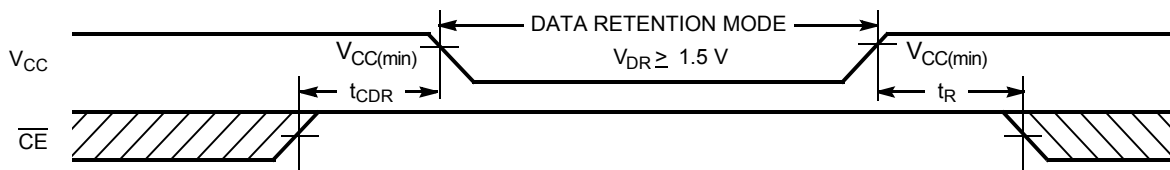
## Data Retention Characteristics

Over the Operating Range

| Parameter         | Description                          | Conditions                                                                                                                                                                   | Min | Typ <sup>[9]</sup> | Max | Unit          |
|-------------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------------|-----|---------------|
| $V_{DR}$          | $V_{CC}$ for data retention          |                                                                                                                                                                              | 1.5 | –                  | –   | V             |
| $I_{CCDR}^{[10]}$ | Data retention current               | $V_{CC} = 1.5\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$<br>or $CE_2 \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$<br>or $V_{IN} \leq 0.2\text{ V}$ | –   | 1                  | 4   | $\mu\text{A}$ |
| $t_{CDR}^{[11]}$  | Chip deselect to data retention time |                                                                                                                                                                              | 0   | –                  | –   | ns            |
| $t_R^{[12]}$      | Operation recovery time              |                                                                                                                                                                              | 45  | –                  | –   | ns            |

## Data Retention Waveform

Figure 6. Data Retention Waveform <sup>[13]</sup>



### Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ.)}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
10. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be at CMOS level to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
13.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

## Switching Characteristics

Over the Operating Range

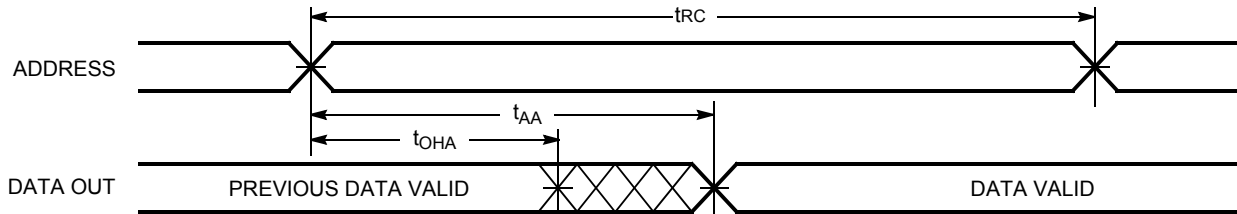
| Parameter <sup>[14, 15]</sup>   | Description                                                                 | 45 ns (Industrial/<br>Automotive-A) |     | Unit |
|---------------------------------|-----------------------------------------------------------------------------|-------------------------------------|-----|------|
|                                 |                                                                             | Min                                 | Max |      |
| Read Cycle                      |                                                                             |                                     |     |      |
| t <sub>RC</sub>                 | Read cycle time                                                             | 45                                  | –   | ns   |
| t <sub>AA</sub>                 | Address to data valid                                                       | –                                   | 45  | ns   |
| t <sub>OHA</sub>                | Data hold from address change                                               | 10                                  | –   | ns   |
| t <sub>ACE</sub>                | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to data valid                | –                                   | 45  | ns   |
| t <sub>DOE</sub>                | $\overline{OE}$ LOW to data valid                                           | –                                   | 22  | ns   |
| t <sub>LZOE</sub>               | $\overline{OE}$ LOW to Low Z <sup>[16]</sup>                                | 5                                   | –   | ns   |
| t <sub>HZOE</sub>               | $\overline{OE}$ HIGH to High Z <sup>[16, 17]</sup>                          | –                                   | 18  | ns   |
| t <sub>LZCE</sub>               | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low Z <sup>[16]</sup>     | 10                                  | –   | ns   |
| t <sub>HZCE</sub>               | $\overline{CE}_1$ HIGH or CE <sub>2</sub> LOW to High Z <sup>[16, 17]</sup> | –                                   | 18  | ns   |
| t <sub>PU</sub>                 | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Power-up                  | 0                                   | –   | ns   |
| t <sub>PD</sub>                 | $\overline{CE}_1$ HIGH or CE <sub>2</sub> LOW to Power-down                 | –                                   | 45  | ns   |
| Write Cycle <sup>[18, 19]</sup> |                                                                             |                                     |     |      |
| t <sub>WC</sub>                 | Write cycle time                                                            | 45                                  | –   | ns   |
| t <sub>SCE</sub>                | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to write end                 | 35                                  | –   | ns   |
| t <sub>AW</sub>                 | Address setup to write end                                                  | 35                                  | –   | ns   |
| t <sub>HA</sub>                 | Address hold from write end                                                 | 0                                   | –   | ns   |
| t <sub>SA</sub>                 | Address setup to Write Start                                                | 0                                   | –   | ns   |
| t <sub>PWE</sub>                | $\overline{WE}$ pulse Width                                                 | 35                                  | –   | ns   |
| t <sub>SD</sub>                 | Data setup to write end                                                     | 25                                  | –   | ns   |
| t <sub>HD</sub>                 | Data hold from write end                                                    | 0                                   | –   | ns   |
| t <sub>HZWE</sub>               | $\overline{WE}$ LOW to High Z <sup>[16, 17]</sup>                           | –                                   | 18  | ns   |
| t <sub>LZWE</sub>               | $\overline{WE}$ HIGH to Low Z <sup>[16]</sup>                               | 10                                  | –   | ns   |

### Notes

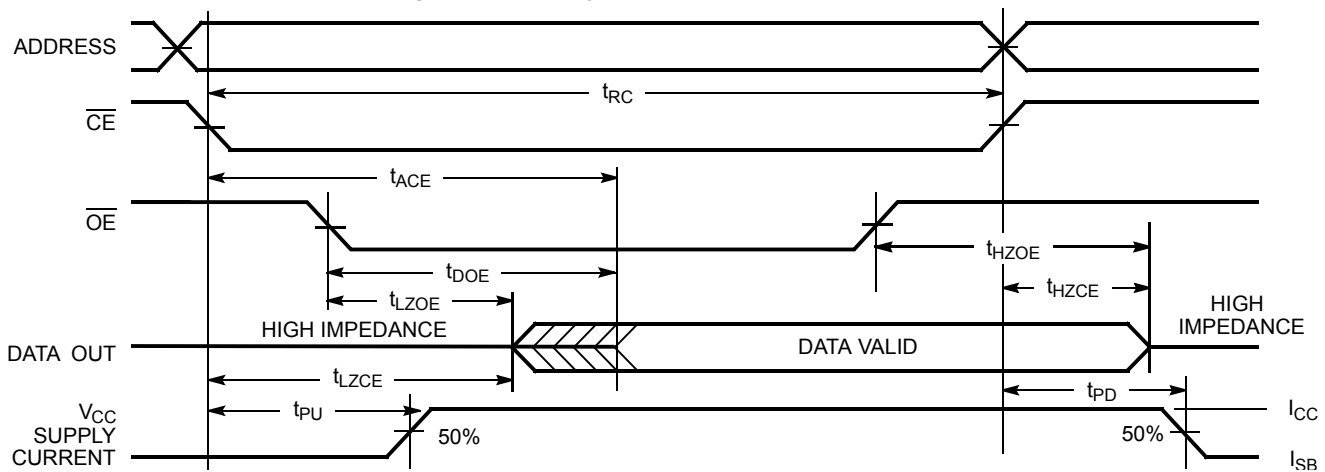
14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tristate parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [AC Test Loads and Waveforms on page 5](#).
16. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
17.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the output enters a high impedance state.
18. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $CE_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.
19. The minimum write pulse width for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

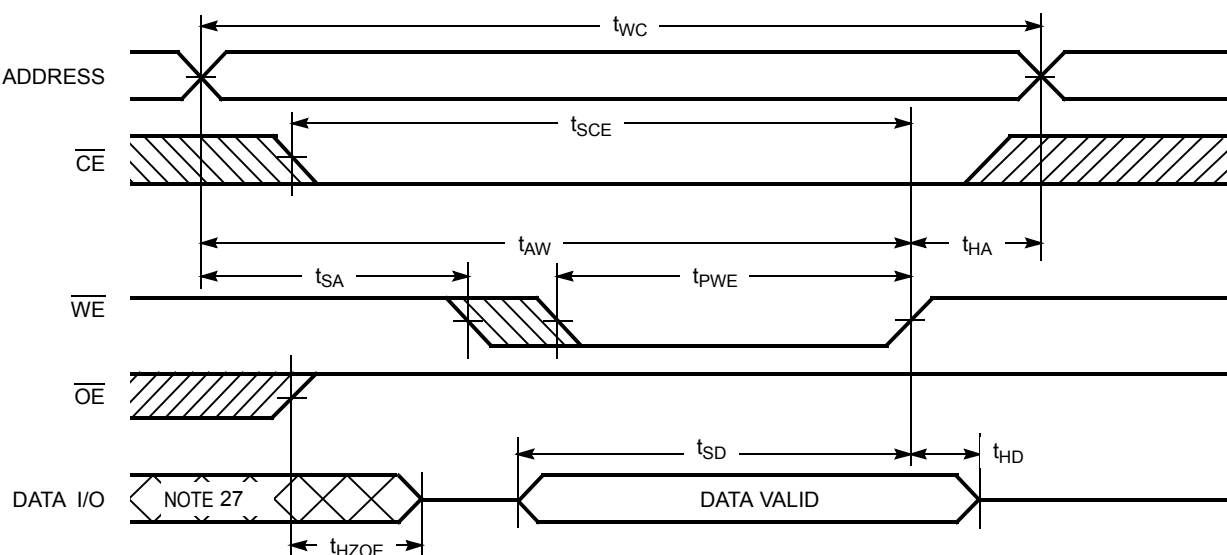
**Figure 7. Read Cycle 1 (Address Transition Controlled)** [20, 21]



**Figure 8. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** [21, 22, 23]



**Figure 9. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)** [23, 24, 25, 26]



### Notes

20. The device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}_1 = V_{IL}$ ,  $\text{CE}_2 = V_{IH}$ .

21. WE is HIGH for read cycle.

22. Address valid before or similar to  $\overline{\text{CE}}_1$  transition LOW and  $\text{CE}_2$  transition HIGH.

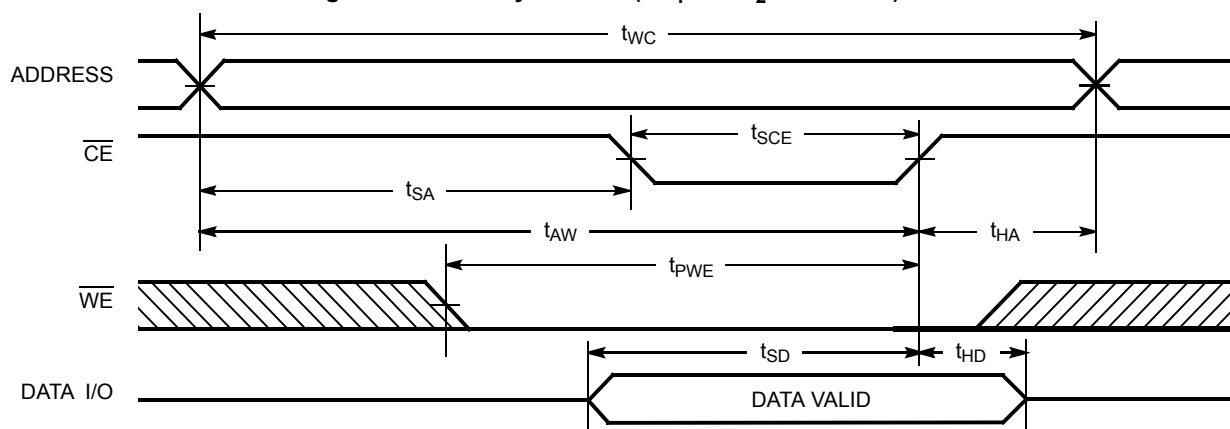
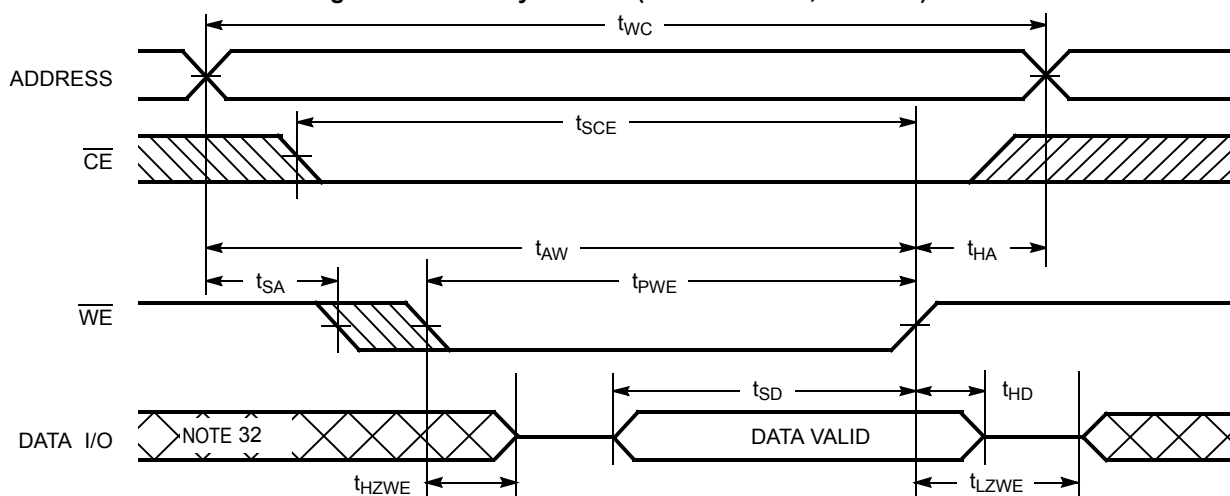
23. CE is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.

24. The internal write time of the memory is defined by the overlap of WE,  $\overline{\text{CE}}_1 = V_{IL}$ , and  $\text{CE}_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.

25. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .

26. If  $\overline{\text{CE}}_1$  goes HIGH or  $\text{CE}_2$  goes LOW simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in high impedance state.

27. During this period, the I/Os are in output state. Do not apply input signals.

**Switching Waveforms (continued)**
**Figure 10. Write Cycle No. 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled) [28, 29, 30, 31]**

**Figure 11. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [28, 31, 33]**

**Notes**

28.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
29. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.
30. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
31. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
32. During this period, the I/Os are in output state. Do not apply input signals.
33. The minimum write pulse width for Write Cycle No. 2 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Truth Table

| $\overline{CE}_1$ | $CE_2$            | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs | Mode                | Power                |
|-------------------|-------------------|-----------------|-----------------|----------------|---------------------|----------------------|
| H                 | X <sup>[34]</sup> | X               | X               | High Z         | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| X <sup>[34]</sup> | L                 | X               | X               | High Z         | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| L                 | H                 | H               | L               | Data out       | Read                | Active ( $I_{CC}$ )  |
| L                 | H                 | H               | H               | High Z         | Output disabled     | Active ( $I_{CC}$ )  |
| L                 | H                 | L               | X               | Data in        | Write               | Active ( $I_{CC}$ )  |

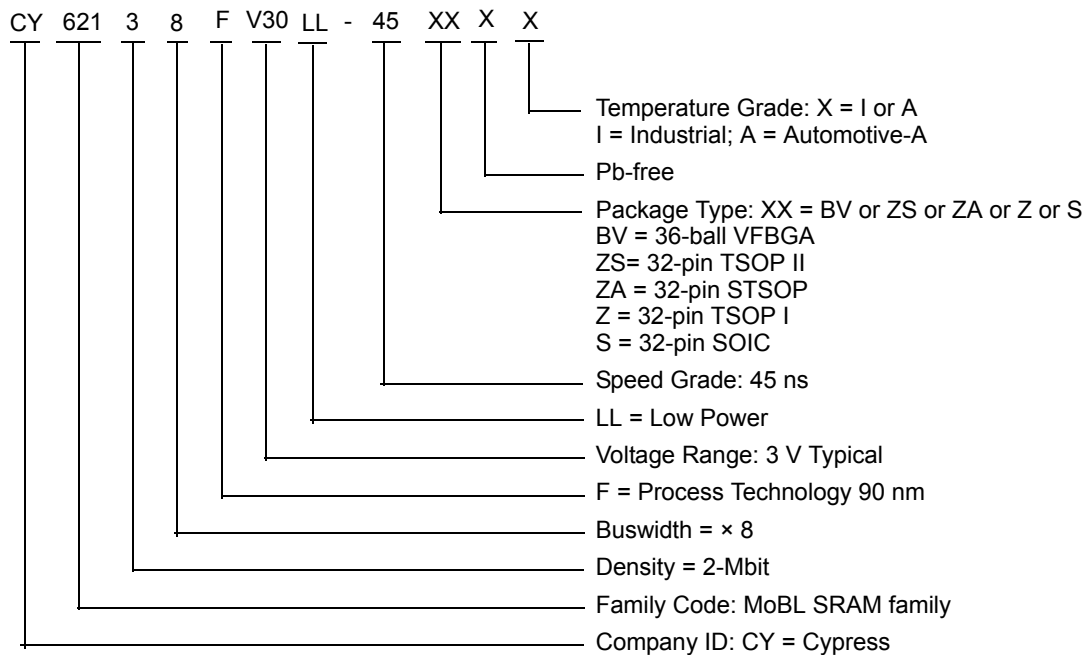
### Note

34. The 'X' (Don't care) state for the Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

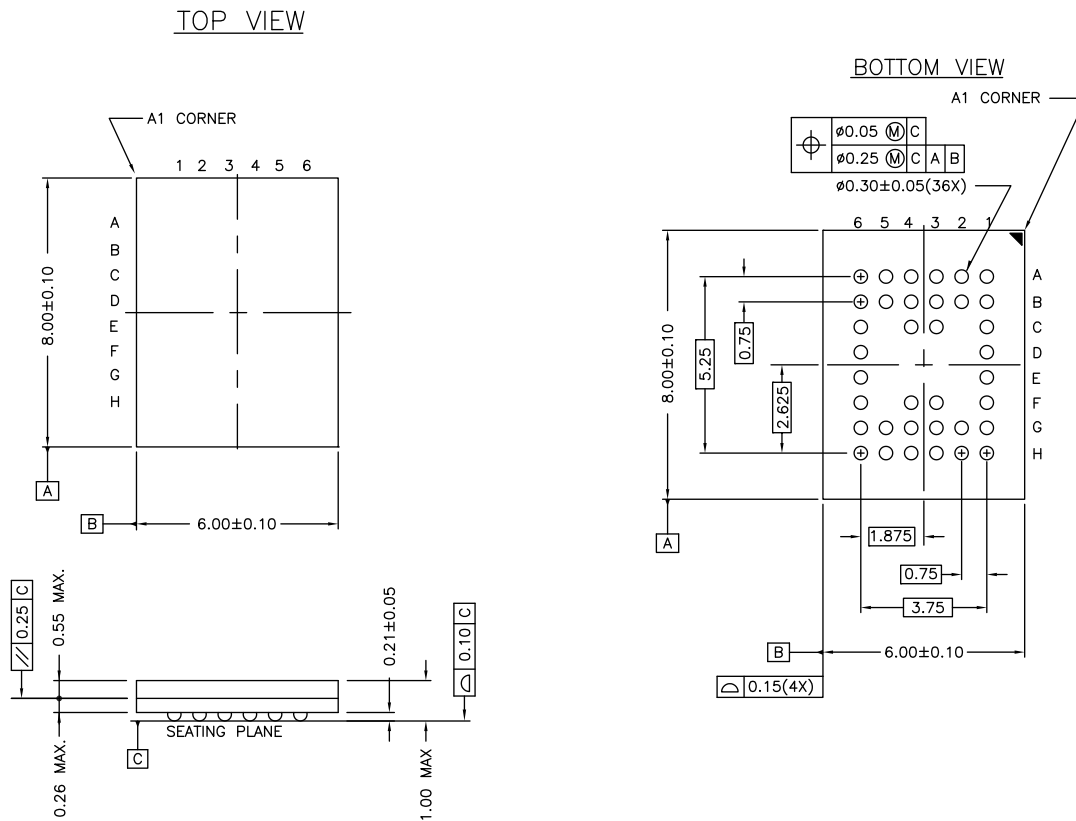
| Speed (ns) | Ordering Code        | Package Diagram | Package Type            | Operating Range |
|------------|----------------------|-----------------|-------------------------|-----------------|
| 45         | CY62138FV30LL-45BVXI | 51-85149        | 36-ball VFBGA (Pb-free) | Industrial      |
|            | CY62138FV30LL-45ZAXI | 51-85094        | 32-pin STSOP (Pb-free)  |                 |
|            | CY62138FV30LL-45ZXI  | 51-85056        | 32-pin TSOP I (Pb-free) |                 |
|            | CY62138FV30LL-45SXI  | 51-85081        | 32-pin SOIC (Pb-free)   |                 |
|            | CY62138FV30LL-45ZAXA | 51-85094        | 32-pin STSOP (Pb-free)  | Automotive-A    |

## Ordering Code Definitions



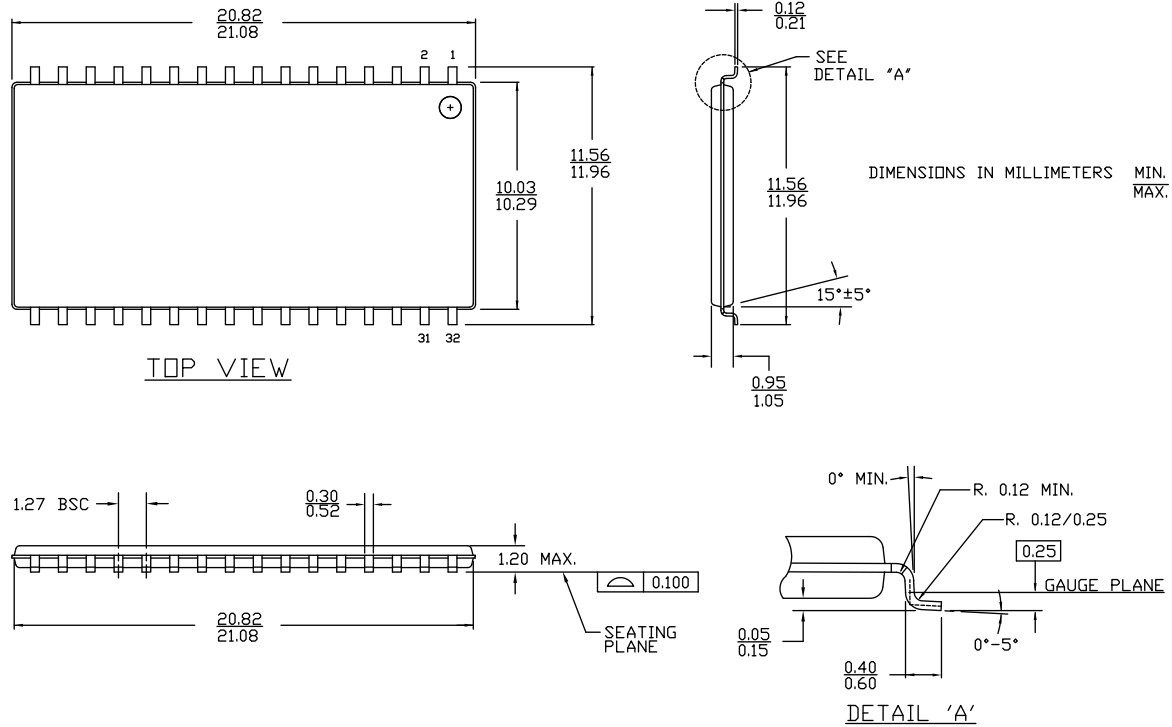
## Package Diagrams

Figure 12. 36-ball VFBGA (6 × 8 × 1.0 mm) BV36A Package Outline, 51-85149



**Package Diagrams** (continued)

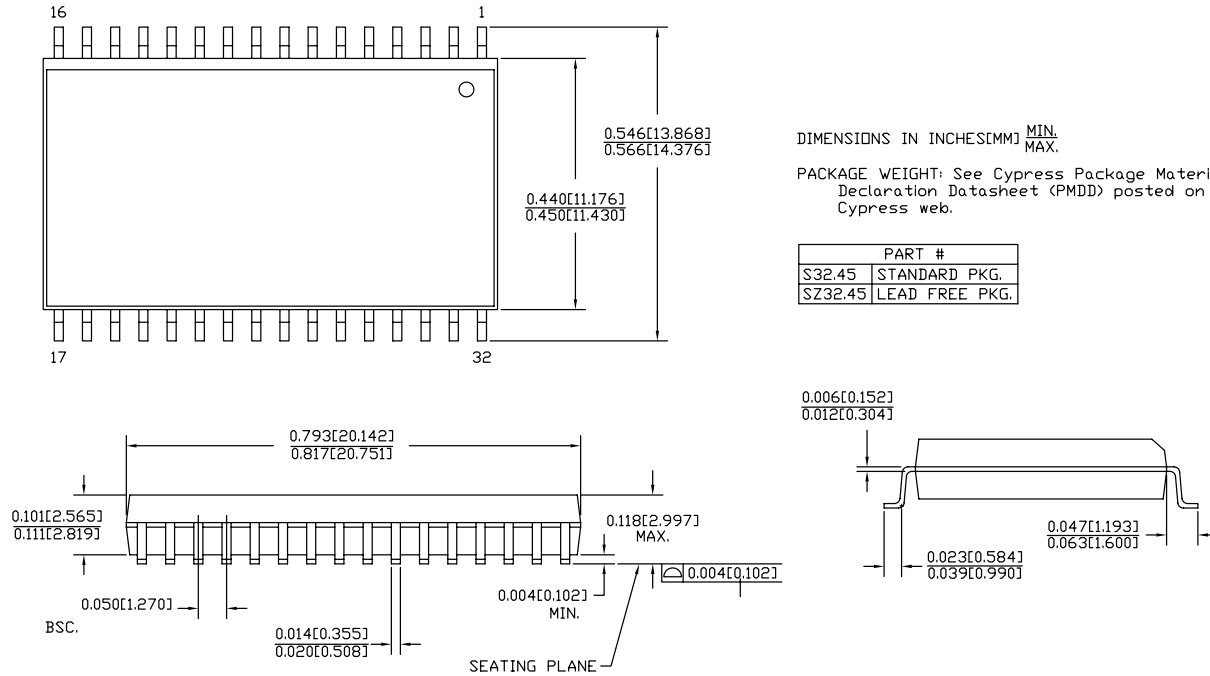
**Figure 13. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095**



51-85095 \*B

**Package Diagrams** (continued)

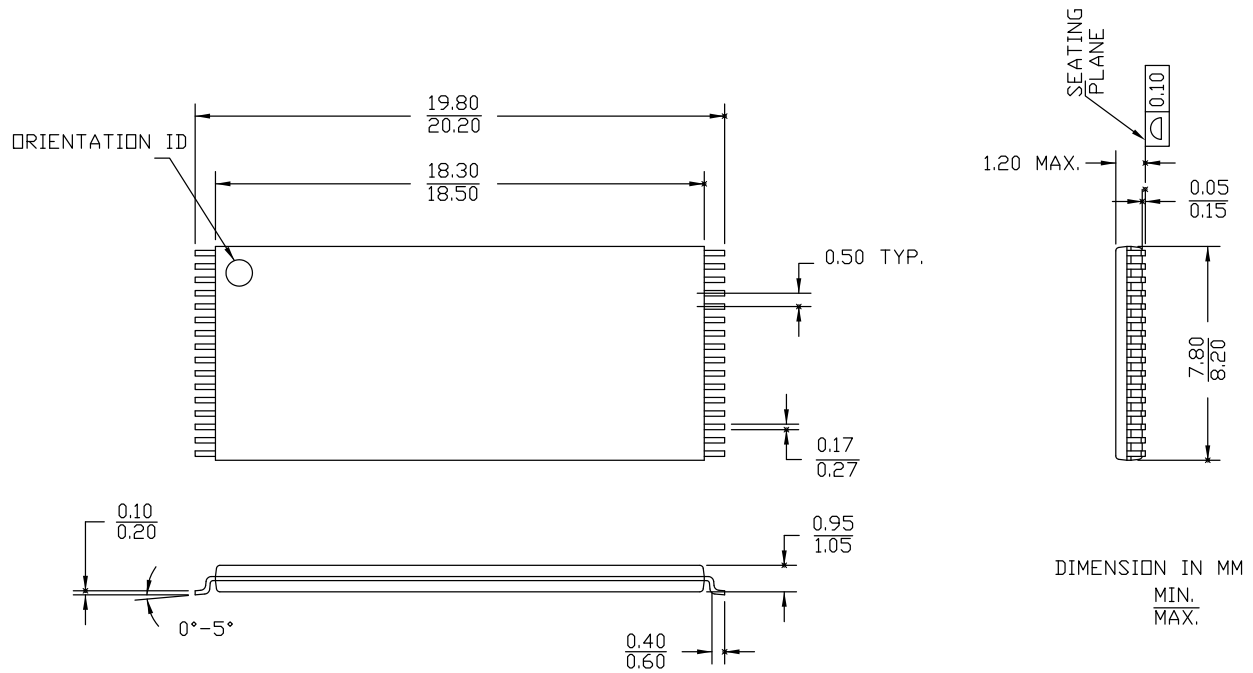
**Figure 14. 32-pin Molded SOIC (450 Mil) S32.45/SZ32.45 Package Outline, 51-85081**



51-85081 \*E

**Package Diagrams** (continued)

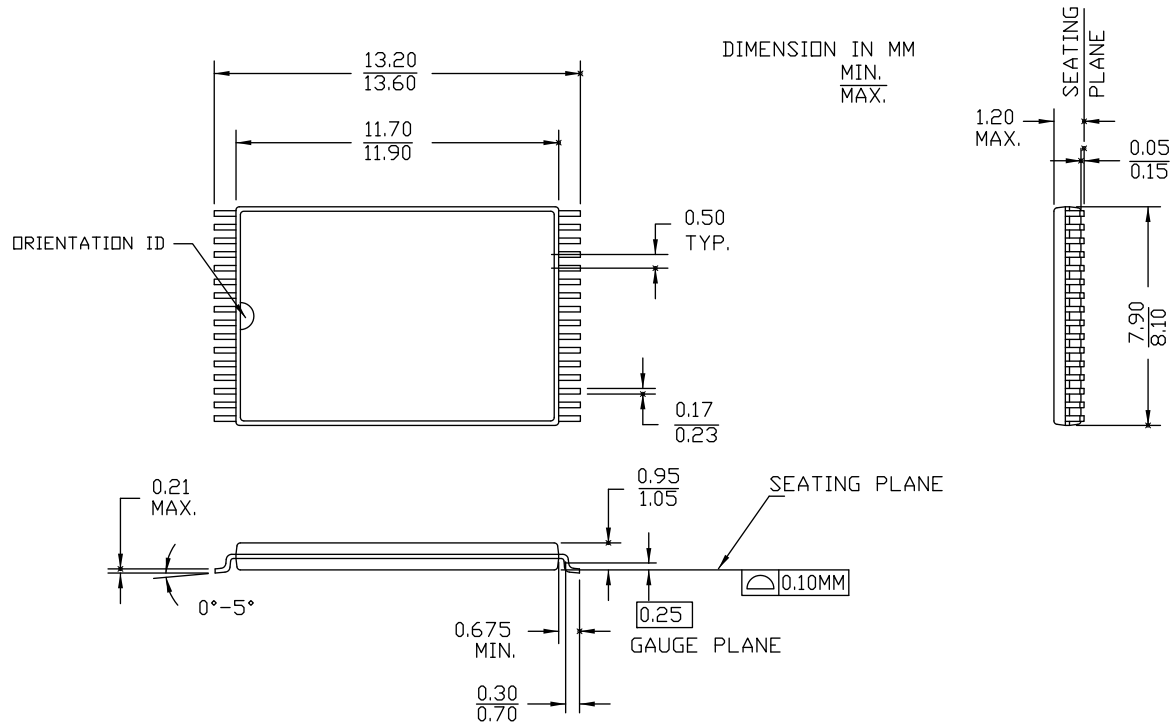
**Figure 15. 32-pin TSOP I (8 × 20 × 1.0 mm) Z32R Package Outline, 51-85056**



51-85056 \*G

**Package Diagrams** (continued)

**Figure 16. 32-pin STSOP (8 × 13.4 × 1.2 mm) ZA32 Package Outline, 51-85094**



51-85094 \*G

## Acronyms

| Acronym | Description                             |
|---------|-----------------------------------------|
| BGA     | Ball Grid Array                         |
| CMOS    | Complementary Metal Oxide Semiconductor |
| I/O     | Input/Output                            |
| OE      | Output Enable                           |
| SOIC    | Small-Outline Integrated Circuit        |
| SRAM    | Static Random Access Memory             |
| STSOP   | Small Thin Small Outline Package        |
| TSOP    | Thin Small Outline Package              |
| VFBGA   | Very Fine-Pitch Ball Grid Array         |
| WE      | Write Enable                            |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| μA     | microampere     |
| μs     | microsecond     |
| mA     | milliampere     |
| mm     | millimeter      |
| ns     | nanosecond      |
| Ω      | ohm             |
| %      | percent         |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

## Document History Page

| Document Title: CY62138FV30 MoBL®, 2-Mbit (256 K × 8) Static RAM<br>Document Number: 001-08029 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                           | ECN No. | Submission Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| **                                                                                             | 463660  | See ECN         | NXR             | New data sheet.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| *A                                                                                             | 467351  | See ECN         | NXR             | Added 32-pin TSOP II package, 32 pin TSOP I and 32 pin STSOP packages<br>Changed ball A3 from NC to CE <sub>2</sub> in 36-ball FBGA pin out                                                                                                                                                                                                                                                                                                                                                                                                    |
| *B                                                                                             | 566724  | See ECN         | NXR             | Converted from Preliminary to Final<br>Corrected typo in 32 pin TSOP II pin configuration diagram on page #2 (changed pin 24 from CE <sub>1</sub> to OE and pin 22 from CE to CE <sub>1</sub> )<br>Changed the I <sub>CC(max)</sub> value from 2.25 mA to 2.5 mA for test condition f=1 MHz<br>Changed the I <sub>SB2(typ)</sub> value from 0.5 μA to 1 μA<br>Changed the I <sub>SB2(max)</sub> value from 2.5 μA to 5 μA<br>Changed the I <sub>CCDR(typ)</sub> value from 0.5 μA to 1 μA and I <sub>CCDR(max)</sub> value from 2.5 μA to 4 μA |
| *C                                                                                             | 797956  | See ECN         | VKN             | Added 32-pin SOIC package<br>Updated VIL spec for SOIC, TSOP-II, TSOP-I, and STSOP packages on Electrical characteristics table                                                                                                                                                                                                                                                                                                                                                                                                                |
| *D                                                                                             | 809101  | See ECN         | VKN             | Corrected typo in the Ordering Information table                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| *E                                                                                             | 940341  | See ECN         | VKN             | Added footnote #7 related to I <sub>SB2</sub> and I <sub>CCDR</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| *F                                                                                             | 2769239 | 09/25/09        | VKN / AESA      | Included Automotive-A information                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| *G                                                                                             | 3055119 | 10/12/2010      | RAME            | Updated and converted all tablenotes into Footnote<br>Added <a href="#">Ordering Code Definitions</a> .<br>Updated All <a href="#">Package Diagrams</a> .<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> table<br>Updated data sheet as per new template.                                                                                                                                                                                                                                                              |
| *H                                                                                             | 3061313 | 10/15/2010      | RAME            | Minor changes: Corrected "IO" to "I/O"                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| *I                                                                                             | 3078557 | 11/04/2010      | RAME            | Corrected 55 C to -55C in Ambient Temperature with Power applied in Maximum Ratings Section                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| *J                                                                                             | 3235744 | 04/20/2011      | RAME            | Removed the note "For best practice recommendations, refer to the Cypress application Note "System Design Guidelines" at <a href="http://www.cypress.com">http://www.cypress.com</a> " in page 1 and its reference in <a href="#">Functional Description</a> .<br>Updated <a href="#">Package Diagrams</a> .                                                                                                                                                                                                                                   |
| *K                                                                                             | 3285093 | 06/16/2011      | RAME            | Updated in new template.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| *L                                                                                             | 3845087 | 12/18/2012      | TAVA            | Updated <a href="#">Ordering Information</a> (Updated part numbers).<br>Updated <a href="#">Package Diagrams</a> :<br>spec 51-85149 – Changed revision from *D to *E.<br>spec 51-85081 – Changed revision from *C to *E.                                                                                                                                                                                                                                                                                                                       |
| *M                                                                                             | 4099045 | 08/19/2013      | VINI            | Updated <a href="#">Switching Characteristics</a> :<br>Added Note 14 and referred the same note in "Parameter" column.<br><br>Updated in new template.                                                                                                                                                                                                                                                                                                                                                                                         |

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|------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                           | ECN No. | Submission Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                             |
| *N                                                                                             | 4377056 | 05/12/2014      | MEMJ            | <p>Updated <a href="#">Switching Characteristics</a>:<br/>Added Note 19 and referred the same note in "Write Cycle".</p> <p>Updated <a href="#">Switching Waveforms</a>:<br/>Added Note 33 and referred the same note in <a href="#">Figure 11</a>.</p> <p>Updated <a href="#">Package Diagrams</a>:<br/>spec 51-85056 – Changed revision from *F to *G.<br/>spec 51-85094 – Changed revision from *F to *G.</p> <p>Completing Sunset Review.</p> |

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