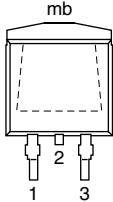
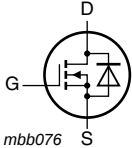


2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

3. Ordering information

Table 3. Ordering information

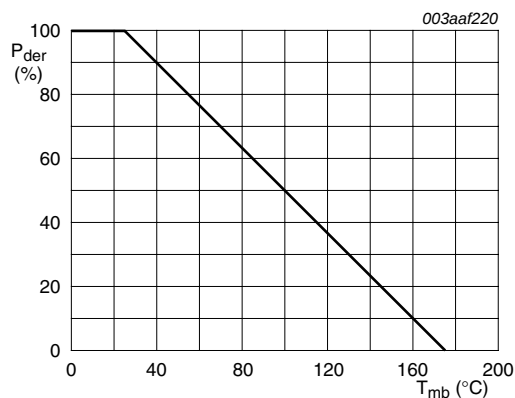
Type number	Package		
	Name	Description	Version
BUK9628-100A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

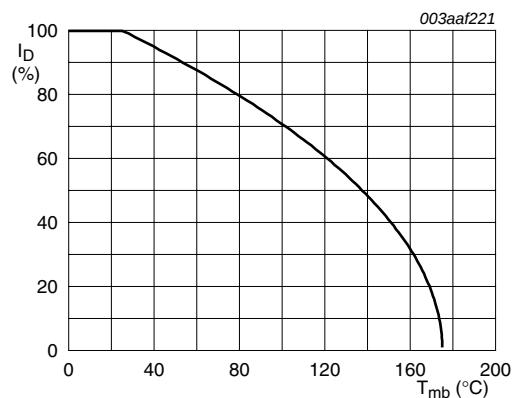
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-10	10	V
I_D	drain current	$T_{mb} = 25\text{ °C}$	-	49	A
		$T_{mb} = 100\text{ °C}$	-	34	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed	-	195	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	166	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
V_{GSM}	peak gate-source voltage	pulsed; $t_p \leq 50\text{ }\mu\text{s}$	-15	15	V
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	49	A
I_{SM}	peak source current	pulsed; $T_{mb} = 25\text{ °C}$	-	195	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 30\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	45	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

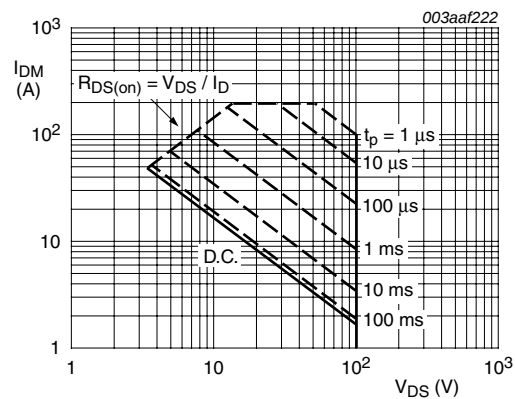
Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

$V_{GS} \geq 5\text{ V}$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25\text{ }^{\circ}\text{C}$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

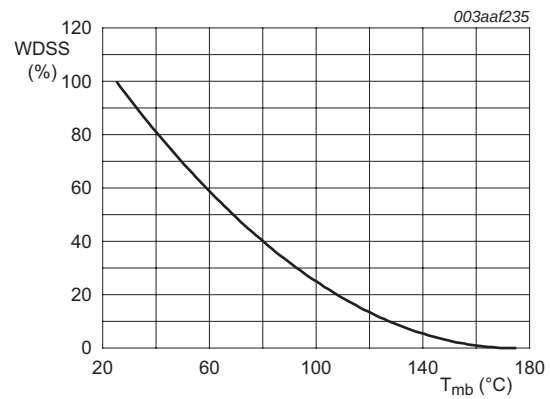
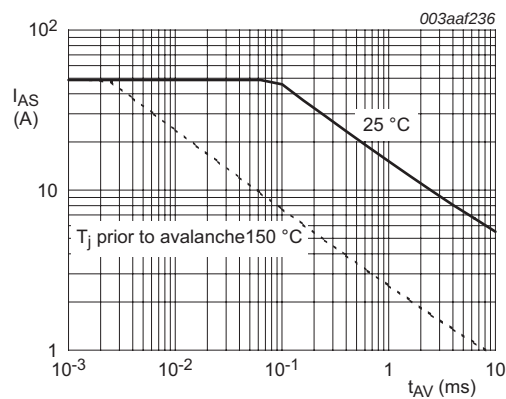


Fig 4. Normalised drain-source non-repetitive avalanche energy as a function of mounting-base temperature



unclamped inductive load

Fig 5. Single-shot avalanche rating; avalanche current as a function of avalanche period

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; FR4 board	-	50	-	K/W

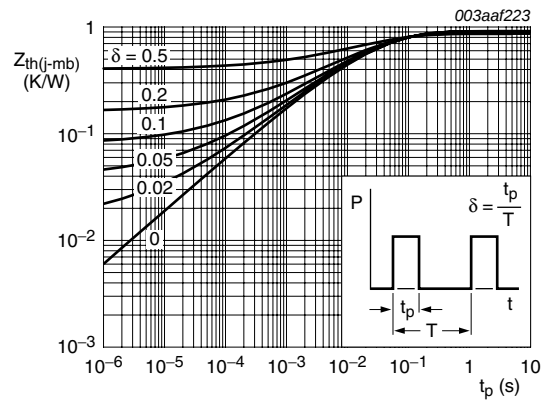


Fig 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C	100	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C	89	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C	1	1.5	2	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C	0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C	-	-	2.3	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	10	µA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	µA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C	-	18.5	28	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C	-	-	70	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C	-	17	27	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C	-	18.8	31	mΩ
Dynamic characteristics						
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C	-	3220	4293	pF
C _{oss}	output capacitance		-	315	378	pF
C _{rss}	reverse transfer capacitance		-	187	256	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 5 V; R _{G(ext)} = 10 Ω; T _j = 25 °C	-	11	16	ns
t _r	rise time		-	58	87	ns
t _{d(off)}	turn-off delay time		-	250	350	ns
t _f	fall time		-	106	148	ns
L _D	internal drain inductance	measured from drain lead 6 mm from package to centre of die ; T _j = 25 °C	-	4.5	-	nH
		measured from upper edge of drain tab to centre of die ; T _j = 25 °C	-	2.5	-	nH
L _S	internal source inductance	measured from source lead to source bond pad ; T _j = 25 °C	-	7.5	-	nH
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C	-	0.85	1.2	V
		I _S = 49 A; V _{GS} = 0 V; T _j = 25 °C	-	1.1	-	V
t _{rr}	reverse recovery time	I _S = 49 A; dI _S /dt = -100 A/µs; V _{GS} = -10 V; V _{DS} = 30 V; T _j = 25 °C	-	63	-	ns
Q _r	recovered charge		-	0.22	-	µC

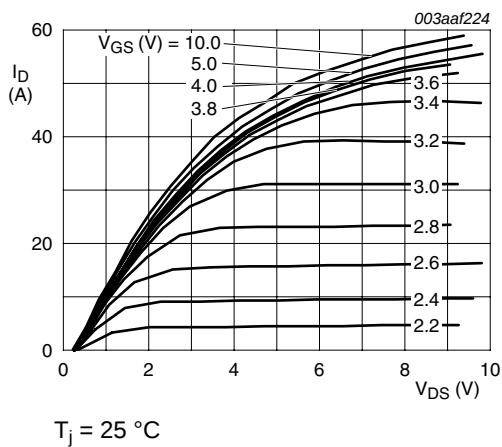


Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values

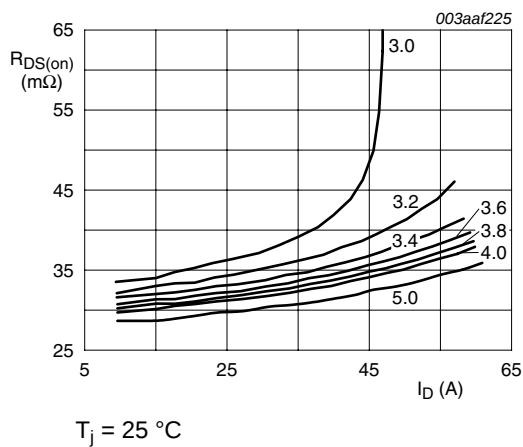


Fig 8. Drain-source on-state resistance as a function of drain current; typical values

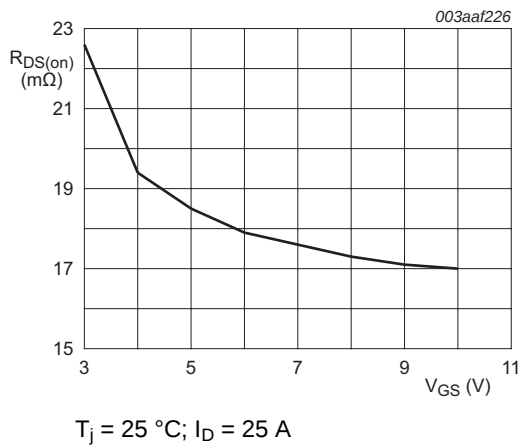


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

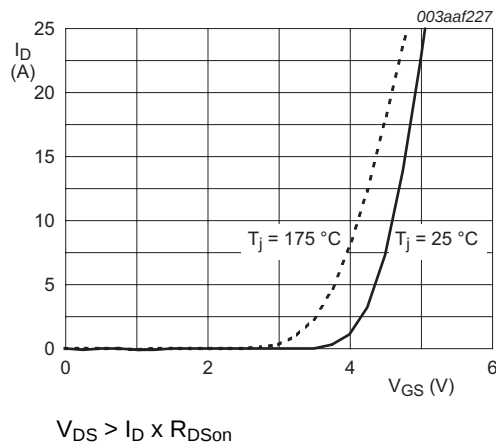


Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

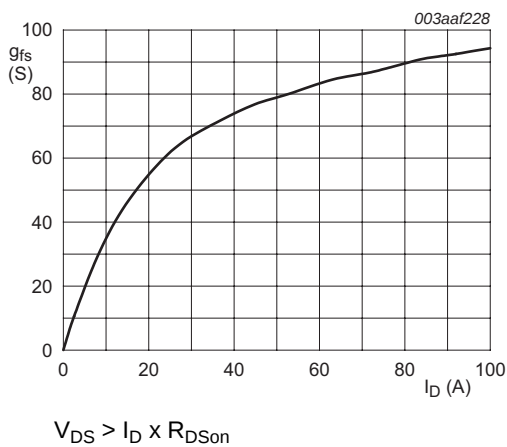


Fig 11. Forward transconductance as a function of drain current; typical values

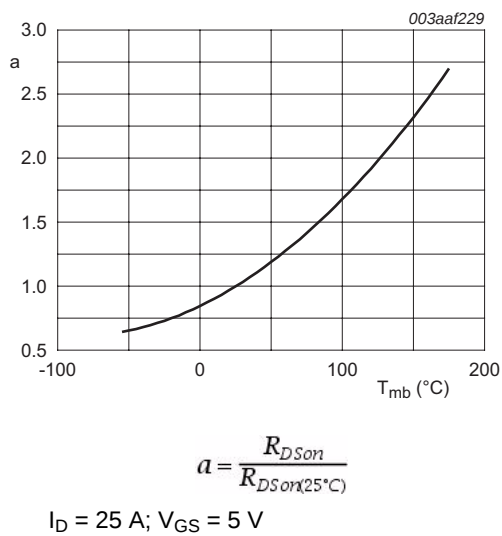


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

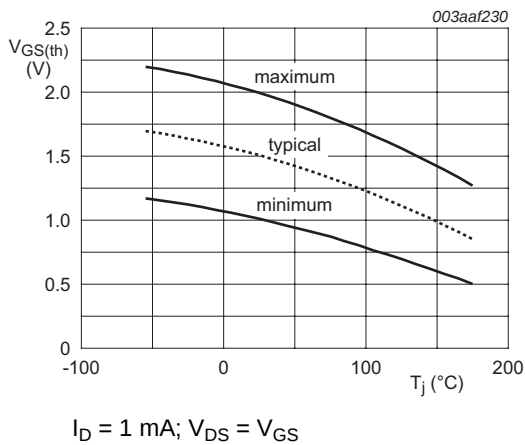


Fig 13. Gate-source threshold voltage as a function of junction temperature

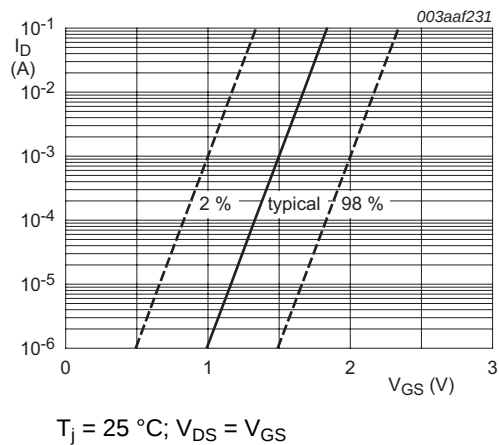


Fig 14. Sub-threshold drain current as a function of gate-source voltage

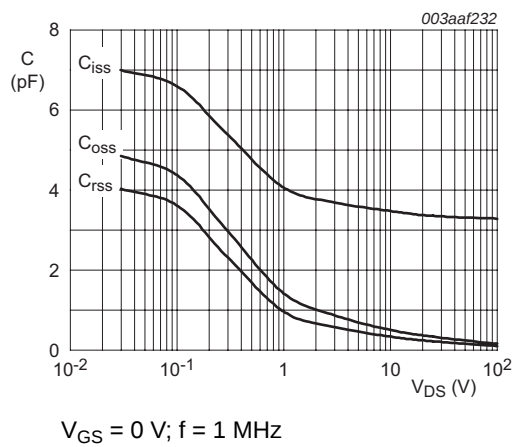


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

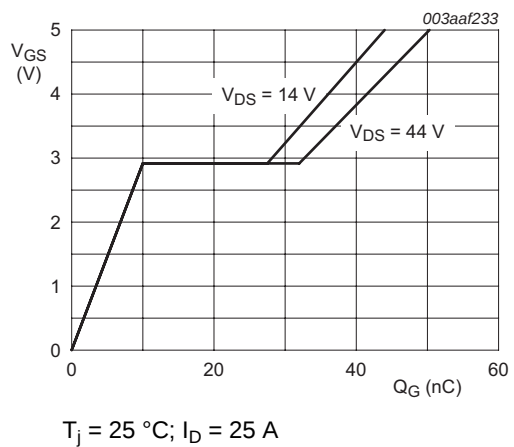


Fig 16. Gate-source voltage as a function of gate charge; typical values

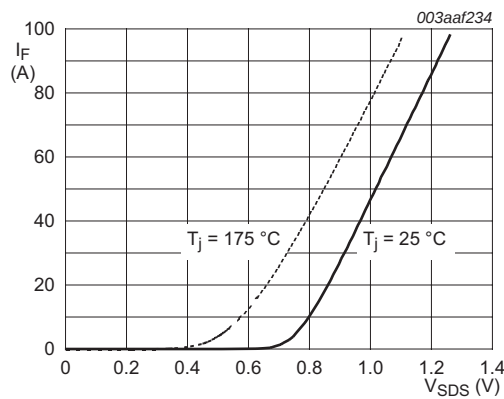
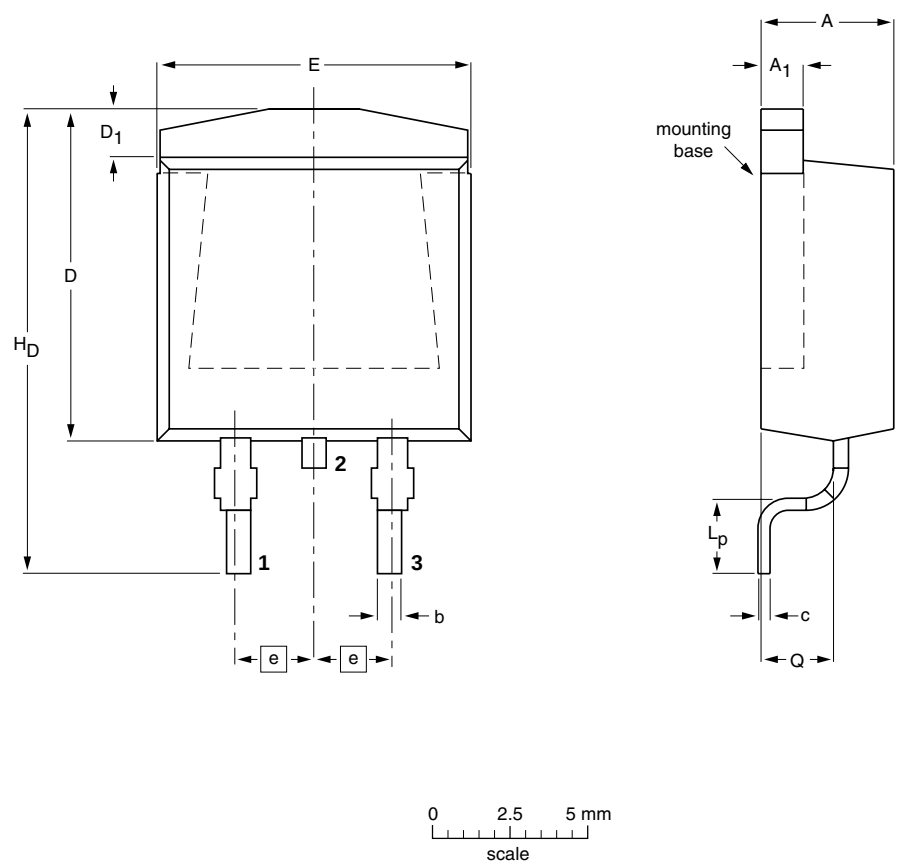


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 18. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9628-100A v.2	20110426	Product data sheet	-	BUK9528_9628-100A v.1
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Type number BUK9628-100A separated from data sheet BUK9528_9628-100A v.1.			
BUK9528_9628-100A v.1	20000301	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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