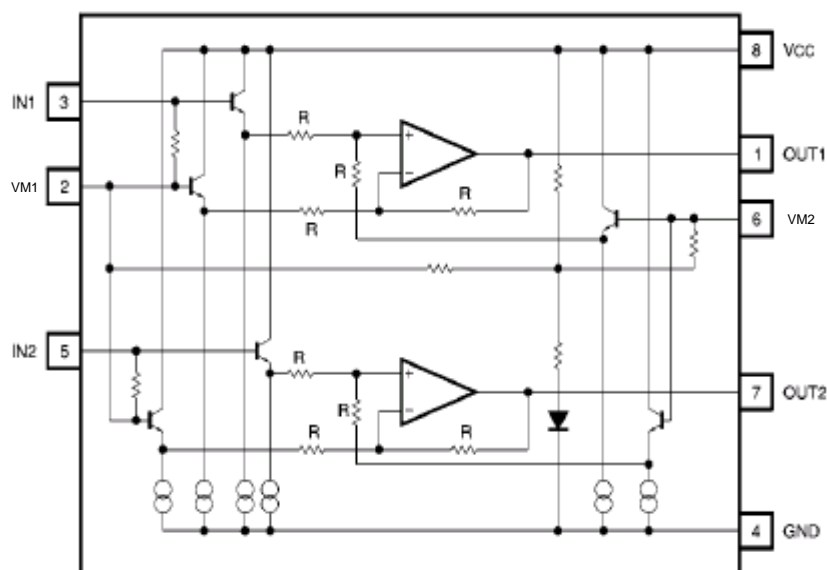


Block Diagram and Pin Configuration

TOP VIEW



Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V _{CC}	18	V
Power Dissipation	P _d	0.45 (Note 1)	W
Operation Temperature	T _{opr}	-30 to +85	°C
Storage Temperature	T _{stg}	-55 to +125	°C

(Note 1) Reduced by 4.5mW in Ta of 1°C over 25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V _{CC}	4	12	18	V

Electrical Characteristics

(Unless otherwise noted, Ta = 25°C, V_{CC} = 12V, f = 1kHz, R_g = 1.8kΩ)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent Current	I _Q	5.6	9.0	14.0	mA	V _{IN} = 0Vrms
Output Noise Voltage	V _{NO}	-	3.5	8.0	μVrms	BPF = 20Hz-20kHz
Voltage Gain	G _V	-1.5	-0.04	+1.5	dB	V _{OUT} = -10dBm, R _g = 0Ω
Maximum Output Voltage	V _{OM}	1.8	2.0	-	Vrms	THD = 0.1%, V _{CC} = 8V
Total Harmonic Distortion	THD	-	0.002	0.02	%	V _{OUT} = 0.7Vrms
Common-mode Rejection Ratio	CMRR	41	57	-	dB	
Common-mode Voltage	V _{CM}	2.5	3.75	-	Vrms	V _{CC} = 8V, CMRR = 40dB
Ripple Rejection Ratio	RR	72	80	-	dB	f _{RR} = 100Hz, V _{RR} = -10dBm, R _g = 0Ω
Channel Separation	CS	-	82	-	dB	V _{IN} = -10dBm, R _g = 1.8kΩ/OPEN
Slew Rate	SR	-	2.0	-	V/μS	
Input Resistance	R _{IN}	44	55	66	kΩ	

Typical Performance Curves

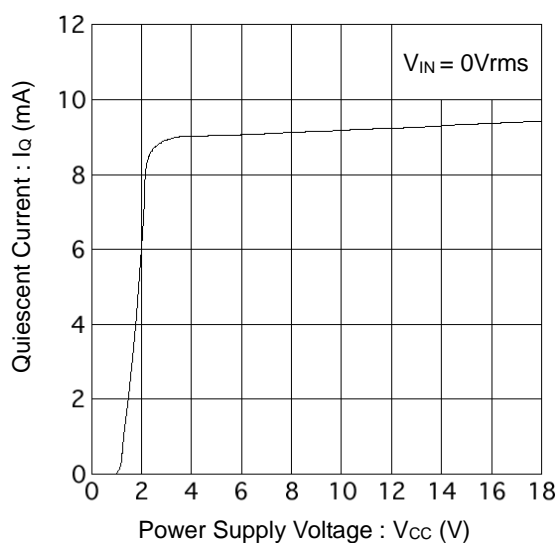


Figure 1. Quiescent Current vs Power Supply Voltage

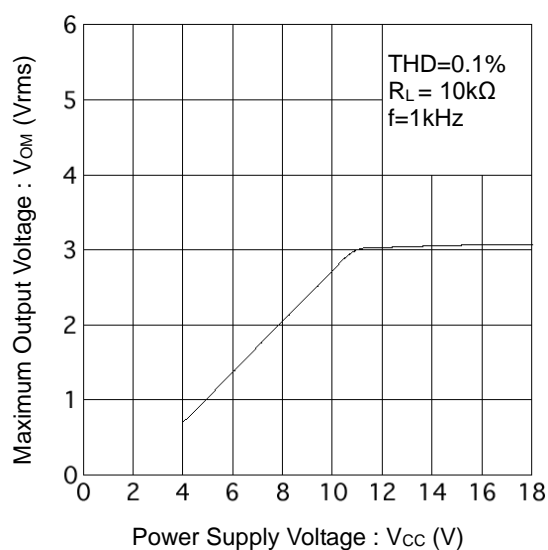


Figure 2. Maximum Output Voltage vs Power Supply Voltage

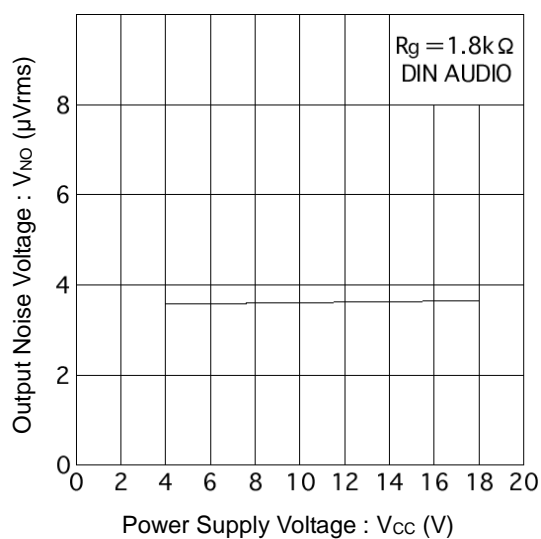


Figure 3. Output Noise Voltage vs Power Supply Voltage

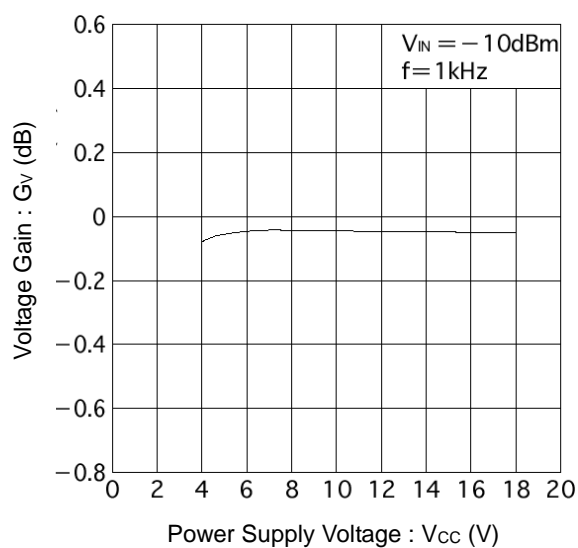


Figure 4. Voltage Gain vs Power Supply Voltage

Typical Performance Curves – continued

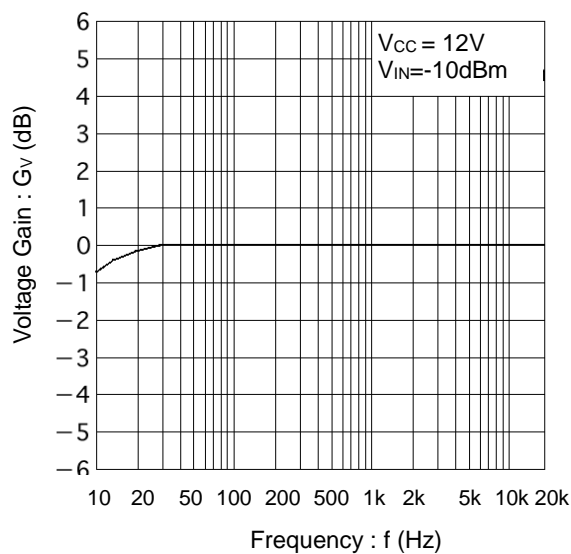


Figure 5. Voltage Gain vs Frequency

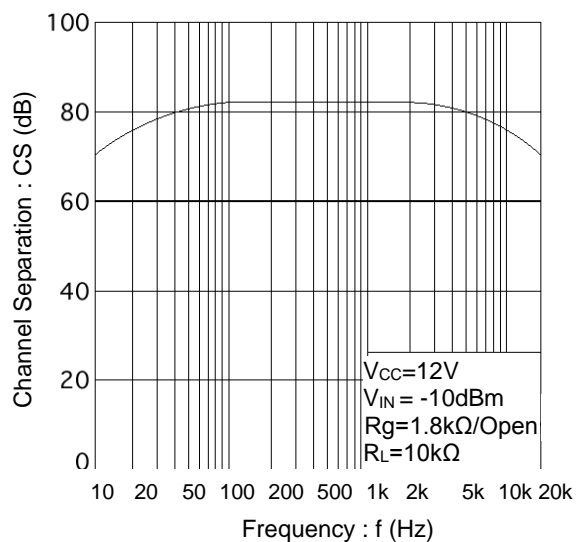


Figure 6. Channel Separation vs Frequency

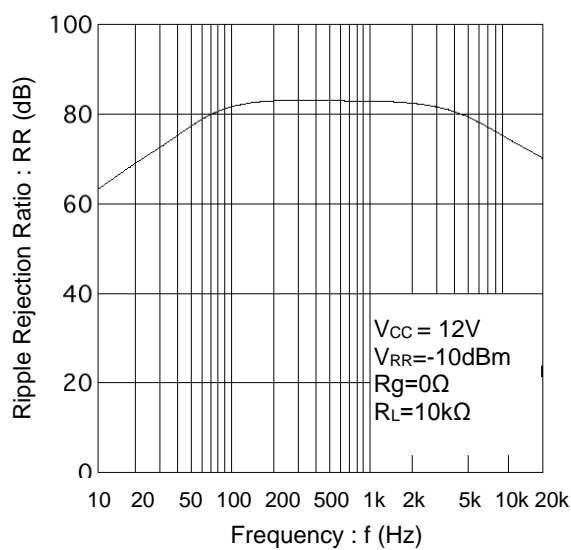


Figure 7. Ripple Rejection Ratio vs Frequency

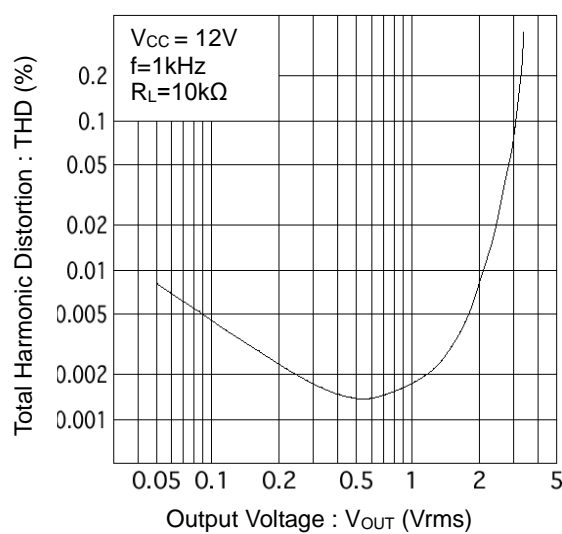


Figure 8. Total Harmonic Distortion vs Output Voltage

Typical Performance Curves – continued

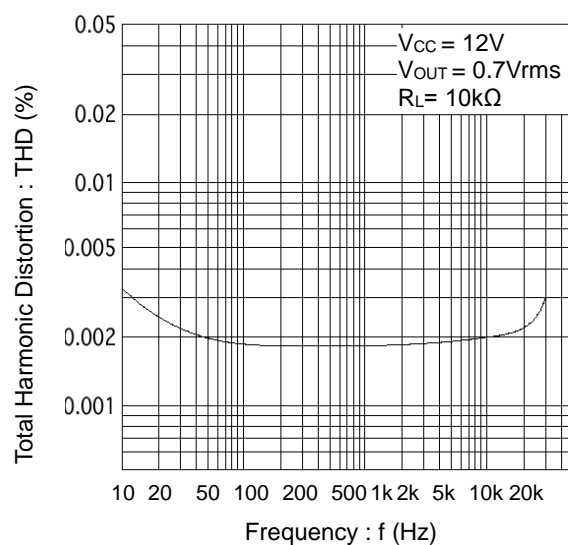


Figure 9. Total Harmonic Distortion vs Frequency

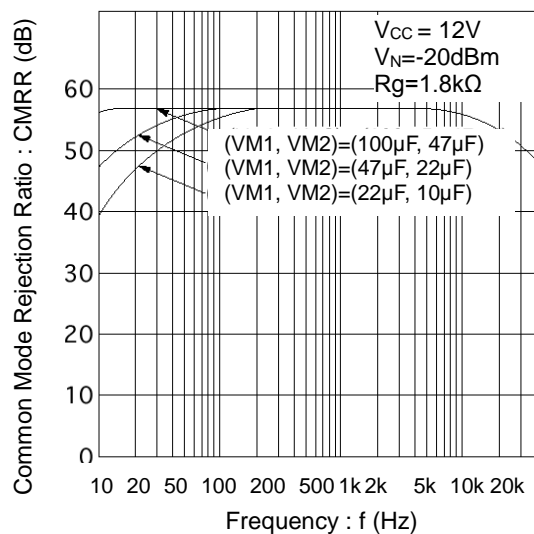


Figure 10. Common Mode Rejection Ratio vs Frequency

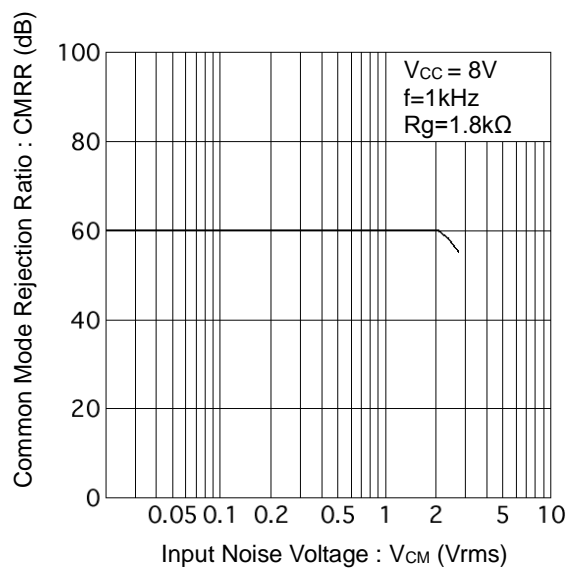


Figure 11. Common Mode Rejection Ratio vs Input Noise Voltage

Measurement Circuits

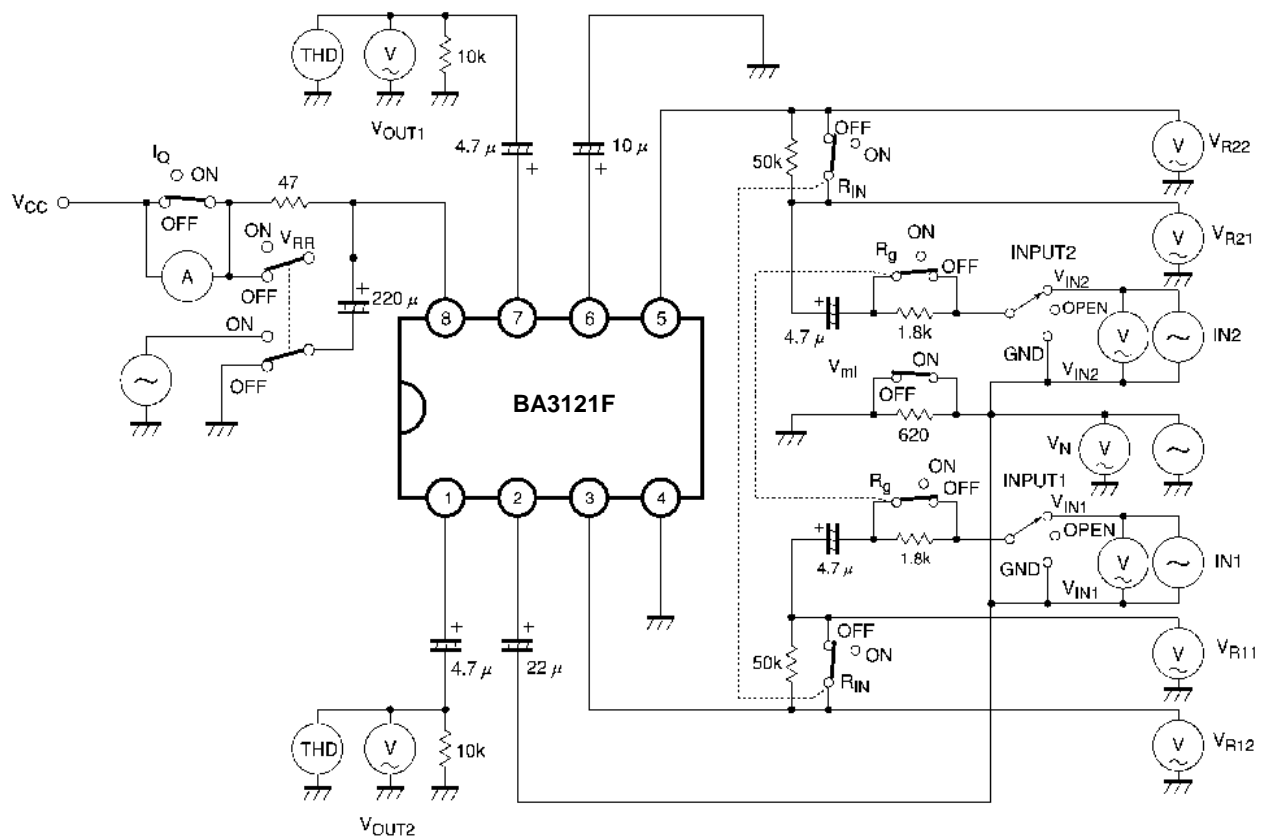


Figure 12

Application Information

1. Circuit Operation

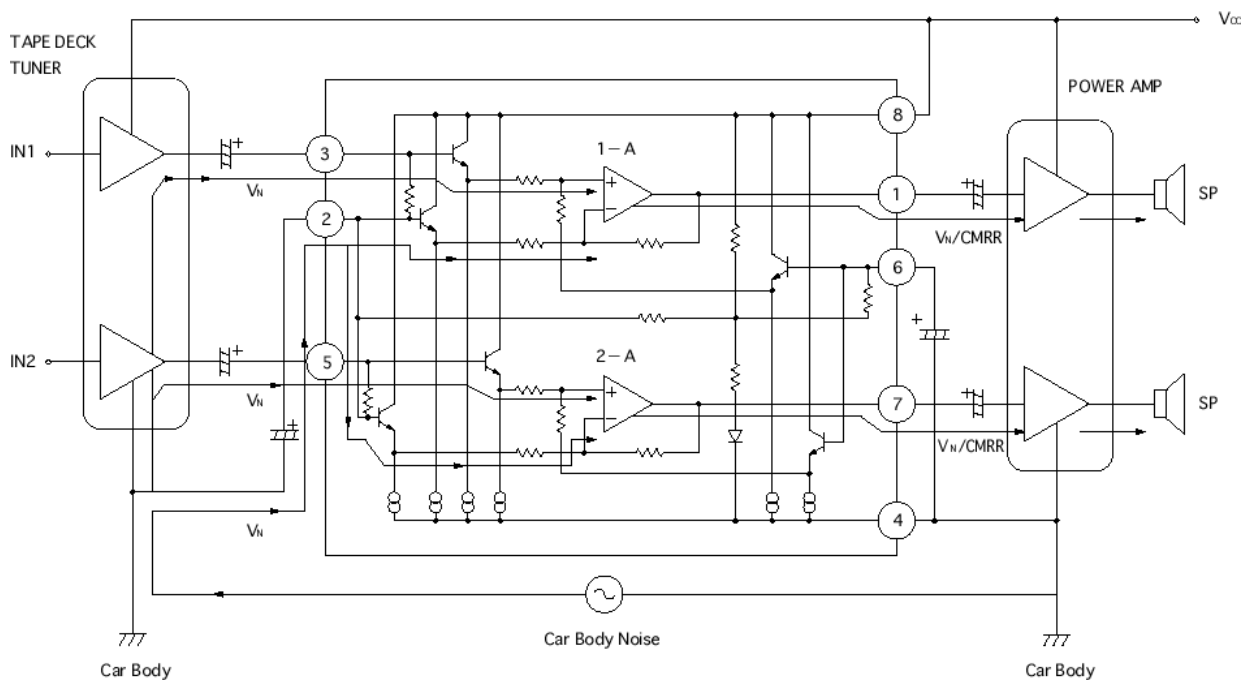


Figure 13. Flow of Noise in Car Audio Systems

Car audio systems are grounded to the car body. For this reason, electrical noise generated by the car electrical system can enter the power amplifier input through the chassis and become audible. BA3121F utilizes the common-mode rejection characteristics of an operational amplifier to eliminate this noise. Without BA3121F noise enters the power amplifier inputs directly. With BA3121F, the CMRR of operational amplifiers 1-A and 2-A eliminates the noise.

Principle of noise elimination:

To obtain the output voltage (e_o)

$$V_i = \frac{R_4}{(R_3 + R_4)} \cdot e_2 \quad (1)$$

$$e_o = -\frac{R_2}{R_1} e_1 + \frac{R_1 + R_2}{R_1} \cdot V_i \quad (2)$$

From (1) and (2)

$$\begin{aligned} e_o &= -\frac{R_2}{R_1} e_1 + \frac{R_1 + R_2}{R_1} \cdot \frac{R_4}{(R_3 + R_4)} \cdot e_2 \\ &= -\frac{R_2}{R_1} \cdot (e_1 - e_2) + \frac{R_1 R_4 - R_2 R_3}{R_1 (R_3 + R_4)} \cdot e_2 \end{aligned}$$

Ideally, if $R_1 R_4 = R_2 R_3$, and $e_1 = e_2$, the noise voltage will be zero. However, due to resistor mismatch, difference in the noise voltages (e_1 and e_2), and tolerances in the operational amplifier, a noise voltage is generated.

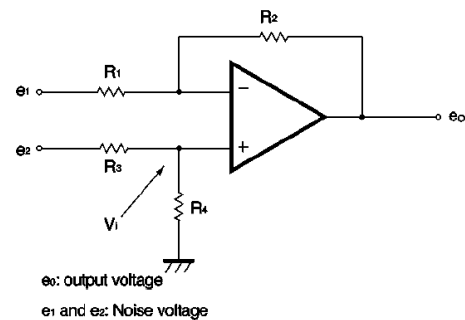


Figure 14. The Principle of Noise Rejection

With BA3121F, the elimination level of the noise is expressed as:

$$\text{CMRR} = 20 \log (e_o/e_i) (e_1 = e_2 = e_i)$$

Therefore, CMRR \geq 41dB can be guaranteed.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin\ A$ and $GND > Pin\ B$, the P-N junction operates as a parasitic diode.

When $GND > Pin\ B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

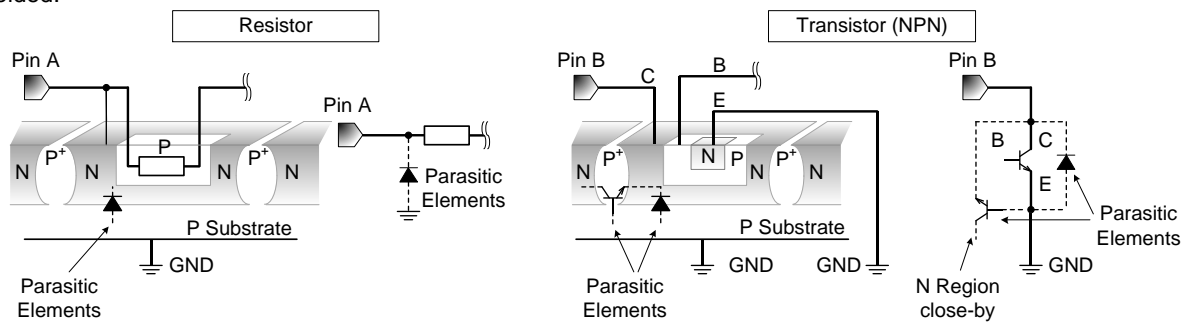


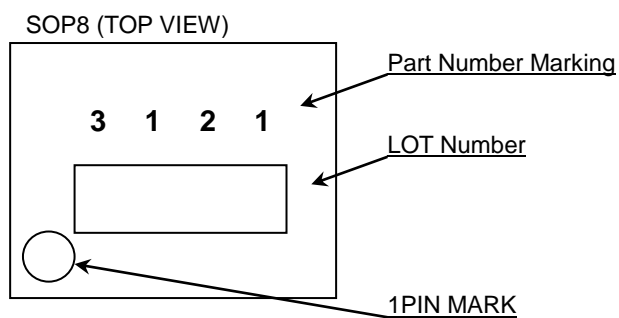
Figure 15. Example of monolithic IC structure

13. The capacitors of Pin2 (VM1), and Pin 6 (VM2) should maintain the ratio of 2:1 for ripple rejection characteristics. Maintaining this ratio will prevent the significant decrease on ripple rejection even if the capacitance is reduced to half.
14. Setting the capacitor value to twice or half will make CMRR +6dB or -6dB respectively (Figure 10) in the low frequency range.

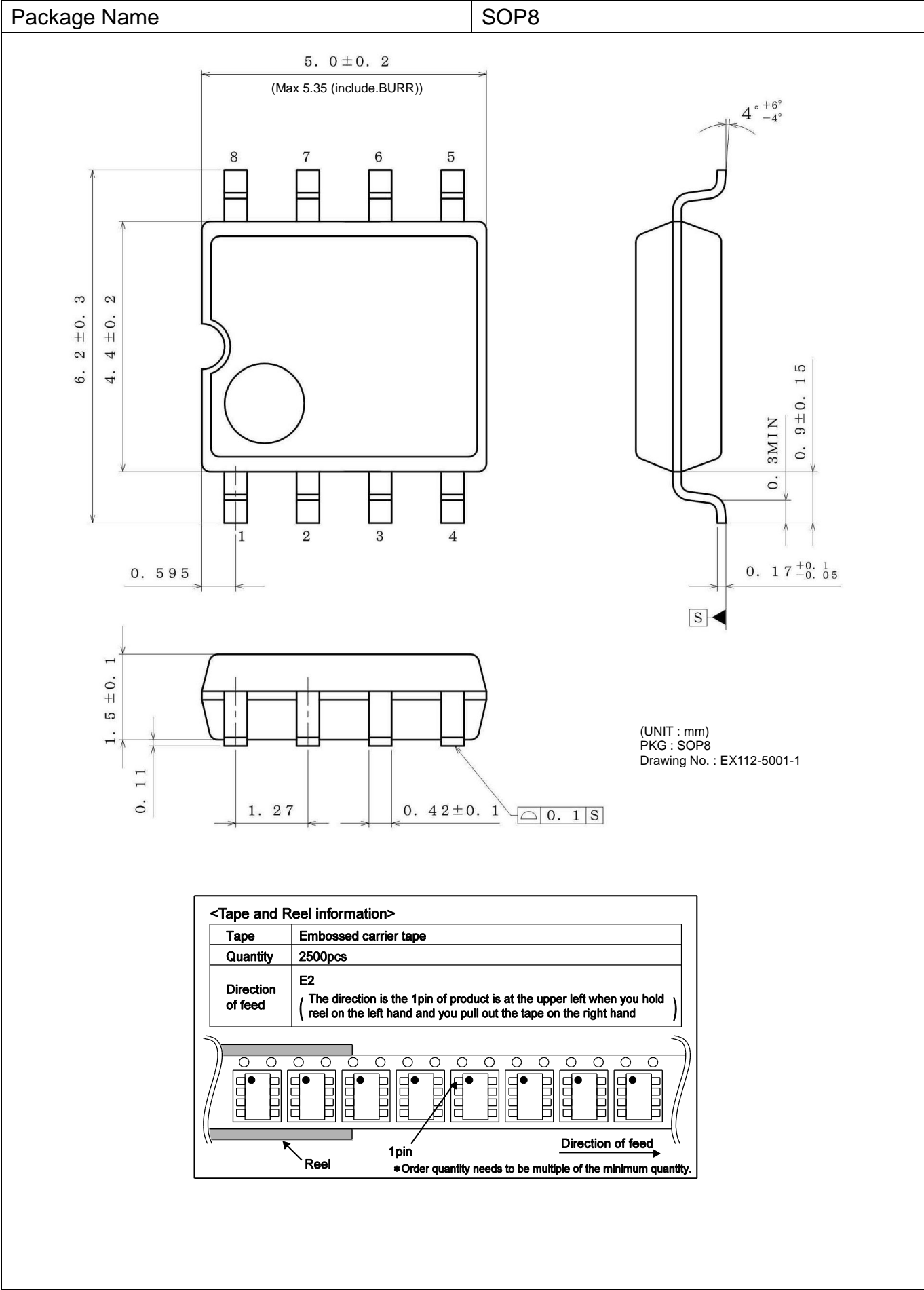
Ordering Information

B A 3 1 2 1 F							-	E 2
Part Number							Package F: SOP8	Packaging and forming specification E2: Embossed tape and reel

Marking Diagram



Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Changes
13.Nov.2015	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
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- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
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- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
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2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
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Package	SOP8
Unit Quantity	2500
Minimum Package Quantity	2500
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Constitution Materials List	inquiry
RoHS	Yes