

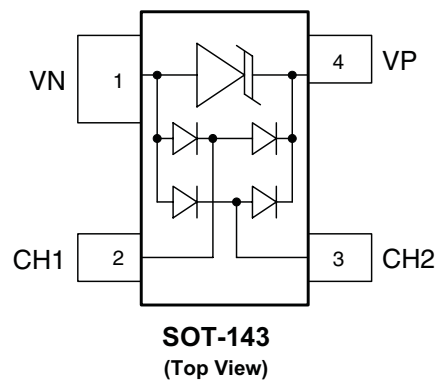
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8001AJI-05	-40°C to +85°C	SOT-143	RoHS Compliant Green Product
AOZ8001AJI-12	-40°C to +85°C	SOT-143	RoHS Compliant Green Product



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Storage Temperature (T_S)	-65°C to +150°C

Maximum Transient Rating

Device	HBM ⁽¹⁾	ESD (Contact) ⁽²⁾	ESD (Air) ⁽²⁾	Surge (8/20μs)
AOZ8001AJI-05	±30kV	±30kV	±30kV	±18A
AOZ8001AJI-12	±30kV	±30KV	±30kV	±13A

Notes:

- Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge} = 100pF$, $R_{Discharge} = 1.5k\Omega$.
- IEC 61000-4-2 discharge with $C_{Discharge} = 150pF$, $R_{Discharge} = 330\Omega$.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40°C to +125°C

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise specified.

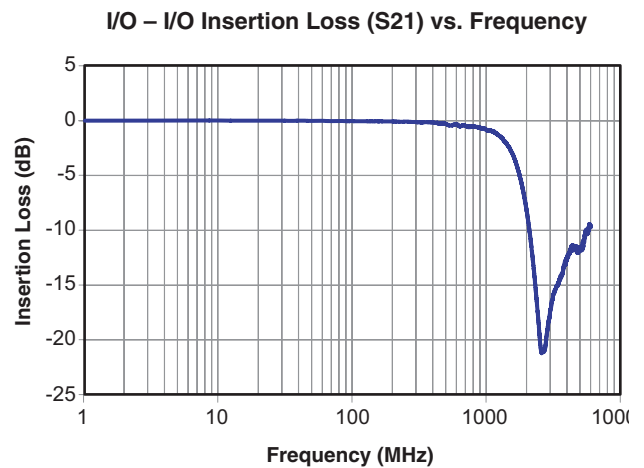
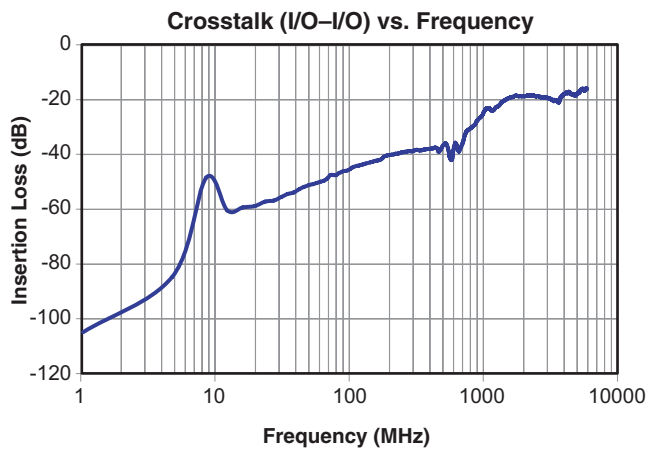
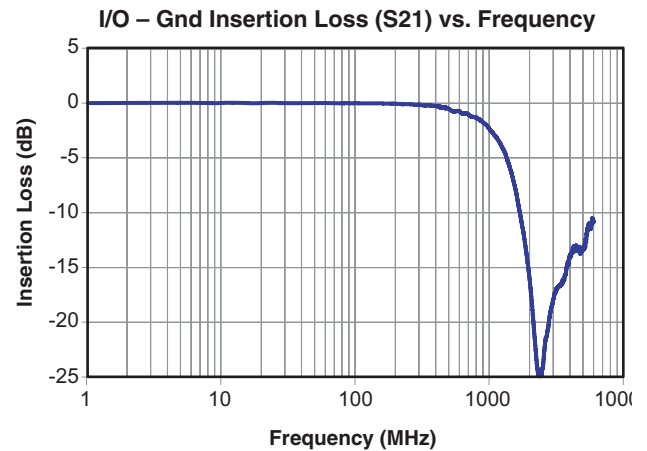
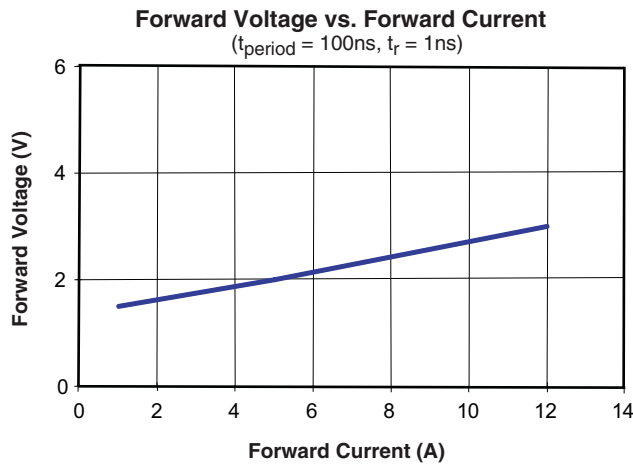
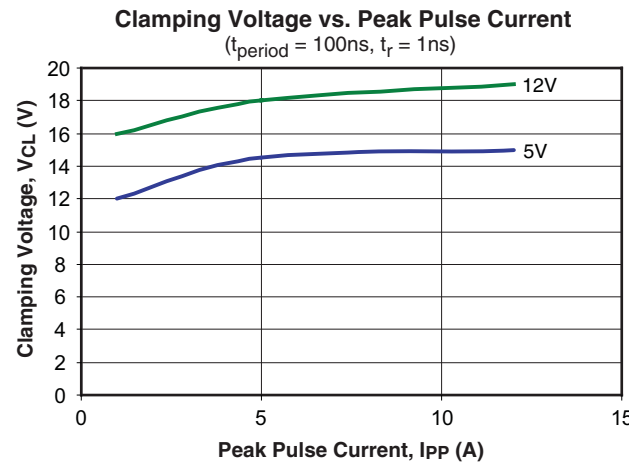
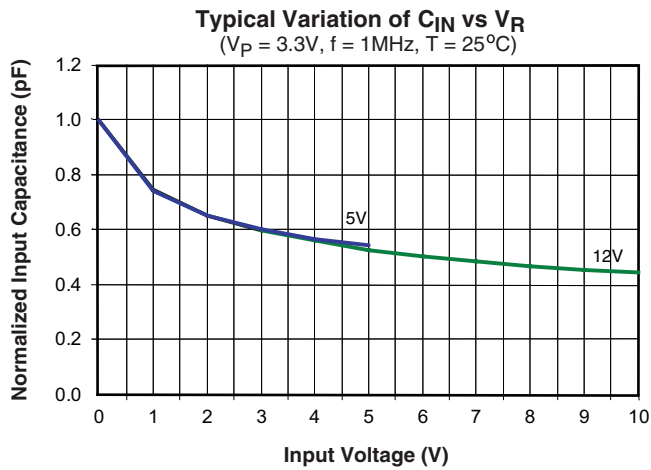
Symbol	Parameter	Diagram
I_{PP}	Reverse Peak Pulse Current	
$V_{CL}^{(5)(7)}$	Clamping Voltage @ I_{PP}	
$V_{RWM}^{(3)}$	Working Peak Reverse Voltage	
I_R	Maximum Reverse Leakage Current @ V_{RWM}	
$V_{BR}^{(4)}$	Breakdown Voltage	
I_F	Forward Current	
V_F	Forward Voltage	
P_{PK}	Peak Power Dissipation	
$C_J^{(6)}$	I/O–GND Capacitance @ $V_R = 0$ and $f = 1\text{MHz}$	

Device	Device Marking	V_{RWM} (V) Max.	V_{BR} (V) Typ. @ 1mA	I_R (μA) Max.	V_F (V) Typ.	V_{CL} Max.			C_J (pF) Typ.	C_J (pF) Max.
						$I_{PP} = 1\text{A}$	$I_{PP} = 5\text{A}$	$I_{PP} = 12\text{A}$		
AOZ8001AJI-05	AD	5.5	8.5	1.0	0.85	12.50	15.00	16.00	1.80	2.50
AOZ8001AJI-12	AD	12.5	15.0	1.0	0.85	16.00	18.00	19.00	1.80	2.50

Notes:

- The working peak reverse voltage, V_{RWM} , should be equal to or greater than the DC or continuous peak operating voltage level.
- V_{BR} is measured at the pulse test current I_T .
- Measurements performed with no external capacitor on V_P (pin 4 floating).
- Measurements performed with V_P biased to 3.3 Volts (pin 4 @ 3.3V).
- Measurements performed using a 100ns Transmission Line Pulse (TLP) system.

Typical Performance Characteristics



Application Information

The AOZ8001A TVS is design to protect two data lines from fast damaging transient over-voltage by clamping it to a reference. When the transient on a protected data line exceed the reference voltage the steering diode is forward bias thus, conducting the harmful ESD transient away from the sensitive circuitry under protection.

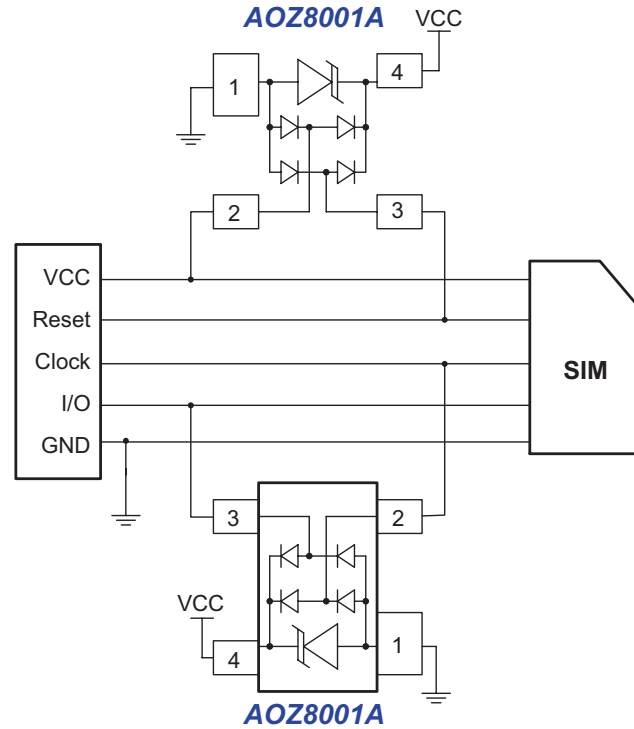
PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8001A devices should be located as close as possible to the noise source. The placement of the AOZ8001A devices should be used on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8001A devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8001A device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize inter-connecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by

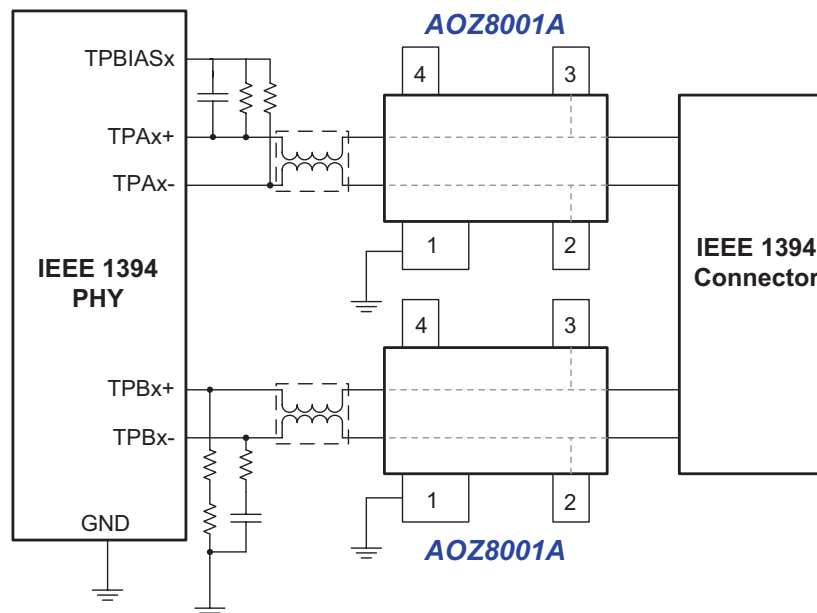
using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design. The AOZ8001A ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

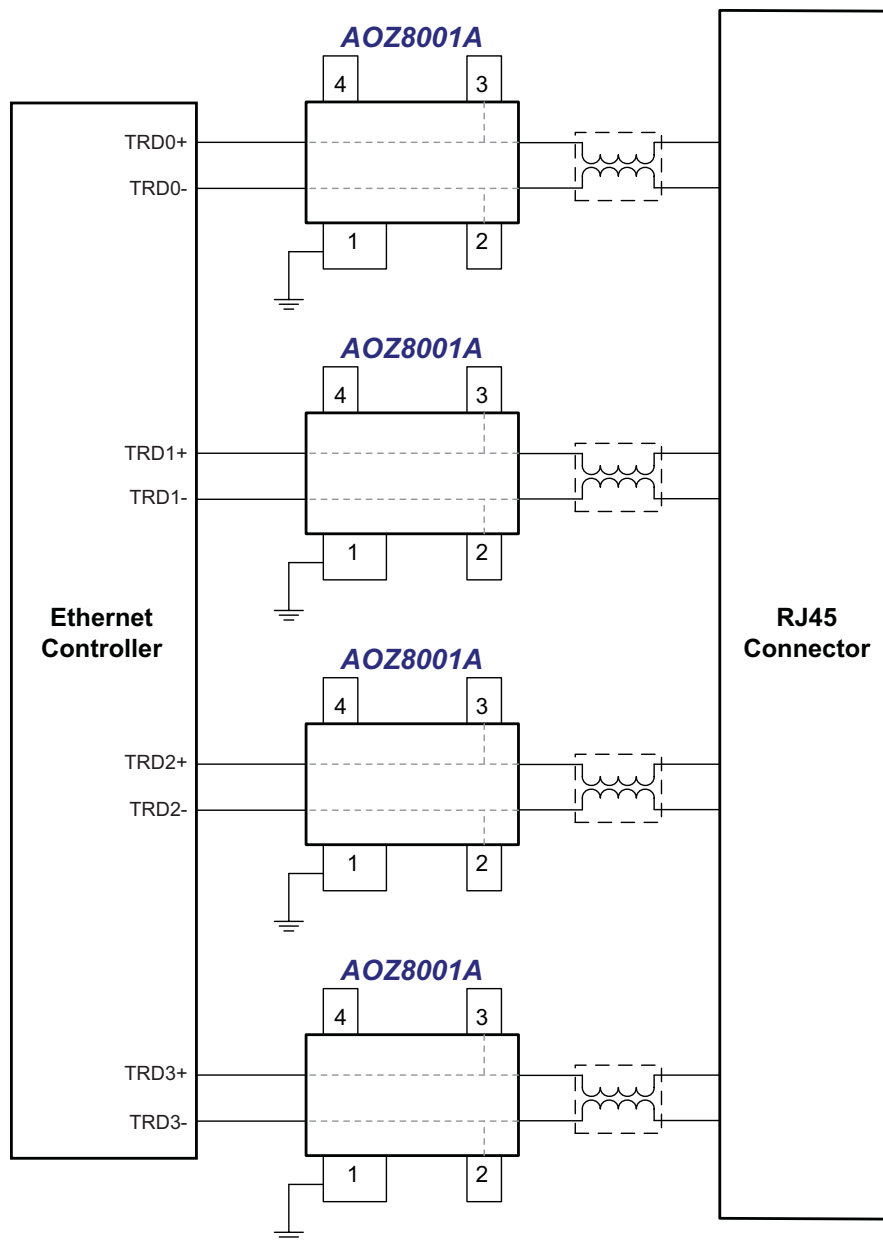
1. Place the TVS near the IO terminals or connectors to restrict transient coupling.
2. Fill unused portions of the PCB with ground plane.
3. Minimize the path length between the TVS and the protected line.
4. Minimize all conductive loops including power and ground loops.
5. The ESD transient return path to ground should be kept as short as possible.
6. Never run critical signals near board edges.
7. Use ground planes whenever possible.
8. Avoid running critical signal traces (clocks, resets, etc.) near PCB edges.
9. Separate chassis ground traces from components and signal traces by at least 4mm.
10. Keep the chassis ground trace length-to-width ratio <5:1 to minimize inductance.
11. Protect all external connections with TVS diodes.



SIM Card Port Connection

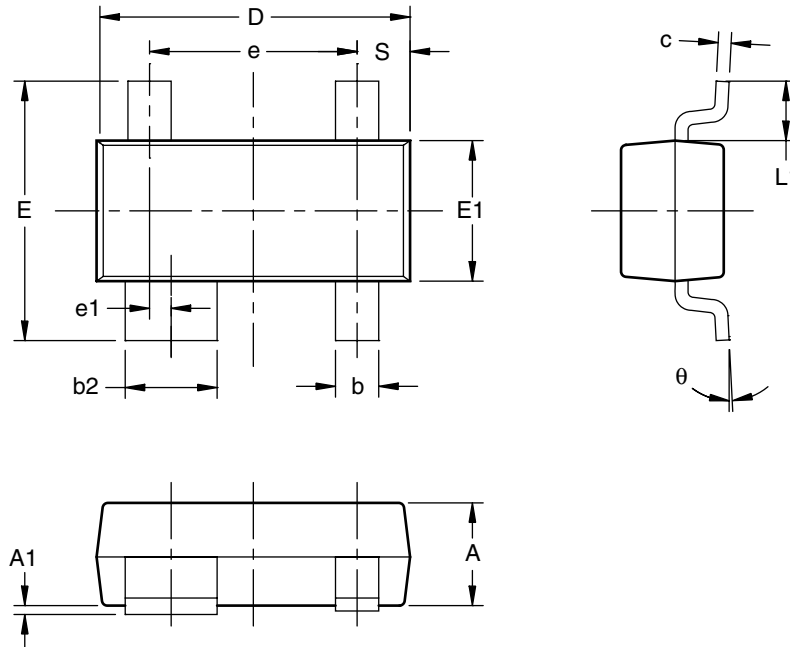


IEEE1394 Port Connection

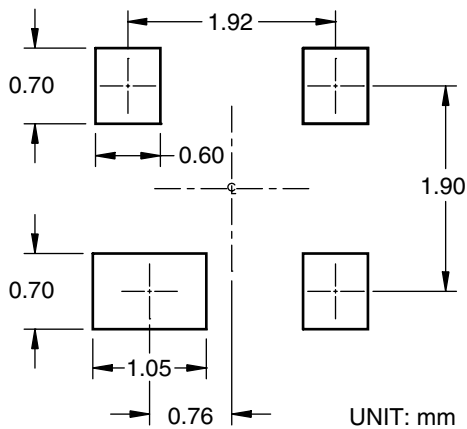


10/100 Ethernet Port Connection

Package Dimensions, SOT143-4L



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.890	—	1.120
A1	0.013	—	0.100
b	0.370	—	0.510
b2	0.760	—	0.940
c	0.085	—	0.180
D	2.800	—	3.040
E	2.100	—	2.640
E1	1.200	—	1.400
e	1.920 BSC		
e1	0.200 BSC		
L1	0.550 REF		
S	0.450	—	0.600
θ	0°	—	8°

Dimensions in inches

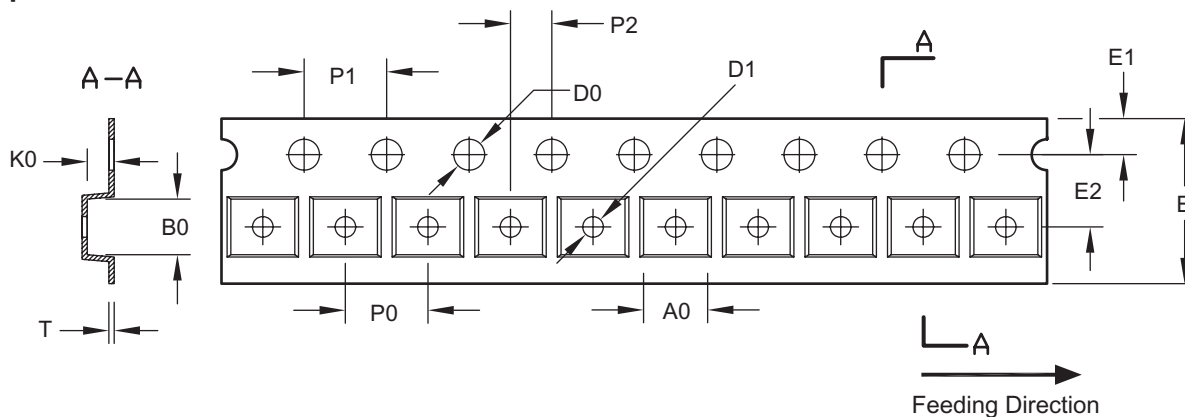
Symbols	Min.	Nom.	Max.
A	0.035	—	0.044
A1	0.001	—	0.004
b	0.015	—	0.020
b2	0.030	—	0.037
c	0.003	—	0.007
D	0.110	—	0.120
E	0.083	—	0.104
E1	0.047	—	0.055
e	0.076 BSC		
e1	0.008 BSC		
L1	0.022 REF		
S	0.018	—	0.024
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Tolerances are 0.10mm unless otherwise specified.
3. Package body sizes exclude mold flash and gate burrs.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SOT143-4L

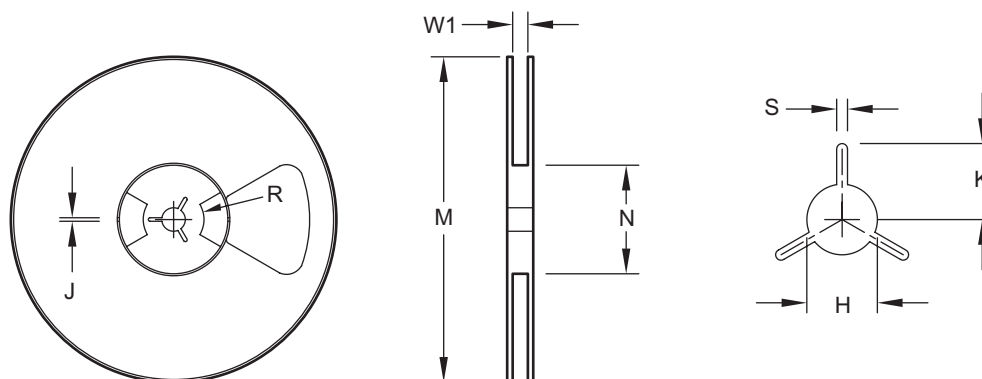
Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOT-143	3.10 ± 0.10	2.69 ± 0.10	1.30 ± 0.10	1.50 ± 0.10	1.00 $+0.25/-0.00$	8.00 $+0.30/-0.10$	1.75 ± 0.10	3.50 ± 0.05	4.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.254 ± 0.013

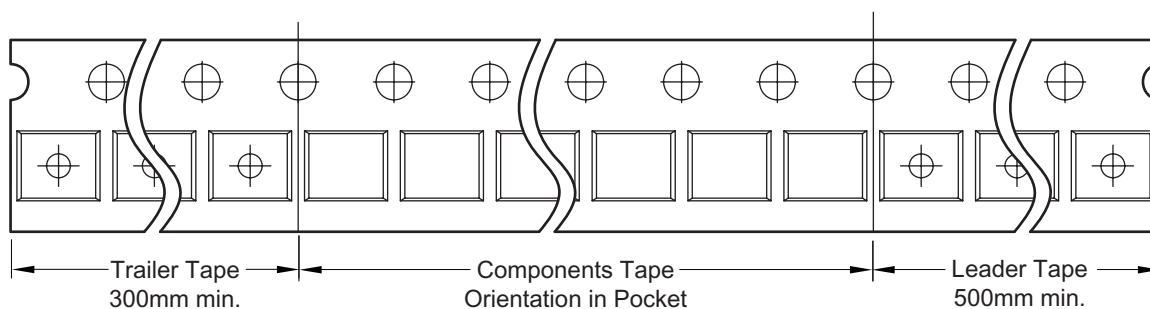
Reel



UNIT: mm

Tape Size	Reel Size	M	N	W1	H	S	K	R	J
8mm	$\phi 177.8$	$\phi 177.8$ Max.	55.0 Min.	8.4 $+1.50/-0.0$	13.0 $+0.5/-0.2$	1.5 Min.	10.1 Min.	12.7	4.0 ± 0.1

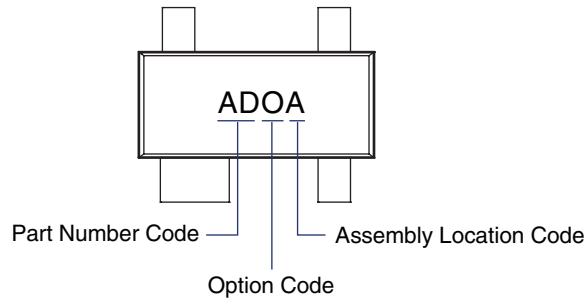
Leader/Trailer and Orientation



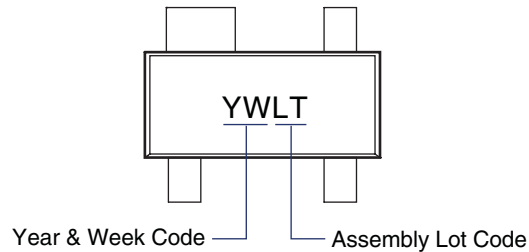
Part Marking

AOZ8001AJI (SOT-143)

Top Marking



Bottom Marking



This datasheet contains preliminary data; supplementary data may be published at a later date. Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.