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REVISION HISTORY

10/2019—Rev. D to Rev. E

Changes to Output Capacitor Section ... 25
Updated Outline Dimensions ... 32
Change to Ordering Guide ... 32

2/2014—Rev. C to Rev. D

Change to Figure 13 ... 9
Updated Outline Dimensions ... 32

11/2012—Rev. B to Rev. C

Change to Figure 6 ... 8
Changes to Ordering Guide ... 32

8/2012—Rev. A to Rev. B

Change to Figure 62 ... 17
Changes to Figure 63, Figure 64, Figure 65, and Figure 66 ... 18

5/2012—Rev. 0 to Rev. A

Changed Voltage Range for SW to PGND and Ground Plane from −0.3 V to VIN + 0.3 V to −0.7 V to VIN + 0.3 V ... 6
Changes to Ordering Guide ... 32

4/2012—Revision 0: Initial Version

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SPECIFICATIONS

V_{IN} = V_{OUT} + 1 V or 3.2 V, whichever is greater, EN = V_{IN}, I_{OUT} = 100 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, T_A = 25°C for typical specifications, T_J = −40°C to +125°C for minimum/maximum specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Input Voltage Range	V_{IN}		3.2		15	V
Quiescent Current	I_{Q-PSM}	FSEL = V_{IN}, SYNC = 0 V, no load, device not switching		13.5		µA
	I_{Q-PWM}	FSEL = V_{IN}, SYNC = V_{IN}, no load, device not switching		725		µA
	I_{SW-PWM}	FSEL = V_{IN}, SYNC = V_{IN}, no load, device switching		5.7		mA
Shutdown Current	I_{SHUT}	EN = GND, T_J = −40°C to +85°C		1.2	3.5	µA
FIXED OUTPUT						
Output Current	I_{OUT}		800			mA
Fixed Output Accuracy	V_{OUT}	Initial set point, I_{OUT} = 250 mA, T_J = 25°C	−1		+1	%
		I_{OUT} = 250 mA	−1.5		+1.5	%
		No load to full load, PWM mode	−3		+3	%
ADJUSTABLE OUTPUT						
Feedback Voltage	V_{FB}			0.8		V
Feedback Voltage Accuracy	V_{FB-TOL}	Initial set point, I_{OUT} = 250 mA, T_J = 25°C	−1		+1	%
Output Voltage Range	$V_{OUT-ADJ}$	No load to full load	0.8		14	V
FIXED AND ADJUSTABLE OUTPUT						
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	No load to full load		0.125		%/A
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 250 mA		0.01		%/V
Efficiency	EFF	I_{OUT} = 250 mA, V_{IN} = 7.2 V, V_{OUT} = 3.3 V		92		%
Overcurrent Frequency Foldback Threshold						
Rising	$OC_{FOLDBACK-RISE}$	% of V_{OUT}, V_{OUT} rising		50		%
Falling	$OC_{FOLDBACK-FALL}$	% of V_{OUT}, V_{OUT} falling		37.5		%
PSM Threshold	$PSM_{THRESHOLD}$	V_{IN} = 7.2 V, V_{OUT} = 3.3 V		170		mA
Feedback Pin Input Current						
Fixed	$I_{FB-FIXED}$	Fixed output voltage model		2.5		µA
Adjustable	$I_{FB-ADJUST}$	Adjustable output voltage model		10		nA
Minimum On Time	$ON\text{-}TIME_{MIN}$	V_{IN} < 5.5 V		65	100	ns
		V_{IN} > 5.5 V		40	60	ns
Soft Start Time	SS_{TIME}	When EN rises from 0 V to V_{IN}, and V_{OUT} = 0.9 × V_{OUT}		350		µs
Active Pull-Down Resistance (ADP2371)	$R_{PULL-DOWN}$			260	400	Ω
POWER SWITCH						
P-Channel On Resistance	RDS_{ON-P}	V_{IN} > 5.5 V, I_{OUT} = 400 mA		400		mΩ
		V_{IN} < 5.5 V, I_{OUT} = 400 mA		500		mΩ
N-Channel On Resistance	RDS_{ON-N}	V_{IN} > 5.5 V, I_{OUT} = 400 mA		280		mΩ
		V_{IN} < 5.5 V, I_{OUT} = 400 mA		400		mΩ
Current Limit						
P-Channel	I_{LIM-P}	Peak inductor current		1200	1300	mA
N-Channel	I_{LIM-N}	Peak inductor current		500	550	mA
Leakage Current	$I_{LEAK-SW}$					
P-Channel				0.01	1	µA
N-Channel				0.01	1	µA

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Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OSCILLATOR						
Oscillator Frequency	f_{OSC}	FSEL = V_{IN}, 3.2 V ≤ V_{IN} ≤ 15 V	1.0	1.2	1.4	MHz
		FSEL = 0 V, 3.2 V ≤ V_{IN} ≤ 15 V	500	600	700	kHz
Frequency Synchronization Range	f_{SYNC_RANGE}	FSEL = 0 V, 3.2 V ≤ V_{IN} ≤ 15 V	400		800	kHz
		FSEL = V_{IN}, 3.2 V ≤ V_{IN} ≤ 15 V	0.8		1.6	MHz
Synchronization Threshold						
High	$SYNC_{HIGH}$	3.2 V ≤ V_{IN} ≤ 15 V	1.2			V
Low	$SYNC_{LOW}$	3.2 V ≤ V_{IN} ≤ 15 V			0.4	V
Hysteresis	$SYNC_{HYS}$	3.2 V ≤ V_{IN} ≤ 15 V		200		mV
Typical Sync Duty Cycle Range	$SYNC_{DUTY}$	V_{IN} (1.2 MHz), 3.2 V ≤ V_{IN} ≤ 5 V, FSEL = V_{IN}	20		55	%
		V_{IN} (1.2 MHz), 5 V ≤ V_{IN} ≤ 15 V, FSEL = V_{IN}	20		70	%
SYNC Pin Leakage Current	$SYNC_{LKG}$	SYNC = 0 V or SYNC = V_{IN}		0.05	1	µA
FSEL Threshold		3.2 V ≤ V_{IN} ≤ 15 V				
High	$FESL_{HIGH}$		1			V
Low	$FSEL_{LOW}$				0.4	V
Hysteresis	$FSEL_{HYS}$			125		mV
FSEL Pin Leakage Current	$FSEL_{LKG}$	FSEL = 0 V or FSEL = V_{IN}		0.04	1	µA
POWER GOOD (PG PIN)						
PG Threshold		3.2 V ≤ V_{IN} ≤ 15 V				
Rising	PG_{RISE}			92	95	%
Falling	PG_{FALL}		82.5	87		%
Hysteresis	PG_{HYS}			5		%
PG Output Low	PG_{LOW}	Pull-up current < 1 mA			0.3	V
PG Delay						
Rising	$PG_{DELAYRISE}$	V_{OUT} crossing PG rising threshold, pull-up current < 1 mA		20		µs
Falling	$PG_{DELAYFALL}$	V_{OUT} crossing PG falling threshold, pull-up current < 1 mA		0.5		µs
PG Leakage	PG_{LKG}			0.04	1	µA
UNDERVOLTAGE LOCKOUT (UVLO)						
Input Voltage Rising	$UVLO_{RISE}$				3.19	V
Input Voltage Falling	$UVLO_{FALL}$		2.80			V
Hysteresis	$UVLO_{HYS}$			190		mV
ENABLE INPUT STANDBY (EN PIN)		3.2 V ≤ V_{IN} ≤ 15 V				
EN Input Logic						V
High	$EN_{STBY-HIGH}$		1			
Low	$EN_{STBY-LOW}$				0.4	V
Hysteresis	$EN_{STBY-HYS}$			125		mV
ENABLE INPUT PRECISION (EN PIN)		3.2 V ≤ V_{IN} ≤ 15 V				
EN Input Logic						
High	EN_{HIGH}		1.135	1.2	1.26	V
Low	EN_{LOW}		1.045	1.1	1.155	V
Hysteresis	EN_{HYS}			100		mV
EN Input Leakage Current	I_{EN-LKG}	EN = V_{IN} or GND		0.05	1	µA
EN Input Delay Time	TI_{EN-DLY}	For V_{OUT} = 0 V to 0.1 × V_{OUT} when EN rises from 0 V to V_{IN}		70		µs
THERMAL SHUTDOWN		3.2 V ≤ V_{IN} ≤ 15 V				
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C

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RECOMMENDED SPECIFICATIONS: CAPACITORS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE[1]	C_{MIN}	T_A = −40°C to +125°C	6.5	10		µF
CAPACITOR ESR	R_{ESR}	T_A = −40°C to +125°C	1		10	mΩ

[1] The minimum input and output capacitance should be greater than 7 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R- and X5R-type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any buck.

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ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to PGND and Ground Plane	−0.3 V to +17 V
SW to PGND and Ground Plane	−0.7 V to VIN + 0.3 V
FB to PGND and Ground Plane	−0.3 V to +6 V
EN to PGND and Ground Plane	−0.3 V to +17 V
PG to PGND and Ground Plane	−0.3 V to +17 V
SYNC to PGND and Ground Plane	−0.3 V to +17 V
FSEL to PGND and Ground Plane	−0.3 V to +17 V
Temperature Range	
Storage	−65°C to +150°C
Operating Ambient	−40°C to +85°C
Operating Junction	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. Exceeding the junction temperature (T_J) limit can cause damage to the ADP2370/ADP2371. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. The maximum ambient temperature may require derating in applications with high power dissipation and poor thermal resistance.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature of the device is dependent on the ambient temperature, the power dissipation of the device, and the junction to ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. θ_{JA} is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} can vary, depending on PCB material, layout, and environmental conditions.

The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. See JESD 51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, for detailed information on board construction. For more information, see Application Note AN-772, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

Ψ_{JB} is the junction to board thermal characterization parameter with units of °C/W. The Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

For more detailed information regarding Ψ_{JB}, see JESD51-12 and JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JC} is a parameter for surface-mount packages with top mounted heat sinks.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
8-Lead 3 mm × 3 mm LFCSP	36.7	23.5	17.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

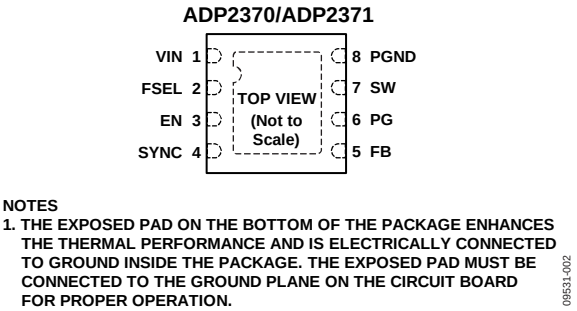

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Power Input.
2	FSEL	Frequency Select. High = 1.2 MHz, low = 600 kHz.
3	EN	Enable. Enable input with precision thresholds.
4	SYNC	Synchronize. This pin is used to synchronize the device to an external 600 kHz to 1.2 MHz clock or forces PWM mode when it is held high. SYNC held low forces automatic PWM/PSM operation.
5	FB	Feedback. This pin provides feedback from the output.
6	PG	Power Good. PG is an open-drain output.
7	SW	Switch. This pin serves as the connection from the power MOSFETs to the inductor.
8	PGND	Power Ground.
	EPAD	Exposed Pad. The exposed pad on the bottom of the package enhances the thermal performance and is electrically connected to ground inside the package. The exposed pad must be connected to the ground plane on the circuit board for proper operation.

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TYPICAL PERFORMANCE CHARACTERISTICS

BUCK OUTPUT

Using recommended inductor values, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, automatic PSM/PWM mode, T_A = 25°C, unless otherwise noted.

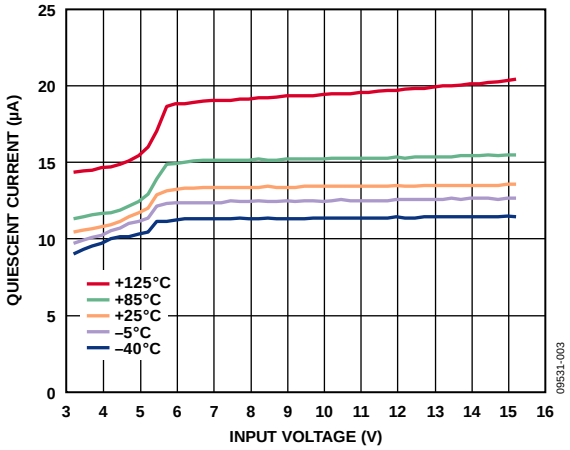

Figure 3. Quiescent Supply Current vs. Input Voltage, Nonswitching, Different Temperatures

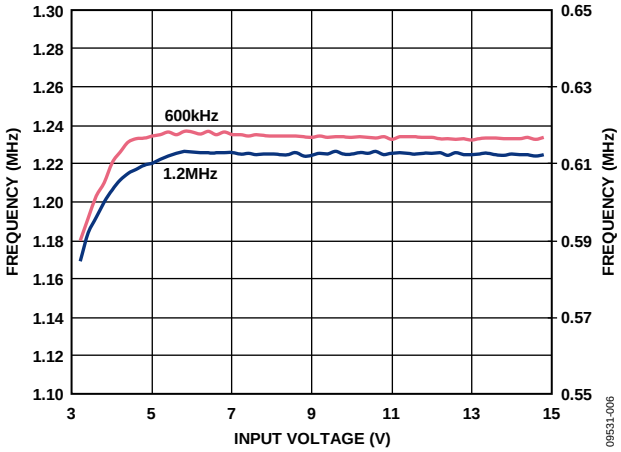

Figure 6. Switching Frequency vs. Input Voltage, FPWM Mode

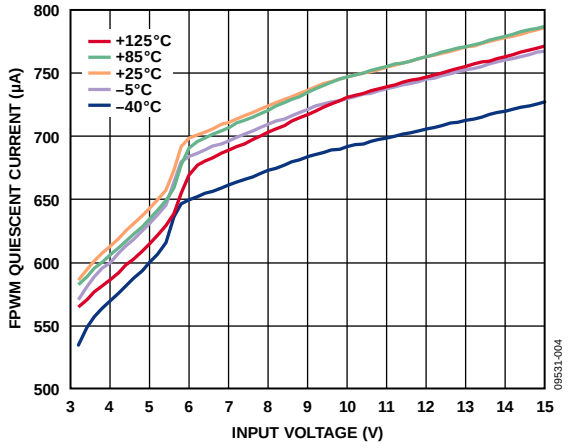

Figure 4. FPWM Quiescent Supply Current vs. Input Voltage, Nonswitching, Different Temperatures

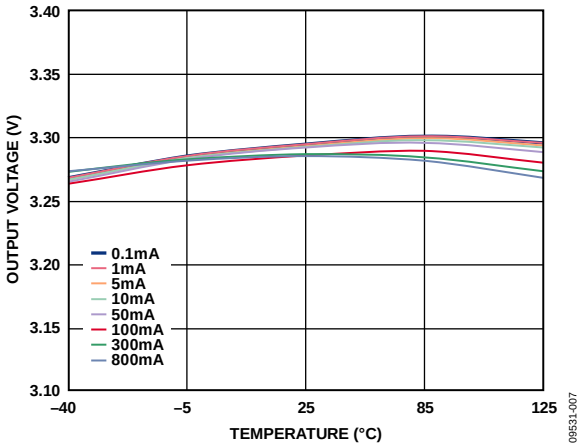

Figure 7. Output Voltage vs. Temperature, V_{OUT} = 3.3 V, V_{IN} = 7.3 V, Different Loads

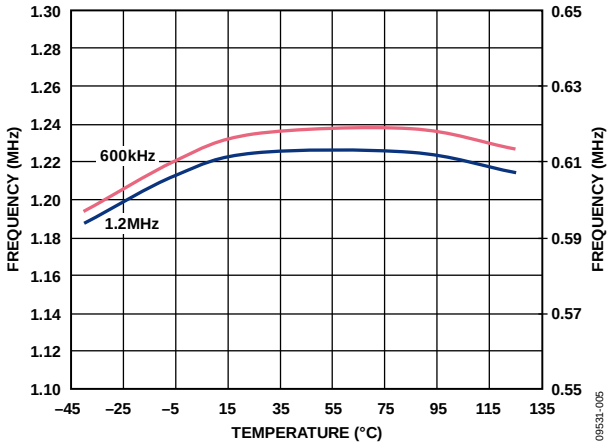

Figure 5. Switching Frequency vs. Temperature, FPWM Mode, V_{IN} = 8 V

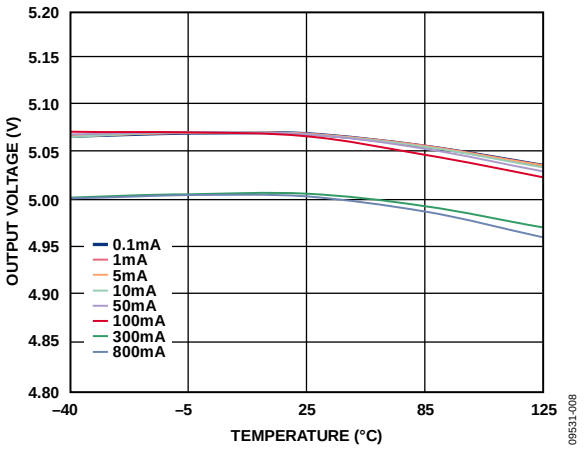

Figure 8. Output Voltage vs. Temperature, V_{OUT} = 5 V, V_{IN} = 7.2 V, Different Loads

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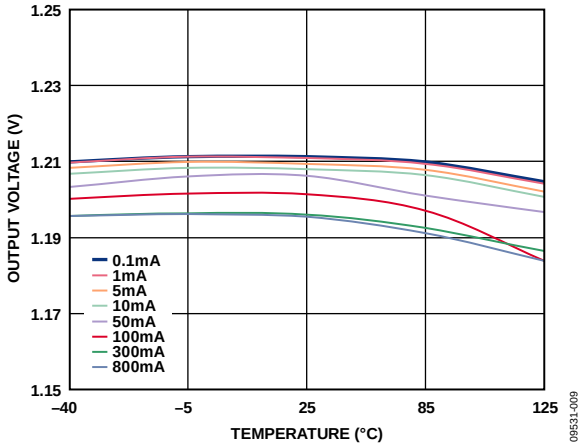

Figure 9. Output Voltage vs. Temperature, V_{OUT} = 1.2 V, V_{IN} = 4 V, Different Loads

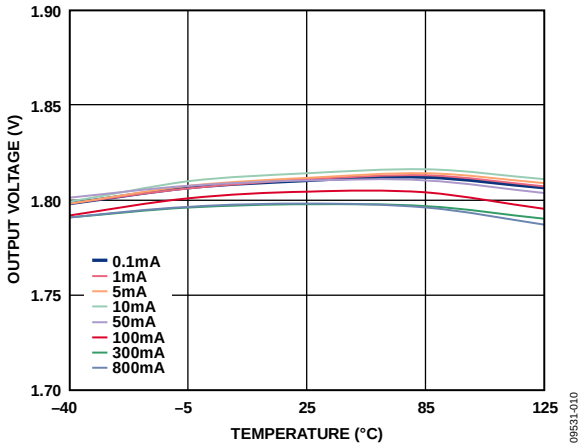

Figure 10. Output Voltage vs. Temperature, V_{OUT} = 1.8 V, V_{IN} = 7.2 V, Different Loads

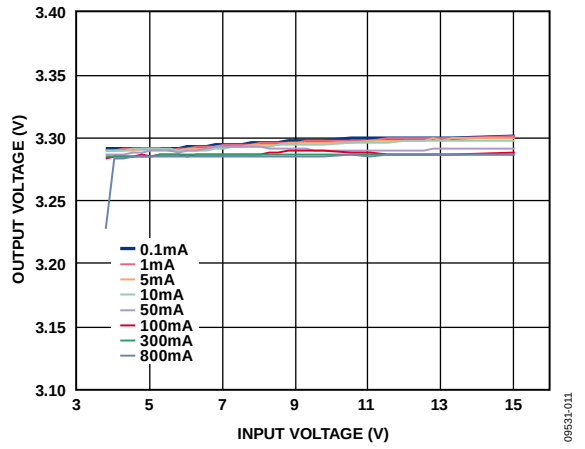

Figure 11. Line Regulation, V_{OUT} = 3.3 V, Different Loads

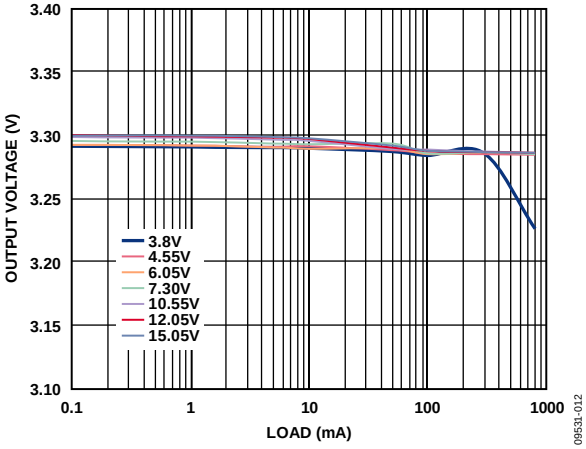

Figure 12. Load Regulation, V_{OUT} = 3.3 V

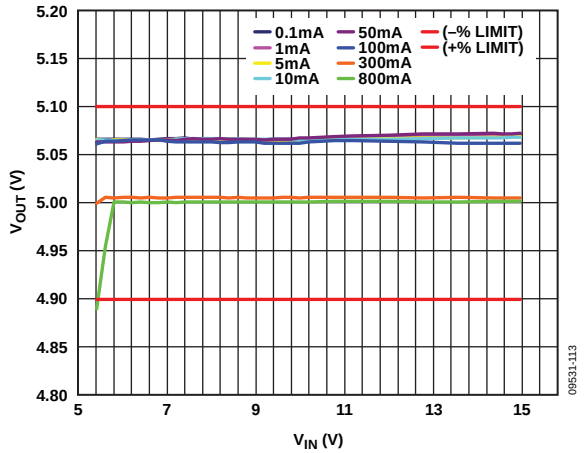

Figure 13. Line Regulation, V_{OUT} = 5.0 V, Different Loads

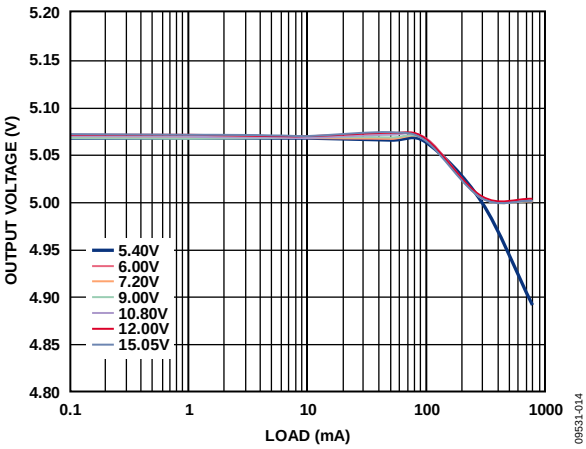

Figure 14. Load Regulation, V_{OUT} = 5.0 V

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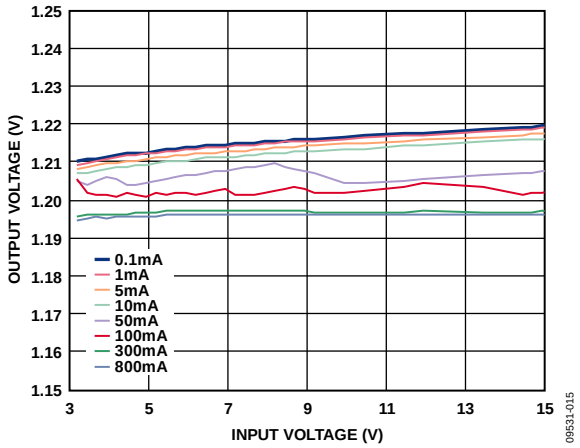

Figure 15. Line Regulation, V_{OUT} = 1.2 V, Different Loads

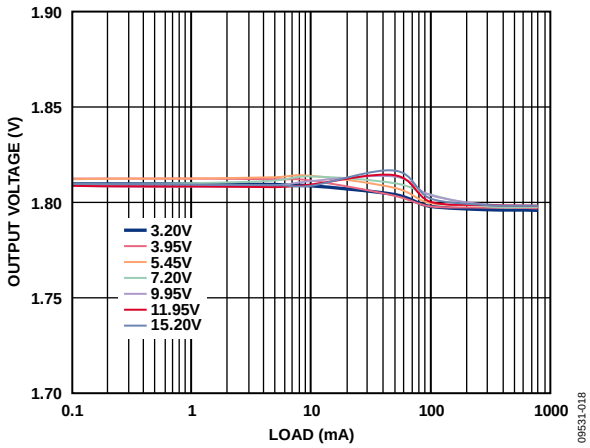

Figure 18. Load Regulation, V_{OUT} = 1.8 V

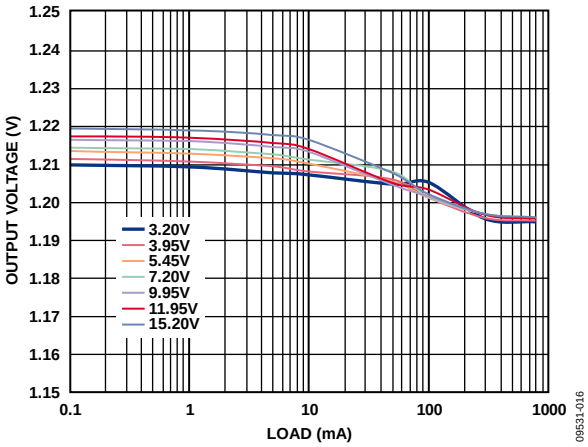

Figure 16. Load Regulation, V_{OUT} = 1.2 V

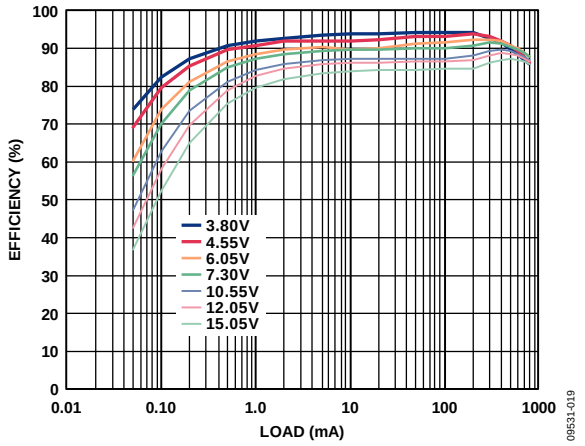

Figure 19. Efficiency vs. Load Current, V_{OUT} = 3.3 V, Different Input Voltages

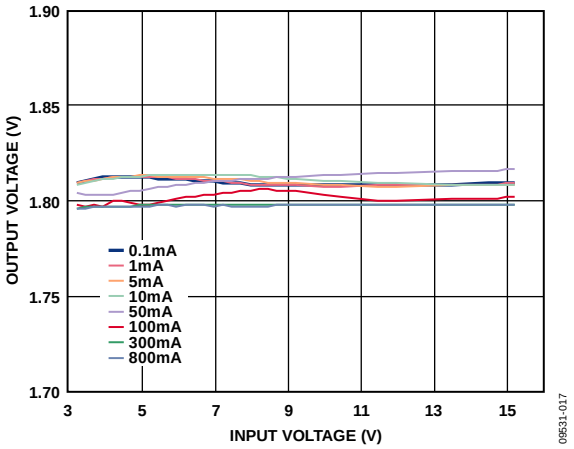

Figure 17. Line Regulation, V_{OUT} = 1.8 V, Different Loads

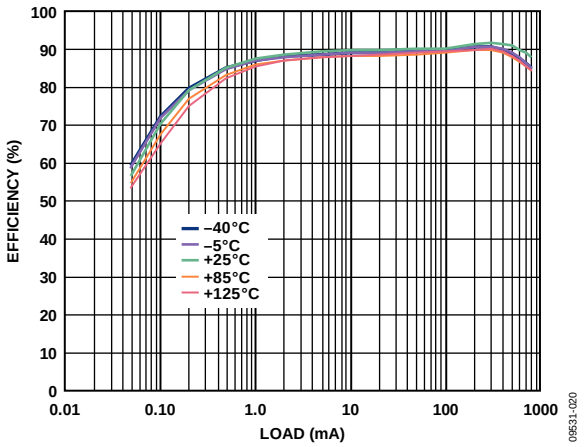

Figure 20. Efficiency vs. Load Current, V_{OUT} = 3.3 V, Different Temperatures, V_{IN} = 7.3 V

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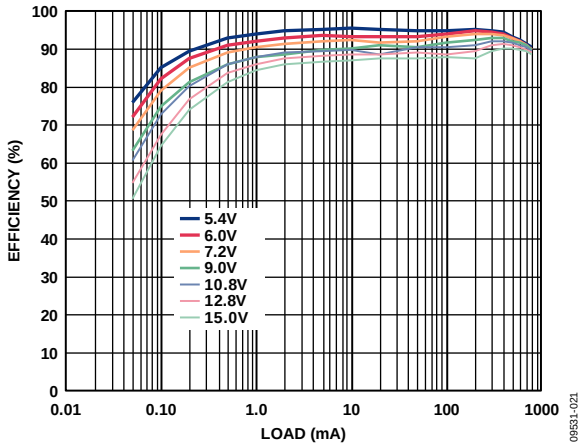

Figure 21. Efficiency vs. Load Current, V_{OUT} = 5.0 V, Different Input Voltages

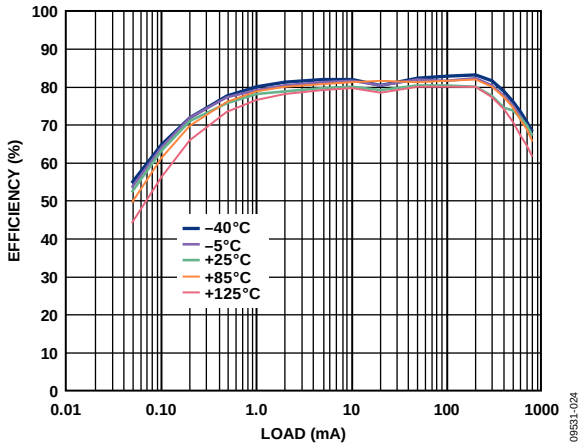

Figure 24. Efficiency vs. Load Current, V_{OUT} = 1.2 V, Different Temperatures, V_{IN} = 4 V

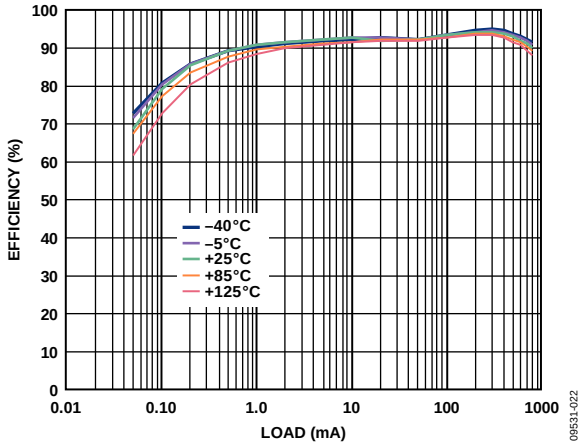

Figure 22. Efficiency vs. Load Current, V_{OUT} = 5.0 V, Different Temperatures

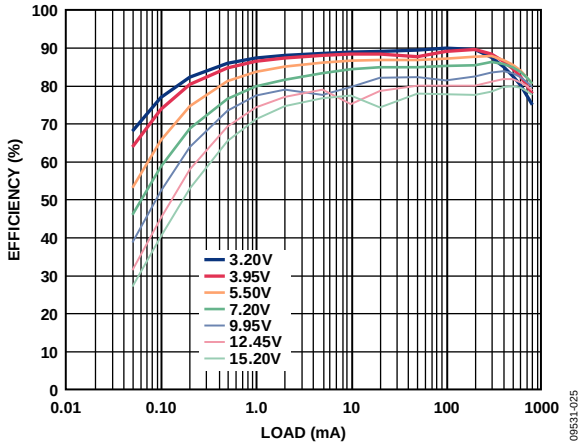

Figure 25. Efficiency vs. Load Current, V_{OUT} = 1.8 V, Different Input Voltages

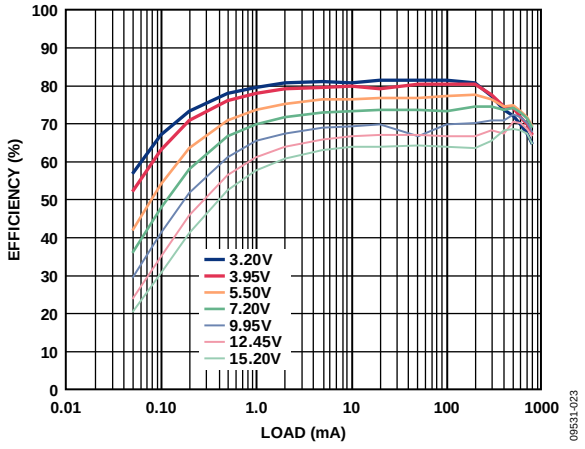

Figure 23. Efficiency vs. Load Current, V_{OUT} = 1.2 V, Different Input Voltages

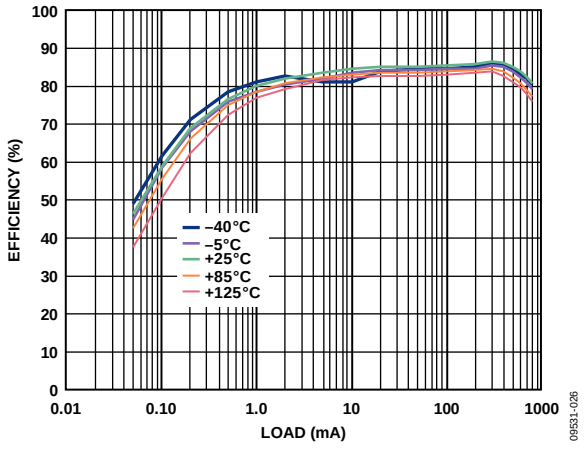

Figure 26. Efficiency vs. Load Current, V_{OUT} = 1.8 V, Different Temperatures, V_{IN} = 4 V

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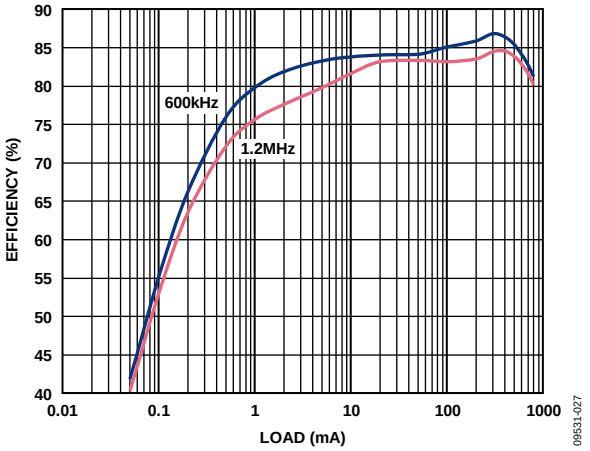

Figure 27. Efficiency vs. Load Current, Different Switching Frequency, V_{OUT} = 1.8 V, V_{IN} = 9 V

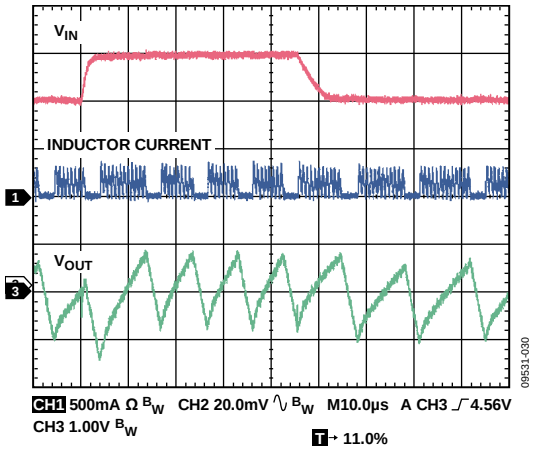

Figure 30. Line Transient, V_{OUT} = 1.2 V, PSM Mode, 100 mA, V_{IN1} = 4 V to 5 V, 2 µs Rise Time, C_{IN} = 3.3 µF

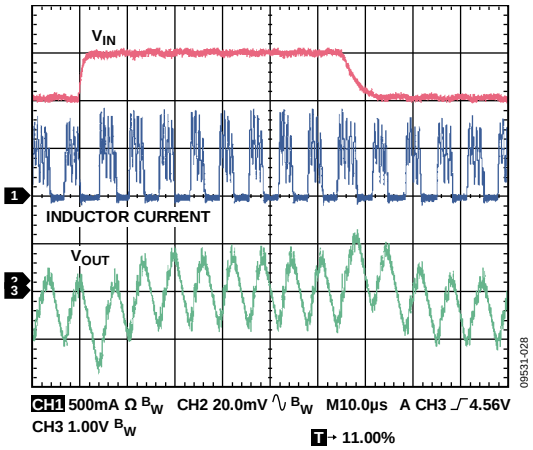

Figure 28. Line Transient, V_{OUT} = 1.8 V, PSM Mode, 100 mA, V_{IN1} = 4 V to 5 V, 2 µs Rise Time, C_{IN} = 3.3 µF

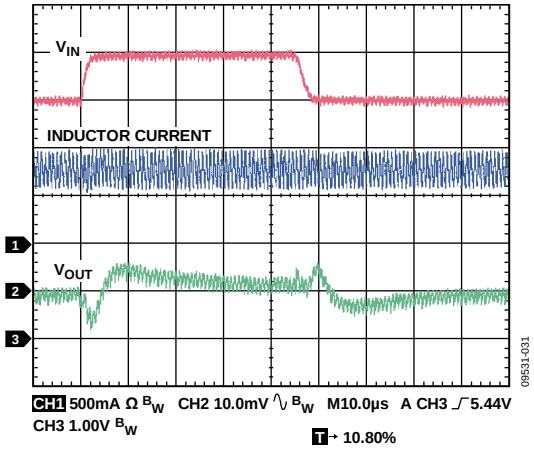

Figure 31. Line Transient, V_{OUT} = 1.2 V, PWM Mode, 800 mA, V_{IN1} = 4 V to 5 V, 2 µs Rise Time, C_{IN} = 3.3 µF

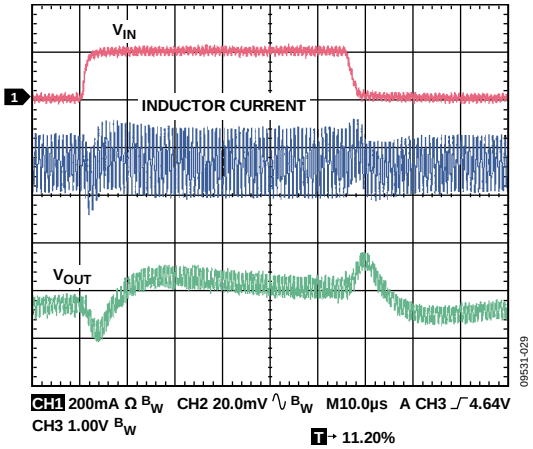

Figure 29. Line Transient, V_{OUT} = 1.8 V, PWM Mode, 800 mA, V_{IN1} = 4 V to 5 V, 2 µs Rise Time, C_{IN} = 3.3 µF

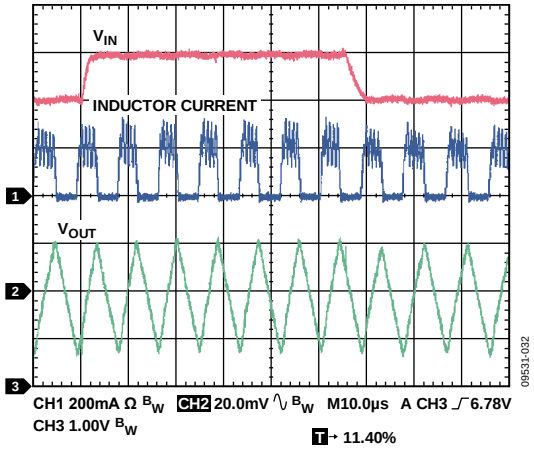

Figure 32. Line Transient, V_{OUT} = 3.3 V, PSM Mode, 100 mA, V_{IN1} = 6 V to 7 V, 2 µs Rise Time, C_{IN} = 3.3 µF

Downloaded from Arrow.com.

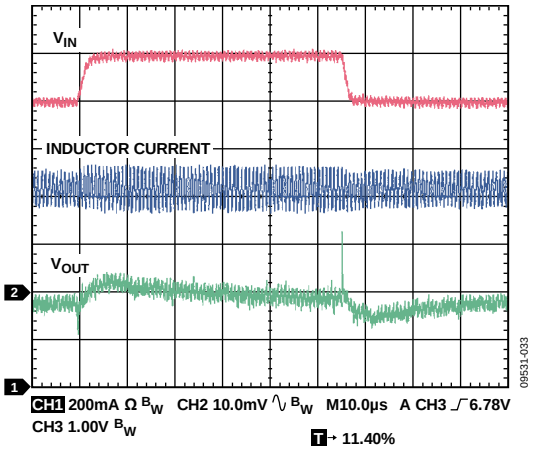

Figure 33. Line Transient, V_{OUT} = 3.3 V, PWM Mode, 800 mA, V_{IN1} = 6 V to 7 V, 2 µs Rise Time, C_{IN} = 3.3 µF

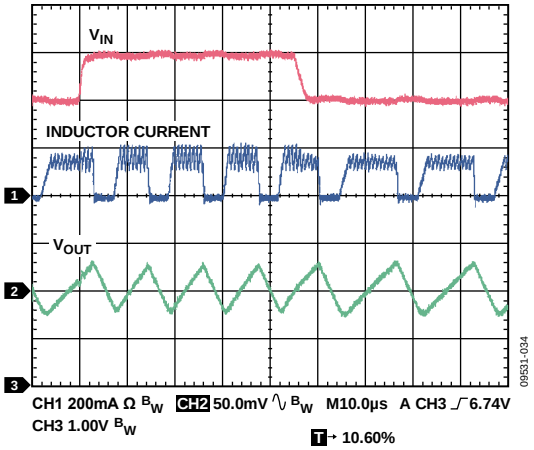

Figure 34. Line Transient, V_{OUT} = 5 V, PSM Mode, 100 mA, V_{IN1} = 6 V to 7 V, 2 µs Rise Time, C_{IN} = 3.3 µF

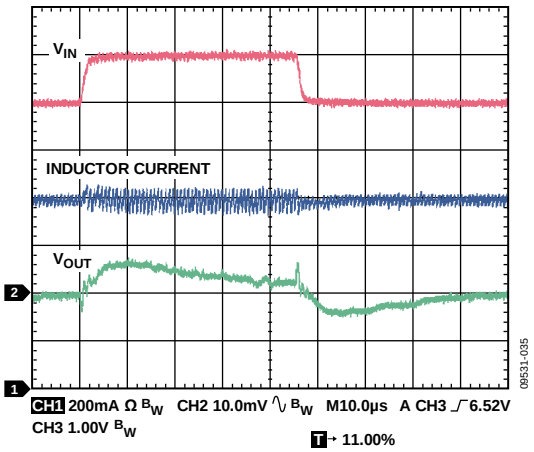

Figure 35. Line Transient, V_{OUT} = 5 V, PWM Mode, 800 mA, V_{IN1} = 6 V to 7 V, 2 µs Rise Time, C_{IN} = 3.3 µF

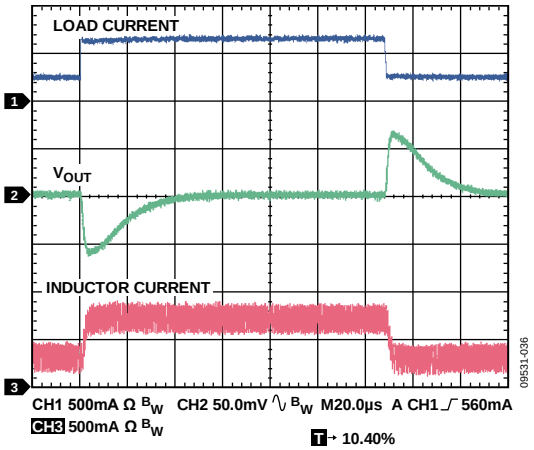

Figure 36. Load Transient, V_{OUT} = 1.8 V, 300 mA to 800 mA, Load Current Rise Time = 200 ns

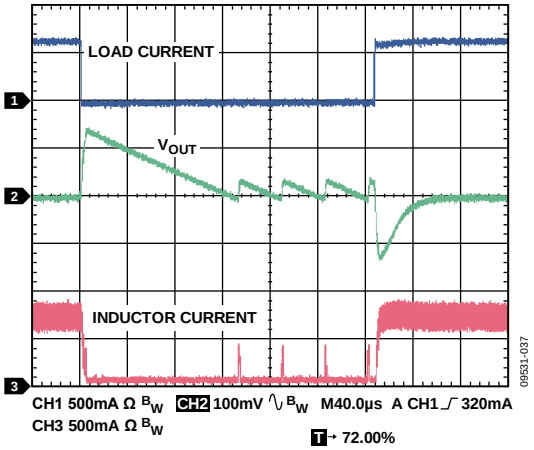

Figure 37. Load Transient, V_{OUT} = 1.8 V, 10 mA to 800 mA, Load Current Rise Time = 200 ns

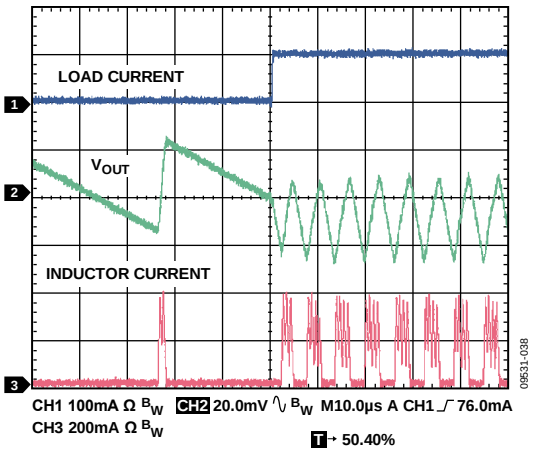

Figure 38. Load Transient, V_{OUT} = 1.8 V,10 mA to 110 mA, Load Current Rise Time = 200 ns

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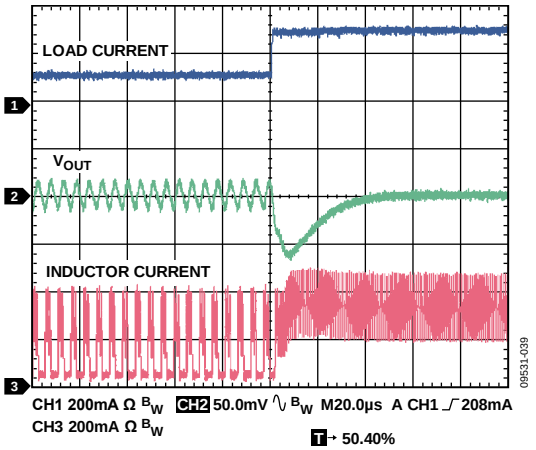

Figure 39. Load Transient, V_{OUT} = 1.8 V,100 mA to 300 mA, Load Current Rise Time = 200 ns

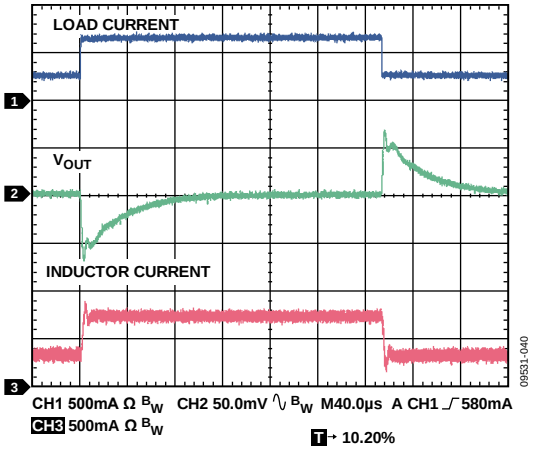

Figure 40. Load Transient, V_{OUT} = 3.3 V, 300 mA to 800 mA, Load Current Rise Time = 200 ns

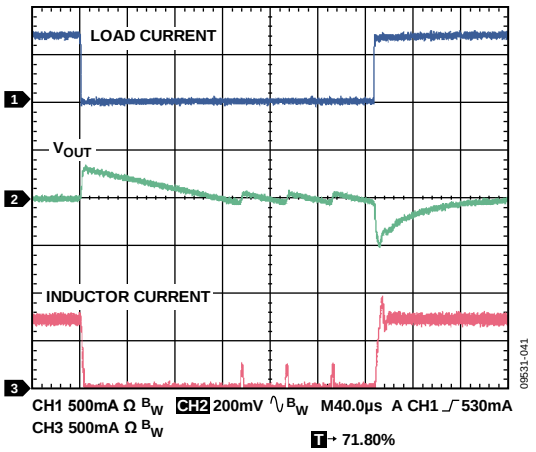

Figure 41. Load Transient, V_{OUT} = 3.3 V, 10 mA to 800 mA, Load Current Rise Time = 200 ns

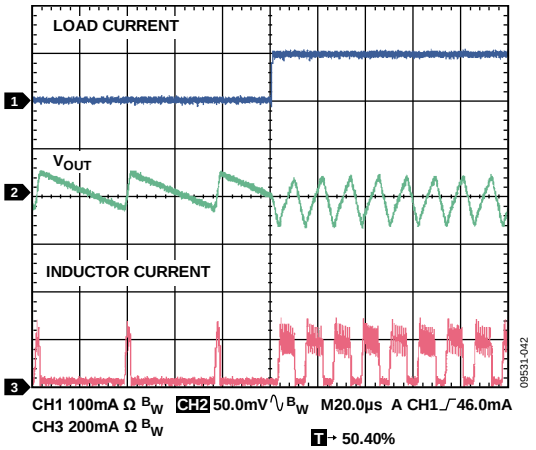

Figure 42. Load Transient, V_{OUT} = 3.3 V, 10 mA to 110 mA, Load Current Rise Time = 200 ns

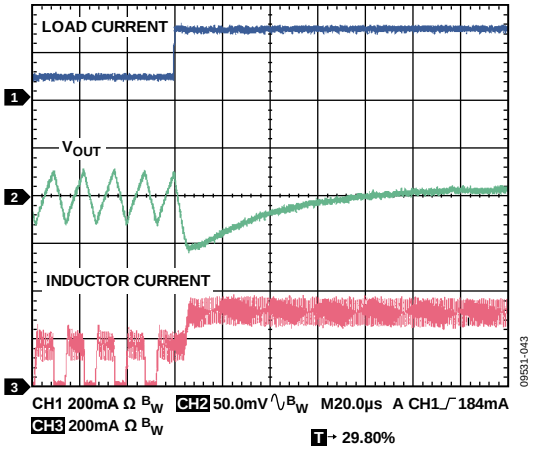

Figure 43. Load Transient, V_{OUT} = 3.3 V, 100 mA to 300 mA, Load Current Rise Time = 200 ns

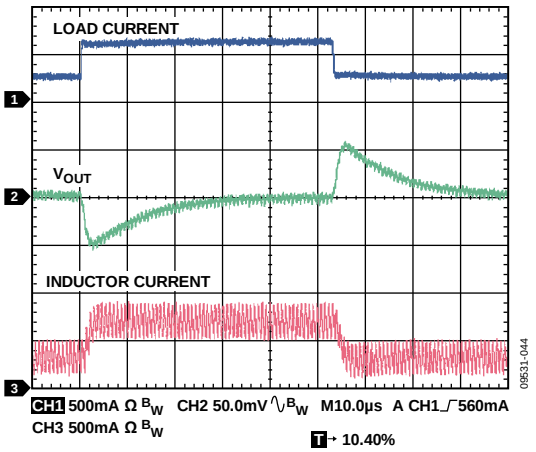

Figure 44. Load Transient, V_{OUT} = 1.2 V, 300 mA to 800 mA, Load Current Rise Time = 200 ns, V_{IN} = 5 V

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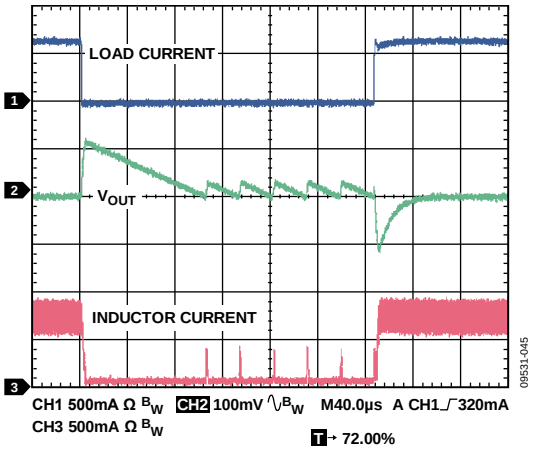

Figure 45. Load Transient, V_{OUT} = 1.2 V, 10 mA to 800 mA, Load Current Rise Time = 200 ns, V_{IN} = 5 V

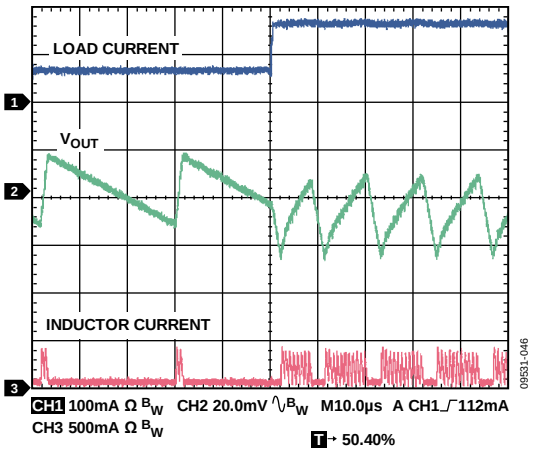

Figure 46. Load Transient, V_{OUT} = 1.2 V,10 mA to 110 mA, Load Current Rise Time = 200 ns, V_{IN} = 5 V

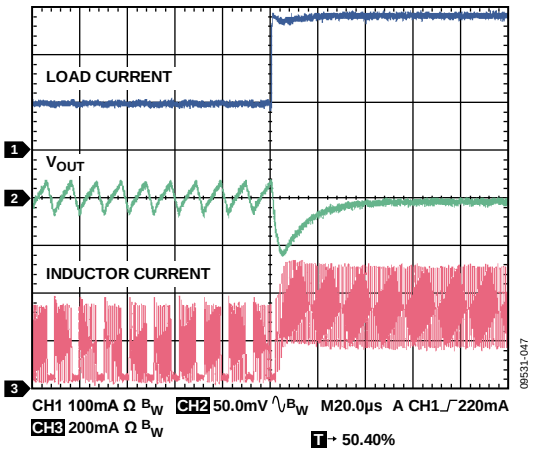

Figure 47. Load Transient, V_{OUT} = 1.2 V,100 mA to 300 mA, Load Current Rise Time = 200 ns, V_{IN} = 5 V

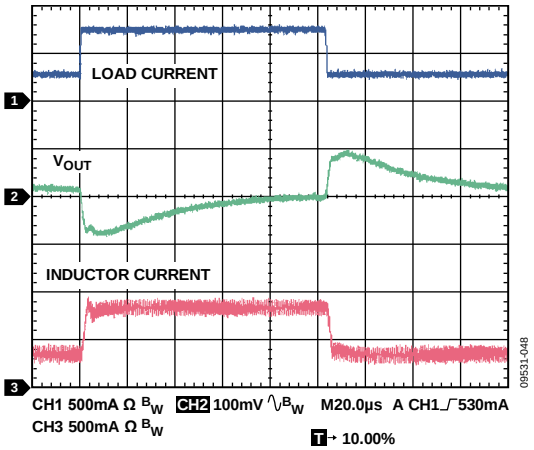

Figure 48. Load Transient, V_{OUT} = 5 V, 300 mA to 800 mA, Load Current Rise Time = 200 ns, V_{IN} = 8 V

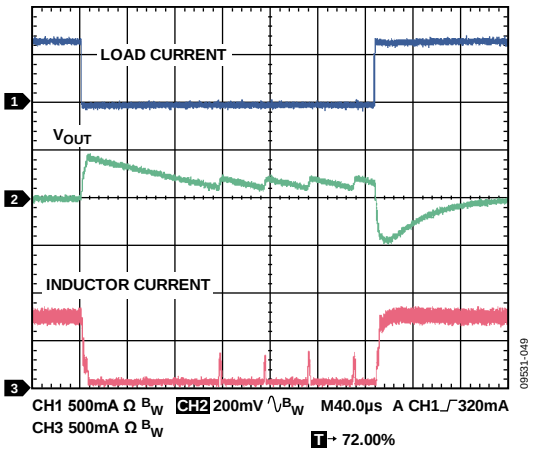

Figure 49. Load Transient, V_{OUT} = 5 V, 1 mA to 800 mA, Load Current Rise Time = 200 ns, V_{IN} = 8 V

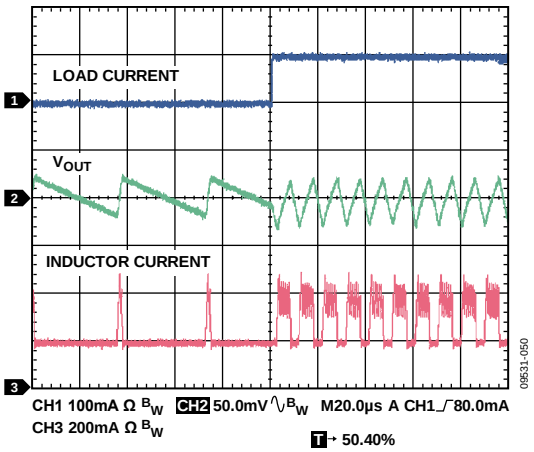

Figure 50. Load Transient, V_{OUT} = 5 V,10 mA to 110 mA, Load Current Rise Time = 200 ns, V_{IN} = 8 V

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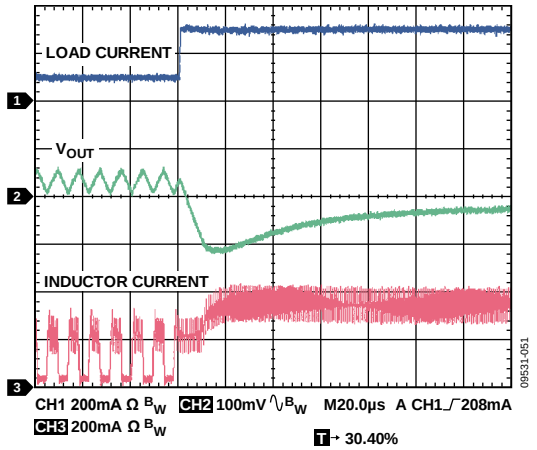

Figure 51. Load Transient, V_{OUT} = 5 V, 100 mA to 300 mA, Load Current Rise Time = 200 ns, V_{IN} = 8 V

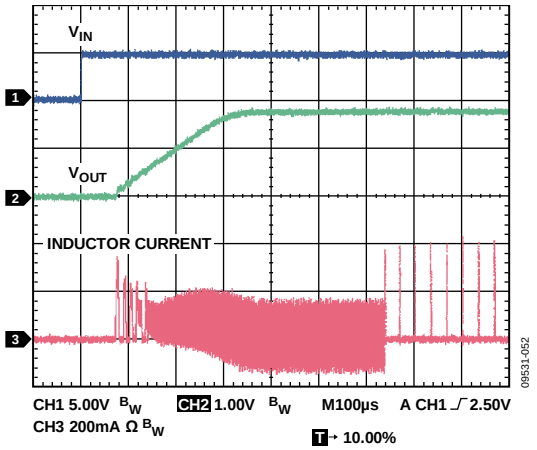

Figure 52. Startup, V_{OUT} = 1.8 V, 10 mA

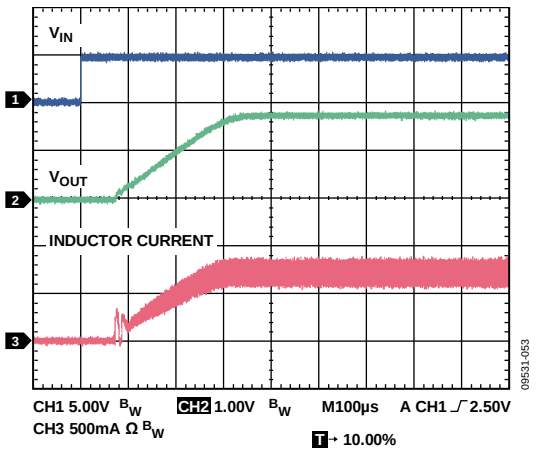

Figure 53. Startup, V_{OUT} = 1.8 V, 800 mA

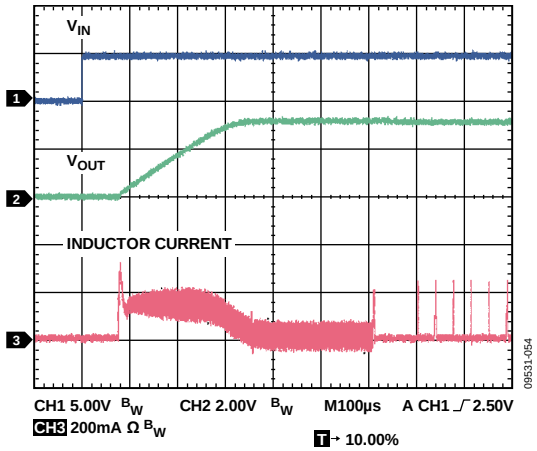

Figure 54. Startup, V_{OUT} = 3.3 V, 10 mA

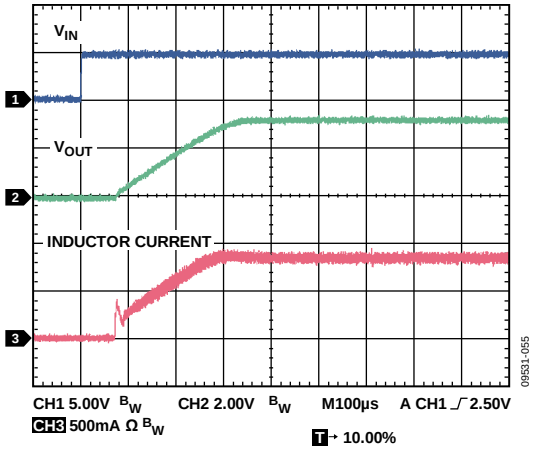

Figure 55. Startup, V_{OUT} = 3.3 V, 800 mA

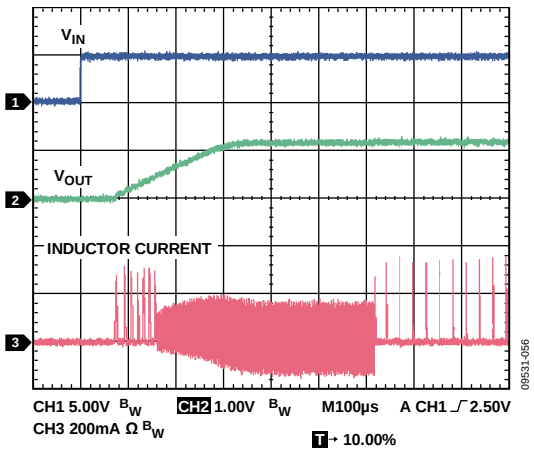

Figure 56. Startup, V_{OUT} = 1.2 V, 10 mA, V_{IN} = 5 V

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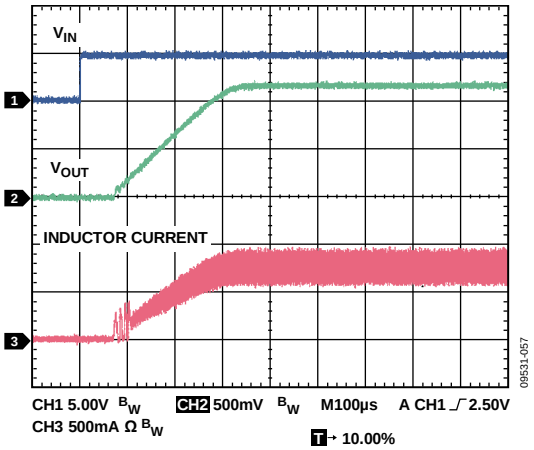

Figure 57. Startup, V_{OUT} = 1.2 V, 800 mA, V_{IN} = 5 V

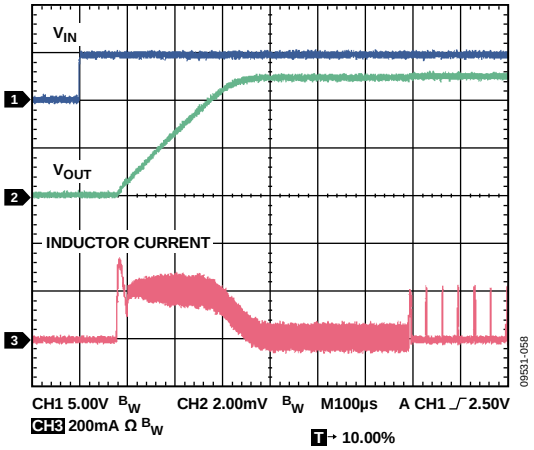

Figure 58. Startup, V_{OUT} = 5 V, 10 mA, V_{IN} = 7 V

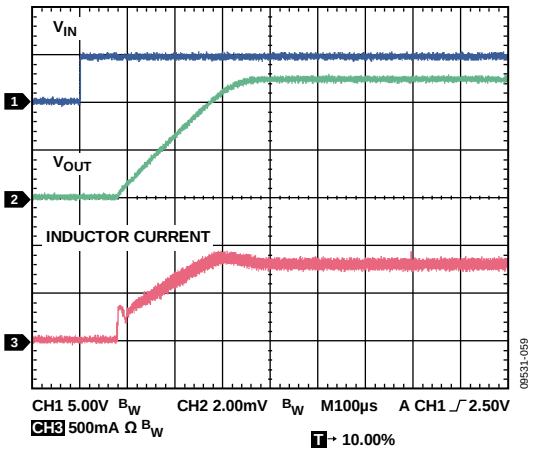

Figure 59. Startup, V_{OUT} = 5 V, 800 mA, V_{IN} = 7 V

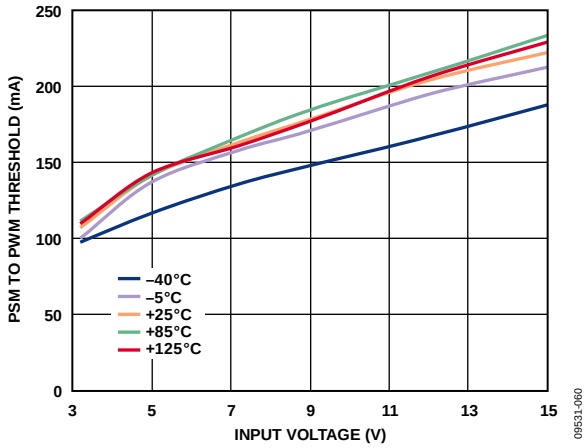

Figure 60. PSM to PWM Mode Transition vs. Input Voltage, Different Temperatures

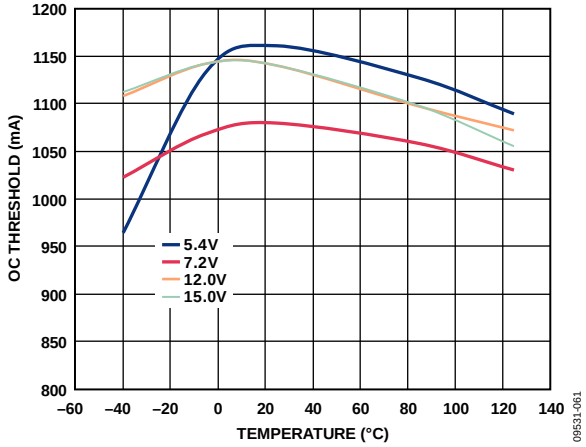

Figure 61. Overcurrent Limit vs. Temperature, V_{OUT} = 5 V, Different Input Voltages

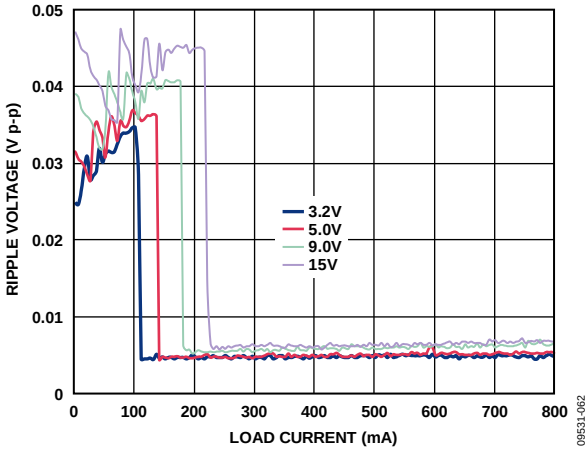

Figure 62. Output Ripple vs. Load Current, V_{OUT} = 1.2 V, Different Input Voltages, Automatic Mode

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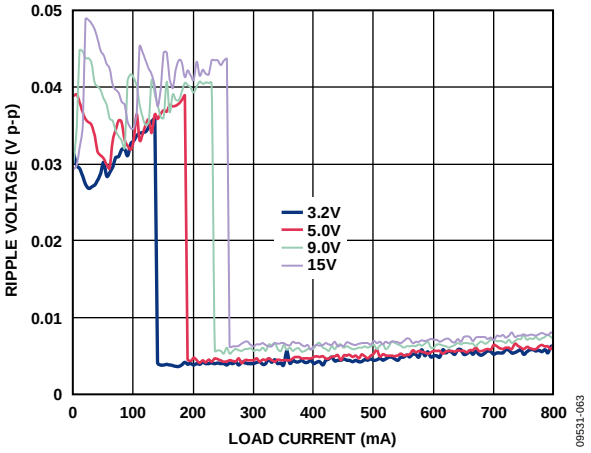

Figure 63. Output Ripple vs. Load Current, V_{OUT} = 1.8 V, Different Input Voltages, Automatic Mode

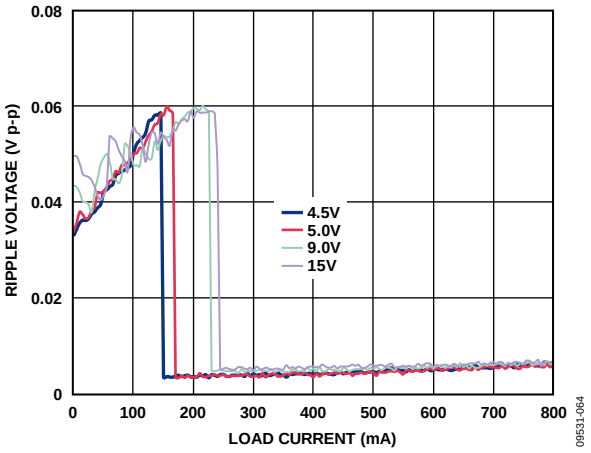

Figure 64. Output Ripple vs. Load Current, V_{OUT} = 3.3 V, Different Input Voltages, Automatic Mode

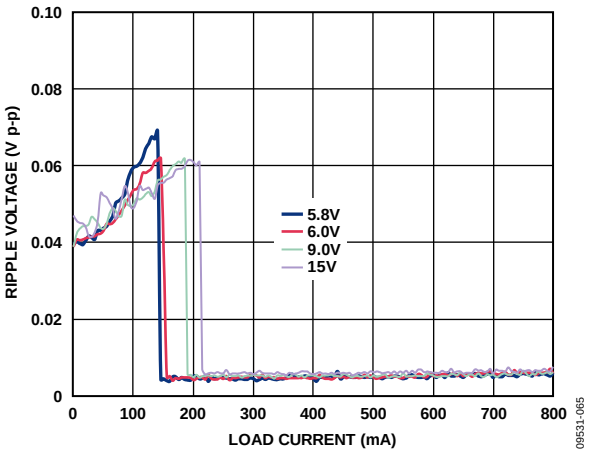

Figure 65. Output Ripple vs. Load Current, V_{OUT} = 5 V, Different Input Voltages, Automatic Mode

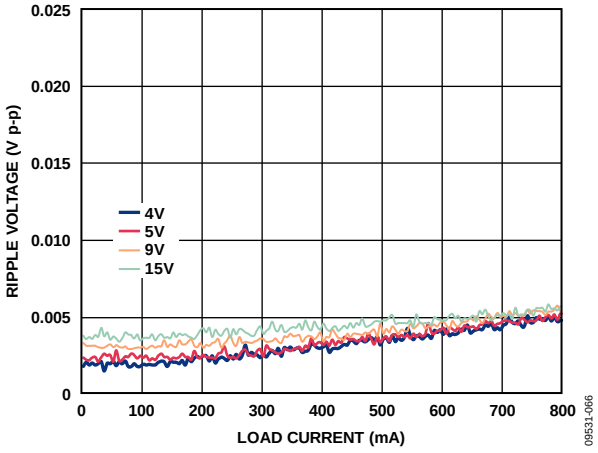

Figure 66. Output Ripple vs. Load Current, V_{OUT} = 3.3 V, Different Input Voltages, Force PWM Mode

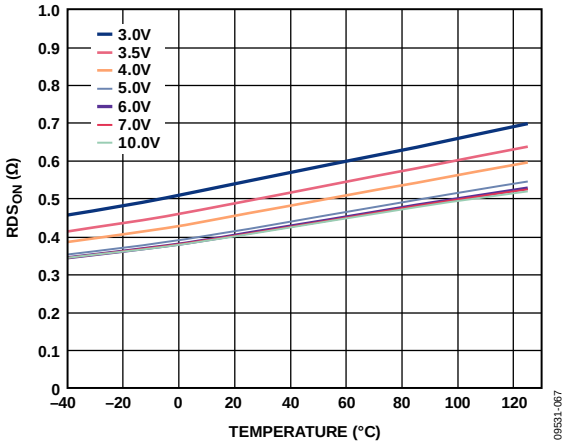

Figure 67. PMOS RDS_{ON} vs. Temperature at 400 mA, Different Input Voltages

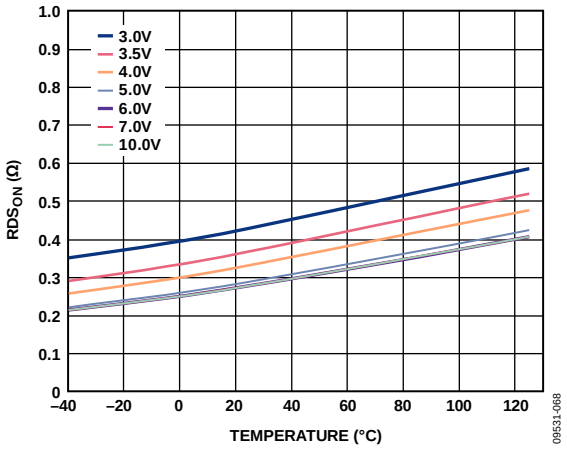

Figure 68. NMOS RDS_{ON} vs. Temperature at 400 mA, Different Input Voltages

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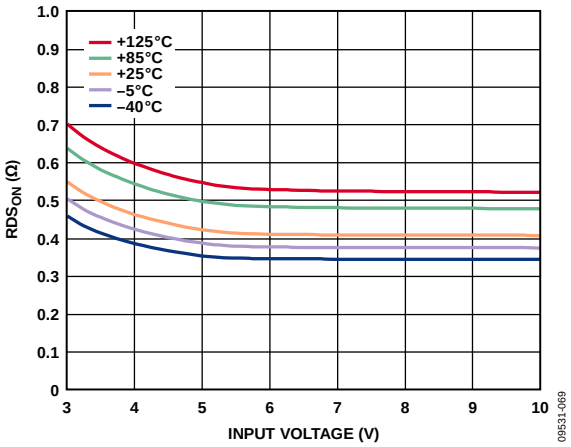

Figure 69. PMOS RDS_{ON} vs. Input Voltage at 400 mA, Different Temperatures

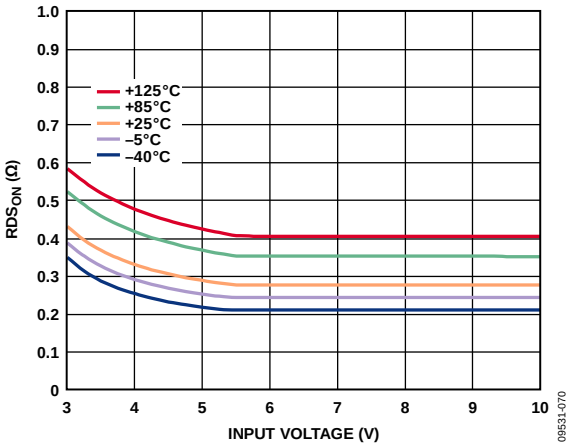

Figure 70. NMOS RDS_{ON} vs. Input Voltage at 400 mA, Different Temperatures

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THEORY OF OPERATION

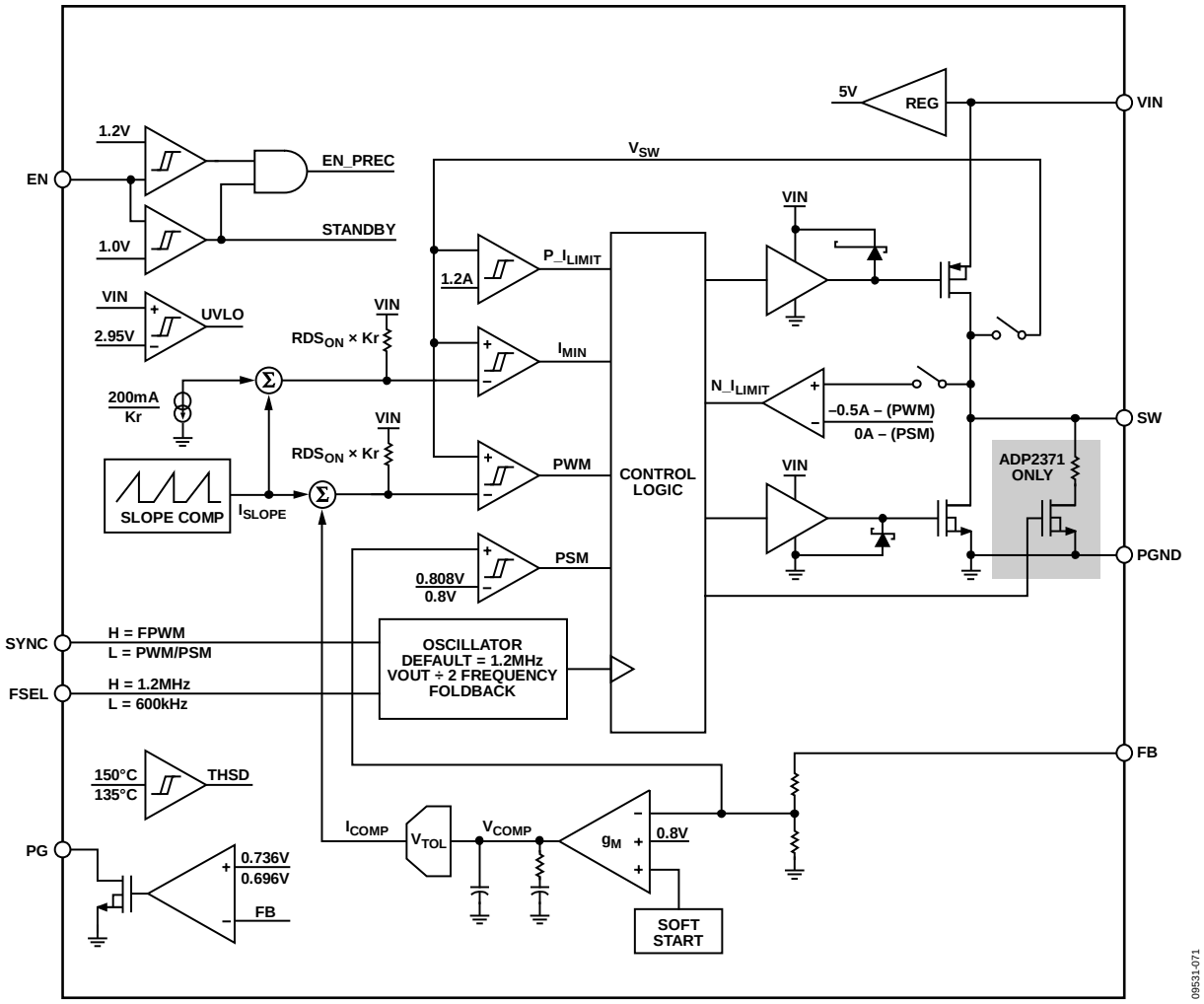

Figure 71. Functional Block Diagram

The ADP2370/ADP2371 use a high speed, current mode, constant frequency PWM control scheme for excellent stability and transient response. To ensure the longest battery life in portable applications, the ADP2370/ADP2371 has a power saving mode. Under light load conditions, the output capacitor is charged as needed to maintain regulation; otherwise, the ADP2370/ADP2371 enter sleep mode, a low 14 µA quiescent state. The architecture ensures smooth transitions from PWM mode to and from PSM, and maintains high efficiencies at light loads. The following sections describe the two modes of operation and provide detailed descriptions of the ADP2370/ADP2371 features.

PWM OPERATION

The ADP2370/ADP2371 PWM mode is a fixed frequency, 1.2 MHz typical, current mode architecture. Use the SYNC pin to synchronize the regulator to an external clock frequency or use the FSEL pin to select an internal clock frequency of 600 kHz or 1.2 MHz.

The ADP2370/ADP2371 use a constant slope compensation scheme where the inductor scales with the output voltage. The equation for choosing the inductor for a particular output voltage is

$$L = \frac{1.2 \times V_{OUT}}{0.478 \times f_{SW}}$$

See the Applications Information section for details regarding choosing an appropriate inductor value.

Cycle to cycle operation of the PWM mode begins with the falling edge of the internal clock. Note that when using an external clock, the rising edge synchronizes the regulator and the falling edge is determined by the internal clock, typically a 25 ns pulse width. The falling edge of the clock starts the cycle by turning on the high-side switch, which produces a positive di/dt current in the inductor. The PWM comparator controls when the high-side switch turns off. The positive input of the comparator monitors the peak inductor current via the SW node.

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The negative side of the comparator input voltage is set by the voltage control loop minus the slope compensation. When the high-side switch turns off, the low-side switch turns on for the remainder of the clock period.

While in PWM/PSM mode, the low-side switch turns off when the inductor current reaches zero, operating in discontinuous conduction (DCC) mode. If SYNC is tied high to force the device into PWM only mode, the low-side switch stays on until the next clock cycle or until the inductor current reaches the negative current limit.

PSM OPERATION

The ADP2370/ADP2371 smoothly transition to the variable frequency PSM operation. The ADP2370/ADP2371 select a minimum current value, I_{MIN}, for the peak current of the inductor based on the input and output voltages. The design of the I_{MIN} value is based on the recommended inductor values. Deviating from the recommended inductor value for a particular output voltage results in shifting the PSM to PWM threshold and could result in the device entering DCC mode.

As long as the required peak inductor current is above I_{MIN}, the regulator remains in PWM mode. As the load decreases, the PSM circuitry prevents the peak inductor current from dropping below the PSM peak current value. This circuitry causes the regulator to supply more current to the output filter than the load requires, resulting in the output voltage increasing and the output of the internal compensation node of the error amplifier, V_{COMP}, decreasing.

When the FB pin voltage rises above 1% of the nominal output voltage and the V_{COMP} node voltage is below a predetermined PSM threshold voltage level, the regulator enters sleep mode. While in sleep mode, the high-side and low-side switches and a majority of the circuitry are disabled to allow for a low sleep mode quiescent current as well as high efficiency performance.

During sleep mode, the output voltage decreases as the output capacitor discharges into the load. Fixed frequency operation starts when the FB voltage reaches the nominal output voltage. When the load requirement increases past the I_{MIN} peak current level, the V_{COMP} node rises and the PWM control loop sets the duty cycle. While the part is entering and exiting sleep mode, the PSM voltage ripple is larger than 1% because of the delay in the comparators.

Figure 72 and Figure 73 illustrate how the output voltage and inductor current change with loads and transitions in and out of PSM operation. The output voltage ripple in PSM is ~40 mV p-p, and the ripple in PWM is <10 mV p-p.

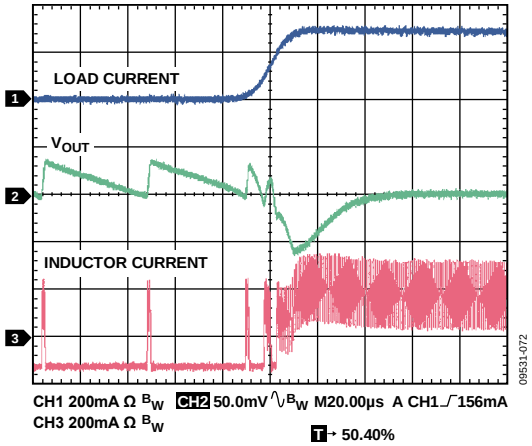

Figure 72. PSM to PWM Transition Waveforms, V_{OUT} = 1.8 V, 10 mA Load to 300 mA Load

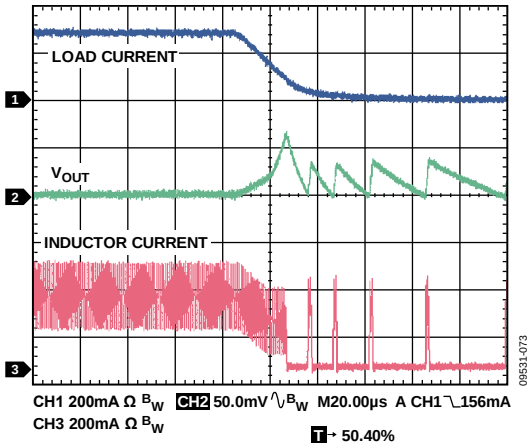

Figure 73. PWM to PSM Transition Waveforms, V_{OUT} = 1.8 V, 300 mA Load to 10 mA Load

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FEATURES DESCRIPTIONS

PRECISION ENABLE

The enable circuit of the ADP2370/ADP2371 minimizes the input current during shutdown and simultaneously provides an accurate enable threshold. When the enable input voltage is below 400 mV, the regulators are in shutdown mode and the supply current is typically 1.2 µA. As the enable input voltage rises above the standby enable threshold of 1.0 V, the internal bias currents and voltages are activated, turning on the precision enable circuitry. This allows the precision enable circuitry to detect accurately when the EN pin voltage exceeds the precision enable rising threshold of 1.2 V.

FORCED PWM OR PWM/PSM SELECTION

Connecting the SYNC pin to a voltage greater than 1.2 V forces the device to operate permanently in the PWM mode. This means that the ADP2370/ADP2371 continue to operate at a fixed frequency even when the output current is less than the PWM/PSM threshold. In PWM mode, the efficiency is lower compared to the PSM mode during light loads. The low-side NMOS remains on when the output current drops to less than zero thereby preventing the device from entering discontinuous conduction (DCC) mode.

It is possible to switch from FPWM mode to the power-save mode during operation by pulling the SYNC pin low. The flexible configuration of the SYNC pin during operation of the device allows for efficient power management.

Connecting the SYNC pin to a voltage less than 0.4 V allows the part to operate in either PWM or PSM modes, depending on the output current. Whenever the average output current goes below the PWM/PSM threshold, the ADP2370/ADP2371 enter PSM mode operation. During PSM mode the part operates with reduced switching frequency and with a minimal quiescent current to maintain high efficiency. The low-side NMOS turns off when the output current reaches zero, causing the part to operate in DCC mode.

QUICK OUTPUT DISCHARGE (QOD) FUNCTION

The ADP2371 includes an output discharge resistor that forces the output voltage to zero when the buck is disabled. This ensures that the output of the buck is always in a well-defined state, whether or not it is enabled. The ADP2370 does not include this output discharge function.

SHORT-CIRCUIT PROTECTION

The ADP2370/ADP2371 include frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below 0.3 V, indicating the possibility of a hard short at the output, the switching frequency is reduced to 1/4 of the internal oscillator frequency. The reduction in the switching frequency gives more time for the inductor to discharge, preventing a runaway of output current.

UNDERVOLTAGE LOCKOUT

To protect against battery discharge, an undervoltage lockout (UVLO) circuit is incorporated into the ADP2370/ADP2371. When the input voltage drops below the UVLO threshold, the ADP2370/ADP2371 shuts down, and both the power switch and synchronous rectifier turn off. Once the input voltage rises above the UVLO threshold, the soft start period is initiated and the device is enabled.

THERMAL PROTECTION

In the event that the junction temperature on either the ADP2370 or ADP2371 rises above 150°C, the thermal shutdown protection circuit turns off the regulator. Extreme junction temperature can be the result of high current operation, poor circuit board design, and/or high ambient temperature. A 20°C hysteresis is included in the protection circuit so that when a thermal shutdown occurs, the device does not return to operation until the on-chip temperature drops below 130°C. When exiting a thermal shutdown, soft start is initiated.

SOFT START

The ADP2370/ADP2371 have an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter. Typical soft start time is 350 µs. The ADP2370/ADP2371 are also capable of starting up into a precharged output capacitor. If soft start is invoked when the output capacitor charge is greater than zero, the device delays the start of switching until the internal soft start ramp reaches the corresponding FB voltage. This feature prevents discharging the output capacitor at the beginning of soft start.

CURRENT LIMIT

The ADP2370/ADP2371 have protection circuitry that limits the direction and amount of current to 1200 mA that flows through the power switch and synchronous rectifier, cycle by cycle. The positive current limit on the power switch limits the amount of current that can flow from the input to the output. The negative current limit on the synchronous rectifier prevents the inductor current from reversing direction and flowing out of the load.

A negative current limit is provided by the ADP2370/ADP2371 to prevent an excessive reverse inductor current when the switching section sinks current from the load in forced continuous conduction mode. Under negative current-limit conditions, both the high-side and low-side switches are disabled.

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100% DUTY CYCLE

The ADP2370/ADP2371 enter and exit 100% duty cycle smoothly. The control loop seeks the next clock cycle while the high-side switch is engaged. When this occurs, the clock signal is masked and the PMOS remains on. When the input voltage increases, the internal V_{COMP} node decreases its signal to the control loop; thus, the device stops skipping clock cycles and exits 100% duty cycle.

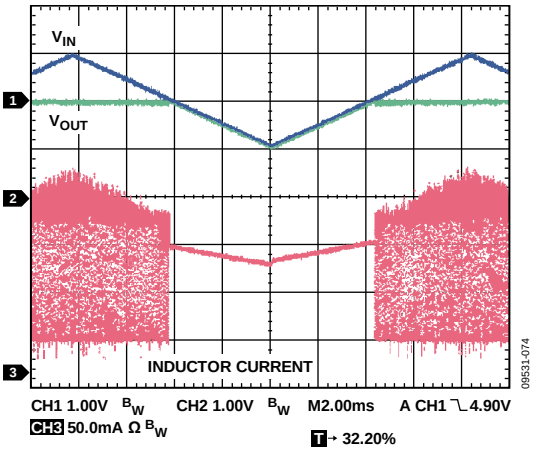

Figure 74. Transition into and out of Dropout in PSM Mode, V_{OUT} = 5 V, 100 mA Load

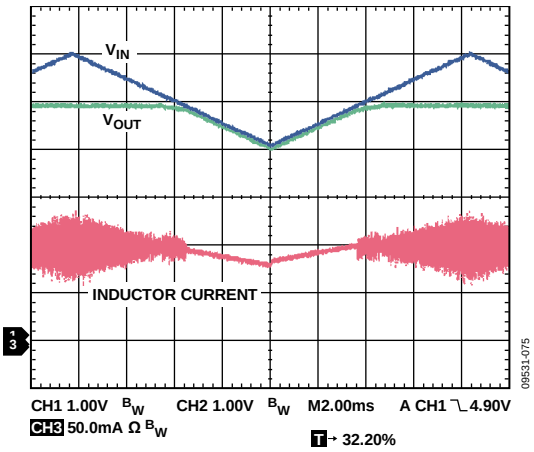

Figure 75. Transition into and out of Dropout in PWM Mode, V_{OUT} = 5 V, 100 mA Load

SYNCHRONIZING

It is possible to synchronize the ADP2370/ADP2371 to an external clock within a frequency range from 400 kHz to 1.6 MHz. The device automatically detects the rising edge of the first clock and synchronizes to the external clock. When the clock signal stops, the device automatically switches back to the internal clock and continues operating.

The switchover is initiated when no rising edge on the SYNC pin can be detected on the internal clock for a duration of four clock cycles. Therefore, the maximum delay time can be 6.7 µs if the internal clock is running at its minimum frequency of 600 kHz. During this time, there is no clock signal available. The output stops switching until the ADP2370 circuitry switches to the internal clock signal.

If the device is synchronized to an external clock, the PSM mode is disabled and the device stays in forced PWM mode. Connect FSEL to ground when synchronizing to a frequency range from 400 kHz to 800 kHz, and connect FSEL to the input voltage when the external frequency is in the range of 800 kHz to 1600 kHz. FSEL has an internal pull-down resistor and defaults to the 600 kHz mode when FSEL is unconnected.

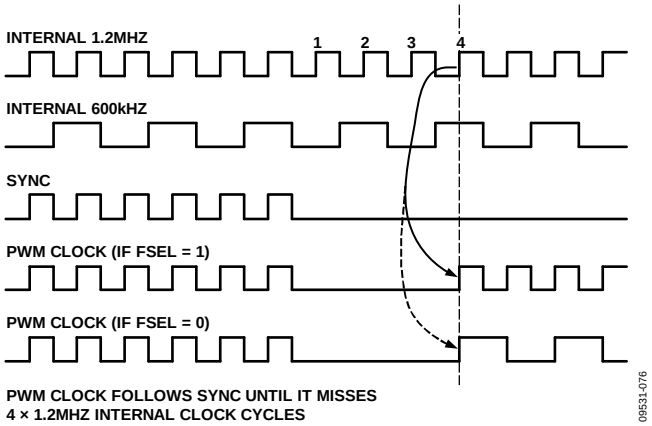

Figure 76. Typical SYNC Timing

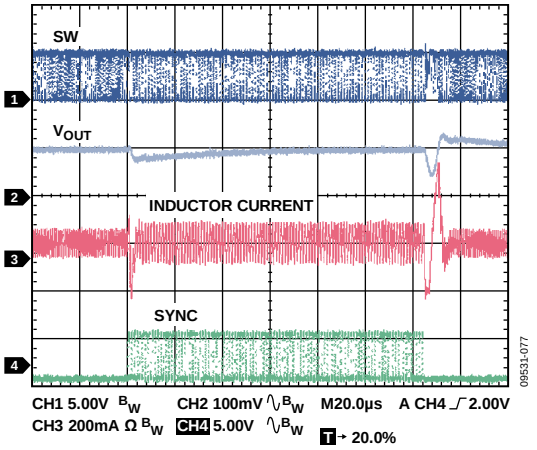

Figure 77. Typical SYNC Transient, 1.2 MHz to 800 kHz to 1.2 MHz

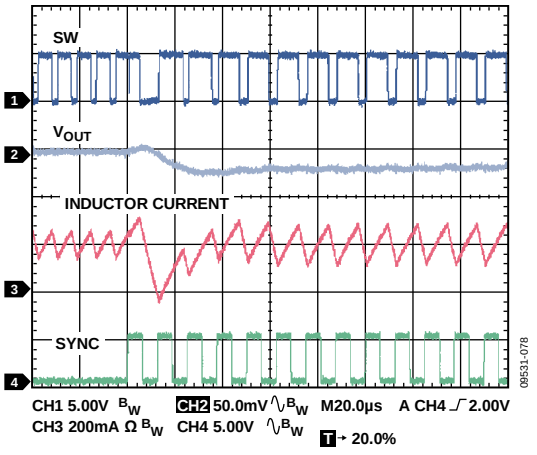

Figure 78. SYNC Transient 1.2 MHz to 800 kHz

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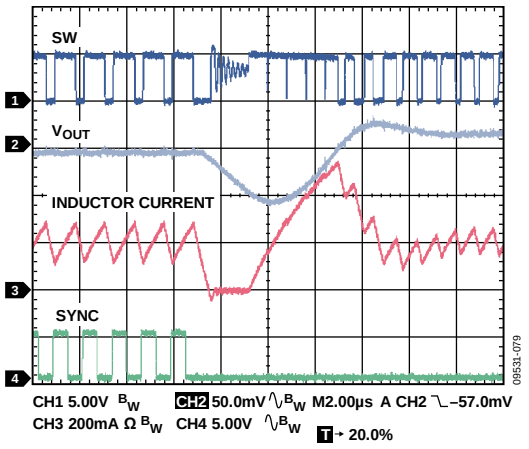

Figure 79. SYNC Transient 800 kHz to 1.2 MHz

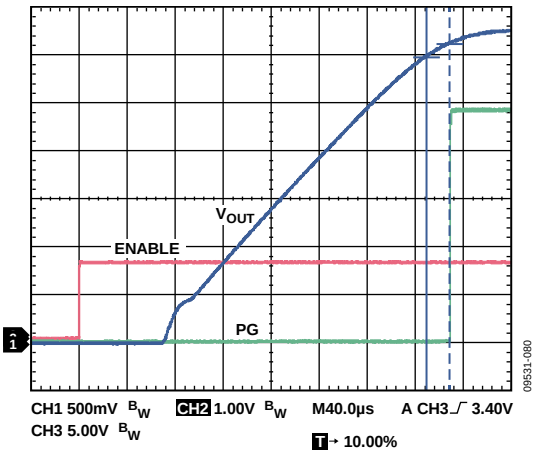

Figure 80. Typical PG Timing at Startup

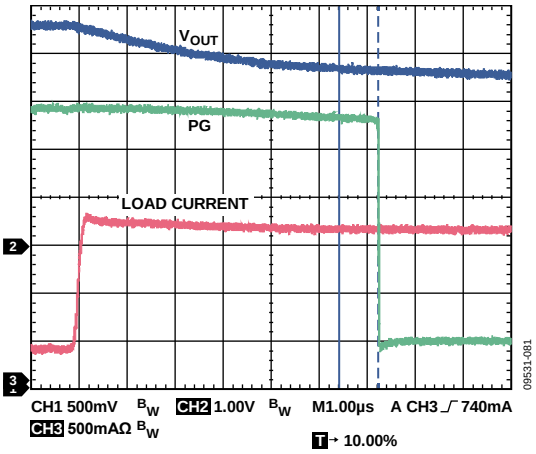

Figure 81. Typical PG Timing with 200 mA to 1100 mA Load Transient

POWER GOOD

The ADP2370/ADP2371 power-good (PG) output indicates the state of the monitored output voltage. The PG function is an active high, open-drain output, requiring an external pull-up resistor that is typically supplied from the I/O supply rail, as shown in Figure 1.

When the sensed output voltage is below 87% of its nominal value, the PG pin is held low. When the sensed output voltage rises above 92% of the nominal level, the PG line is pulled high after t_{RESET}. The PG pin remains high when the sensed output voltage is above 92% of the nominal output voltage level.

The typical PG delay when the buck is in PWM mode is 20 µs. Figure 80 shows the typical PG operation during startup. Figure 81 shows the PG operation when there is a large load transient that causes the output voltage to fall just below the PG threshold.

When not using the PG function, remove the pull-up resistor and leave the PG pin either open or shorted to ground.

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APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

ADP2370/ADP2371 are supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about, and to obtain ADIsimPower design tools, visit www.analog.com/ADIsimPower. Users can also request an unpopulated board through the ADIsimPower tool.

EXTERNAL COMPONENT SELECTION

Table 6 and Table 7 list external component selections for the ADP2370/ADP2371 application circuit shown in Figure 82. The selection of components is dependent on the input voltage, output voltage, and load current requirements. Additionally, trade-offs among performance parameters, such as efficiency and transient response, are made by varying the choice of external components.

SELECTING THE INDUCTOR

The high frequency switching of the ADP2370/ADP2371 allows for the use of small surface-mount power inductors. The inductor value affects the transition from PWM to PSM, efficiency, output ripple, and current-limit values. Use the following equation to calculate the ideal inductance, which is derived from the inductor current slope compensation, for a given output voltage and switching frequency:

$$L = \frac{1.2 \times V_{OUT}}{0.478 \times f_{SW}}$$

The ripple current is calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:
f_{SW} is the switching frequency in MHz (1.2 MHz typical).
L is the inductor value in µH.

The dc resistance (DCR) value of the selected inductor affects efficiency; however, a decrease in this value typically means an increase in root mean square (rms) losses in the core and skin. A minimum requirement of the dc current rating of the inductor is for it to be equal to the maximum load current plus half of the inductor current ripple, as shown by the following equation:

$$I_{PK} = I_{LOAD(MAX)} + \left(\frac{\Delta I_L}{2}\right)$$

OUTPUT CAPACITOR

Output capacitance is required to minimize the voltage overshoot, voltage undershoot, and the ripple voltage present on the output. Capacitors with low equivalent series resistance (ESR) are recommended to produce low output ripple. For a good stability over temperature, use capacitors such as the X5R or X7R dielectric. Do not use Y5V and Z5U capacitors. Y5V and Z5U capacitors are unsuitable choices because of their large capacitance variation over temperature and their dc bias voltage changes. The minimum output capacitance (C_{OUT_MIN}) is determined by the following V_{RIPPLE} and C_{OUT_MIN} equations.

For allowable peak-to-peak output voltage ripple,

$$V_{RIPPLE} \approx \Delta I_L \times (ESR_{COUT} + 1/(8 \times f_{SW} \times C_{OUT_MIN}))$$

Therefore,

$$C_{OUT_MIN} = \Delta I_L/(8 \times f_{SW} \times (V_{RIPPLE} - \Delta I_L \times ESR_{COUT}))$$

where:
V_{RIPPLE} is allowable peak-to-peak output voltage ripple in V.
ΔI_L is the inductor ripple current in A.
ESR_{COUT} is the equivalent series resistance of the capacitor in Ω.
f_{SW} is the converter switching frequency in Hz.

Increasing the output capacitor value has no effect on stability and may reduce output ripple and enhance load transient response. When choosing the output capacitor value, it is important to account for the loss of capacitance due to output voltage dc bias. For recommended 10 µF capacitors, refer to Table 7.

INPUT CAPACITOR

An input capacitor is required to reduce input voltage ripple, input ripple current, and source impedance. Place the input capacitor as close as possible to the VIN pin. A low ESR X7R- or X5R-type capacitor is highly recommended to minimize the input voltage ripple. Use the following equation to determine the rms input current:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

$$I rms \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

ADJUSTABLE OUTPUT VOLTAGE PROGRAMMING

The ADP2370/ADP2371 feature an adjustable output voltage range from 0.8 V to 12 V. The output voltage is set by the ratio of two external resistors, R2 and R3, as shown in Figure 83. The device servos the output to maintain the voltage at the FB pin at 0.8 V, referenced to ground; the current in R2 is then equal to 0.8 V/R3 plus the FB pin bias current. The bias current of the FB pin, 10 nA at 25°C, flows through R2 into the FB pin.

The output voltage is calculated using the equation

$$V_{OUT} = 0.8\ V(1 + R2/R3) + (FB_{I\text{-}BIAS})(R2)$$

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To minimize errors in the output voltage caused by the bias current of the FB pin, maintain a value of R2 that is less than 250 kΩ. For example, when R2 and R3 each equal 250 kΩ, the output voltage is 1.6 V. The output voltage error introduced by the FB pin bias current is 2.5 mV, or 0.156%, assuming a typical FB pin bias current of 10 nA at 25°C.

Note that in shutdown mode, the output is turned off and the divider current is zero.

Select the output inductor and capacitor as described in the Selecting the Inductor, Output Capacitor, and Input Capacitor sections, as well as Table 6 for more information.

EFFICIENCY

Efficiency is defined as the ratio of output power to input power. The high efficiency of the ADP2370/ADP2371 has two distinct advantages. First, only a small amount of power is lost in the dc-to-dc converter package, which in turn, reduces thermal constraints. Second, high efficiency delivers the maximum output power for the given input power, thereby extending battery life in portable applications.

Power Switch Conduction Losses

Power switch dc conduction losses are caused by the flow of output current through the P-channel power switch and the N-channel synchronous rectifier, which have internal resistances ($R_{DS(ON)}$) associated with them. The amount of power loss is approximated by

$$P_{SW_COND} = (R_{DS(ON)_P} \times D + R_{DS(ON)_N} \times (1-D)) \times I_{OUT}^2$$

where:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The internal resistance of the power switches increases with temperature and increases when the input voltage is less than 5.5 V.

Inductor Losses

Inductor conduction losses are caused by the flow of current through the inductor, which has an internal resistance (DCR) associated with it. Larger size inductors have smaller DCR, which can decrease inductor conduction losses. Inductor core losses relate to the magnetic permeability of the core material. Because the ADP2370/ADP2371 are high switching frequency dc-to-dc regulators, shielded ferrite core material is recommended because of its low core losses and low EMI.

To estimate the total amount of power lost in the inductor, use the following equation:

$$P_L = DCR \times I_{OUT}^2 + Core\ Losses$$

Switching Losses

Switching losses are associated with the current drawn by the driver to turn-on and turn-off the power devices at the switching frequency. Each time a power device gate is turned on and turned off, the driver transfers a charge from the input supply to the gate, and then from the gate to ground.

Estimate switching losses using the following equation:

$$P_{SW} = (C_{GATE_P} + C_{GATE_N}) \times V_{IN}^2 \times f_{SW}$$

where:
C_{GATE_P} is the gate capacitance of the internal high-side switch.
C_{GATE_N} is the gate capacitance of the internal low-side switch.
f_{SW} is the switching frequency.

The typical value for gate capacitances, C_{GATE_P} and C_{GATE_N}, is 150 pF.

Transition Losses

Transition losses occur because the P-channel switch cannot turn on or turn off instantaneously. In the middle of an SW node transition, the power switch provides all of the inductor current. The source-to-drain voltage of the power switch is half the input voltage, resulting in power loss. Transition losses increase with both load current and input voltage and occur twice for each switching cycle.

Use the following equation to estimate transition losses:

$$P_{TRAN} = V_{IN}/2 \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:
t_R is the rise time of the SW node.
t_F is the fall time of the SW node.

The typical value for the rise and fall times, t_R and t_F, is 2 ns.

RECOMMENDED BUCK EXTERNAL COMPONENTS

The recommended external components for use with the ADP2370/ADP2371 are listed in Table 6 (inductors) and Table 7 (capacitors).

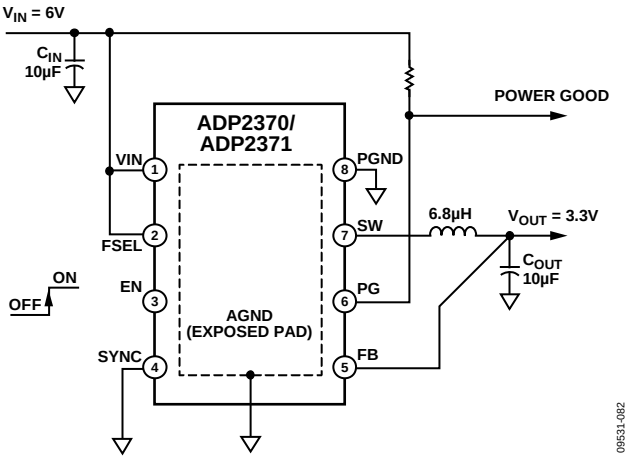

Figure 82. Typical Application, 1.2 MHz, Fixed Output

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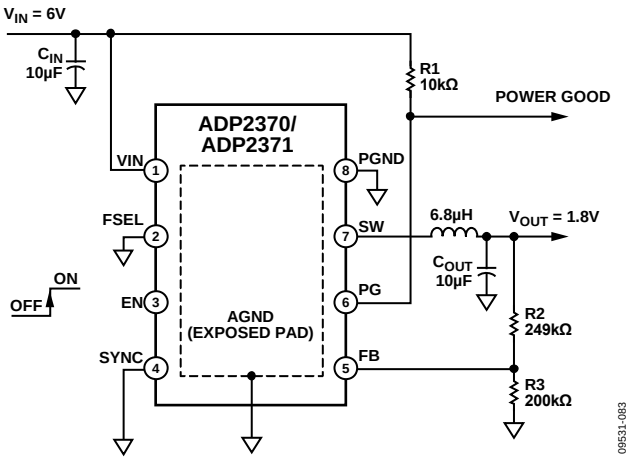

Figure 83. Typical Application, 600 kHz, Adjustable Output

Table 6. Inductors

Vendor	Model	Frequency	Output Voltage	Ideal Value (µH)	Standard Value (µH)	Dimensions (mm)	I_{SAT} (A)	DCR (mΩ)
Coilcraft	XFL4020-222ME	1.2 MHz	1.2	2.5	2.2	4 × 4 × 2	4.1	24
Coilcraft	XFL4020-332ME	1.2 MHz	1.5	3.1	3.3	4 × 4 × 2	3.1	38
Coilcraft	XFL4020-332ME	1.2 MHz	1.8	3.8	3.3	4 × 4 × 2	3.1	38
Coilcraft	XFL4020-472ME	1.2 MHz	2.5	5.2	4.7	4 × 4 × 2	2.0	57
Coilcraft	XAL4030-682ME	1.2 MHz	3.0	6.3	6.8	4 × 4 × 3	1.9	74
Coilcraft	XAL4030-682ME	1.2 MHz	3.3	6.9	6.8	4 × 4 × 3	1.9	74
Coilcraft	XAL4040-103ME	1.2 MHz	5	10.5	10	4 × 4 × 4	1.5	92
Coilcraft	LPS6235-183ML	1.2 MHz	9	18.8	18	6 × 6 × 3.5	1.7	14
Coilcraft	XFL4020-472ME	600 kHz	1.2	5.0	4.7	4 × 4 × 2	2.0	57
Coilcraft	XAL4030-682ME	600 kHz	1.5	6.3	6.8	4 × 4 × 3	1.9	74
Coilcraft	XAL4030-682ME	600 kHz	1.8	7.5	6.8	4 × 4 × 3	1.9	74
Coilcraft	XAL4040-103ME	600 kHz	2.5	10.5	10	4 × 4 × 4	1.5	92
Coilcraft	XAL4040-103ME	600 kHz	3.0	12.6	10	4 × 4 × 4	1.5	92
Coilcraft	XAL4040-153ME	600 kHz	3.3	13.8	15	4 × 4 × 4	1.3	120
Coilcraft	LPS6235-223ML	600 kHz	5	20.9	22	6 × 6 × 3.5	1.6	145
Coilcraft	LPS6235-333ML	600 kHz	9	37.7	33	6 × 6 × 3.5	1.3	130

Table 7. 10 µF Capacitors

Vendor	Model	Case Size	Voltage Rating	Location	Input Voltage	Output Voltage
Murata	GRM32ER7YA106KA12	1210	35	Input or Output	<15 V	
Murata	GRM32DR61E106KA12	1210	25	Input or Output	<12 V	
Murata	GRM31CR61C106KA88	1206	16	Input or Output	<8 V	
Murata	GRM32ER7YA106KA12	1210	35	Input or Output		<12 V
Murata	GRM32DR61E106KA12	1210	25	Input or Output		<9 V
Murata	GRM31CR61C106KA88	1206	16	Input or Output		<7 V
Murata	GRM21BR61C106KE15	0805	16	Output		<2.5 V

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CAPACITOR SELECTION

Output Capacitor

The ADP2370/ADP2371 are designed for operation with small, space-saving ceramic capacitors, but function with most commonly used capacitors provided that the effective series resistance (ESR) value is carefully considered. The ESR of the output capacitor affects stability of the control loop. A minimum output capacitance of 7 µF with an ESR of 10 mΩ or less is recommended to ensure stability of the ADP2370/ADP2371.

Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP2370/ADP2371 to large changes in load current. Figure 84 shows the transient response for an output capacitance value of 10 µF.

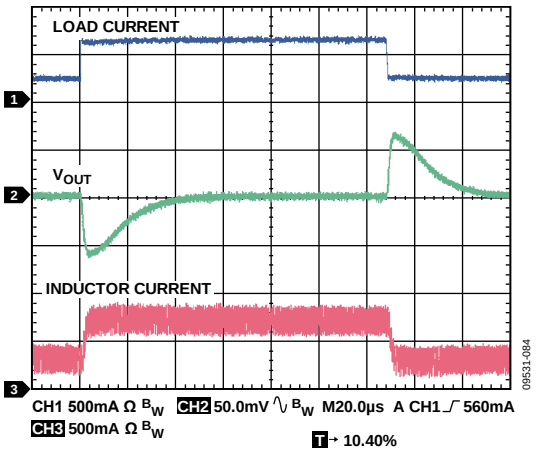

Figure 84. Output Transient Response, V_{OUT2} = 1.8 V, C_{OUT} = 10 µF, 300 mA to 800 mA, Load Current Rise Time = 200 ns

Input Bypass Capacitor

Connecting a 10 µF capacitor from VIN to GND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance are encountered. If greater than 10 µF of output capacitance is required, increase the input capacitor to match it to improve the transient response.

Input and Output Capacitor Properties

Use any good quality ceramic capacitors with the ADP2370/ADP2371; however they must meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectric capacitors with a voltage rating of 6.3 V to 25 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended because of their poor temperature and dc bias characteristics.

Figure 85 depicts the capacitance vs. voltage bias characteristic of a several 10 µF capacitors in different case sizes and voltage ratings. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

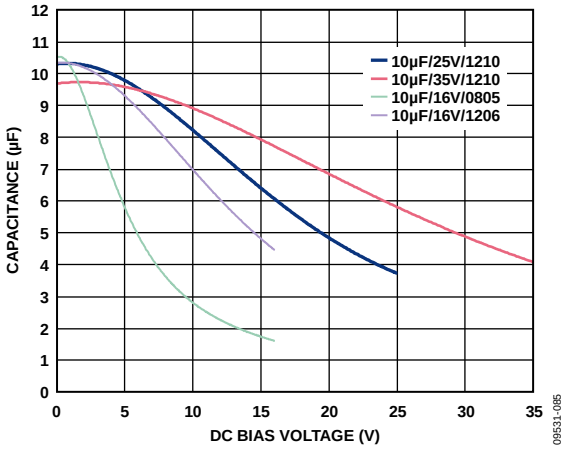

Figure 85. Capacitance vs. Voltage Characteristic Different Case Sizes

Use Equation 1 to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case TEMPCO over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 8.53 µF at 12 V for the 10 µF, 35 V capacitor in a 1210 package (see Figure 85).

Substituting these values in Equation 1 yields

$$C_{EFF} = 8.53\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 6.53\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the ADP2370/ADP2371 over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP2370/ADP2371, it is imperative that the effects of dc bias, temperature, and tolerances of the capacitors are evaluated for each application.

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THERMAL CONSIDERATIONS

In most applications, the ADP2370/ADP2371 do not dissipate much heat due to their high efficiency. However, in applications with high ambient temperature and high supply voltage-to-output voltage differential, the heat dissipated in the package may be large enough to cause the junction temperature of the die to exceed the 125°C maximum.

If the junction temperature of the ADP2370/ADP2371 exceeds 150°C, the regulator enters thermal shutdown. The regulator recovers only after the junction temperature has fallen below 130°C, this helps to prevent any permanent damage to the IC. Thermal analysis for the chosen application is clearly very important to guarantee reliable operation under all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP2370/ADP2371 must not exceed 125°C. To ensure the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and the thermal resistance between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of PCB copper soldered to the package GND and EPAD. Table 8 shows typical θ_{JA} values of the 8-lead, 3 mm × 3 mm LFCSP for various PCB copper sizes.

Table 8. Typical θ_{JA} Values

Copper Size (mm²)	θ_{JA} (°C/W)
25[1]	162.2
100	124.1
500	68.7
1000	56.5
6400	42.4

[1] The device is soldered to minimum size pin traces.

The junction temperature of the ADP2370/ADP2371 is calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:

T_A is the ambient temperature.

P_D is the total power dissipation in the die, given by

$$P_D = P_{BUCK} = P_{SW} + P_{TRAN} + P_{SW_COND} \quad (3)$$

where:

P_{SW}, P_{TRAN}, and P_{SW_COND} are defined in the Efficiency section.

For a given ambient temperature and total power dissipation, there exists a minimum copper size requirement for the PCB to ensure the junction temperature does not rise above 125°C. The following figures (Figure 86 to Figure 89) show junction temperature calculations for different ambient temperatures, total power dissipation, and areas of PCB copper.

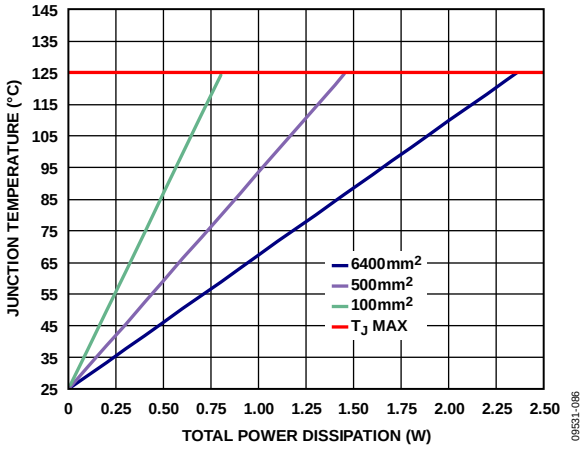

Figure 86. Junction Temperature vs. Power Dissipation, T_A = 25°C

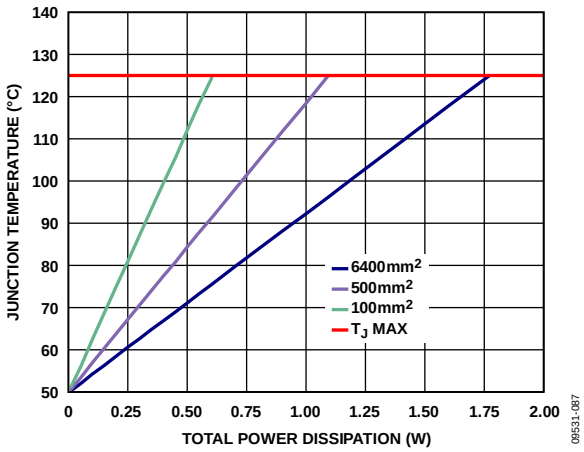

Figure 87. Junction Temperature vs. Power Dissipation, T_A = 50°C

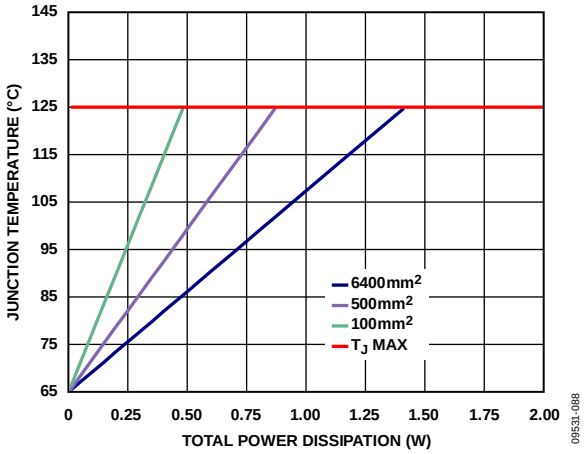

Figure 88. Junction Temperature vs. Power Dissipation, T_A = 65°C

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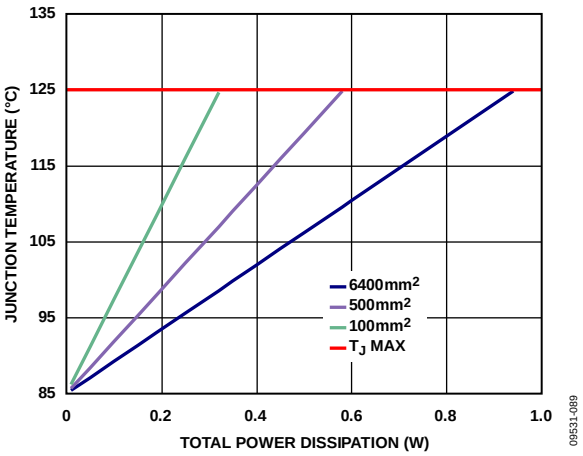

Figure 89. Junction Temperature vs. Power Dissipation, T_A = 85°C

In cases where the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical Ψ_{JB} value for the 8-lead, 3 mm × 3 mm LFCSP is 22.2°C/W.

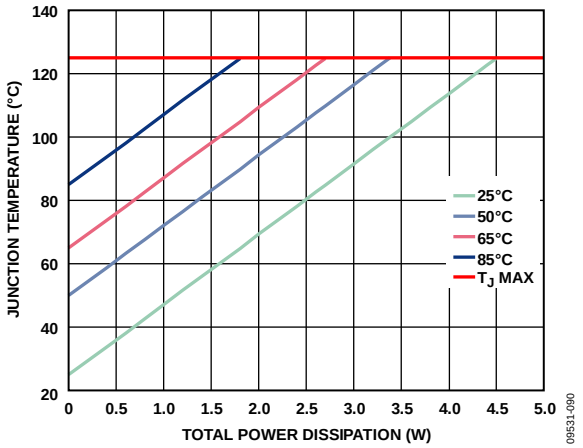

Figure 90. Junction Temperature vs. Power Dissipation, Different Board Temperatures

PCB LAYOUT CONSIDERATIONS

Improve heat dissipation from the package by increasing the amount of copper attached to the pins of the ADP2370/ADP2371. However, as listed in Table 8, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Poor layout can affect the ADP2370/ADP2371 buck performance causing electromagnetic interference (EMI), poor electromagnetic compatibility (EMC) performance, ground bounce, and voltage losses; thus, regulation and stability can be affected. Implement a good PCB layout to ensure optimum performance by applying the following rules:

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies and long, large tracks act like antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Use a ground plane with several vias connected to the component-side ground to reduce noise interference on sensitive circuit nodes.
- Use of 0402-size or 0603-size capacitors achieves the smallest possible footprint solution on boards where area is limited.

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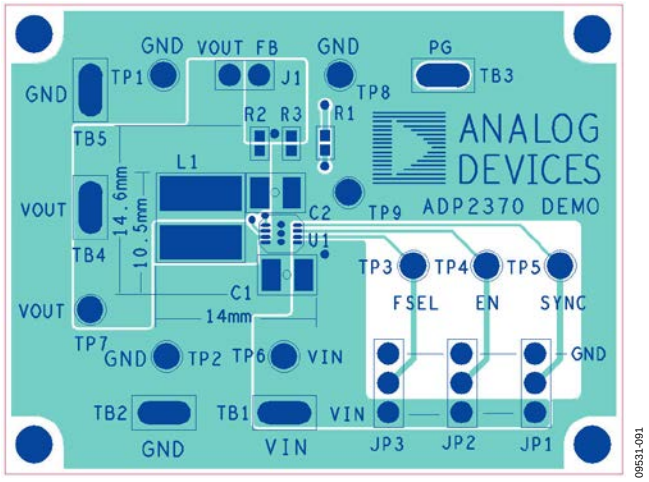

Figure 91. PCB Layout, Top

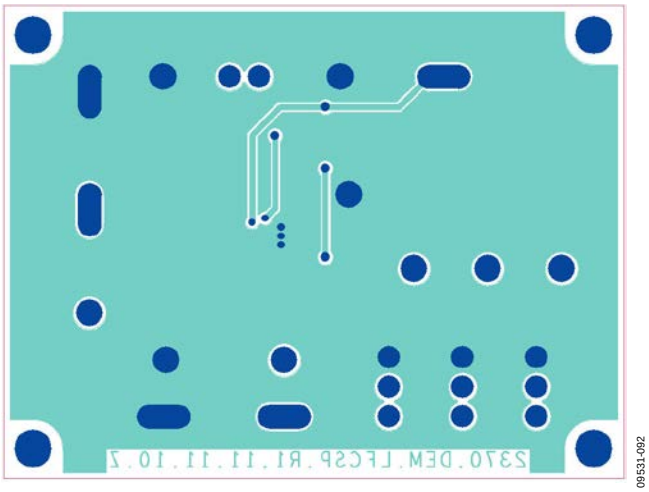

Figure 92. PCB Layout, Bottom

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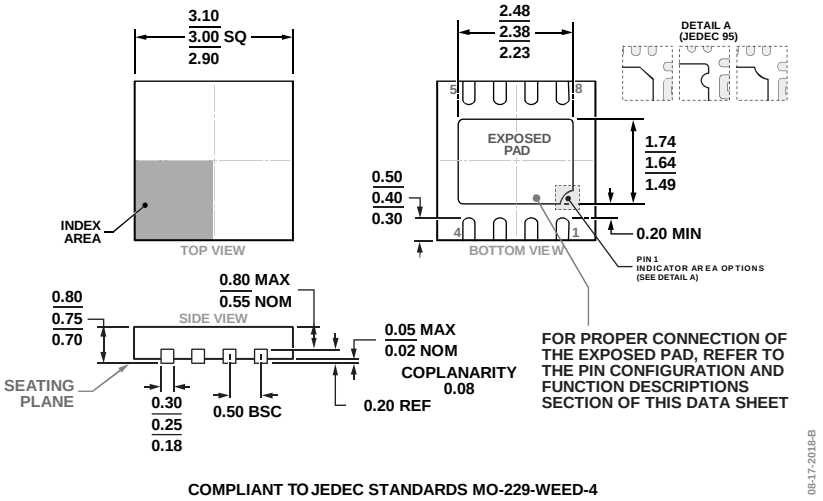
PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-229-WEED-4

Figure 93. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Buck Output Voltage (V)	Temperature Range	Package Description	Package Option	Marking Code
ADP2370ACPZ-1.2-R7	1.2	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LL4
ADP2370ACPZ-1.5-R7	1.5	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LL5
ADP2370ACPZ-1.8-R7	1.8	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LL6
ADP2370ACPZ-2.5-R7	2.5	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LL7
ADP2370ACPZ-3.0-R7	3.0	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LL8
ADP2370ACPZ-3.3-R7	3.3	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LL9
ADP2370ACPZ-5.0-R7	5.0	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LLB
ADP2370ACPZ-R7	Adjustable	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LGZ
ADP2370ACPZ-R2	Adjustable	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LGZ
ADP2371ACPZ-1.2-R7	1.2 with QOD	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LLJ
ADP2371ACPZ-1.8-R7	1.8 with QOD	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LLK
ADP2371ACPZ-3.3-R7	3.3 with QOD	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LLL
ADP2371ACPZ-R7	Adjustable with QOD	−40°C to +125°C	8-Lead LFCSP	CP-8-5	LLM
ADP2370CPZ-REDYKIT			REDYKIT		

[1] Z = RoHS Compliant Part.

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