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REVISION HISTORY

11/2017—Rev. B. to Rev. C

Changed R_S to R_{SN} ... Throughout
Change to Figure 1 ... 1
Changes to Maximum Full-Scale Output Current Parameter and Power Supply Rejection Ratio Parameter, Table 1 ... 3
Moved Timing Characteristics Section, Table 2, and Figure 2 ... 4
Added Lead Temperature Range (Soldering 10 sec) Parameter, Table 3 ... 5
Changes to Figure 3 and Table 4 ... 6
Changes to Setting Full-Scale Output Current Section ... 10
Changes to Adding Dither to the Output Current Section, Figure 20, and Figure 21 ... 12
Changes to PCB Layout Recommendations Section and Figure 25 ... 13
Updated to Outline Dimensions ... 14

3/2016—Rev. A to Rev. B

Changes to Figure 3 and Table 4 ... 7
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 15

4/2009—Rev. 0 to Rev. A

Changes to Table 3 ... 6
Changes to Figure 25 ... 14
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 15

1/2004—Revision 0: Initial Version

SPECIFICATIONS

AVDD = DVDD = 5 V, PVDD = 3.3 V, AVSS = DVSS = DGND = 0 V, T_A = 25°C, covering output current (I_{OUT}) from 2% full-scale current (I_{FS}) to 100% I_{FS}, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC PERFORMANCE						
Resolution	N			12		Bits
Relative Accuracy	INL				±4	LSB
Differential Nonlinearity	DNL				±0.75	LSB
Offset				4	8	LSB
Offset Drift		RSN resistance (R_{SN}) = 1.6 Ω; I_{OUT} = 127 mA			15	ppm/°C
Gain Error					1	%FS
REFERENCE INPUT						
Reference Input Voltage	V_{REF}		3.9	4.096	4.3	V
Input Current					1	µA
Bandwidth	BW_{REF}			2		MHz
ANALOG OUTPUT						
Output Current Change vs. Output Voltage Change	$\Delta I_{OUT}/\Delta V_{OUT}$	V_{OUT} = 0.7 V to 2.0 V		100	400	ppm/V
Maximum Full-Scale Output Current	$I_{FS, MAX}$	R_{SN} = 1.37 Ω	300			mA
Output Compliance Voltage	V_{COMP}	−40°C to +85°C; I_{FS} = 300 mA	2.0	2.5		V
AC PERFORMANCE						
Settling Time	τ_S			3		µs
Bandwidth	BW			5		MHz
Current Noise Density at 10 kHz	i_N	I_{FS} = 250 mA		7.5		nA/√Hz
		I_{FS} = 100 mA		3		nA/√Hz
		I_{FS} = 50 mA		1.5		nA/√Hz
Standby Recovery				6		µs
POWER SUPPLY[1]						
Power Supply Voltage	DVDD		3.0	5	5.5	V
	AVDD		4.5	5	5.5	V
	PVDD		3.0	3.3	5.5	V
Power Supply Rejection Ratio	PSRR	AVDD = 4.5 V to 5.5 V[2]		0.4	5	µA/V
		PVDD = 3.0 V to 3.6 V[2]		0.4	5	µA/V
Supply Current	I_{DVDD}	I_{OUT} = 0 mA, $\overline{SB}$ = DVDD		11	50	µA
	I_{AVDD}	I_{OUT} = 0 mA, $\overline{SB}$ = DVDD		1	2	mA
	I_{PVDD}	I_{OUT} = 0 mA, $\overline{SB}$ = DVDD		3		mA
	I_{AVDD}	$\overline{SB}$ = 0 V		1		mA
	I_{PVDD}	$\overline{SB}$ = 0 V		0.33		mA
FAULT DETECTION						
Load Open Threshold				PVDD − 0.6		V
Load Short Threshold				AVSS + 0.2		V
FAULT Logic Output	V_{OH}	DVDD = 5.0 V	4.5			V
	V_{OL}	DVDD = 5.0 V			0.5	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS						
Input Leakage Current	I_{IL}				1	μA
Input Low Voltage	V_{IL}	DVDD = 3.0 V			0.5	V
		DVDD = 5 V			0.8	V
Input High Voltage	V_{IH}	DVDD = 3.0 V	2.4			V
		DVDD = 5 V	4			V
INTERFACE TIMING[3]						
Clock Frequency	f_{CLK}				12.5	MHz
$\overline{\text{RESET}}$ Pulse Width	t_{11}		40			ns

[1] With respect to AVSS.
[2] R_{SN} = 20 Ω.
[3] See Table 2 for timing specifications.

TIMING CHARACTERISTICS

Table 2. Timing Characteristics[1, 2]

Parameter	Description	Min	Typ	Max	Unit
f_{CLK}	SCLK frequency			12.5	MHz
t_1	SCLK cycle time	80			ns
t_2	SCLK width high	40			ns
t_3	SCLK width low	40			ns
t_4	$\overline{\text{CS}}$ low to SCLK high setup	15			ns
t_5	$\overline{\text{CS}}$ high to SCLK high setup	15			ns
t_6	SCLK high to $\overline{\text{CS}}$ low hold	35			ns
t_7	SCLK high to $\overline{\text{CS}}$ high hold	20			ns
t_8	Data setup	15			ns
t_9	Data hold	2			ns
t_{10}	$\overline{\text{CS}}$ high pulse width	30			ns
t_{11}	$\overline{\text{RESET}}$ pulse width	40			ns
t_{12}	$\overline{\text{CS}}$ high to $\overline{\text{RESET}}$ low hold	30			ns

[1] Guaranteed by design. Not production tested.
[2] Sample tested during initial release and after any redesign or process change that may affect these parameters. All input signals are measured with tr = tf = 5 ns (10% to 90% of DVDD) and timed from a voltage level of (V_{IL} + V_{IH})/2.

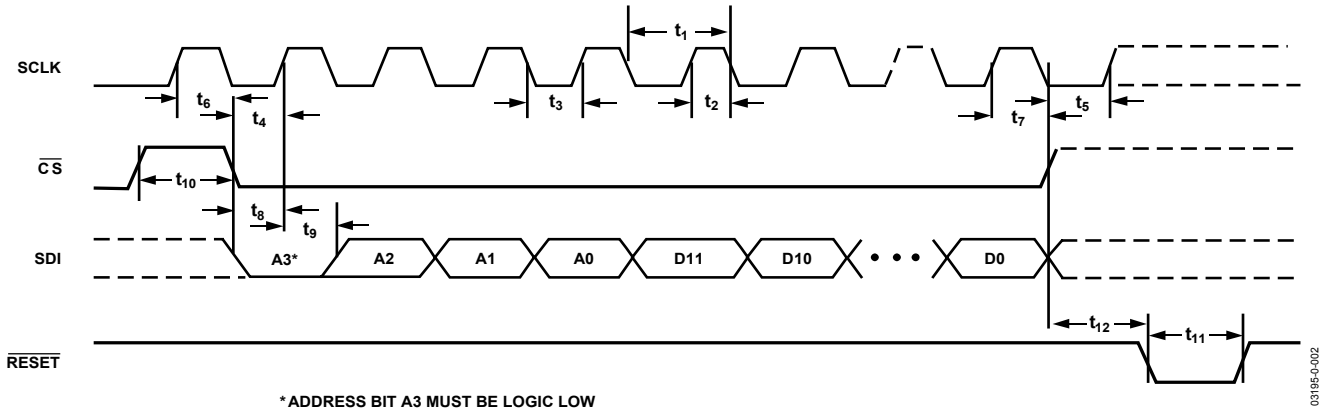


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S+ 0.3 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range, CP Package	−65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

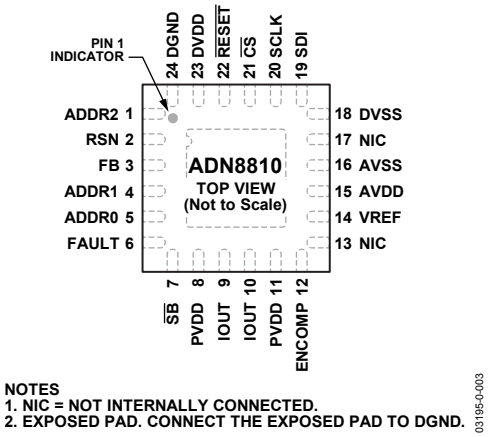


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	ADDR2	Digital Input	Chip Address, Bit 2.
2	RSN	Analog Input	Sense Resistor RS2 Feedback.
3	FB	Analog Input	Sense Resistor RS1 Feedback.
4	ADDR1	Digital Input	Chip Address, Bit 1.
5	ADDR0	Digital Input	Chip Address, Bit 0.
6	FAULT	Digital Output	Load Open/Short Indication.
7	$\overline{SB}$	Digital Input	Active Deactivates Output Stage (High Output Impedance State).
8, 11	PVDD	Analog Power	Power Supply for IOUT (3.3 V Recommended).
9, 10	IOUT	Analog Output	Current Output.
12	ENCOMP	Digital Input	Connect to AVSS.
13, 17	NIC	Not Applicable	Not Internally Connected.
14	VREF	Analog Input	Input for High Accuracy External Reference Voltage (ADR292ER).
15	AVDD	Analog Power	Power Supply for DAC.
16	AVSS	Analog Ground	Connect to Analog Ground or Most Negative Potential in Dual-Supply Applications.
18	DVSS	Digital Ground	Connect to Digital Ground or Most Negative Potential in Dual-Supply Applications.
19	SDI	Digital Input	Serial Data Input.
20	SCLK	Digital Input	Serial Clock Input.
21	$\overline{CS}$	Digital Input	Chip Select; Active Low.
22	$\overline{RESET}$	Digital Input	Asynchronous Reset to Return DAC Output to Code Zero; Active Low.
23	DVDD	Digital Power	Power Supply for Digital Interface.
24	DGND	Digital Ground	Digital.
	EPAD	Heat Sink	Exposed Pad. Connect the exposed pad to DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

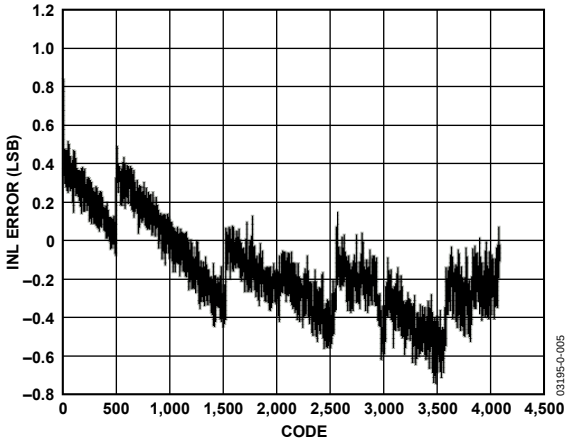


Figure 4. Typical INL Plot

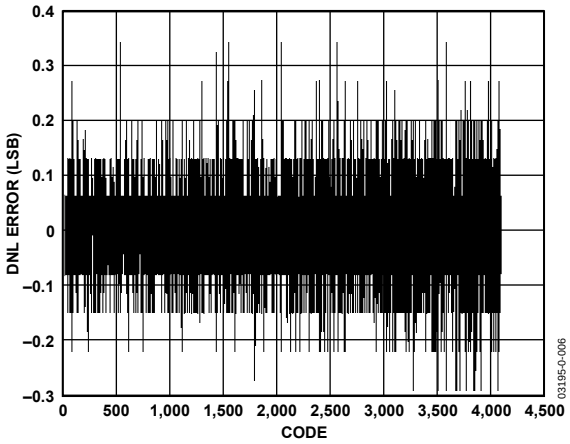


Figure 5. Typical DNL Plot

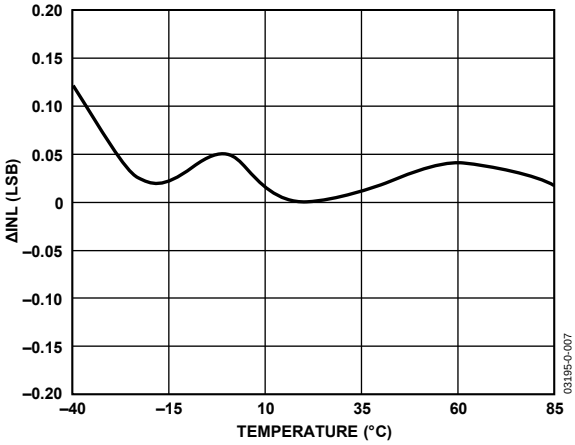


Figure 6. ΔINL vs. Temperature

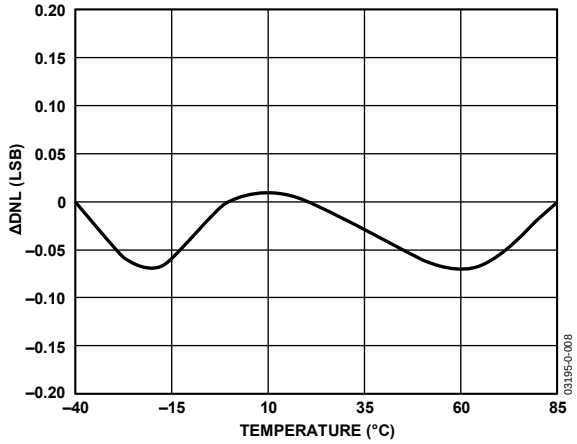


Figure 7. ΔDNL vs. Temperature

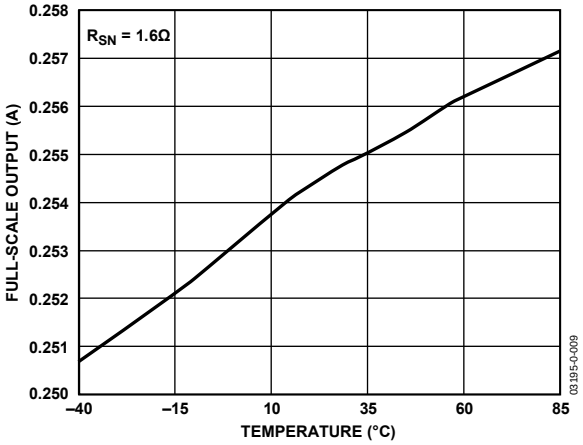


Figure 8. Full-Scale Output vs. Temperature

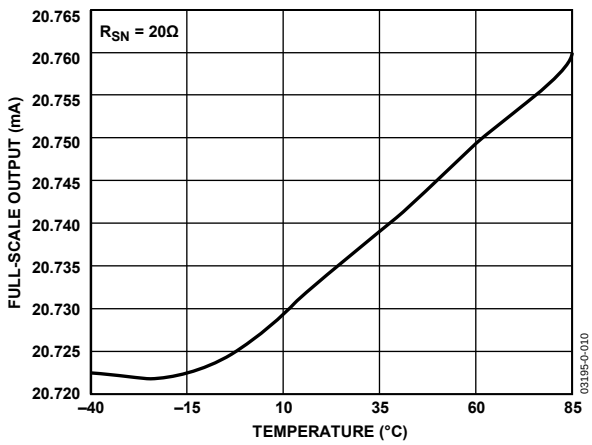


Figure 9. Full-Scale Output vs. Temperature

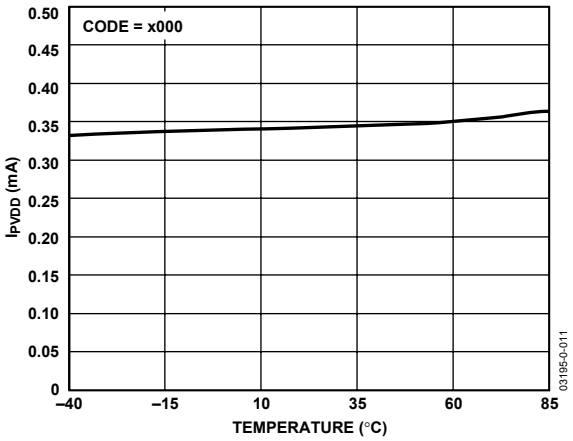


Figure 10. PVDD Supply Current (I_{PVDD}) vs. Temperature

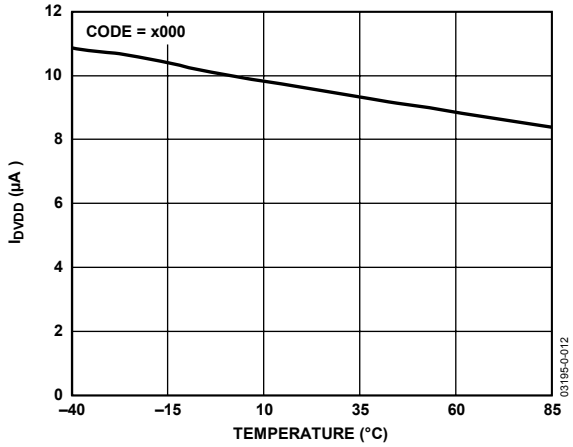


Figure 11. DVDD Supply Current (I_{DVDD}) vs. Temperature

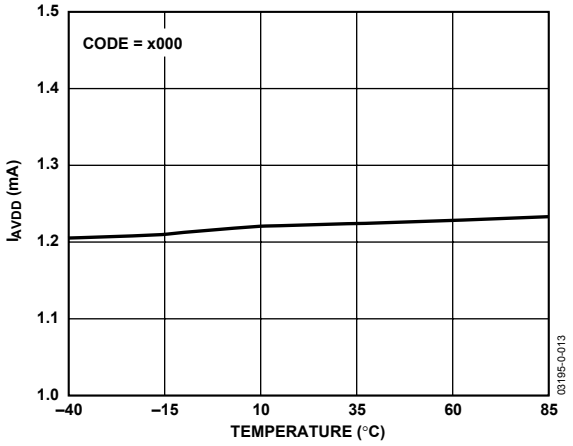


Figure 12. AVDD Supply Current (I_{AVDD}) vs. Temperature

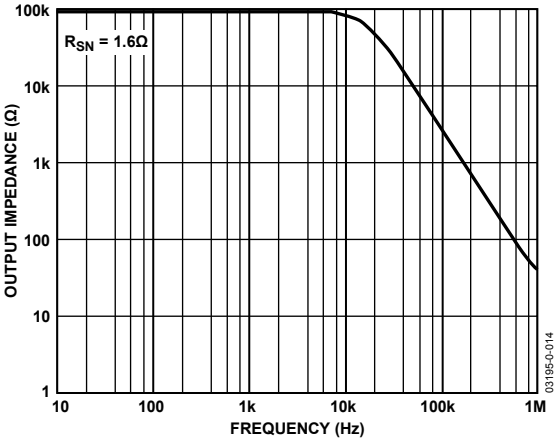


Figure 13. Output Impedance vs. Frequency

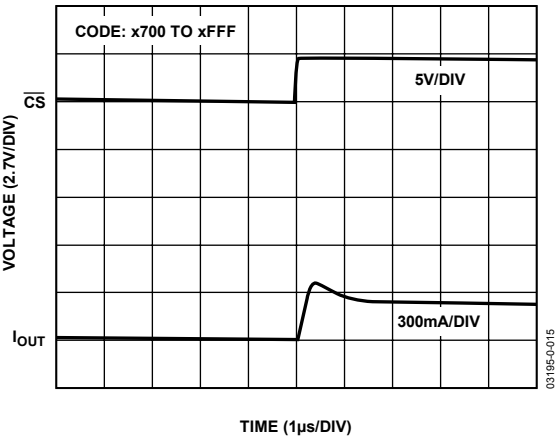


Figure 14. Full-Scale Settling Time

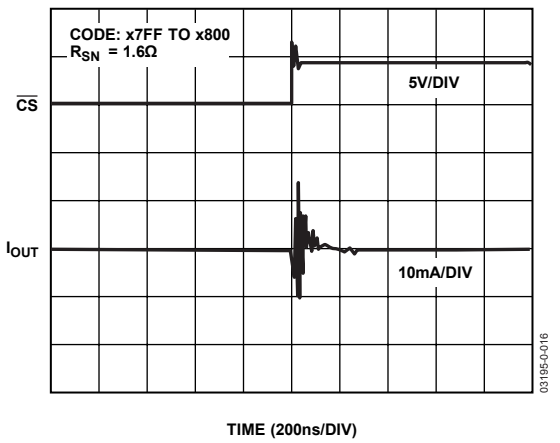


Figure 15. 1 LSB Settling Time

TERMINOLOGY

Relative Accuracy
Relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in least significant bits (LSBs), from an ideal line passing through the endpoints of the DAC transfer function. Figure 4 shows a typical INL vs. code plot. The ADN8810 INL is measured from 2% to 100% of the full-scale (FS) output.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB maximum ensures monotonicity. The ADN8810 is guaranteed monotonic by design. Figure 5 shows a typical DNL vs. code plot.

Offset Error
Offset error, or zero-code error, is an interpolation of the output voltage at code 0x000 as predicted by the line formed from the output voltages at code 0x040 (2% FS) and code 0xFFF (100% FS). Ideally, the offset error is 0 V. Offset error occurs from a combination of the offset voltage of the amplifier and offset errors in the DAC. It is expressed in LSBs.

Offset Drift
This is a measure of the change in offset error with a change in temperature. It is expressed in (ppm of full-scale range)/°C.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the output transfer characteristic from ideal. The transfer characteristic is the line formed from the output voltages at code 0x040 (2% FS) and code 0xFFF (100% FS). It is expressed as a percent of the full-scale range.

Compliance Voltage
The maximum output voltage from the ADN8810 is a function of output current and supply voltage. Compliance voltage defines the maximum output voltage at a given current and supply voltage to guarantee the device operates within its INL, DNL, and gain error specifications.

Output Current Change vs. Output Voltage Change
This is a measure of the ADN8810 output impedance and is similar to a load regulation spec in voltage references. For a given code, the output current changes slightly as output voltage increases. It is measured as an absolute value in (ppm of full-scale range)/V.

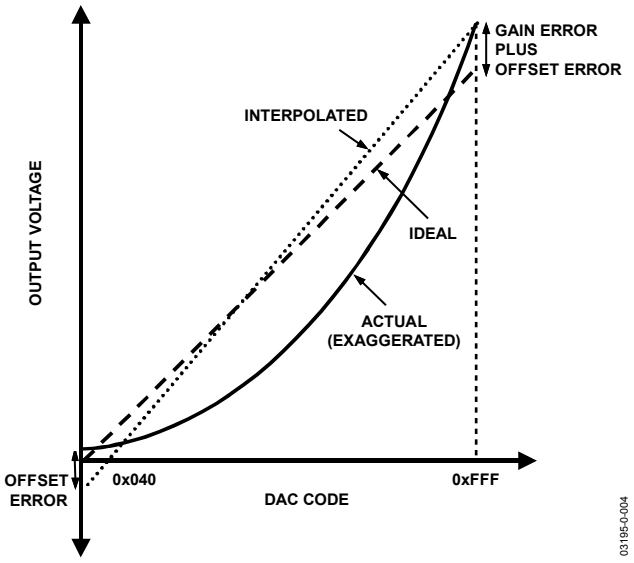


Figure 16. Output Transfer Function

FUNCTIONAL DESCRIPTION

The ADN8810 is a single 12-bit current output digital-to-analog converter (DAC) with a 3-wire SPI interface. Up to eight devices can be independently programmed from the same SPI bus.

The full-scale output current is set with two external resistors. The maximum output current can reach 300 mA. Figure 17 shows the functional block diagram of the ADN8810.

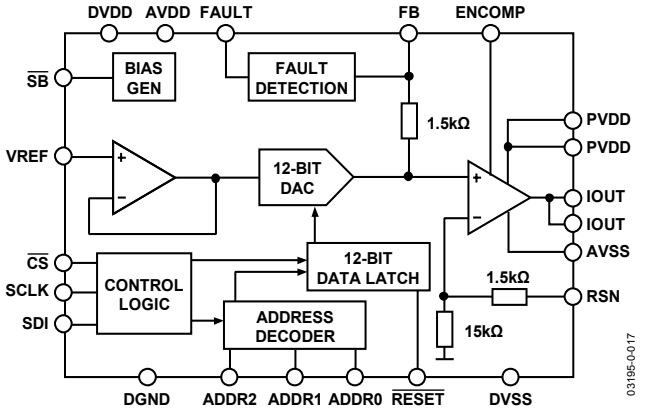


Figure 17. Functional Blocks, Pins, and Internal Connections

SETTING FULL-SCALE OUTPUT CURRENT

Two external resistors set the full-scale output current from the ADN8810. These resistors are equal in value and are labeled R_{SN} in Figure 1. Use 1% or better tolerance resistors to achieve the most accurate output current and the highest output impedance.

Equation 3 shows the approximate full-scale output current. The exact output current is determined by the data register code as shown in Equation 4. The variable code is an integer from 0 to 4095, representing the full 12-bit range of the ADN8810.

$$I_{FS} \approx \frac{4.096}{10 \times R_{SN}} \quad (3)$$

$$I_{OUT} = \frac{Code}{1{,}000} \times \frac{1}{R_{SN}} \times \left(\frac{R_{SN}}{15\ k\Omega} + 0.1 \right) \quad (4)$$

The ADN8810 is designed to operate with a 4.096 V reference voltage connected to VREF. The output current is directly proportional to this reference voltage. To achieve the best performance, use a low noise precision (the ADR292, ADR392, or REF198 is recommended).

POWER SUPPLIES

There are three principal supply current paths through the ADN8810:

- AVDD provides power to the analog front end of the ADN8810 including the DAC. Use this supply line to power the external voltage reference. For best performance, AVDD must be low noise.
- DVDD provides power for the digital circuitry. This includes the serial interface logic, the $\overline{SB}$ and $\overline{RESET}$ logic inputs, and the FAULT output. Tie DVDD to the same supply line used for other digital circuitry. It is not necessary for DVDD to be low noise.
- PVDD is the power pin for the output amplifier. It can operate from as low as 3.0 V to minimize power dissipation in the ADN8810. For best performance, PVDD must be low noise.

Current is returned through the following three pins:

- AVSS is the return path for both AVDD and PVDD. This pin is connected to the substrate of the die as well as the slug on the bottom of the lead frame chip scale package (LFCSP). For single-supply operation, connect this pin to a low noise ground plane.
- DVSS returns current from the digital circuitry powered by DVDD. Connect DVSS to the same ground line or plane used for other digital devices in the application.
- DGND is the ground reference for the digital circuitry. In a single-supply application, connect DGND to DVSS.

For single-supply operation, set AVDD to 5 V, set PVDD from 3.0 V to 5 V, and connect AVSS, AGND, and DGND to ground.

SERIAL DATA INTERFACE

The ADN8810 uses a serial peripheral interface (SPI) with three input signals: SDI, CLK, and $\overline{CS}$. Figure 2 shows the timing diagram for these signals.

Data applied to the SDI pin is clocked into the input shift register on the rising edge of CLK. After all 16 bits of the data-word have been clocked into the input shift register, a logic high on $\overline{CS}$ loads the shift register byte into the ADN8810. If more than 16 bits of data are clocked into the shift register before $\overline{CS}$ goes high, bits are pushed out of the register in first-in first-out (FIFO) fashion.

The four MSB of the data byte are checked against the address of the device. If they match, the next 12 bits of the data byte are loaded into the DAC to set the output current. The first bit (MSB) of the data byte must be a logic zero, and the following three bits must correspond to the logic levels on pins ADDR2, ADDR1, and ADDR0, respectively, for the DAC to be updated. Up to eight ADN8810 devices with unique addresses can be driven from the same serial data bus.

Table 5 shows how the 16-bit DATA input word is divided into an address byte and a data byte. The first four bits in the input word correspond to the address. Note that the first bit loaded (A3) must always be zero. The remaining bits set the 12-bit data byte for the DAC output. Three example inputs are demonstrated.

- Example 1: This SDI input sets the device with an address of 111 to its minimum output current, 0 A. Connecting the ADN8810 pins ADDR2, ADDR1, and ADDR0 to VDD sets this address.
- Example 2: This input sets the device with an address of 000 to a current equal to half of the full-scale output.
- Example 3: The ADN8810 with an address of 100 is set to full-scale output.

STANDBY AND RESET MODES

Applying a logic low to the $\overline{SB}$ pin deactivates the ADN8810 and puts the output into a high impedance state. The device continues to draw 1.3 mA of typical supply current in standby. When logic high is reasserted on the $\overline{SB}$ pin, the output current returns to its previous value within 6 µs.

Applying logic low to $\overline{RESET}$ sets the ADN8810 data register to all zeros, bringing the output current to 0 A. When $\overline{RESET}$ is deasserted, the data register can be reloaded. Data cannot be loaded into the device while it is in standby or reset mode.

POWER DISSIPATION

The power dissipation of the ADN8810 is equal to the output current multiplied by the voltage drop from PVDD to the output.

$$P_{DISS} = I_{OUT} \times (PVDD - V_{OUT}) - I_{OUT}^2 \times R_{SN} \quad (5)$$

The power dissipated by the ADN8810 causes a temperature increase in the device. For this reason, PVDD must be as low as possible to minimize power dissipation.

While in operation, the ADN8810 die temperature, also known as junction temperature, must remain below 150°C to prevent damage. The junction temperature is approximately

$$T_J = T_A + \theta_{JA} \times P_{DISS} \quad (6)$$

where:
T_A is the ambient temperature in °C,
θ_{JA} is the thermal resistance of the package (32°C/W).

- Example 4: A 300 mA full-scale output current is required to drive a laser diode within an 85°C environment. The laser diode has a 2 V drop and PVDD is 3.3 V.

Using Equation 5, the power dissipation in the ADN8810 is found to be 267 mW. At T_A = 85°C, this makes the junction temperature 93.5°C, which is well below the 150°C limit. Note that even with PVDD set to 5 V, the junction temperature increases to only 110°C.

USING MULTIPLE ADN8810 DEVICES FOR ADDITIONAL OUTPUT CURRENT

Connect multiple ADN8810 devices in parallel to increase the available output current. Each device can deliver up to 300 mA of current. To program all parallel devices simultaneously, set all device addresses to the same address byte and drive all $\overline{CS}$, SDI, and CLK from the same serial data interface bus. The circuit in Figure 18 uses two ADN8810 devices and delivers 600 mA to the pump laser.

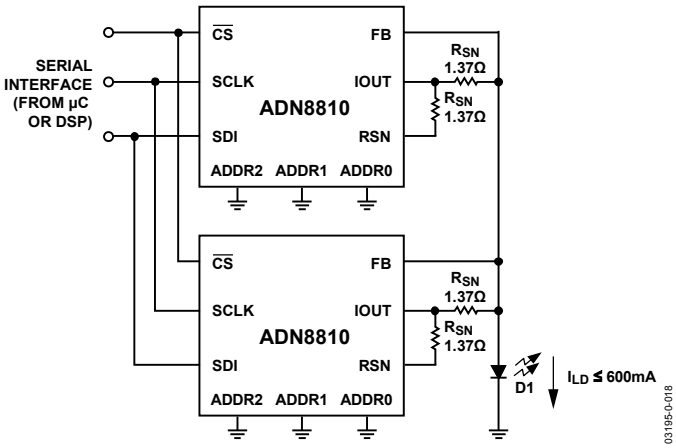


Figure 18. Using Multiple Devices for Additional Output Current

Table 5. Serial Data Input Examples

	Address Byte				Data Byte											
SDI Input	A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Example 1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Example 2	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Example 3	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1

ADDING DITHER TO THE OUTPUT CURRENT

Some tunable laser applications require the laser diode bias current to be modulated or dithered. This is accomplished by dithering the V_{REF} voltage input to the ADN8810. Figure 19 demonstrates one method.

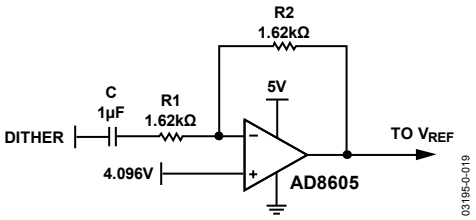


Figure 19. Adding Dither to the Reference Voltage

Set the gain of the dither by adjusting the ratio of R2 to R1. Increase C to lower the cutoff frequency of the high-pass filter created by C and R1. The cutoff frequency of Figure 19 is approximately 98 Hz.

The AD8605 is recommended as a low offset, rail-to-rail input amplifier for this circuit.

DRIVING COMMON-ANODE LASER DIODES

The ADN8810 can power common-anode laser diodes. These are laser diodes whose anodes are fixed to the laser module case. The module case is typically tied to either VDD or ground. For common anode to ground applications, a −5 V supply must be provided.

In Figure 20, R_{SN} sets up the diode current by the following equation:

$$I = 4.096 \times 1.1\left(\frac{1}{R_{SN}} + \frac{1}{16.5\ k\Omega}\right) \times \frac{Code}{4096} \qquad (7)$$

where Code is an integer value from 0 to 4095.

Using the values in Figure 20, the diode current is 300.7 mA at a code value of 2045 (0x7FF), or half full-scale. This effectively provides 11-bit current control from 0 mA to 300 mA of diode current.

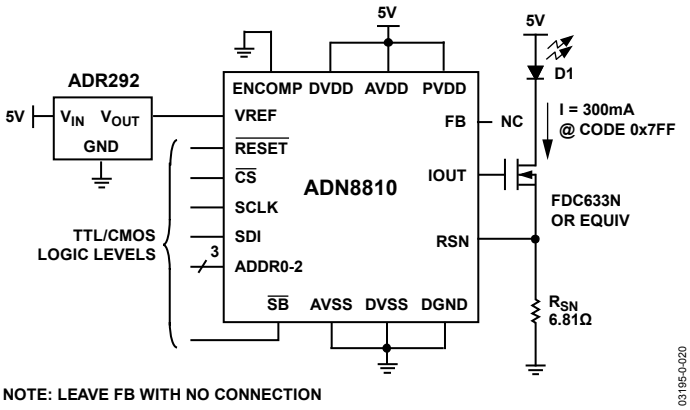
The maximum output current of this configuration is limited by the compliance voltage at the IOUT pin of the ADN8810. The voltage at IOUT cannot exceed 1 V below PVDD, in this case, 4 V. The IOUT voltage is equal to the voltage drop across R_{SN} plus the gate-to-source voltage of the external FET. For this reason, select a FET with a low threshold voltage.

In addition, the voltage across the R_{SN} resistor cannot exceed the voltage at the cathode of the laser diode. Given a forward laser diode voltage drop of 2 V in Figure 20, the voltage at the RSN pin ($I \times R_{SN}$) cannot exceed 3 V. This sets an upper limit to the value of code in Equation 5.

Although the configuration for anode-to-ground diodes is similar, the supply voltages must be shifted down to 0 V and −5 V, as shown in Figure 21. The AVDD, DVDD, and PVDD pins are connected to ground with AVSS connected to −5 V.

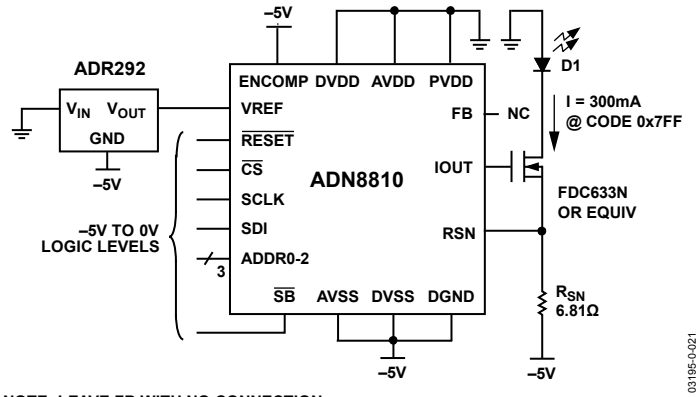
The 4.096 V reference must also be referred to the −5 V supply voltage. The diode current is still determined by Equation 7.

All logic levels must be shifted down to 0 V and −5 V levels as well. This includes $\overline{\text{RESET}}$, $\overline{\text{CS}}$, SCLK, SDI, $\overline{\text{SB}}$, and all ADDR pins. Figure 22 shows a simple method to level shift a standard TTL or CMOS (0 V to 5 V) signal down using external FETs.



NOTE: LEAVE FB WITH NO CONNECTION

Figure 20. Driving Common-Anode-to-VDD Laser Diodes



NOTE: LEAVE FB WITH NO CONNECTION

Figure 21. Driving Common-Anode-to-Ground Laser Diodes with a Negative Supply

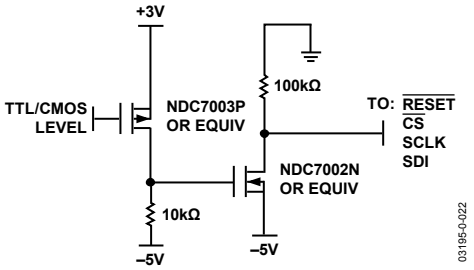


Figure 22. Level Shifting TTL/CMOS Logic

PCB LAYOUT RECOMMENDATIONS

Although they can be driven from the same power supply voltage, keep DVDD and AVDD current paths separate on the printed circuit board (PCB) to maintain the highest accuracy; likewise for AVSS and DGND. Tie common potentials together at a single point located near the power regulator. This technique is known as star grounding and is shown in Figure 23. This method reduces digital crosstalk into the laser diode or load.

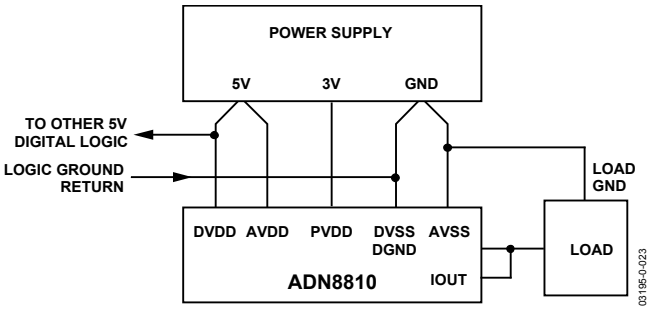


Figure 23. Star Supply and Ground Technique

To improve thermal dissipation, solder the slug on the bottom of the LFCSP package be soldered to the PCB with multiple vias into a low noise ground plane. Connecting these vias to a copper area on the bottom side of the board further improves thermal dissipation.

Use identical trace width and lengths for the two output sense resistors. These lengths are shown as X and Y in Figure 24. Differences in trace lengths cause differences in parasitic series resistance. Because the sense resistors can be as low as 1.37 Ω, small parasitic differences can lower both the output current accuracy and the output impedance. See the AN-619 Application Note for a sample layout for these traces.

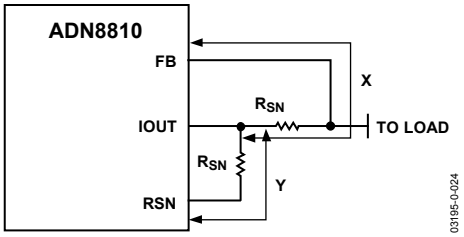


Figure 24. Use Identical Trace Lengths for Sense Resistors

SUGGESTED PAD LAYOUT FOR CP-24 PACKAGE

Figure 25 shows the dimensions for the PCB pad layout for the ADN8810. The package is a 4 mm × 4 mm, 24-lead LFCSP. The metallic slug underneath the package must be soldered to a copper pad connected to AVSS, the lowest supply voltage to the ADN8810. For single-supply applications, this is ground. Use multiple vias to this pad to improve the thermal dissipation of the package.

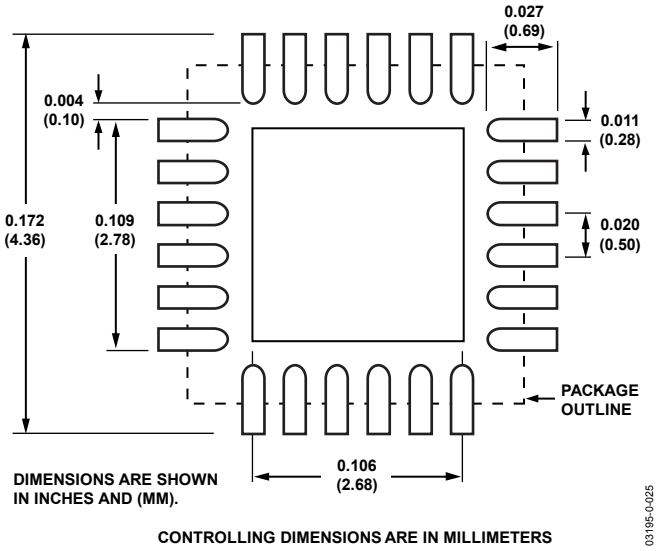


Figure 25. Suggested PCB Layout for the CP-24-10 Pad Landing

OUTLINE DIMENSIONS

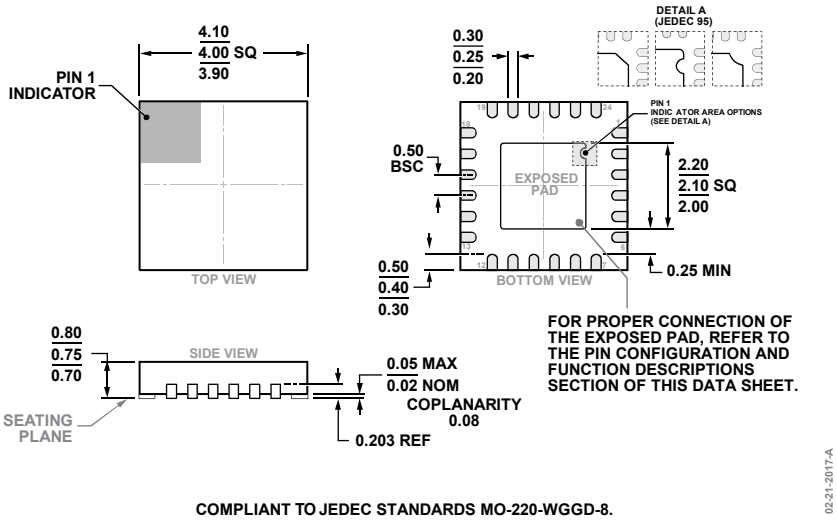


Figure 26. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADN8810ACPZ	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-10
ADN8810ACPZ-REEL7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-10

[1] Z = RoHS Compliant Part.

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