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REVISION HISTORY

5/09—Revision 0: Initial Version

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SPECIFICATIONS

$+V_S$ = +15 V, $-V_S$ = −15 V, V_{REF} = 0 V, T_A = 25°C, G = 5, R_L = 10 kΩ, specifications referred to input, unless otherwise noted.

Table 2.

Parameter	Test Conditions/ Comments	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
COMMON-MODE REJECTION RATIO	V_{CM} = −10 V to +10 V							
DC to 60 Hz								
G = 5		90			100			dB
G = 10		96			105			dB
G = 100		105			110			dB
G = 1000		105			110			dB
5 kHz								
G = 5		80			80			dB
G = 10		86			86			dB
G = 100		86			86			dB
G = 1000		86			86			dB
NOISE	Total noise: $e_N = \sqrt{(e_{NI}^2 + (e_{NO}/G)^2)}$							
Voltage Noise, 1 kHz								
Input Voltage Noise, e_{NI}			24	25		24	25	nV/√Hz
Output Voltage Noise, e_{NO}			310	315		310	315	nV/√Hz
RTI	f = 0.1 Hz to 10 Hz							
G = 5			1.5			1.5		µV p-p
G = 10			0.9			0.9		µV p-p
G = 100 to 1000			0.5			0.5		µV p-p
Current Noise	f = 1 kHz		100			100		fA/√Hz
	f = 0.1 Hz to 10 Hz		3			3		pA p-p
VOLTAGE OFFSET	Total offset voltage: $V_{OS} = V_{OSI} + (V_{OSO}/G)$							
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V			200			100	µV
Average Temperature Drift	T_A = −40°C to +125°C		0.2	2		0.2	1	µV/°C
Output Offset, V_{OSO}	V_S = ±5 V to ±15 V			1000			500	µV
Average Temperature Drift	T_A = −40°C to +125°C		2	10		2	5	µV/°C
Offset RTI vs. Supply (PSR)	V_S = ±5 V to ±15 V							
G = 5		90			100			dB
G = 10		96			105			dB
G = 100		105			110			dB
G = 1000		105			110			dB
INPUT CURRENT								
Input Bias Current[1]	T_A = +25°C	5	20	27	5	20	27	nA
	T_A = +125°C	5	15	25	5	15	25	nA
	T_A = −40°C	5	30	35	5	30	35	nA
Average Temperature Drift	T_A = −40°C to +125°C		70			70		pA/°C
Input Offset Current	T_A = +25°C			1.5			1.5	nA
	T_A = +125°C			1.5			1.5	nA
	T_A = −40°C			2			2	nA
Average Temperature Drift	T_A = −40°C to +125°C		5			5		pA/°C
REFERENCE INPUT								
R_{IN}			60			60		kΩ
I_{IN}			12			12		µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1			1		V/V
Reference Gain Error			0.01			0.01		%

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Parameter	Test Conditions/ Comments	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 5			250			250		kHz
G = 10			200			200		kHz
G = 100			50			50		kHz
G = 1000			5			5		kHz
Settling Time 0.01%	10 V step							
G = 5			14			14		µs
G = 10			15			15		µs
G = 100			35			35		µs
G = 1000			275			275		µs
Slew Rate[2]	G = 5 to 100		0.8			0.8		V/µs
GAIN[3]	G = 5 + (80 kΩ/R_G)							
Gain Range		5		1000	5		1000	V/V
Gain Error	V_{OUT} = −10 V to +10 V							
G = 5				0.04			0.02	%
G = 10 to 1000				0.3			0.15	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V							
G = 5	R_L ≥ 2 kΩ			10			10	ppm
G = 10	R_L ≥ 2 kΩ			15			15	ppm
G = 100	R_L ≥ 2 kΩ			15			50	ppm
G = 1000	R_L ≥ 2 kΩ			750			150	ppm
Gain vs. Temperature	T_A = −40°C to +125°C							
G = 5				5			5	ppm/°C
G > 5				−100			−100	ppm/°C
INPUT	V_S = ±1.5 V to +36 V							
Impedance								
Differential			0.8‖2			0.8‖2		GΩ‖pF
Common Mode			0.4‖2			0.4‖2		GΩ‖pF
Operating Voltage Range[4]	T_A = +25°C	$-V_S$ − 0.1		$+V_S$ − 0.8	$-V_S$ − 0.1		$+V_S$ − 0.8	V
	T_A = +125°C	$-V_S$ − 0.05		$+V_S$ − 0.6	$-V_S$ − 0.05		$+V_S$ − 0.6	V
	T_A = −40°C	$-V_S$ − 0.15		$+V_S$ − 0.9	$-V_S$ − 0.15		$+V_S$ − 0.9	V
Overvoltage Range	T_A = −40°C to +125°C	$+V_S$ − 40		$-V_S$ + 40	$+V_S$ − 40		$-V_S$ + 40	V
OUTPUT								
Output Swing								
R_L = 10 kΩ to ground	T_A = −40°C to +85°C	$-V_S$ + 0.2		$+V_S$ − 0.2	$-V_S$ + 0.2		$+V_S$ − 0.2	V
	T_A = +85°C to +125°C	$-V_S$ + 0.2		$+V_S$ − 0.3	$-V_S$ + 0.2		$+V_S$ − 0.3	V
R_L = 100 kΩ to ground	T_A = −40°C to +125°C	$-V_S$ + 0.1		$+V_S$ − 0.1	$-V_S$ + 0.1		$+V_S$ − 0.1	V
Short-Circuit Current			13			13		mA
POWER SUPPLY								
Operating Range	Dual-supply operation	±1.5		±18	±1.5		±18	V
Quiescent Current	T_A = +25°C		350	425		350	425	µA
	T_A = −40°C		250	325		250	325	µA
	T_A = +85°C		450	525		450	525	µA
	T_A = +125°C		525	600		525	600	µA
TEMPERATURE RANGE		−40		+125	−40		+125	°C

[1] The input stage uses pnp transistors, so input bias current always flows into the part.
[2] At high gains, the part is bandwidth limited rather than slew rate limited.
[3] For G > 5, gain error specifications do not include the effects of External Resistor R_G.
[4] Input voltage range of the AD8227 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See the Input Voltage Range section for more information.

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$+V_S$ = 2.7 V, $-V_S$ = 0 V, V_{REF} = 0 V, T_A = 25°C, G = 5, R_L = 10 kΩ, specifications referred to input, unless otherwise noted.

Table 3.

Parameter	Test Conditions/ Comments	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
COMMON-MODE REJECTION RATIO	V_{CM} = 0 V to 1.7 V							
DC to 60 Hz								
G = 5		90			100			dB
G = 10		96			105			dB
G = 100		105			110			dB
G = 1000		105			110			dB
5 kHz								
G = 5		80			80			dB
G = 10		86			86			dB
G = 100		86			86			dB
G = 1000		86			86			dB
NOISE	Total noise: $e_N = \sqrt{(e_{NI}^2 + (e_{NO}/G)^2)}$							
Voltage Noise, 1 kHz								
Input Voltage Noise, e_{NI}			25	28		25	28	nV/√Hz
Output Voltage Noise, e_{NO}			310	330		310	330	nV/√Hz
RTI	f = 0.1 Hz to 10 Hz							
G = 5			1.5			1.5		µV p-p
G = 10			0.8			0.8		µV p-p
G = 100 to 1000			0.5			0.5		µV p-p
Current Noise	f = 1 kHz		100			100		fA/√Hz
	f = 0.1 Hz to 10 Hz		3			3		pA p-p
VOLTAGE OFFSET	Total offset voltage: $V_{OS} = V_{OSI} + (V_{OSO}/G)$							
Input Offset, V_{OSI}	V_S = 0 V to 1.7 V			200			100	µV
Average Temperature Drift	T_A = −40°C to +125°C		0.2	2		0.2	1	µV/°C
Output Offset, V_{OSO}	V_S = 0 V to 1.7 V			1000			500	µV
Average Temperature Drift	T_A = −40°C to +125°C		2	10		2	5	µV/°C
Offset RTI vs. Supply (PSR)	V_S = 0 V to 1.7 V							
G = 5		90			100			dB
G = 10		96			105			dB
G = 100		105			110			dB
G = 1000		105			110			dB
INPUT CURRENT								
Input Bias Current[1]	T_A = +25°C	5	20	27	5	20	27	nA
	T_A = +125°C	5	15	25	5	15	25	nA
	T_A = −40°C	5	30	35	5	30	35	nA
Average Temperature Drift	T_A = −40°C to +125°C		70			70		pA/°C
Input Offset Current	T_A = +25°C			1.5			1.5	nA
	T_A = +125°C			1.5			1.5	nA
	T_A = −40°C			2			2	nA
Average Temperature Drift	T_A = −40°C to +125°C		5			5		pA/°C
REFERENCE INPUT								
R_{IN}			60			60		kΩ
I_{IN}			12			12		µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1			1		V/V
Reference Gain Error			0.01			0.01		%

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Parameter	Test Conditions/ Comments	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 5			250			250		kHz
G = 10			200			200		kHz
G = 100			50			50		kHz
G = 1000			5			5		kHz
Settling Time 0.01%	2 V step							
G = 5			6			6		µs
G = 10			6			6		µs
G = 100			30			30		µs
G = 1000			275			275		µs
Slew Rate[2]	G = 5 to 10		0.6			0.6		V/µs
GAIN[3]	G = 5 + (80 kΩ/R_G)							
Gain Range		5		1000	5		1000	V/V
Gain Error								
G = 5	V_{OUT} = 0.8 V to 1.8 V			0.04			0.04	%
G = 10 to 1000	V_{OUT} = 0.2 V to 2.5 V			0.3			0.3	%
Gain vs. Temperature	T_A = −40°C to +125°C							
G = 5				5			5	ppm/°C
G > 5				−100			−100	ppm/°C
INPUT	−V_S = 0 V; +V_S = 2.7 V to 36 V							
Impedance								
Differential			0.8‖2			0.8‖2		GΩ‖pF
Common Mode			0.4‖2			0.4‖2		GΩ‖pF
Operating Voltage Range[4]	T_A = +25°C	−0.1		+V_S − 0.7	−0.1		+V_S − 0.7	V
	T_A = −40°C	−0.15		+V_S − 0.9	−0.15		+V_S − 0.9	V
	T_A = +125°C	−0.05		+V_S − 0.6	−0.05		+V_S − 0.6	V
Overvoltage Range	T_A = −40°C to +125°C	+V_S − 40		−V_S + 40	+V_S − 40		−V_S + 40	V
OUTPUT								
Output Swing	T_A = −40°C to +125°C							
R_L = 2 kΩ to 1.35 V		0.2		+V_S − 0.2	0.2		+V_S − 0.2	V
R_L = 10 kΩ to 1.35 V		0.1		+V_S − 0.1	0.1		+V_S − 0.1	V
Short-Circuit Current			13			13		mA
POWER SUPPLY								
Operating Range	Single-supply operation	2.2		36	2.2		36	V
Quiescent Current	+V_S = 2.7 V							
	T_A = +25°C		325	400		325	400	µA
	T_A = −40°C		250	325		250	325	µA
	T_A = +85°C		425	500		425	500	µA
	T_A = +125°C		475	550		475	550	µA
TEMPERATURE RANGE		−40		+125	−40		+125	°C

[1] Input stage uses pnp transistors, so input bias current always flows into the part.
[2] At high gains, the part is bandwidth limited rather than slew rate limited.
[3] For G > 5, gain error specifications do not include the effects of External Resistor R_G.
[4] Input voltage range of the AD8227 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See the Input Voltage Range section for more information.

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ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current	Indefinite
Maximum Voltage at −IN or +IN	$-V_S$ + 40 V
Minimum Voltage at −IN or +IN	$+V_S$ − 40 V
REF Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature	140°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device in free air.

Table 5.

Package	θ_{JA}	Unit
8-Lead MSOP, 4-Layer JEDEC Board	135	°C/W
8-Lead SOIC, 4-Layer JEDEC Board	121	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

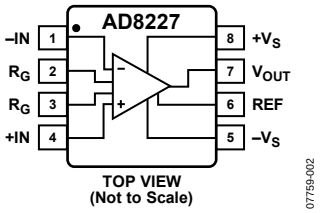

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN	Negative Input.
2, 3	R_G	Gain Setting Pins. Place a gain resistor between these two pins.
4	+IN	Positive Input.
5	$-V_S$	Negative Supply.
6	REF	Reference. This pin must be driven by low impedance.
7	V_{OUT}	Output.
8	$+V_S$	Positive Supply.

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TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, V_S = ±15 V, R_L = 10 kΩ, unless otherwise noted.

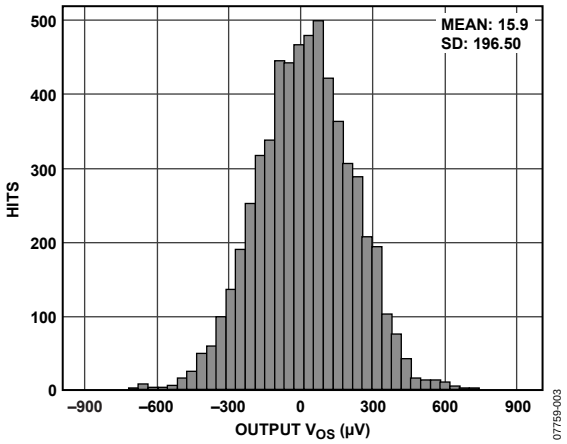

Figure 3. Typical Distribution of Output Offset Voltage

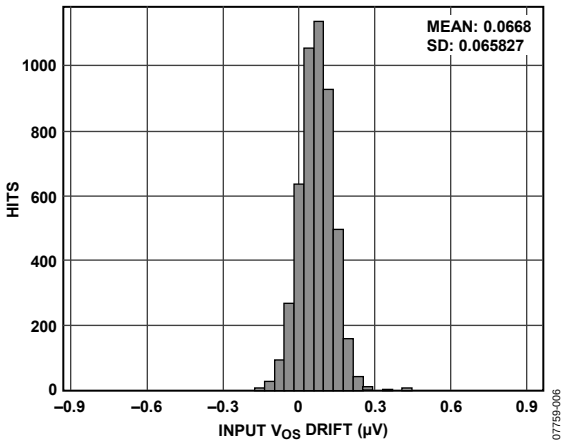

Figure 6. Typical Distribution of Input Offset Voltage Drift, G = 100

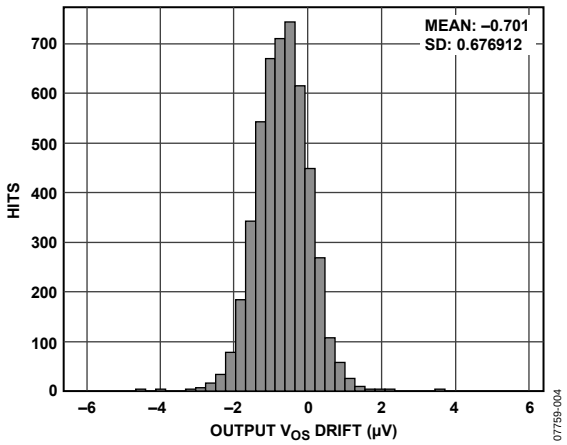

Figure 4. Typical Distribution of Output Offset Voltage Drift

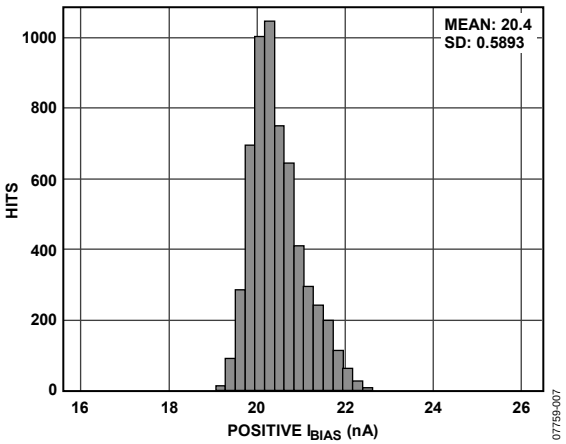

Figure 7. Typical Distribution of Input Bias Current

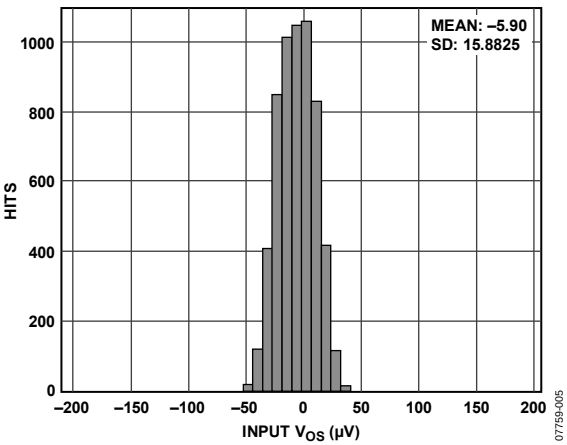

Figure 5. Typical Distribution of Input Offset Voltage

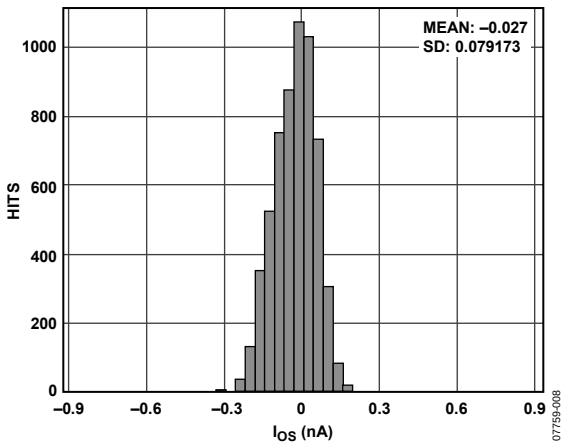

Figure 8. Typical Distribution of Input Offset Current

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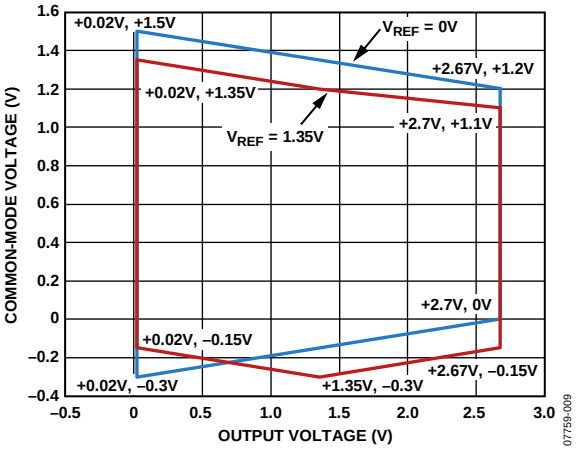

Figure 9. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = 2.7 V, G = 5

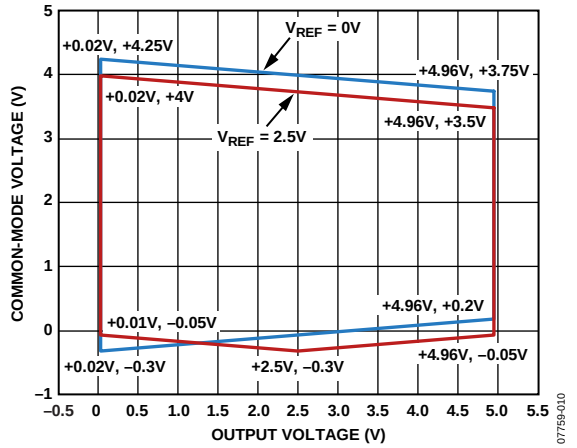

Figure 10. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = 5 V, G = 5

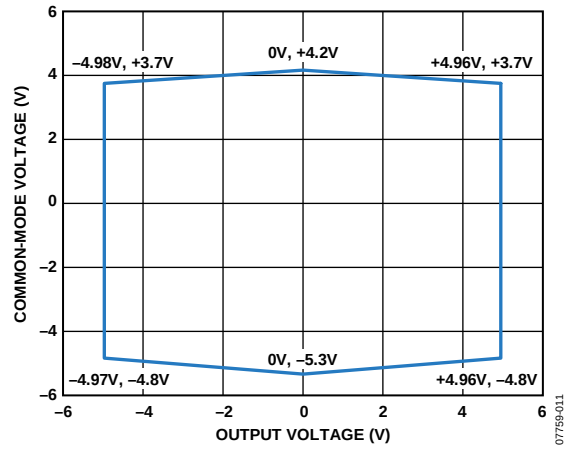

Figure 11. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±5 V, G = 5

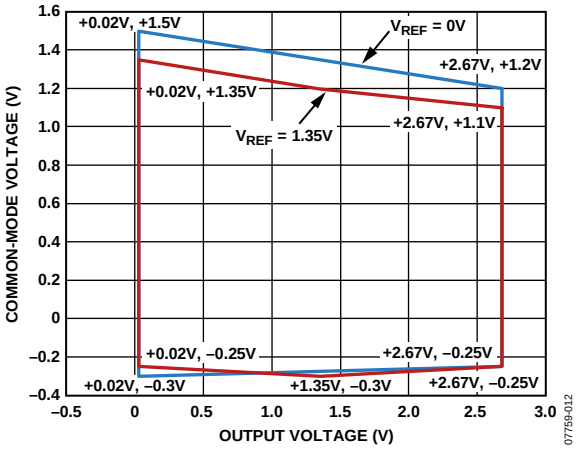

Figure 12. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = 2.7 V, G = 100

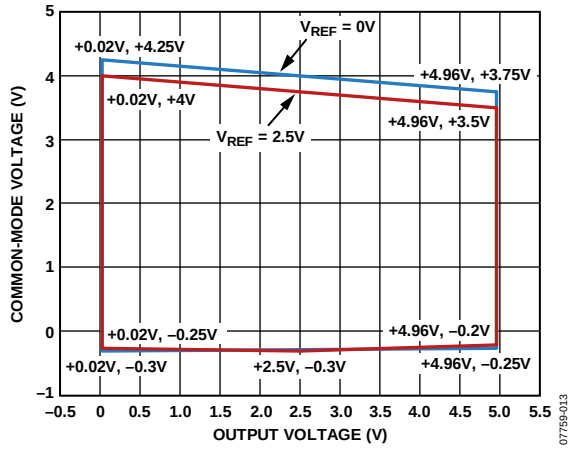

Figure 13. Input Common-Mode Voltage vs. Output Voltage, Single Supply, V_S = 5 V, G = 100

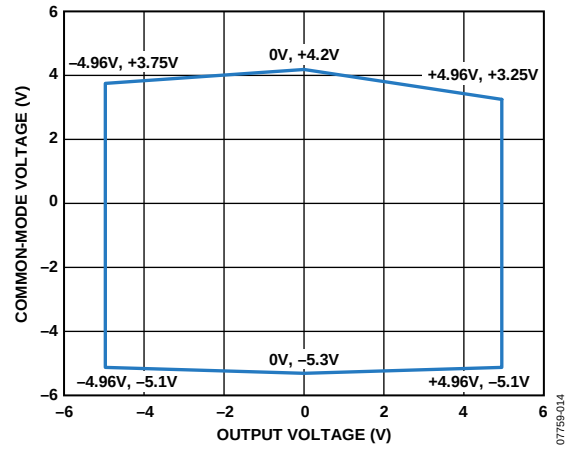

Figure 14. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±5 V, G = 100

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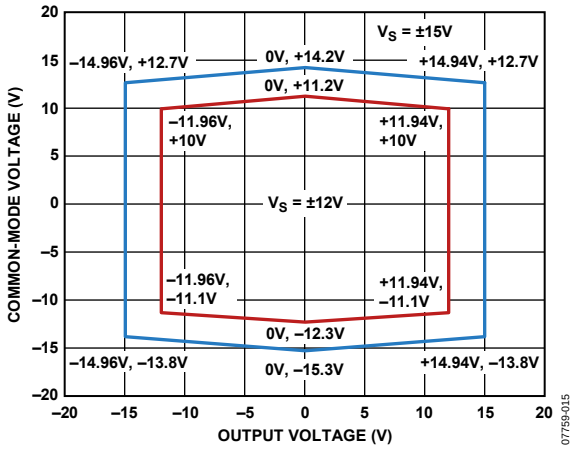

Figure 15. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±15 V, G = 5

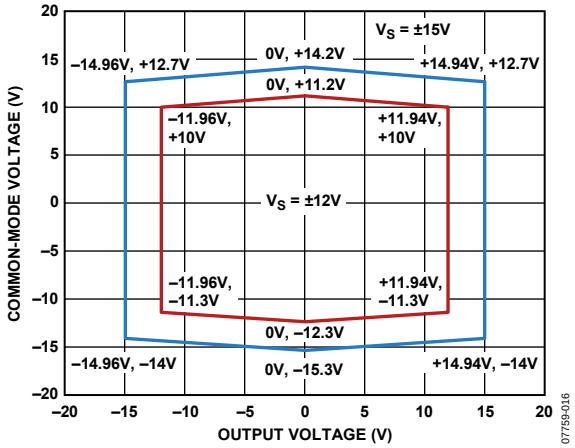

Figure 16. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±15 V, G = 100

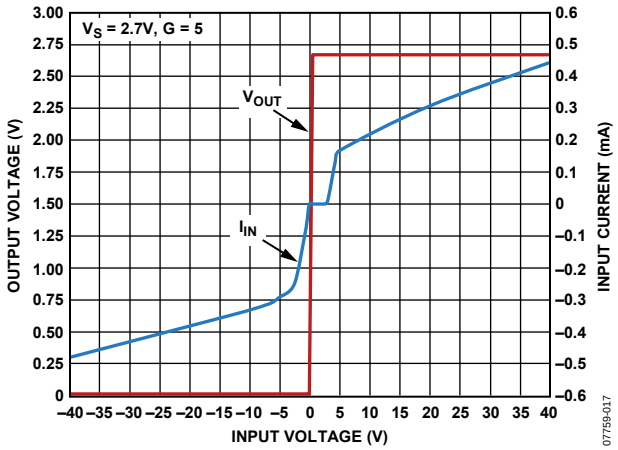

Figure 17. Input Overvoltage Performance, G = 5, V_S = 2.7 V

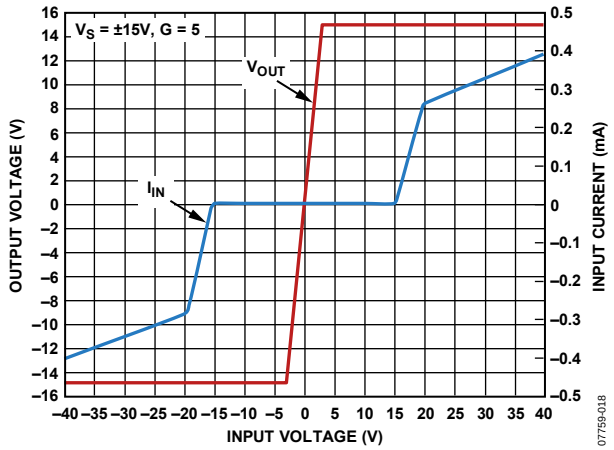

Figure 18. Input Overvoltage Performance, G = 5, V_S = ±15 V

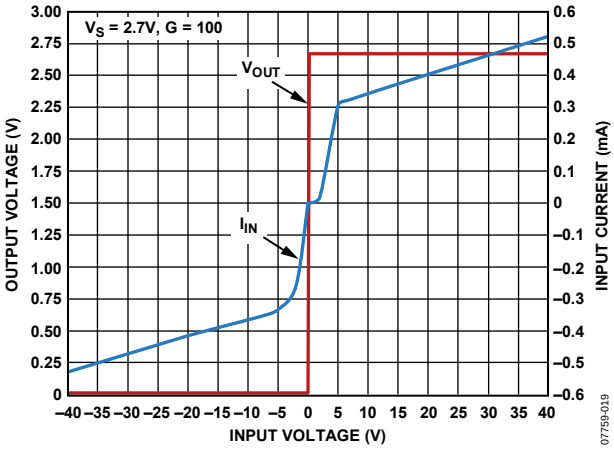

Figure 19. Input Overvoltage Performance, G = 100, V_S = 2.7 V

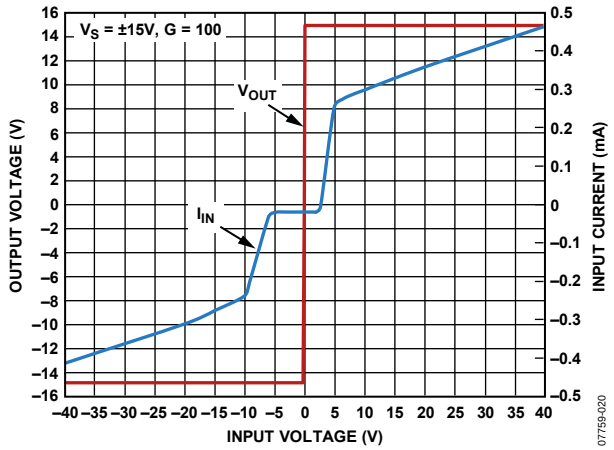

Figure 20. Input Overvoltage Performance, G = 100, V_S = ±15 V

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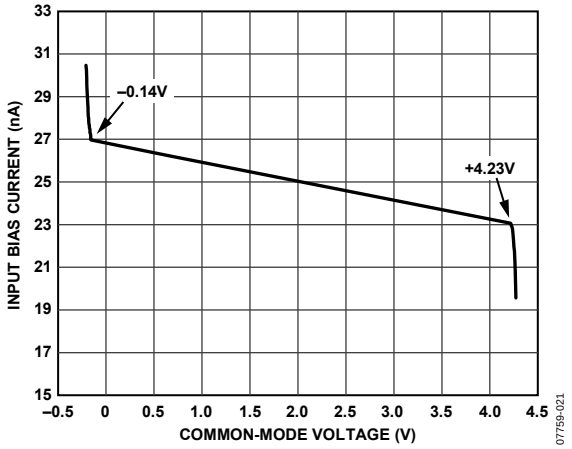

Figure 21. Input Bias Current vs. Common-Mode Voltage, V_S = 5 V

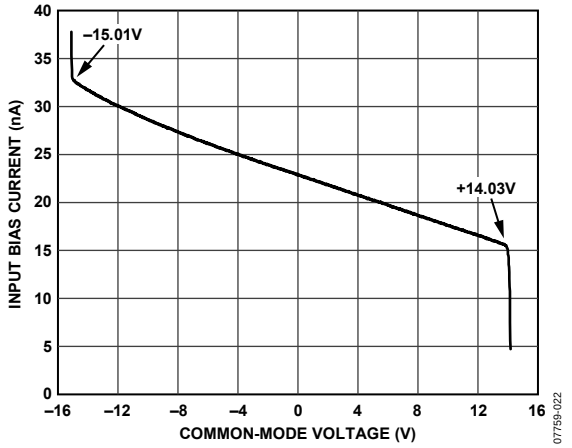

Figure 22. Input Bias Current vs. Common-Mode Voltage, V_S = ±15 V

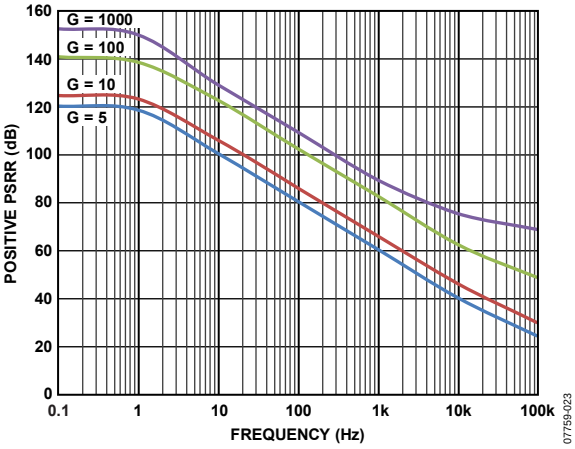

Figure 23. Positive PSRR vs. Frequency, RTI

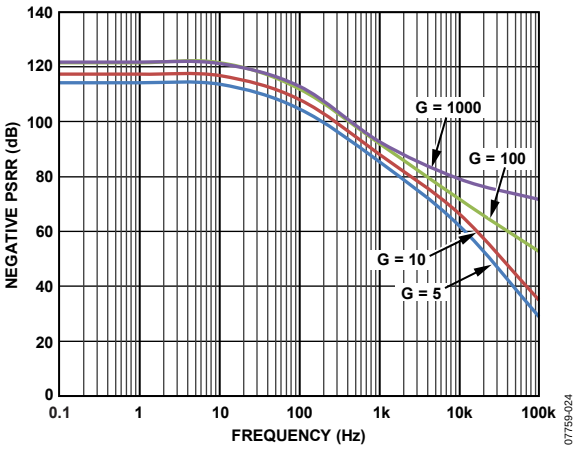

Figure 24. Negative PSRR vs. Frequency

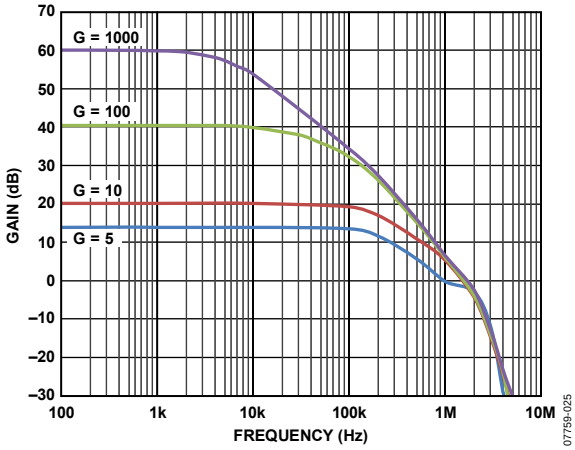

Figure 25. Gain vs. Frequency, V_S = ±15 V

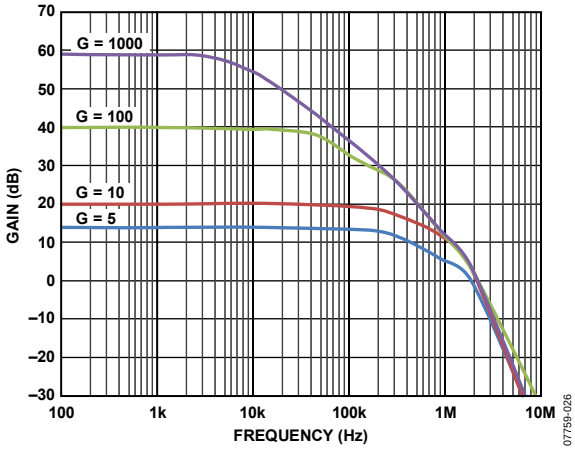

Figure 26. Gain vs. Frequency, V_S = 2.7 V

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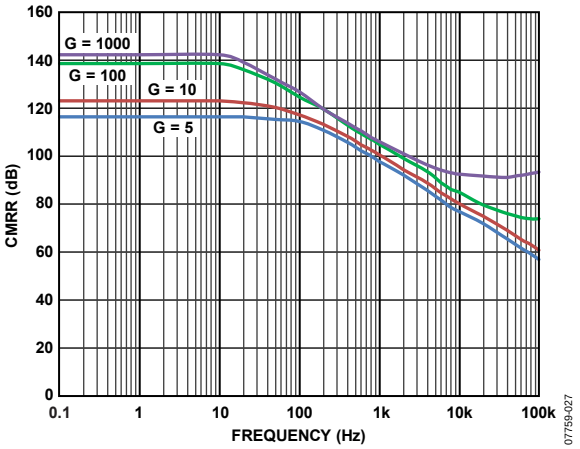

Figure 27. CMRR vs. Frequency, RTI

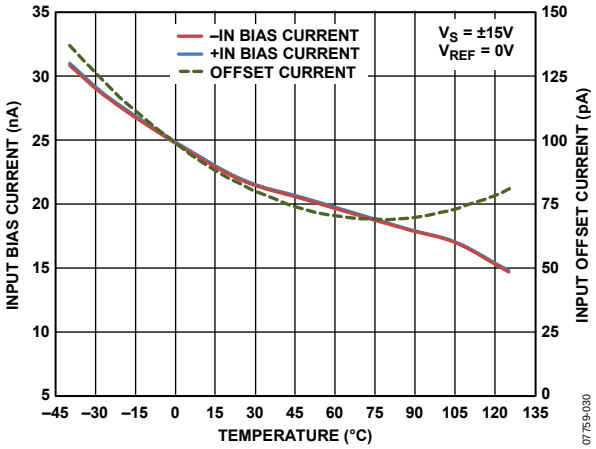

Figure 30. Input Bias Current and Offset Current vs. Temperature

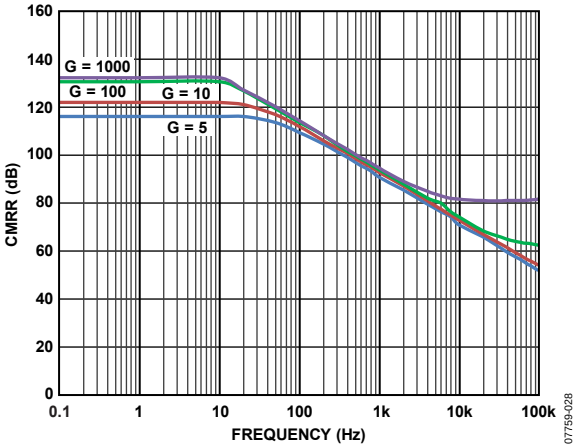

Figure 28. CMRR vs. Frequency, RTI, 1 kΩ Source Imbalance

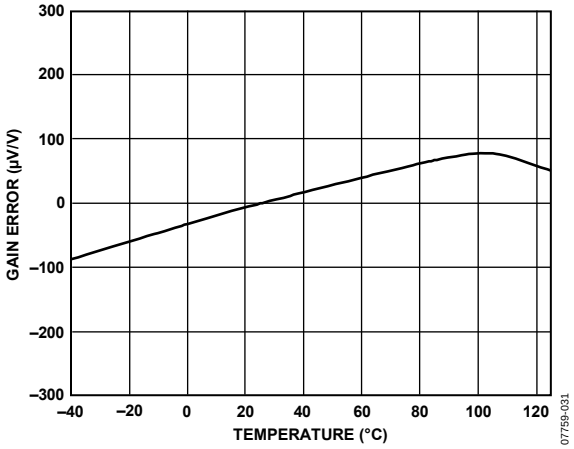

Figure 31. Gain Error vs. Temperature, G = 5

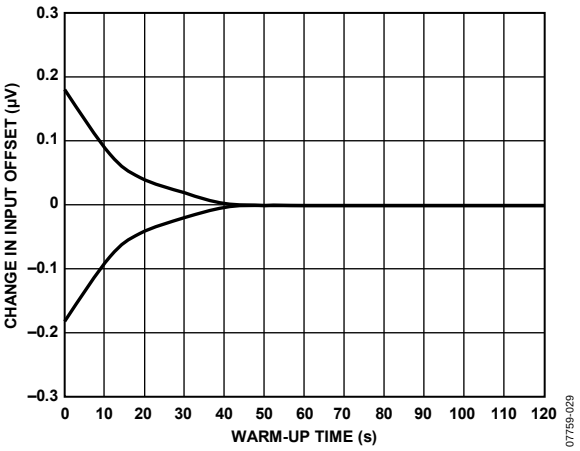

Figure 29. Change in Input Offset Voltage vs. Warm-Up Time

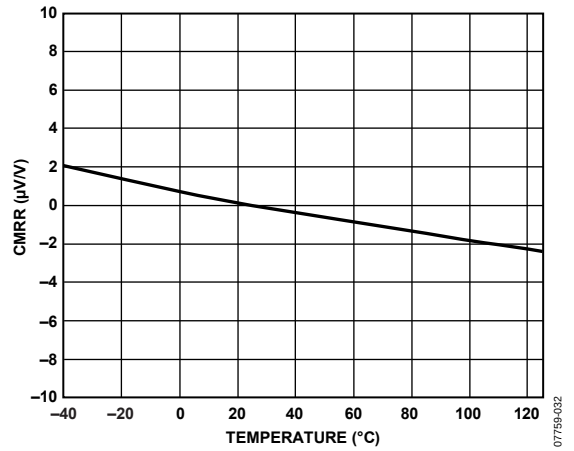

Figure 32. CMRR vs. Temperature, G = 5

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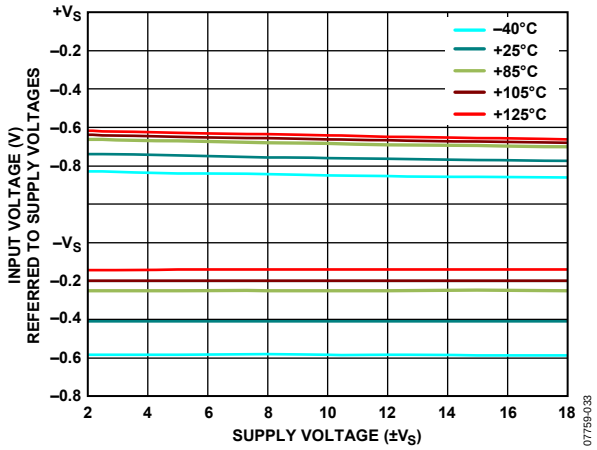

Figure 33. Input Voltage Limit vs. Supply Voltage

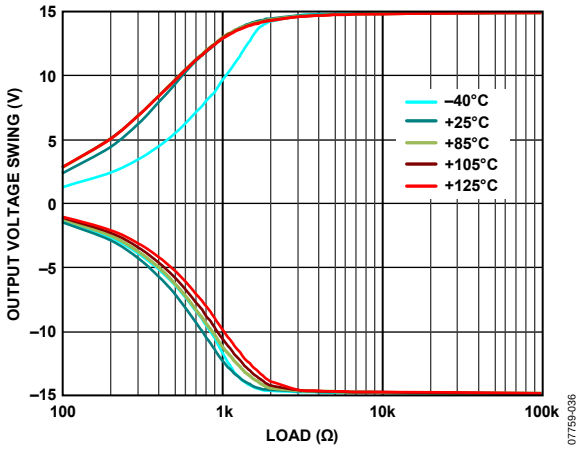

Figure 36. Output Voltage Swing vs. Load Resistance

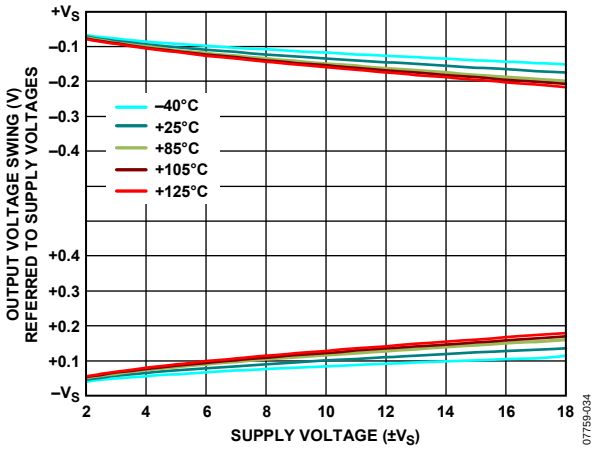

Figure 34. Output Voltage Swing vs. Supply Voltage, R_L = 10 kΩ

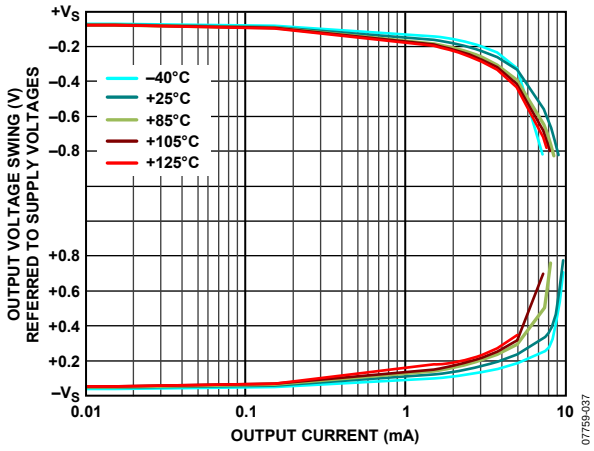

Figure 37. Output Voltage Swing vs. Output Current

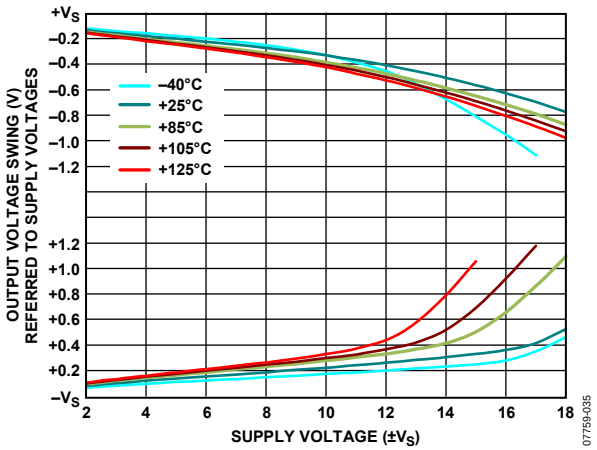

Figure 35. Output Voltage Swing vs. Supply Voltage, R_L = 2 kΩ

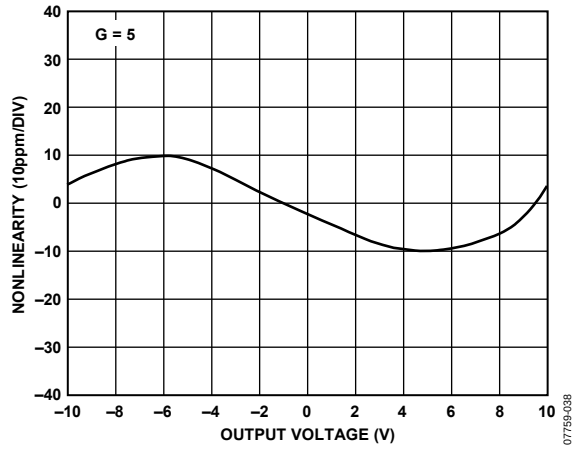

Figure 38. Gain Nonlinearity, G = 5, R_L ≥ 2 kΩ

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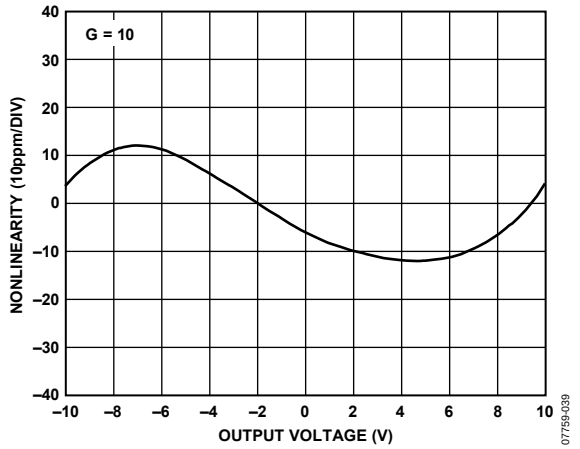

Figure 39. Gain Nonlinearity, G = 10, $R_L \geq 2$ kΩ

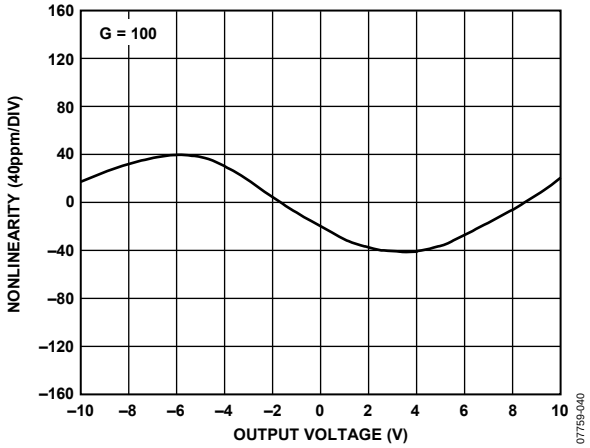

Figure 40. Gain Nonlinearity, G = 100, $R_L \geq 2$ kΩ

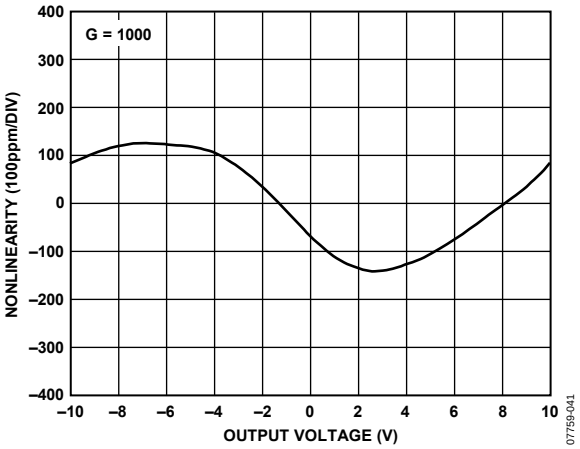

Figure 41. Gain Nonlinearity, G = 1000, $R_L \geq 2$ kΩ

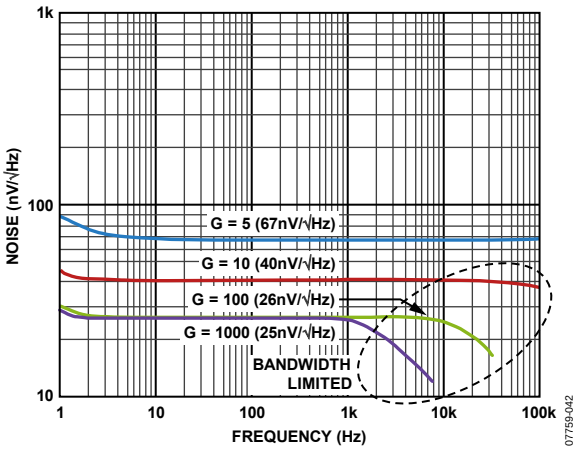

Figure 42. Voltage Noise Spectral Density vs. Frequency

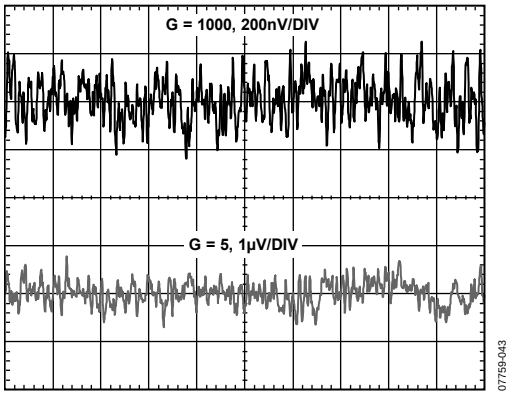

Figure 43. 0.1 Hz to 10 Hz RTI Voltage Noise, G = 5, G = 1000

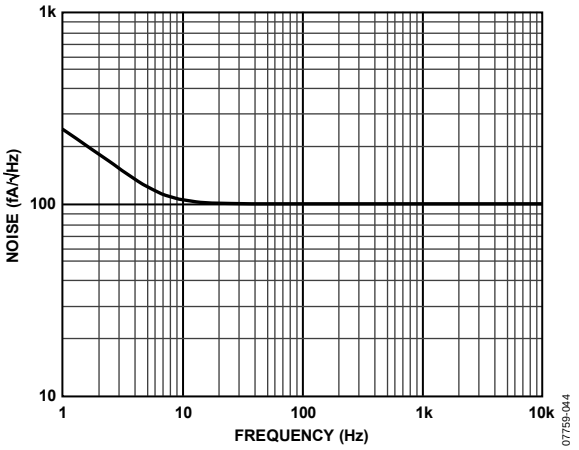

Figure 44. Current Noise Spectral Density vs. Frequency

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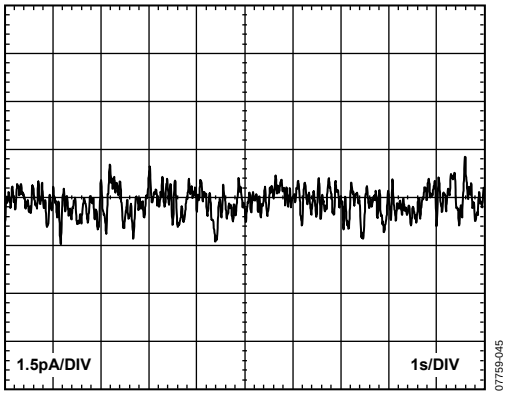

Figure 45. 0.1 Hz to 10 Hz Current Noise

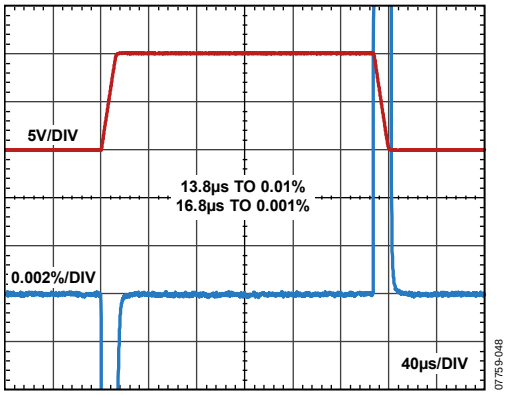

Figure 48. Large-Signal Pulse Response and Settling Time, G = 10, 10 V Step, V_S = ±15 V

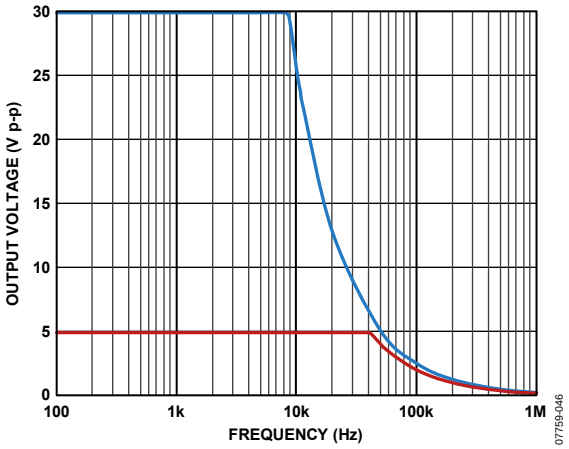

Figure 46. Large-Signal Frequency Response

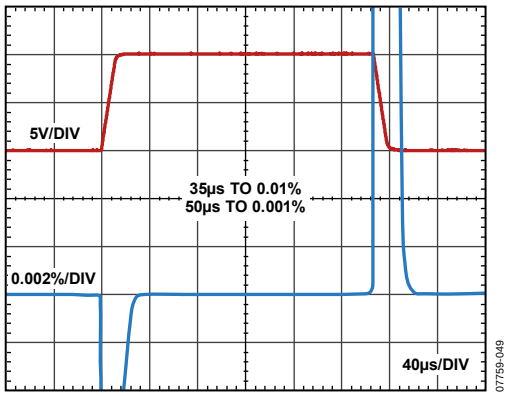

Figure 49. Large-Signal Pulse Response and Settling Time, G = 100, 10 V Step, V_S = ±15 V

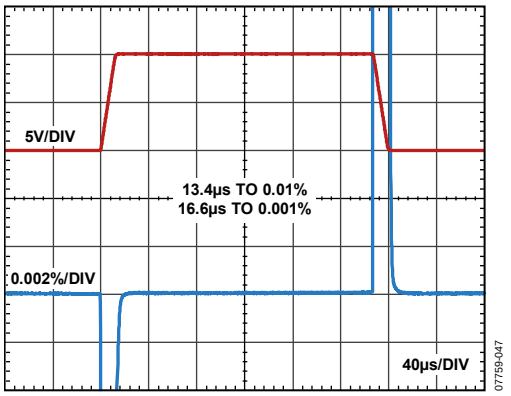

Figure 47. Large-Signal Pulse Response and Settling Time, G = 5, 10 V Step, V_S = ±15 V

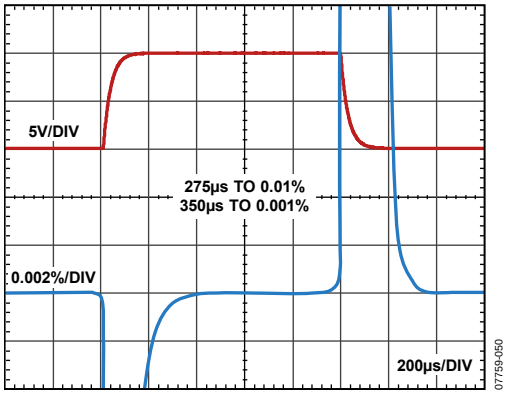

Figure 50. Large-Signal Pulse Response and Settling Time, G = 1000, 10 V Step, V_S = ±15 V

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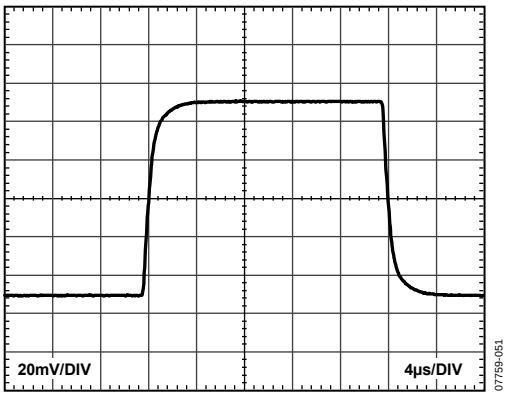

Figure 51. Small-Signal Pulse Response, G = 5, R_L = 10 kΩ, C_L = 100 pF

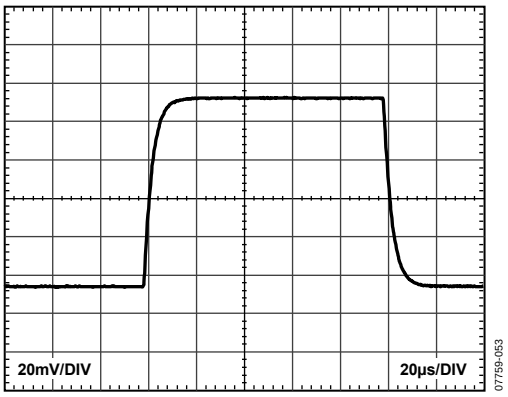

Figure 53. Small-Signal Pulse Response, G = 100, R_L = 10 kΩ, C_L = 100 pF

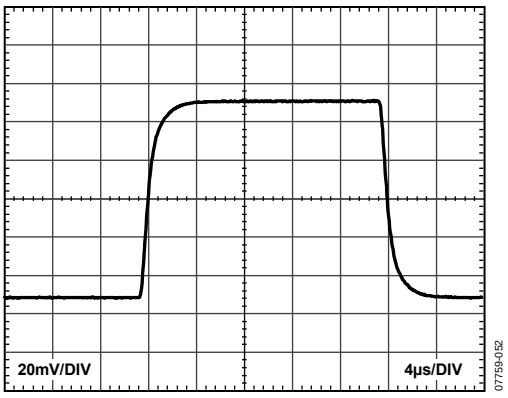

Figure 52. Small-Signal Pulse Response, G = 10, R_L = 10 kΩ, C_L = 100 pF

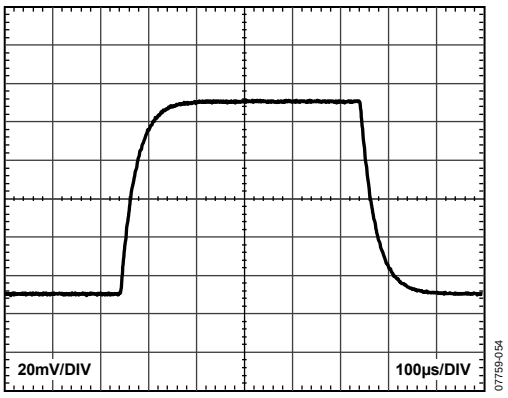

Figure 54. Small-Signal Pulse Response, G = 1000, R_L = 10 kΩ, C_L = 100 pF

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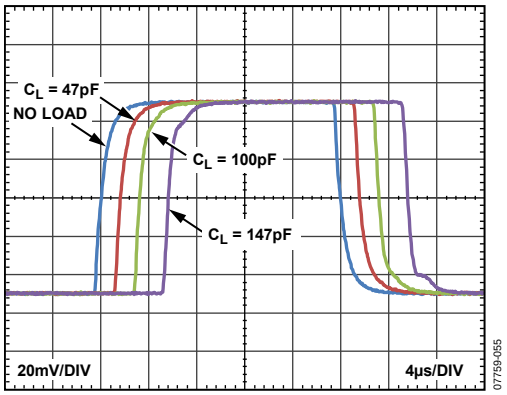

Figure 55. Small-Signal Pulse Response with Various Capacitive Loads, G = 5, R_L = Infinity

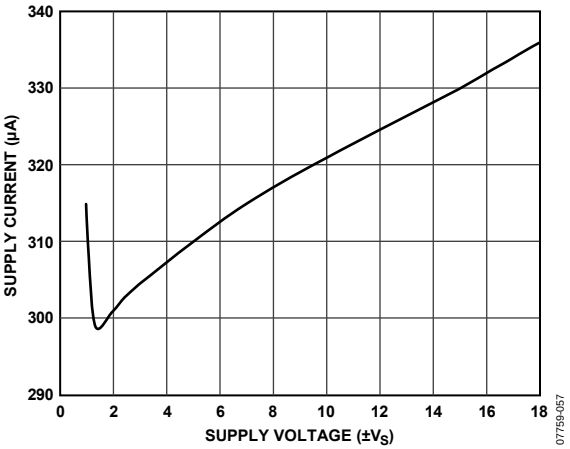

Figure 57. Supply Current vs. Supply Voltage

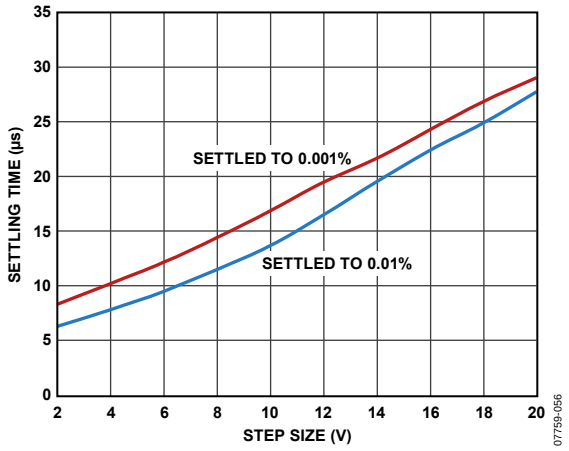

Figure 56. Settling Time vs. Step Size, V_S = ±15 V, Dual Supply

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THEORY OF OPERATION

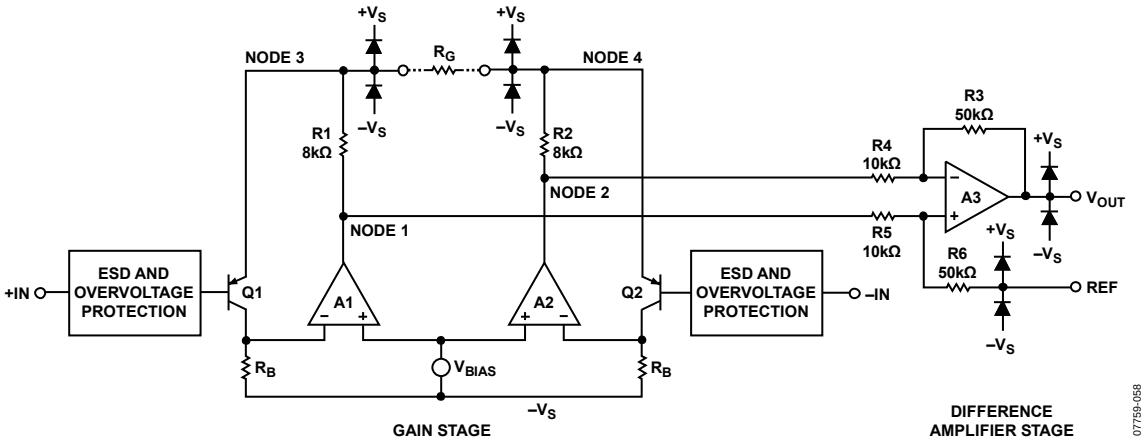

Figure 58. Simplified Schematic

ARCHITECTURE

The AD8227 is based on the classic three op amp topology. This topology has two stages: a preamplifier to provide differential amplification followed by a difference amplifier that removes the common-mode voltage and provides additional amplification. Figure 58 shows a simplified schematic of the AD8227.

The first stage works as follows. To maintain a constant voltage across the bias resistor, R_B, Amplifier A1 must keep Node 3 at a constant diode drop above the positive input voltage. Similarly, Amplifier A2 keeps Node 4 at a constant diode drop above the negative input voltage. Therefore, a replica of the differential input voltage is placed across the gain setting resistor, R_G. The current that flows across this resistance must also flow through the R1 and R2 resistors, creating a gained differential signal between the A2 and A1 outputs. Note that, in addition to a gained differential signal, the original common-mode signal, shifted a diode drop up, is also still present.

The second stage is a difference amplifier, composed of Amplifier A3 and the R3 through R6 resistors. This stage removes the common-mode signal from the amplified differential signal and gains it by 5.

The transfer function of the AD8227 is

$$V_{OUT} = G \times (V_{IN+} - V_{IN-}) + V_{REF}$$

where:

$$G = 5 + \frac{80\ \text{k}\Omega}{R_G}$$

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8227. The gain can be calculated by referring to Table 7 or by using the following gain equation:

$$R_G = \frac{80\ \text{k}\Omega}{G - 5}$$

Table 7. Gains Achieved Using Common Resistor Values

Standard Table Value of R_G	Calculated Gain
No resistor	5
100 kΩ	5.8
49.9 kΩ	6.6
26.7 kΩ	8
20 kΩ	9
16 kΩ	10
10 kΩ	13
5.36 kΩ	19.9
2 kΩ	45
1.78 kΩ	49.9
1 kΩ	85
845 Ω	99.7
412 Ω	199
162 Ω	499
80.6 Ω	998

The AD8227 defaults to G = 5 when no gain resistor is used. The tolerance and gain drift of the R_G resistor should be added to the specifications of the AD8227 to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are minimal.

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REFERENCE TERMINAL

The output voltage of the AD8227 is developed with respect to the potential on the reference terminal. This is useful when the output signal needs to be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8227 can drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For best performance, source impedance to the REF terminal should be kept below 2 Ω. As shown in Figure 58, the reference terminal, REF, is at one end of a 50 kΩ resistor. Additional impedance at the REF terminal adds to this 50 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional R_{REF} can be calculated as follows:

$$6(50\ \text{k}\Omega + R_{REF})/(60\ \text{k}\Omega + R_{REF})$$

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades CMRR.

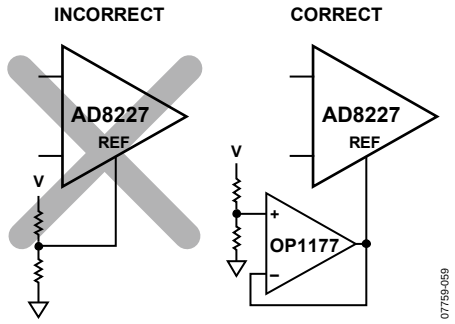

Figure 59. Driving the Reference Pin

INPUT VOLTAGE RANGE

Most instrumentation amplifiers have a very limited output voltage swing when the common-mode voltage is near the upper or lower limit of the part's input range. The AD8227 has very little of this limitation. See Figure 9 through Figure 16 for the input common-mode range vs. output voltage of the part.

LAYOUT

To ensure optimum performance of the AD8227 at the PCB level, care must be taken in the design of the board layout. The pins of the AD8227 are arranged in a logical manner to aid in this task.

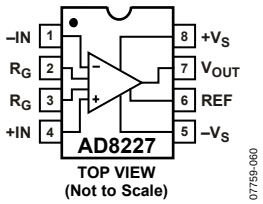

Figure 60. Pinout Diagram

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signals to be converted to differential signals before reaching the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To keep CMRR over frequency high, the input source impedance and capacitance of each path should be closely matched. Additional source resistance in the input path (for example, for input protection) should be placed close to the in-amp inputs, which minimizes the interaction of the source resistance with parasitic capacitance from the PCB traces.

Parasitic capacitance at the gain setting pins can also affect CMRR over frequency. If the board design has a component at the gain setting pins (for example, a switch or jumper), the component should be chosen so that the parasitic capacitance is as small as possible.

Power Supplies

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. See the PSRR performance curves in Figure 23 and Figure 24 for more information.

A 0.1 µF capacitor should be placed as close as possible to each supply pin. As shown in Figure 61, a 10 µF tantalum capacitor can be used farther away from the part. In most cases, it can be shared by other precision integrated circuits.

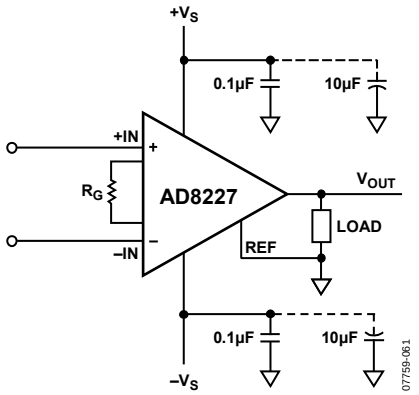

Figure 61. Supply Decoupling, REF, and Output Referred to Local Ground

References

The output voltage of the AD8227 is developed with respect to the potential on the reference terminal. Care should be taken to tie REF to the appropriate local ground.

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INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8227 must have a return path to ground. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 62.

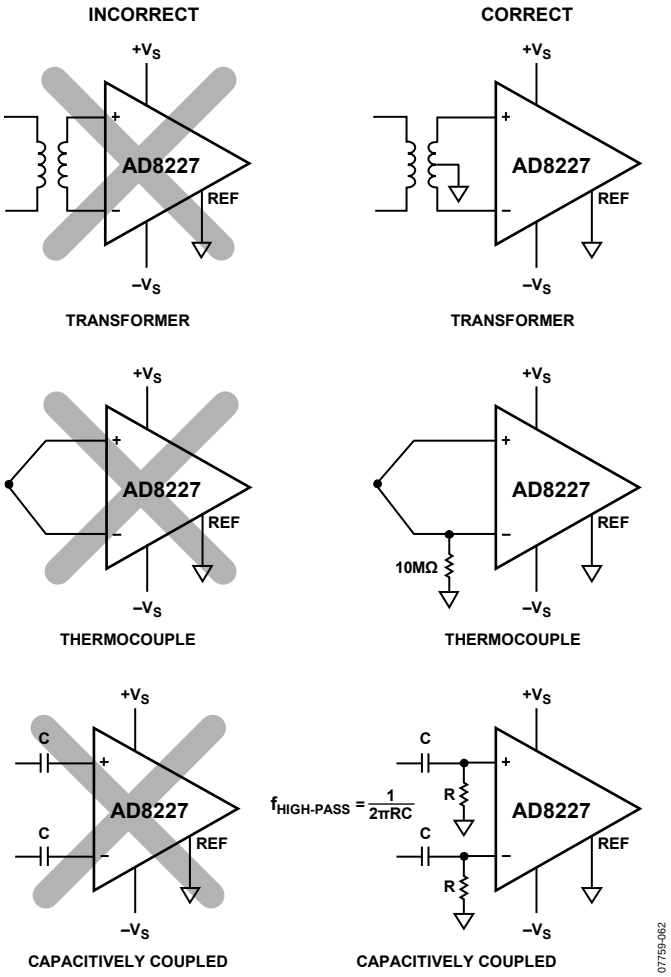

Figure 62. Creating an Input Bias Current Return Path

INPUT PROTECTION

The AD8227 has very robust inputs and typically does not need additional input protection. Input voltages can be up to 40 V from the opposite supply rail. For example, with a +5 V positive supply and a −8 V negative supply, the part can safely withstand voltages from −35 V to +32 V. Unlike some other instrumentation amplifiers, the part can handle large differential input voltages even when the part is in high gain. Figure 17 through Figure 20 show the behavior of the part under overvoltage conditions.

The other AD8227 terminals should be kept within the supplies. All terminals of the AD8227 are protected against ESD.

For applications where the AD8227 encounters voltages beyond the allowed limits, external current limiting resistors and low leakage diode clamps such as the BAV199L, the FJH1100s, or the SP720 should be used.

RADIO FREQUENCY INTERFERENCE (RFI)

RF rectification is often a problem when amplifiers are used in applications that have strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass RC network placed at the input of the instrumentation amplifier, as shown in Figure 63. The filter limits the input signal bandwidth, according to the following relationship:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFrequency_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10\ C_C$.

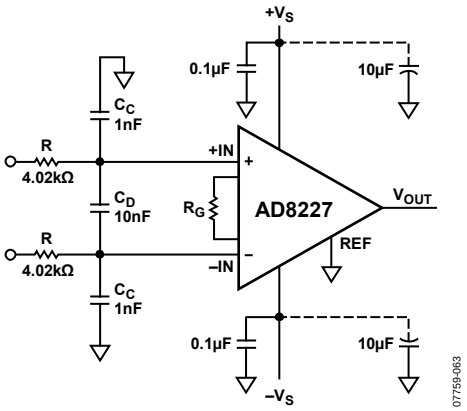

Figure 63. RFI Suppression

C_D affects the differential signal and C_C affects the common-mode signal. Values of R and C_C should be chosen to minimize RFI. A mismatch between R × C_C at the positive input and R × C_C at the negative input degrades the CMRR of the AD8227. By using a value of C_D one magnitude larger than C_C, the effect of the mismatch is reduced, and performance is improved.

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APPLICATIONS INFORMATION

DIFFERENTIAL DRIVE

Figure 64 shows how to configure the AD8227 for differential output.

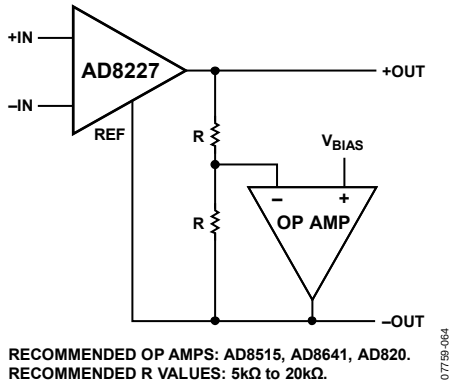

Figure 64. Differential Output Using an Op Amp

The differential output is set by the following equation:

$$V_{DIFF\_OUT} = V_{OUT+} - V_{OUT-} = Gain \times (V_{IN+} - V_{IN-})$$

The common-mode output is set by the following equation:

$$V_{CM\_OUT} = (V_{OUT+} - V_{OUT-})/2 = V_{BIAS}$$

The advantage of this circuit is that the dc differential accuracy depends on the AD8227 and not on the op amp or the resistors. This circuit takes advantage of the AD8227's precise control of its output voltage relative to the reference voltage. Op amp dc performance and resistor matching affect the dc common-mode output accuracy. However, because common-mode errors are likely to be rejected by the next device in the signal chain, these errors typically have little effect on overall system accuracy.

Tips for Best Differential Output Performance

For best ac performance, an op amp with at least 2 MHz gain bandwidth and 1 V/µs slew rate is recommended. Good choices for op amps are the AD8641, AD8515, or AD820.

Keep trace lengths from resistors to the inverting terminal of the op amp as short as possible. Excessive capacitance at this node can cause the circuit to be unstable. If capacitance cannot be avoided, use lower value resistors.

PRECISION STRAIN GAGE

The low offset and high CMRR over frequency of the AD8227 make it an excellent choice for bridge measurements. The bridge can be connected directly to the inputs of the amplifier (see Figure 65).

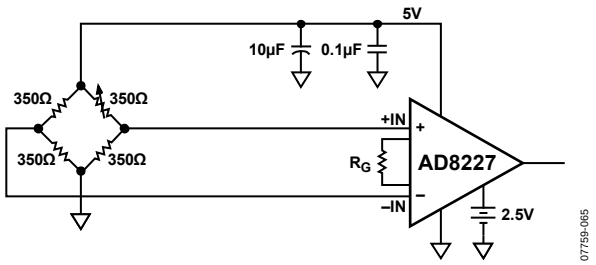

Figure 65. Precision Strain Gage

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DRIVING AN ADC

Figure 66 shows several different methods for driving an ADC. The ADC in the ADuC7026 microcontroller was chosen for this example because it has an unbuffered charge sampling architecture that is typical of most modern ADCs. This type of architecture typically requires an RC buffer stage between the ADC and the amplifier to work correctly.

Option 1 shows the minimum configuration required to drive a charge sampling ADC. The capacitor provides charge to the ADC sampling capacitor, and the resistor shields the AD8227 from the capacitance. To keep the AD8227 stable, the RC time constant of the resistor and capacitor needs to stay above 5 µs. This circuit is mainly useful for lower frequency signals.

Option 2 shows a circuit for driving higher frequency signals. It uses a precision op amp (AD8616) with relatively high bandwidth and output drive. This amplifier can drive a resistor and capacitor with a much higher time constant and is, therefore, suited for higher frequency applications.

Option 3 is useful for applications where the AD8227 needs to run off a large voltage supply but drives a single-supply ADC. In normal operation, the AD8227 output stays within the ADC range, and the AD8616 simply buffers it. However, in a fault condition, the output of the AD8227 may go outside the supply range of both the AD8616 and the ADC. This is not an issue in the circuit, because the 10 kΩ resistor between the two amplifiers limits the current into the AD8616 to a safe level.

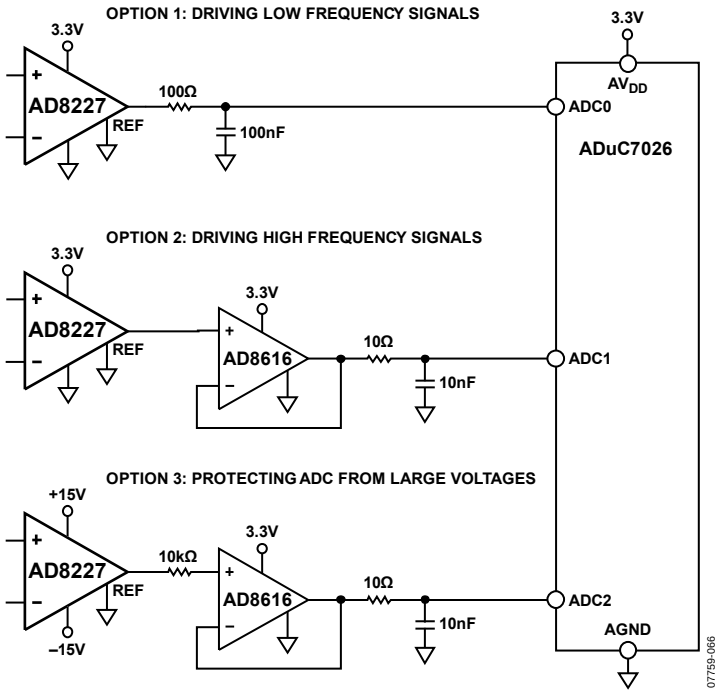

Figure 66. Driving an ADC

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OUTLINE DIMENSIONS

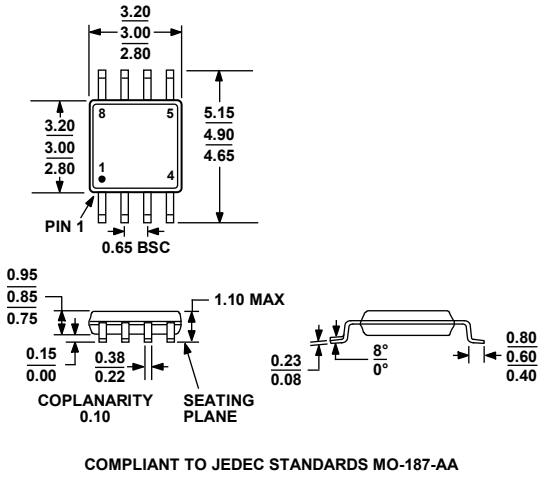

Figure 67. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

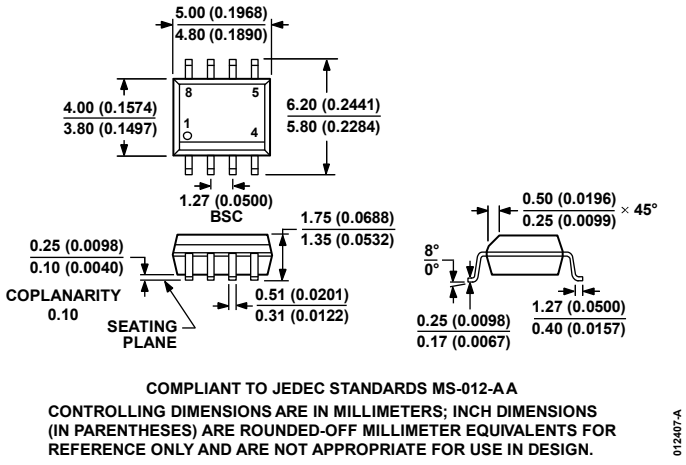

Figure 68. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8227ARMZ[1]	−40°C to +125°C	8-Lead MSOP	RM-8	Y1S
AD8227ARMZ-RL[1]	−40°C to +125°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y1S
AD8227ARMZ-R7[1]	−40°C to +125°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y1S
AD8227ARZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8227ARZ-RL[1]	−40°C to +125°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8227ARZ-R7[1]	−40°C to +125°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8227BRMZ[1]	−40°C to +125°C	8-Lead MSOP	RM-8	Y1U
AD8227BRMZ-RL[1]	−40°C to +125°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y1U
AD8227BRMZ-R7[1]	−40°C to +125°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y1U
AD8227BRZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8227BRZ-RL[1]	−40°C to +125°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8227BRZ-R7[1]	−40°C to +125°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	

[1] Z = RoHS Compliant Part.

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