Selection Guide

Part Number	Packing	Package
A6268KLPTR-T	4000 pieces per 13-in. reel	16-pin TSSOP with exposed thermal pad

Absolute Maximum Ratings With respect to GND at T_A = 25°C, unless otherwise specified

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{IN}		–0.3 to 50	V
Pins FF1, EN			–0.3 to 50	V
Pins FF2, CKOUT			–0.3 to 6.5	V
Pin OSC			–0.3 to 6.5	V
Pin SG			–0.3 to 6.5	V
Pins LA, LN			–0.3 to 50	V
Pin LF		With respect to LA	–6 to 6	V
Pin LP		With respect to LN	–6 to 6	V
Pin SP, SN			–0.3 to 5	V
Pin VREG			–0.3 to 7	V
Pin IREF			–0.3 to 7	V
Junction Temperature	T_J(max)		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A	Range K	–40 to 150	°C

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	34	°C/W
		On 2-layer PCB with 3.8 in.^{2} of copper area each side	43	°C/W
Package Thermal Resistance (Junction to Exposed Pad)	$R_{\theta JP}$		2	°C/W

*Additional thermal information available on the Allegro website

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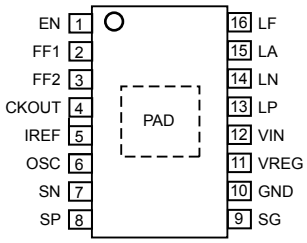
Pinout Diagram



Terminal List Table

Number	Name	Function
1	EN	Enable chip
2	FF1	Fault flag
3	FF2	Fault flag
4	CKOUT	Oscillator output, with phase shift
5	IREF	Current reference
6	OSC	Oscillator input/frequency set
7	SN	Switch current sense –ve input
8	SP	Switch current sense +ve input
9	SG	Switch gate drive
10	GND	Ground
11	VREG	Internal regulator capacitor
12	VIN	Main supply
13	LP	Load current sense +ve input
14	LN	Load current sense –ve input
15	LA	LED string voltage sense
16	LF	Reference LED voltage sense
–	PAD	Exposed thermal pad

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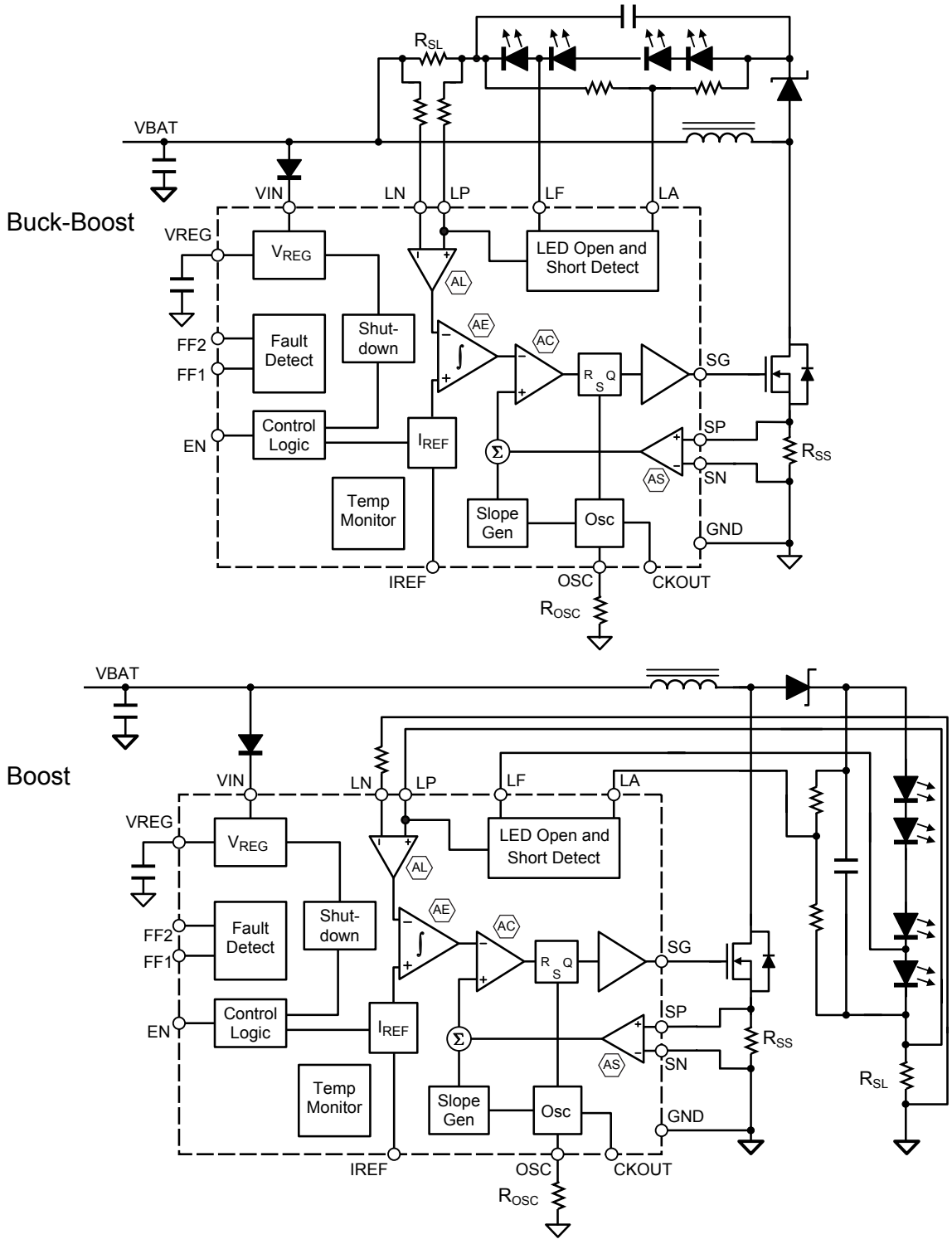
Functional Block Diagrams



AL AE AC AS See Functional Description section.

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ELECTRICAL CHARACTERISTICS[1] Valid at T_J = –40°C to 150°C, V_{IN} = 5 to 40 V; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply and Reference						
V_{IN} Functional Operating Range[2]			5	–	50	V
V_{IN} Quiescent Current	I_{INQ}	SG open circuit	–	–	8	mA
	I_{INS}	EN = GND	–	4	10	µA
VREG Output Voltage	V_{REG}	I_{REG} = 0 to 2 mA, V_{IN} ≥ 5.3 V	4.85	5	5.15	V
		I_{REG} = 2 mA, V_{IN} = 5 V	4.7	–	–	V
VREG Current Limit	V_{REGCL}		25	–	–	mA
Gate Output Drive						
Turn-On Time	t_r	C_{LOAD} = 1 nF, 20% to 80%	–	30	–	ns
Turn-Off Time	t_f	C_{LOAD} = 1 nF, 80% to 20%	–	30	–	ns
Maximum Duty Cycle	D	$t_{ON} \times f_{OSC}$	80	85	–	%
Pull-Up On Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GHx} = –100 mA	–	1.7	–	Ω
		T_J = 150°C, I_{GHx} = –100 mA	–	–	3.5	Ω
Pull-Down On Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GLx} = 100 mA	–	0.75	–	Ω
		T_J = 150°C, I_{GLx} = 100 mA	–	–	1.5	Ω
Output High Voltage	V_{SGH}	I_{SG} = –100 µA	V_{REG} – 0.1	–	V_{REG}	V
Output Low Voltage	V_{SGL}	I_{SG} = 100 µA	–	–	0.1	V
Logic Inputs and Outputs						
Fault Output (Open Drain)	V_{OL}	I_{OL} = 1 mA, fault not asserted	–	–	0.4	V
Fault Output FF1 Sink Current	$I_{OH(snk)}$	0.4 V < V_O < 50 V, fault not asserted	–	1.3	–	mA
Fault Output FF1 Leakage Current[1]	$I_{OH1(lkg)}$	V_O = 12 V, fault asserted	–1	–	1	µA
Fault Output FF2 Leakage Current[1]	$I_{OH2(lkg)}$	V_O = 5 V, fault asserted	–5	–	5	µA
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}		2	–	–	V
Input Hysteresis	V_{Ihys}		120	180	–	mV
Enable Input Internal Clamp Voltage	V_{ENC}		–	8.4	–	V
Enable Input Current Limit Resistor	R_{EN}	Between EN and internal clamp	–	200	–	kΩ
Boost Mode Select Voltage	V_{LNB}	Defined by V_{LN}	–	–	0.8	V
Buck-Boost Mode Select Voltage	V_{LNBB}	Defined by V_{LN}	3.5	–	–	V
Disable Time	t_{DIS}	f_{OSC} = 350 kHz	–	94	–	ms

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ELECTRICAL CHARACTERISTICS[1] (continued) Valid at T_J = –40°C to 150°C, V_{IN} = 5 to 40 V; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Oscillator						
Oscillator Frequency	f_{OSC}	R_{OSC} = 43 kΩ	–	500	–	kHz
		R_{OSC} = 62 kΩ	315	350	385	kHz
		R_{OSC} = V_{REG}	–	350	–	kHz
Minimum Oscillator Frequency[3]	f_{MIN}		90	–	–	kHz
OSC Pin Voltage	V_{OSC}	R_{OSC} = 62 kΩ	1.15	1.2	1.25	V
CKOUT Output Delay	t_{DC}	OSC input rise to CKOUT rise	–	150	–	ns
OSC Input Low Voltage	V_{OIL}		–	–	0.8	V
OSC Input High Voltage	V_{OIH}		3.5	–	–	V
OSC Input Hysteresis	V_{Oihys}		300	600	–	mV
OSC Watchdog Period	t_{OSWD}	Between successive rising edges	7	–	–	µs
CKOUT Output High Voltage	V_{COH}	I_{OH} = –1 mA	V_{REG} – 1	–	V_{REG}	V
CKOUT Output Low Voltage	V_{COL}	I_{OL} = 1 mA	–	–	0.4	V
LED Current Sense						
Input Bias Current LN (BB mode)[4]	I_{LN}	LP = LN = 12 V	–	130	–	µA
Input Bias Current LP (BB mode)[4]	I_{LP}	LP = LN = 12 V	–	125	–	µA
Input Bias Current LN (B mode)[1,4]	I_{LN}	LP = LN = 0 V	–	–1.0	–	µA
Input Bias Current LP (B mode)[1,4]	I_{LP}	LP = LN = 0 V	–	–12	–	µA
Differential Input Voltage (Active)	V_{IDL}	EN = High, V_{IDL} = V_{LP} – V_{LN}	–	100	–	mV
Input Common-Mode Range (BB mode)[4]	V_{CMLH}	V_{LP} = V_{LN}	V_{IN}	–	V_{IN} + 1	V
Input Common-Mode Range (B mode)[4]	V_{CMLL}	V_{LP} = V_{LN}	0	–	1	V
Current Error	E_{ISL}	[(10 × I_{LED} × R_{SL}) – 1] × 100	–5	–	5	%
Switch Current Sense						
Input Bias Current	I_{BIASS}	SP = SN = 0 to 2 V	–30	–	–	µA
Maximum Differential Input Voltage[3]	V_{IDS}	V_{IDS} = V_{SP} – V_{SN} with D = 50%	110	150	200	mV
Input Source Current	I_{INS}	V_{IDS} = 120 mV	–	120	–	µA
Input Common-Mode Range	V_{CMS}	V_{SP} = V_{SN}	0	–	2	V
Diagnostics and Protection						
Fault Blank Timer[5]	t_{FB}	Start-up	–	3	–	ms
VIN Undervoltage Turn-Off	V_{INUV}	Decreasing V_{IN}	–	–	4.6	V
VIN Undervoltage Hysteresis	$V_{INUVhys}$		200	–	400	mV
VREG Undervoltage Turn-Off	V_{REGUV}	Decreasing V_{REG}	2.9	3.65	4.4	V
VREG Undervoltage Hysteresis	$V_{REGUVhys}$		170	300	400	mV

Continued on the next page…

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ELECTRICAL CHARACTERISTICS[1] (continued) Valid at T_J = –40°C to 150°C, V_{IN} = 5 to 40 V; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Diagnostics and Protection (continued)						
LED String Short Voltage	V_{SCL}		350	475	600	mV
Non-Reference LED Short Offset Voltage	V_{SCO}		150	225	300	mV
Reference LED Short Offset Voltage	V_{SCOR}		350	475	600	mV
LED Open Voltage	V_{OCL}		5	5.5	6	V
LF Bias Current (BB mode)[3]	I_{LF}	LF = LA = VIN + 1.7 V	–	50	–	µA
LA Bias Current (BB mode)[3]	I_{LA}	LF = LA = VIN + 1.7 V	–	90	–	µA
LF Bias Current (B mode)[3]	I_{LF}	LF = 1.7 V	–	8	–	µA
LA Bias Current (B mode)[3]	I_{LA}	LA = 1.7 V	–	24	–	µA
LED Undercurrent Voltage Difference[6]	V_{UCL}		–	1	–	mV
LED Overcurrent Voltage Difference[7]	V_{OVCL}		–	1	–	mV
LED Sense Resistor Negative Overcurrent Threshold[8]	V_{NOCL}	$V_{NOCL} = V_{LP} – V_{LN}$	–	–200	–	mV
Open Fault Time-Out	t_{OTO}	f_{OSC} = 350 kHz	–	94	–	ms
Overtemperature Shutdown Threshold	T_{JF}	Temperature increasing	–	170	–	°C
Overtemperature Hysteresis	T_{Jhys}	Recovery = $T_{JF} – T_{Jhys}$	–	15	–	°C

[1]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2]Function is correct but parameters are not guaranteed below the general limit (5 V).
[3]Parameters ensured by design.
[4]BB mode = buck-boost (supply-referenced) mode, B mode = boost (ground-referenced) mode.
[5]Fault Blank timer not enabled for open-LED condition.
[6]Undercurrent when $V_{SENSEL} < V_{IDL} – V_{UCL}$, where V_{SENSEL} is the voltage across the LED current sense resistor R_{SL}.
[7]Overcurrent when $V_{SENSEL} > V_{IDL} + V_{OVCL}$, where V_{SENSEL} is the voltage across the LED current sense resistor R_{SL}.
[8]Protection only provided in buck-boost mode with LED cathode (LP) connection shorted to ground.

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Functional Description

The A6268 is a DC-DC converter controller that is designed to drive series-connected high-power LEDs in automotive applications. It provides programmable constant current output at load voltages and currents limited only by the external components. For automotive applications optimum performance is achieved when driving up to 15 LEDs at currents up to 1 A.

The A6268 can be configured as a standard boost converter or as a supply referenced boost converter. In the supply referenced configuration the load voltage is the difference between the boost voltage and the supply voltage. This difference can be greater than, equal to, or less than the supply voltage, effectively providing a buck-boost capability. This configuration provides seamless, uninterrupted operation over the wide supply voltage range possible in automotive applications and, because the output is referenced to the positive supply, there is no load current to ground. This ensures that there is no leakage path through the LEDs when in shutdown and no inrush current at power-up.

The A6268 integrates all necessary control elements to provide a cost-effective solution using a single external logic-level MOSFET and minimum additional external passive components.

The LED current is set by selecting an appropriate value for the sense resistor value and using the EN input to provide simple on-off control or for PWM brightness control using a suitable externally generated PWM signal. The LED current can be reduced in a single step by reducing the voltage between the IREF pin and GND to less than 1 V.

The pin functions and circuit operation are described in detail in the following sections.

Pin Functions

VIN. Supply to the control circuit. A bypass capacitor must be connected between this pin and GND.

GND. Ground reference connection. This pin should be connected directly to the negative supply.

EN. Logic input to enable operation. Can be used as direct PWM input. Chip enters low power sleep mode when low for longer than the disable time, t_{DIS}.

FF1. Fault Flag output and isolation control. Open drain current sink output, when high impedance indicates detection of a critical circuit fault. An external pull-up resistor should be connected to a suitable logic supply for simple logic fault flag operation or to the source of the PMOS FET used to isolate the load from the supply. Table 1 defines when FF1 is active. If FF1 is pulled low when an output short fault is indicated, then the output disable will be overridden.

FF2. Fault Flag output. Open drain output, when high impedance indicates detection of a circuit fault. An external pull-up resistor should be connected to a suitable logic supply. If VREG is not used, then the logic supply should not be pulled 300 mV above VREG. Table 1 defines when FF2 is active. If FF2 is pulled low when an open LED fault is indicated, then the output disable will be overridden.

OSC. Resistor to ground to set the internal oscillator or clock input from external oscillator. When connected to VREG or GND the oscillator runs at typically 350 kHz. Higher accuracy in the frequency is possible by connecting a resistor from this pin to ground or by driving this pin with an external precision oscillator.

CKOUT. Logic output at the oscillator frequency with phase shift. Used to drive succeeding controllers to interleave switching instants.

IREF. LED current reference modifier. A voltage input that can be used to reduce the LED current sense voltage. When connected to VREG, the current sense voltage, V_{IDL}, and the value of the sense resistor, R_{SL}, define the maximum LED current.

SG. Gate drive for external logic-level MOSFET low-side switch that connects the inductor to ground.

SP, SN. Sense amplifier connections for switch current limit sense resistor, R_{SS}.

LP. Positive sense amplifier connection for LED current limit sense resistor, R_{SL}.

LN. Negative sense amplifier connection for LED current limit sense resistor, R_{SL}. The voltage at LN also determines whether the boost or buck-boost mode is configured.

VREG. Compensation capacitor for internal 5 V regulator.

LA. Anode reference connection to LEDs. Using an external resistor divider with the same ratio as the number of LEDs provides a measurement of the voltage across all LEDs in the load. This is compared to the voltage on the LF pin to provide shorted LED detection. In addition, it is compared against voltage references to provide open circuit or shorted LED string detection.

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LF. Single diode forward voltage reference input. Measures the forward voltage of the first LED. This value is used as a reference against the voltage on the LA pin to detect possible shorted LEDs in the LED string.

Circuit Operation

Converter. A constant frequency, current mode control scheme is used to regulate the current through the LEDs. There are two control loops within the regulator. The inner loop formed by the amplifier, AS (see the Functional Block Diagram for AS, AC, AE, and AL), comparator, AC, and the RS bi-stable, controls the inductor current as measured through the switch by the switch sense resistor, R_{SS}.

The outer loop including the amplifier, AL, and the integrating error amplifier, AE, controls the average LED current by providing a setpoint reference for the inner loop.

The LED current is measured by the LED sense resistor, R_{SL}, and compared to the internal reference current to produce an integrated error signal at the output of AE. This error signal sets the average amount of energy required from the inductor by the LEDs. The average inductor energy transferred to the LEDs is defined by the average inductor current as determined by the inner control loop.

The inner loop establishes the average inductor current by controlling the peak switch current on a cycle-by-cycle basis. Because the relationship between peak current and average current is non-linear, depending on the duty cycle, the reference level for the peak switch current is modified by a slope generator. This compensation reduces the peak switch current measurement by a small amount as the duty cycle increases (refer to figure 1). The slope compensation also removes the instability inherent in a fixed frequency current control scheme.

The control loops work together as follows: the switch current, sensed by the switch current sense resistor, R_{SS}, is compared to the LED current error signal. As the LED current increases the output of AE will reduce, reducing the peak switch current and thus the current delivered to the LEDs. As the LED current decreases the output of AE increases, increasing the peak switch current and thus increasing the current delivered to the LEDs.

Under some conditions, especially when the LED current is set to a low value, the energy required in the inductor may result in the inductor current dropping to zero for part of each cycle. This is known as discontinuous mode operation, and results in some low frequency ripple. The average LED current, however, remains regulated down to zero. In discontinuous mode, when the inductor current drops to zero, the voltage at the drain of the external MOSFET rings, due to the resonant LC circuit formed by the inductor, and the switch and diode capacitance. This ringing is low frequency and is not harmful.

Switch Current Limit. The switch current is measured by the switch sense resistor, R_{SS}, and the switch sense amplifier, AS (see the Functional Block Diagram). The input limit of the sense amplifier, V_{IDS}, and the maximum switch current, I_{SMAX}, define the maximum value of the sense resistor as:

$$R_{SS} = V_{IDS} / I_{SMAX} \quad (1)$$

This defines the maximum measurable value of the switch (and inductor) current.

The maximum switch current is modulated by the on-time of the switch. An internal slope compensation signal is subtracted from the voltage sense signal to produce a peak sense voltage which effectively defines the current limit. This signal is applied at a rate of –16 mV / µs starting with no contribution (t = 0 µs) at the beginning of each switching cycle. Figure 1 illustrates how the peak sense voltage (typical values) changes over a period of 3 µs.

For example, the maximum current (typical) through the switch at t = 1.5 µs (D = 50%) would be 145 mV/R_{SS}, however, if the switch remained on for a further 1 µs, the maximum current through the switch would be 129 mV/R_{SS}.

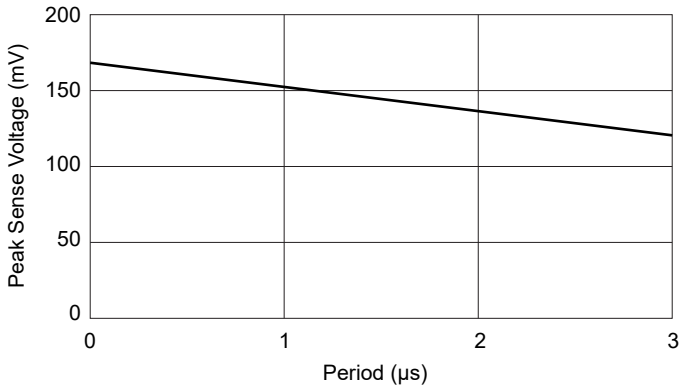

Figure 1. Slope compensation for peak switch current control.

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LED Current Level. The LED current is determined by a combination of the LED sense resistor, R_{SL}, the LED current threshold voltage, V_{IDL}, and the voltage between the IREF pin and GND (V_{IREF}).

The 100% current level, when the IREF pin is connected to VREG, is defined as:

$$I_{LED}(\max) = V_{IDL} / R_{SL} \quad (2)$$

If V_{IREF} is less than 1 V then the 100% current level is defined as:

$$I_{LED}(\max) = V_{IREF} / (10 \times R_{SL}) \quad (3)$$

This feature provides direct analog dimming using a voltage from 0 to 1 V. This can be used for a number of different functions:

- To provide intensity matching between modules or groups of LEDs in critical display or backlighting applications.
- To provide a soft start, by connecting a capacitor from IREF to GND and a resistor from IREF to VREG, or one-step dimming by use of a single logic control.
- To reduce the LED current during cold-crank conditions, thus avoiding overstressing the power components

LED Brightness: PWM Dimming. LED brightness can be controlled by changing the current, which affects the light intensity. However in some applications, for example with amber LEDs, this will have some effect on the color of the LEDs. In these cases it is more desirable to control the brightness by switching the fixed LED current with a pulse width modulated signal. This allows the LED brightness to be set with little effect on the LED color and intensity and allows direct digital control of the LED brightness.

A PWM signal can be applied to the EN input to enable PWM dimming. The period of this signal should be less than the minimum disable time, t_{DIS}. During PWM dimming, the A6268 switches the LED current between 100% and 0% of the full current. Note that during PWM dimming, the gate drive is disabled when EN is low. The rate of change of the LED current is also limited, to reduce any large variations in the input current.

Sleep Mode. If EN is held low for longer than the disable time, t_{DIS}, then the A6268 will shut down and put all sections into a low-power sleep mode. In this mode the bias current is typically less than 4 µA. In the buck-boost configuration the only leakage path remaining will be the path through the MOSFET.

Provided this is low, then the complete circuit may remain connected to the power supply under all conditions. Note that the disable time is derived from the oscillator period by a ratio of 32,768:1, so any variation in the oscillator frequency will change the disable time. For the default switching frequency of 350kHz, this means the disable time would be:

$$t_{DIS} = 32{,}768 \times (1/350 \times 10^3) = 94 \text{ ms} \quad (4)$$

Oscillator. The main oscillator may be configured as a clock source or it may be driven by an external clock signal. The oscillator is designed to run between 100 and 700 kHz.

When the oscillator is configured as a clock source, the frequency is controlled by a single external resistor, R_{OSC} (kΩ), between the OSC pin and the GND pin. The oscillator frequency is approximately:

$$f_{OSC} = 21700 / R_{OSC} \quad \text{(kHz)} \quad (5)$$

Figure 2 shows the resulting f_{OSC} for various values of R_{OSC}. If the OSC pin is connected to VREG or GND, the oscillator frequency will be set internally to approximately 350 kHz.

When an external clock source is used to drive the OSC pin, it can synchronize a number of A6268s operating together. This ensures that only a single fundamental frequency is detectable on the supply line, thus simplifying the design of any required EMC filter. The disadvantage of using a single external clock source is that all controllers will be switching current from the supply at the same time. However, this effect may be reduced, and the EMC performance may be further enhanced, by using

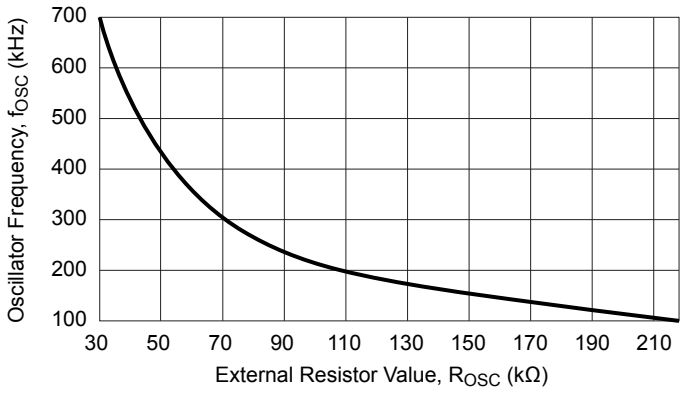

Figure 2. Internal oscillator frequency when set by R_{OSC}

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the CKOUT pin of another A6268 as the external clock source. In this case the switching point of each subsequent A6268 in the chain will be delayed from that of the previous A6268, and the current pulses will be spread across the oscillator period.

Diagnostics

The circuit includes several diagnostic and safety functions to assist in ensuring safe operation of the LEDs, the A6268, and the external components. When any fault is detected, one or both of the fault flag outputs, FF1 and FF2, will be inactive (high impedance, open drain) until the fault is removed. The action taken by the A6268 when a fault occurs is defined in table 1. To be able to monitor the state of FF1 and FF2, add a suitable external pull-up resistor.

The A6268 will continue to drive the LEDs under most fault conditions and will only disable the drive to the LEDs when a high voltage hazard is present or the external components are likely to be over-stressed. For output short circuits, LED sense resistor overcurrents, LED sense resistor negative overcurrents, or shorted LED string, the fault status is latched until a power cycle occurs, or by pulling EN low for a time greater than the disable time ($> t_{DIS}$). In all other cases the drive will be re-established when the hazard is removed.

Table 1. Fault Table

Fault	Pin		Action	Latched
	FF1	FF2		
No Fault	L	L	No Action	–
VIN Undervoltage	Z	Z	Disable*	No
VREG Undervoltage	Z	Z	Disable*	No
Overtemperature	L	Z	No Action	No
Open LED	L	Z	Disable*	Yes
Shorted LED	L	Z	No Action	No
LED Undercurrent	L	Z	No Action	No
Output Short	Z	L	Disable*	Yes
LED Sense Resistor Overcurrent	Z	L	Disable*	Yes
LED Sense Resistor Negative Overcurrent	Z	L	Disable*	Yes
Shorted LED String	Z	L	Disable*	Yes

*SG low, MOSFET off
L = active pull-down, Z = inactive, open drain

If either FF1 is pulled low (due to an output short or overcurrent condition), or FF2 is pulled low when an open LED fault is indicated, then the output disable will be overridden.

At start-up or during pulse width modulation of the Enable pin, a fault blank period, t_{FB}, occurs before the fault detection circuitry becomes active. This period allows steady state conditions to be established before fault monitoring takes place. Note that the fault blank period is derived from the oscillator period by a ratio of 1024:1, so any variation in the oscillator frequency will change the fault blank period. For the default switching frequency of 350 kHz, this means the fault blank period would be:

$$t_{FB} = 1024 \times (1 / 350 \times 10^3) = 3 \text{ ms} \quad (6)$$

Note that no fault blanking is applied to the following faults: open LED, VIN undervoltage, or VREG undervoltage.

VIN Undervoltage. If the voltage at VIN drops below the specified turn-off voltage, V_{INUV}, the gate drive output, SG, will be driven low and both fault flags, FF1 and FF2, will be high impedance. VIN must rise above the turn-on threshold, $V_{INUV} + \Delta V_{INUV}$, before the A6268 can start up.

VREG Undervoltage. If the voltage at VREG, V_{REG}, drops below the specified turnoff voltage, V_{REGUV}, the gate drive output, SG, will be driven low and both fault flags, FF1 and FF2, will be high impedance. V_{REG} must rise above the turn-on threshold, $V_{REGUV} + \Delta V_{REGUV}$, before the output circuits are activated. This ensures that the external FET is operating in its fully enhanced state and avoids permanent damage to the FET, caused by overheating.

The VREG Regulator is designed to operate with a typical maximum load current of 15 mA. The majority of the VREG load will be determined by the total gate charge of the external MOSFET.

The VREG pin can be also be used as a pull-up supply for the fault flag outputs. The current required for this function has to be considered in the overall load calculation. Note that if FF1 is used for driving a series protection MOSFET then only FF2 is pulled up to the VREG supply.

Overtemperature Warning. If the chip temperature exceeds the overtemperature threshold, T_{JF}, fault flag FF2 will be high impedance. No action will be taken by the A6268 to limit the chip temperature. An external control circuit must take action to avoid permanent damage to the A6268 and/or the LEDs. The temperature will continue to be monitored and the fault flags will be deactivated when the temperature drops below the recovery

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threshold provided by the specified hysteresis.

LED Diagnostics. The voltage with respect to ground at the three pins LP, LF, and LA, namely V_{LP}, V_{LF}, and V_{LA}, determine the status of the LEDs in the load. These voltages provide two differential voltage measurements:

• the voltage across a single reference LED:

$$V_{LED} = V_{LF} - V_{LP} \quad (7)$$

• the ratio of the voltage across all LEDs in a single string:

$$V_{STR} = V_{LA} - V_{LP} \quad (8)$$

These measurements are used to determine if there is an open circuit, if one or more LEDs are shorted, if the output is shorted, or if there is a short across the LED string.

The voltage, V_{STR}, is derived from the voltage across all LEDs in the string, by an external resistor divider with a ratio equal to the quantity of LEDs in the string. To minimize the effects of the bias currents introducing an offset voltage, it is recommended that the resistor between LP and LA should be approximately 560 Ω.

So for example, if eight LEDs were used, the ratio required would be an eighth, therefore the resistor connected between LA and the anode end of the LED string would be 3.9 kΩ; $560/[560 + 3900] = 1/8$.

Open LED – An open circuit is evaluated when:

$$V_{STR} > V_{OP} \quad (9)$$

where V_{OP} is the LED open circuit voltage defined in the Electrical Characteristics table.

Because the output is current-controlled it is possible for an open circuit on the output to cause extremely high voltages to be present. Therefore, to prevent any hazardous voltages or damage to the circuits, the gate drive output, SG, is immediately driven low when an open circuit is detected. After an open circuit fault has been detected, FF2 will become high impedance, and the open circuit fault state will remain until the open fault time-out period, t_{OTO}, expires.

Note that the open fault time-out period is derived from the oscillator period by a ratio of 32,768:1, so any variation in the oscillator frequency will change the open fault time-out period. For the default switching frequency of 350 kHz, this means the open fault time-out period would be:

$$t_{OTO} = 32{,}768 \times (1/350 \times 10^3) = 94 \text{ ms} \quad (10)$$

When the gate drive output is re-enabled at the end of the open fault time-out period, the output is again monitored for an open circuit. If the open circuit is still present, then the fault will again be flagged and the switch drive disabled. This cycle will continue, as long as the open circuit condition is present.

Shorted LED – A short circuit on one or more LEDs is detected when:

• for the first (reference) LED:

$$V_{STR} > V_{LED} + V_{SCOR} \quad (11)$$

• for other than the first (reference) LED:

$$V_{LED} > V_{STR} + V_{SCO} \quad (12)$$

where V_{STR} and V_{LED} are as defined above, V_{SCO} is the nonreference LED short offset voltage, and V_{SCOR} is the reference LED short offset voltage. V_{SCO} and V_{SCOR} are defined in the Electrical Characteristics table.

When a short is present, the fault flag FF2 is high impedance, but the regulator continues to operate and drives the remaining LEDs with the correct regulated current. FF2 will remain high impedance while the short circuit condition is present.

A short circuit on one or more LEDs will not cause a hazard because the output is current-controlled. If one LED fails and becomes a short circuit, then the remaining LEDs will continue to be lit with the same current through, and voltage across, each LED.

Note—Accuracy: The output status monitor relies on all the LEDs in the load having a similar forward voltage drop. Where possible all the LEDs forming the load for a single controller should be taken from the same voltage bin. The selection of LEDs from the same bin is more critical when higher numbers of LEDs are used in a single string. With only two or three LEDs a wider variation in forward voltage is acceptable.

LED Undercurrent – Under some circuit conditions, particularly during a low input voltage condition, it is possible that there could be insufficient drive to maintain the current to the LEDs at the required level. If the voltage across the LED current sense resistor, R_{SS}, falls below the target sense voltage, V_{IDL}, by an amount that is more than the LED undercurrent voltage difference, V_{UCL}, the A6268 will indicate an LED undercurrent condition by setting FF2 to high impedance. However, the A6268 will

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continue to drive the output. When the output again reaches the required current level, FF2 will go low.

Output Short – An output short can consist of the LP, LN, or LF terminals of the LED string being shorted, either to the battery terminal or to ground. An output short is detected when both a shorted LED and an LED undercurrent condition occur (defined previously). If the above two conditions occur, the A6268 will set FF1 high impedance. Note that at start-up, or during pulse width modulation of the Enable pin, a fault blank period, t_{FB}, occurs before this fault detection circuitry becomes active.

LED Sense Resistor Overcurrent – Under some circuit fault conditions, for example in boost mode, if the cathode connection is pulled to VBAT, the control loop can no longer control the LED current to the target level. If the voltage across the LED sense resistor, R_{SS}, increases above the target sense voltage, V_{IDL}, by an amount that is more than the overcurrent voltage difference, V_{OVCL}, the A6268 will indicate a LED overcurrent by setting FF1 high impedance.

Note that even if FF1 drives a supply isolation FET, the sense resistor may still be damaged because it is effectively between VBAT and GND. Note that at startup, or during pulse width modulation of the Enable pin, a fault blank period, t_{FB}, occurs before this fault detection circuitry becomes active.

Also in boost mode, if a "soft" short is applied across an LED string, causing the string voltage to be less than the input voltage, the control loop may not control as described previously and FF1 will be set. Alternatively, a soft short may cause a shorted LED string, as described in the section Shorted LED String. The actual detection of a soft short, whether by shorted LED string or LED sense resistor overcurrent detection, will depend on the actual application setup.

LED Sense Resistor Negative Overcurrent – Under some circuit fault conditions, for example in buck-boost mode, if the cathode connection is pulled to GND, current will flow through the sense resistor, R_{SS}, in the opposite direction. If the voltage across the sense resistor exceeds the negative overcurrent threshold, V_{NOCL}, the A6268 will set FF1 high impedance.

Note that if FF1 does not drive a supply isolation FET, the sense resistor may be damaged. Also, note that at start-up, or during pulse width modulation of the Enable pin, a fault blank period, t_{FB}, occurs before this fault detection circuitry becomes active.

Shorted LED Stack – A short circuit across the LED stack, is detected when:

$$V_{STR} < V_{SCL} \quad (13)$$

If the above condition occurs, the A6268 will indicate an LED overcurrent by setting FF1 high impedance. Note that at startup, or during pulse width modulation of the Enable pin, a fault blank period, t_{FB}, occurs before this fault detection circuitry becomes active.

Fault Flag One If any shorted condition occurs, including: output short, LED sense resistor overcurrent, LED sense resistor negative overcurrent, or shorted LED string, the A6268 will stop the switching action by pulling SG low. The fault flag FF1 will go high impedance and should be pulled up to the supply with suitable external pull-up resistors to indicate the fault. Any of the aforementioned faults will be latched and will only be cleared by cycling the power, or by pulling EN low for a time greater than the disable time (> t_{DIS}).

The FF1 output can also be used with pull-up resistors and a P-channel MOSFET in the supply, to isolate the switching elements and the load from the supply. This MOSFET should be connected, as shown in figure 3, with the source connected to the supply and the drain connected to the inductor of the converter.

Two pull-up resistors are used to limit the voltage across the gate-source junction during high input voltages or load dump conditions. If the battery voltage is restricted, one resistor across the gate-source junction can be used. The FF1 provides a sink current of typically 1.3 mA.

This circuit can be used to avoid most hazardous conditions and protect the circuit components from over-stress. Note that under extreme cases, the circuit cannot protect against certain fault conditions as described in the following section.

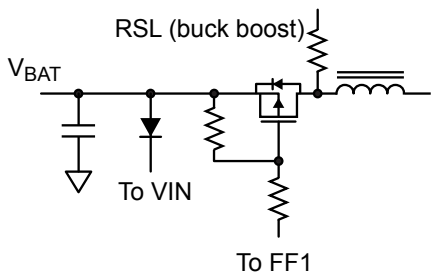

Figure 3. Example of a supply isolation MOSFET

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Protection Not Provided

Boost Mode

- The cathode end of the LED string is shorted to VBAT – Although an LED sense resistor overcurrent fault is produced, causing an FF1 flag, the LED sense resistor, RSS, is effectively between VBAT and ground. Depending on either the current limit of the source supply, or the input fuse rating, the fault current may damage the LED sense resistor.
- The LF node is shorted to VBAT – Although a LED sense resistor overcurrent fault is produced, causing an FF1 flag, the LED sense resistor, RSS, and the reference LED are effectively between VBAT and ground. Depending on the current limit of the source supply, or the input fuse rating, the fault current may damage the LED sense resistor and/or the reference LED.
- The cathode connection is shorted to ground – A fault current determined by the impedance of the shorting link (now effectively the LED sense resistor, RSS) flows through the power circuit. The fault current will either be limited by the maximum switch current sense, V_{IDS}, or if the source supply cannot maintain this current, the source supply will either foldback, or if the current exceeds the input fuse rating, the fuse will blow, causing an open circuit.
- The anode connection is shorted to ground during startup – A fault current determined by the current limit of the source supply (VBAT), or a value less than the input fuse rating, will flow through the series protection FET, inductor, and recirculation diode. If the source supply can supply the fault current for the duration of the fault blank period, t_{BK}, then an FF1 flag will occur. Otherwise, either the source supply voltage will fold back and an input voltage UVLO will occur, disabling the A6268, or the input fuse will blow, causing an open circuit. Assuming the input source supply recovers, the A6268 will automatically restart and the process will be repeated.

Buck-Boost Mode

- The cathode end of the LED string is connected to VBAT – The short circuit impedance effectively appears in parallel with the series protection MOSFET and the LED sense resistor, RSS. This will tend to reduce the effective impedance of the LED sense resistor and correspondingly increase the LED current.
- The anode connection is shorted to ground during startup – A fault current determined by the current limit of the source supply (VBAT), or a value less than the input fuse rating, will flow through the series protection FET, inductor, and recirculation diode. If the source supply can supply the fault current for the duration of the fault blank period, t_{BK}, then an FF1 flag will occur. Otherwise, either the source supply voltage will fold back and an input voltage UVLO will occur, disabling the A6268, or the input fuse will blow, causing an open circuit. Assuming the input source supply recovers, the A6268 will automatically restart and the process will be repeated.

To ensure the A6268 inputs (LP and LN) are not damaged during any of the above faults, it is necessary to add differential resistors between each of the LED sense resistor connections and the respective connection to the A6268. In the case of buck boost mode, one resistor is used on each connection. In the case of boost mode, only one resistor is required between the LN input and the cathode connection of the sense resistor. Refer to the circuit diagrams on page 3. These resistor values should be approximately 150 Ω.

If an output short is detected but it is necessary to keep the output active, the FF1 output can be pulled low. This will override the output disable but will not clear the fault.

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Application Information

Component Selection

External component selection is critical to the successful application of the LED driver. Although the inductor, the switching MOSFET, and the output capacitor are the most critical elements, the specification of the rectifying diode and sense resistors should also be carefully considered.

The starting point for component selection is to define the maximum LED current, the voltage across the LEDs, and the input operating voltage range. This then allows the average inductor current under worst case conditions to be calculated.

The inductor value is then selected based on the acceptable inductor ripple current. The amount of ripple current will then determine the maximum inductor current under worst case conditions. From this current the switch current sense resistor can be calculated.

LED Current Sense Resistor (R_{LS}). If the voltage at the IREF pin, V_{IREF}, is greater than 1 V, or if IREF is tied to VREG, then the value of the LED current sense resistor, R_{LS}, can be calculated from:

$$R_{LS} = V_{IDL} / I_{LED}(max) \quad (14)$$

where V_{IDL} is the differential voltage across the LED current sense amplifier and $I_{LED}(max)$ is the maximum LED current.

If V_{IREF} is less than 1 V, then the value of the LED current sense resistor can be calculated from:

$$R_{LS} = V_{IREF} / (10 \times I_{LED}(max)) \quad (15)$$

The typical value for V_{IDL} is 100 mV. Examples of various sense resistor values are given in table 2.

Table 2. Sense Resistor Values

$I_{LED}(max)$ (mA)	R_{LS} (mΩ)
350	286
700	143
1000	100

In boost mode, the power loss in the current sense resistor is worse at the lowest input voltage:

$$P_{LOSS} = (V_{LED} / V_{IN}(min)) \times R_{LS} \times I^2_{LED} \quad (16)$$

In buck-boost mode, the power loss in the current sense resistor is worse at the lowest input voltage:

$$P_{LOSS} = ([V_{IN} + V_{LED}] / V_{IN}) \times R_{LS} \times I^2_{LED} \quad (17)$$

The power rating of the sense resistor should exceed the above rating at the maximum temperature.

The resistors should be of a low inductance construction. Surface mount chip resistors are usually the most suitable, however, axial or radial leaded resistors can be used provided that the lead length is kept to a minimum.

Inductor Selection. Selecting the correct inductance is a balance between choosing a value that is small enough to help reduce size and cost, but high enough to ensure that the inductor current ripple is kept to an acceptable level. A reasonable target for the ripple current is 20% of the maximum average current.

The inductor current equations differ slightly depending on whether the A6268 is configured as a boost or as a buck-boost converter.

- In a boost converter configuration:
  - The maximum average inductor current is approximately:

$$I_{L(av)}(max) = I_{LED}(max) \times V_{LED} / V_{IN}(min) \quad (18)$$

  - The inductor current ripple is approximately:

$$I_{LRIP} = V_{IN} \times (V_{LED} - V_{IN}) / (f_{OSC} \times L \times V_{LED}) \quad (19)$$

  - The inductor value is therefore:

$$L = V_{IN} \times (V_{LED} - V_{IN}) / (f_{OSC} \times I_{LRIP} \times V_{LED}) \quad (20)$$

- In a buck-boost configuration:
  - The maximum average inductor current is approximately:

$$I_{L(av)}(max) = I_{LED}(max) \times (V_{IN}(min) + V_{LED}) / V_{IN}(min) \quad (21)$$

  - The inductor current ripple is approximately:

$$I_{LRIP} = V_{IN} \times V_{LED} / (f_{OSC} \times L \times [V_{IN} + V_{LED}]) \quad (22)$$

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▫ The inductor value is therefore:

$$L = V_{IN} \times V_{LED} / (f_{OSC} \times I_{LRIP} \times [V_{IN} + V_{LED}]) \quad (23)$$

where:
V_{LED} is the voltage across the LED string,
V_{IN} is the supply voltage,
V_{IN}(min) is the minimum supply voltage,
L is the inductor value, and
f_{OSC} is the oscillator frequency.

With an internal oscillator frequency of 350 kHz, the value of the inductor for most cases will be between 20 and 50 µH.

The maximum inductor current can then be calculated as:

$$I_{L(PK)} = I_{L(av)}(\max) + (I_{RIP} / 2) \quad (24)$$

This defines the minimum peak switch current as set by the switch current sense resistor.

The current rating for the inductor should be greater, by some margin, than the peak value above. When selecting an inductor from manufacturers datasheets, there are two current levels usually defined, the smallest value being the figure to work with:

- Saturation level, where the inductance value typically drops by 10%, or
- Temperature rise, where the part experiences a certain rise in temperature at full rated current. This parameter can be defined between a 20°C and 50°C rise in temperature. It is important to understand how manufacturers define the maximum operating temperature, because this can often incorporate the self-heating temperature rise.

In most cases the limiting current is usually the saturation value. To improve efficiency, the inductor should also have low winding resistance, typically < 50 mΩ, and the core material will usually be ferrite, with low losses at the oscillator frequency.

Recommended inductor manufacturers/series are:

- Coilcraft/ MSS1278T
- TDK/ SLF12575 type H

Diode. The diode should have a low forward voltage, to reduce conduction losses, and a low capacitance, to reduce switching losses. Schottky diodes can provide both these features if carefully selected. The forward voltage drop is a natural advantage for Schottky diodes and reduces as the current rating increases. However, as the current rating increases, the diode capacitance also increases so the optimum selection is usually the lowest current rating above the required maximum, in this case $I_{L(PK)}$.

Switch Current Sense Resistor (RSS). Neither the absolute value of the switch current nor the accuracy of the measurement is important, because the regulator will continuously adjust the switch current, within a closed loop, to provide sufficient energy for the output. For maximum accuracy the switch sense resistor value should be chosen to maximize the differential signal seen by the sense amplifier. The input limit of the sense amplifier, V_{IDS}, and the maximum switch current, I_S(max), therefore define the maximum value of the sense resistor as:

$$R_{SS} = V_{IDS} / I_S(\max) \quad (25)$$

where I_S(max) is the maximum switch current and should be set above the maximum inductor current, $I_{L(PK)}$.

This represents the maximum measurable value of the switch (and inductor) current; however, the peak switch current will always be less than this, set by the control circuit, depending on the input voltage and the required load conditions. Because the switch current control is within a closed loop, it is possible to reduce the value of the sense resistor to reduce its power dissipation. However this will reduce the accuracy of the regulated LED current.

In boost mode, the power loss in the switch sense resistor is worse at the lowest input voltage:

$$P_{LOSS} = R_{SS} \times I^2_{LED} \times (V_{LED} [V_{LED} - V_{IN}(\min)] / V^2_{IN}(\min)) \quad (26)$$

In buck-boost mode, the power loss in the switch sense resistor is worse at the lowest input voltage:

$$P_{LOSS} = R_{SS} \times I^2_{LED} \times (V_{LED} / V_{IN}(\min))(V_{LED} + V_{IN}(\min)) \quad (27)$$

The power rating of the sense resistor should exceed the above rating at the maximum temperature.

External Switch MOSFET. A logic-level N-channel MOSFET is used as the switch for the DC-to-DC converter. In the boost configuration the voltage at the drain of the MOSFET is equal to the maximum voltage across the string of LEDs. In the buck-boost configuration the output voltage is referenced to the positive supply. This means that the voltage at the drain of the MOSFET will reach a voltage equal to the sum of the LED voltage and the supply voltage. Under load dump conditions, up to 90 V may be present on this node. In this case the external MOSFET should

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therefore be rated at greater than 100 V.

The peak switch current is defined by the maximum inductor current, $I_{L(PK)}$. However, in most cases the MOSFET will be chosen by selecting low on-resistance, which usually results in a current rating of several times the required peak current.

In addition to minimizing cost, the choice of MOSFET should consider both the on-resistance and the total gate charge. The total gate charge will determine the average current required from the internal regulator and thus the power dissipation.

When the input voltage, V_{IN}, reduces below the 5 V regulator drop out level, the gate drive voltage will correspondingly reduce. The level that this occurs at will depend on the average current required for the gate charge. This level will typically occur with an input voltage of around 5.3 V. The effect of a reduced gate drive voltage may be an increase in the on-resistance of the switching MOSFET.

Output Capacitor. There are several points to consider when selecting the output capacitor.

Unlike some switch-mode regulators, the value of the output capacitor in this case is not critical for output stability. The capacitor value is only limited by the required maximum ripple voltage.

Due to the switching topology used, the ripple current for this circuit is high because the output capacitor provides the LED current when the switch is active. The capacitor is then recharged each time the inductor passes energy to the output. The ripple current on the output capacitor will be equal to the peak inductor current.

Normally this large ripple current, in conjunction with the requirement for a larger capacitance value for stability, would dictate the use of large electrolytic capacitors. However, in this case stability is not a consideration, and the capacitor value can be low, allowing the use of ceramic capacitors.

To minimize self-heating effects and voltage ripple, the equivalent series resistance (ESR), and the equivalent series inductance (ESL) should be kept as low as possible. This can be achieved by multilayer ceramic chip (MLCC) capacitors. To reduce performance variation over temperature, low drift types such as X7R and X5R should be used.

The value of the output capacitor will typically be about 10 µF and it should be rated above the maximum voltage defined by the series output LEDs.

Reverse Supply Protection. Protection for the A6268 is provided by an external low current diode between the supply and the VIN pin, as shown in the Functional Block Diagrams section. The isolation MOSFET shown in figure 3 is only able to provide isolation when the supply polarity is correct. However, with an additional P-channel MOSFET, it is also possible to provide reverse battery protection to the switching elements and the LEDs. The additional FET should be connected, as shown in figure 4, with the drain to the supply and the source to the source connection of the original isolation MOSFET.

In the complete circuit, consideration should be given to limiting the maximum gate-source voltage of the FET. If the supply voltage is likely to exceed 20 V, then either: a Zener clamp must be added in parallel with the gate-source resistor to prevent damage to the FET, or a second resistor added as shown in figure 3.

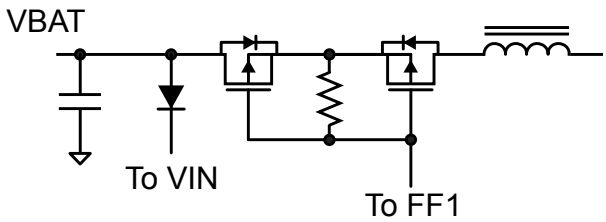

Figure 4. Example of a supply isolation MOSFET

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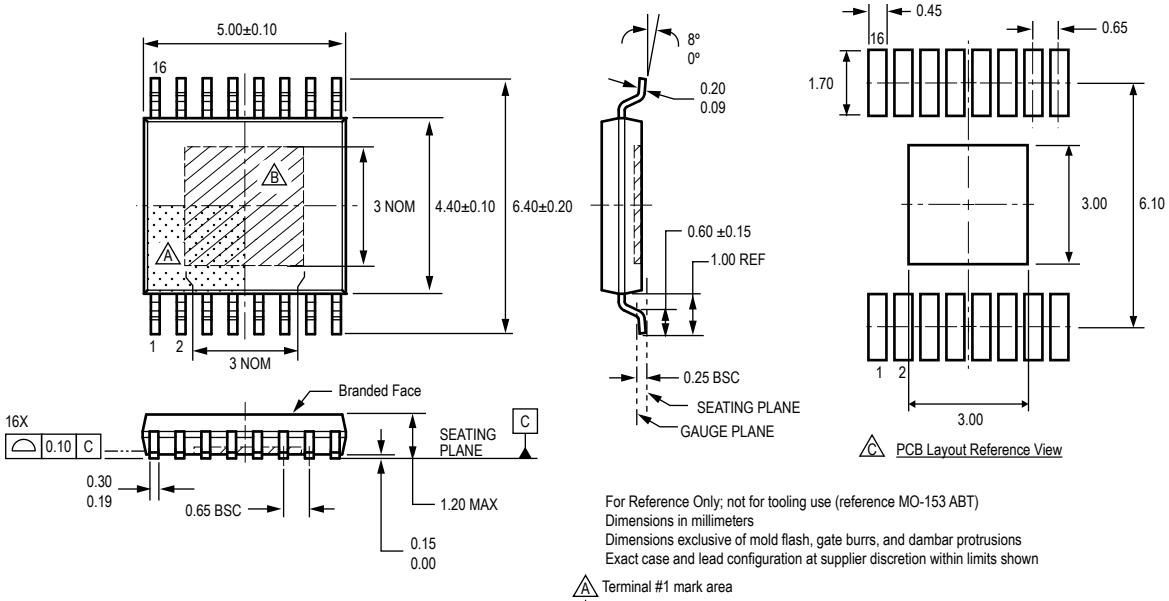
Package LP 16-Pin TSSOP with Exposed Thermal Pad



For Reference Only; not for tooling use (reference MO-153 ABT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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Revision History

Number	Date	Description
2	April 1, 2013	Update f_{MIN}
3	June 19, 2014	At start up, or during pulse width modulation of the enable pin, the fault detection circuitry associated with the LED Sense Resistor Negative Overcurrent protection is inactive for a period defined by the fault blank timer, t_{FB}.
4	May 29, 2020	Minor editorial updates

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