

16-bit dual supply translating transceiver with configurable voltage translation; 3-state

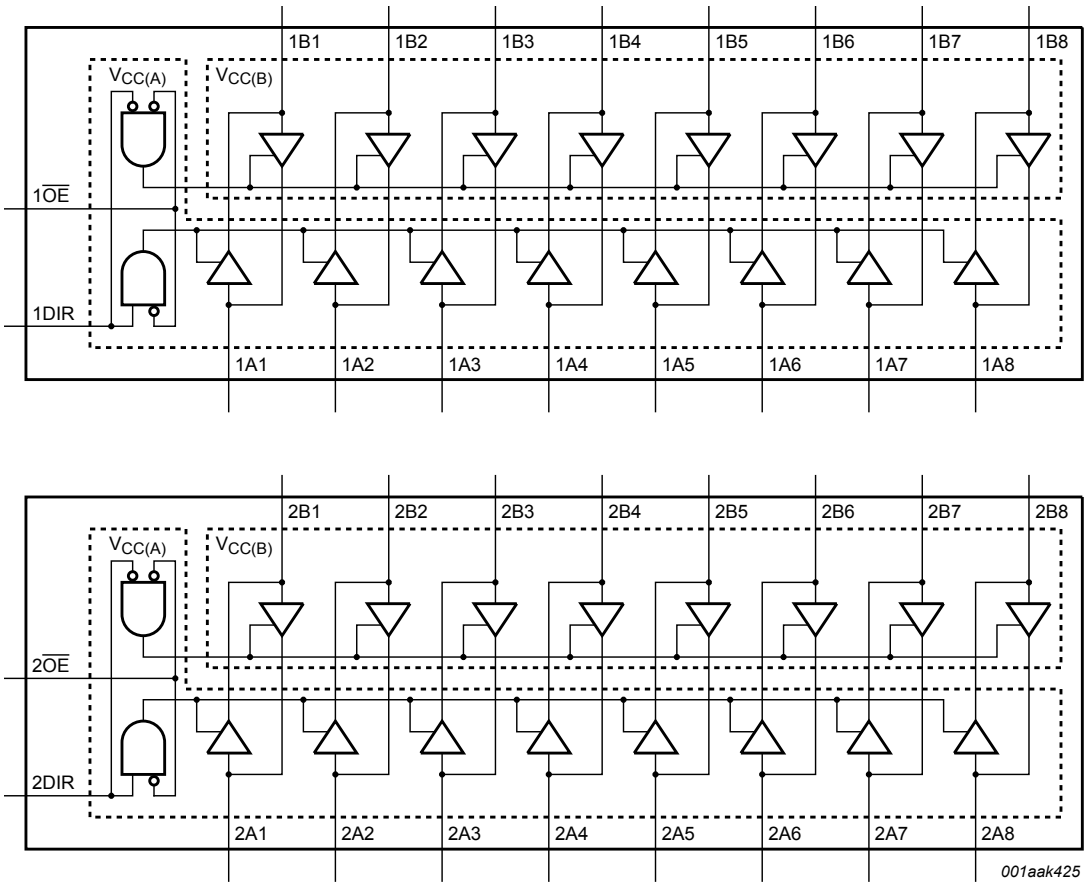


Fig. 2. Logic symbol

5. Pinning information

5.1. Pinning

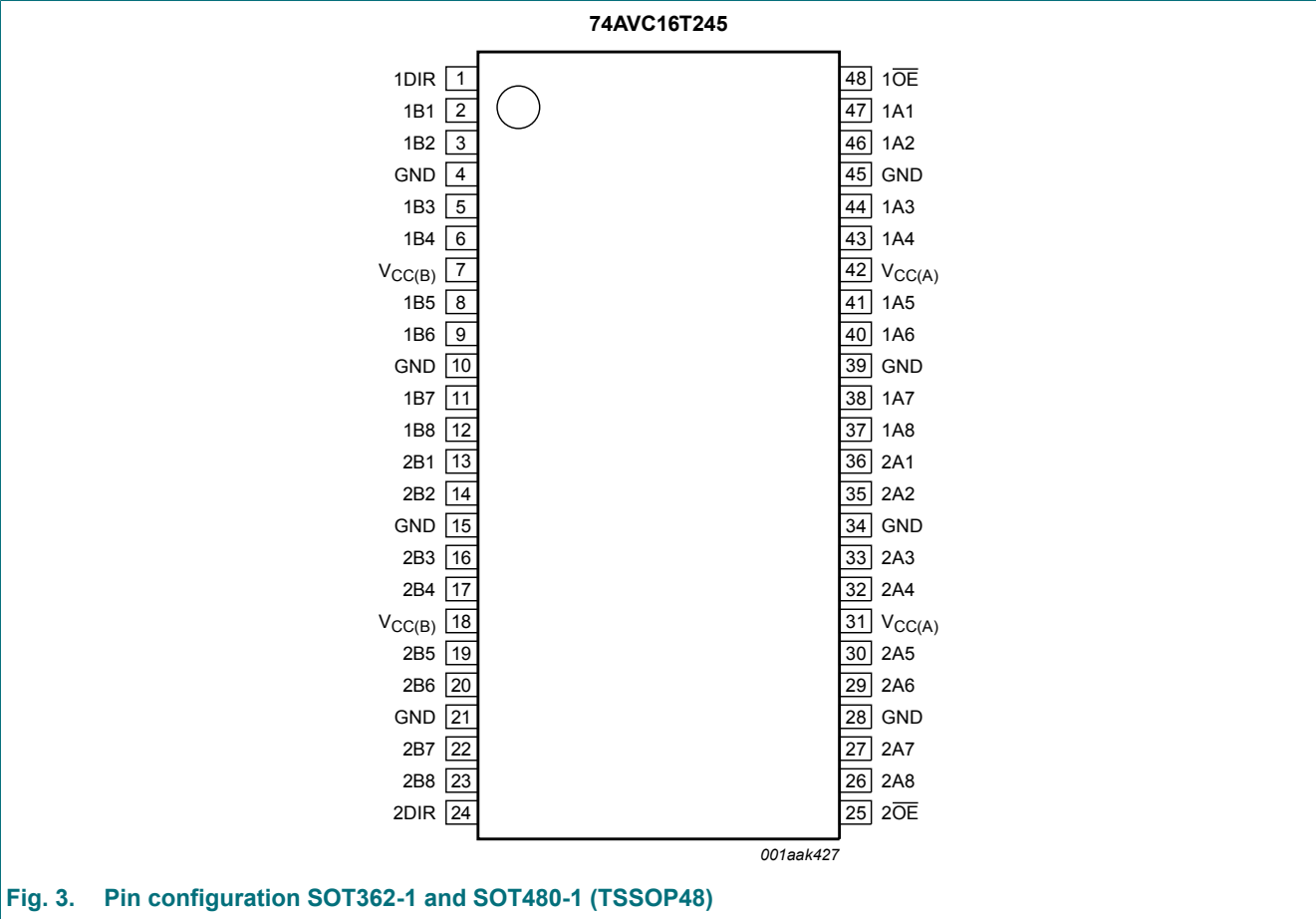


Fig. 3. Pin configuration SOT362-1 and SOT480-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control
1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7, 1B8	2, 3, 5, 6, 8, 9, 11, 12	data input or output
2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7, 2B8	13, 14, 16, 17, 19, 20, 22, 23	data input or output
GND [1]	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V _{CC(B)}	7, 18	supply voltage B (nBn inputs are referenced to V _{CC(B)})
1OE, 2OE	48, 25	output enable input (active LOW)
1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7, 1A8	47, 46, 44, 43, 41, 40, 38, 37	data input or output
2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7, 2A8	36, 35, 33, 32, 30, 29, 27, 26	data input or output
V _{CC(A)}	31, 42	supply voltage A (nAn, nOE and nDIR inputs are referenced to V _{CC(A)})

[1] All GND pins must be connected to ground (0 V).

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage	Input		Input/output [1]	
$V_{CC(A)}$, $V_{CC(B)}$	nOE [2]	nDIR [2]	nAn [2]	nBn [2]
0.8 V to 3.6 V	L	L	nAn = nBn	input
0.8 V to 3.6 V	L	H	input	nBn = nAn
0.8 V to 3.6 V	H	X	Z	Z
GND [1]	X	X	Z	Z

[1] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

[2] The nAn, nDIR and nOE input circuit is referenced to $V_{CC(A)}$; The nBn input circuit is referenced to $V_{CC(B)}$.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode [1][2][3]	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode [1]	-0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CCO} [2]	-	± 50	mA
I_{CC}	supply current	per $V_{CC(A)}$ or $V_{CC(B)}$ pin	-	100	mA
I_{GND}	ground current	per GND pin	-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C; [4]	-	500	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] $V_{CCO} + 0.5$ V should not exceed 4.6 V.

[4] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		0.8	3.6	V
$V_{CC(B)}$	supply voltage B		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode [1]	0	V_{CCO}	V
		Suspend or 3-state mode	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8 \text{ V to } 3.6 \text{ V}$ [2]	-	5	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

9. Static characteristics

Table 6. Typical static characteristics at $T_{amb} = 25 \text{ °C}$

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$ $I_O = -1.5 \text{ mA}; V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$	-	0.69	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$ $I_O = 1.5 \text{ mA}; V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$	-	0.07	-	V
I_I	input leakage current	nDIR, $\overline{nOE}$ input; $V_I = 0 \text{ V or } 3.6 \text{ V};$ $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V to } 3.6 \text{ V}$	-	± 0.025	± 0.25	μA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0 \text{ V or } V_{CCO};$ $V_{CC(A)} = V_{CC(B)} = 3.6 \text{ V}$ [2]	-	± 0.5	± 2.5	μA
		suspend mode A port; $V_O = 0 \text{ V or } V_{CCO};$ $V_{CC(A)} = 3.6 \text{ V}; V_{CC(B)} = 0 \text{ V}$ [2]	-	± 0.5	± 2.5	μA
		suspend mode B port; $V_O = 0 \text{ V or } V_{CCO};$ $V_{CC(A)} = 0 \text{ V}; V_{CC(B)} = 3.6 \text{ V}$ [2]	-	± 0.5	± 2.5	μA
I_{OFF}	power-off leakage current	A port; $V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC(A)} = 0 \text{ V}; V_{CC(B)} = 0.8 \text{ V to } 3.6 \text{ V}$	-	± 0.1	± 1	μA
		B port; $V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC(B)} = 0 \text{ V}; V_{CC(A)} = 0.8 \text{ V to } 3.6 \text{ V}$	-	± 0.1	± 1	μA
C_I	input capacitance	nDIR, $\overline{nOE}$ input; $V_I = 0 \text{ V or } 3.3 \text{ V};$ $V_{CC(A)} = V_{CC(B)} = 3.3 \text{ V}$	-	2.0	-	pF
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3 \text{ V or } 0 \text{ V};$ $V_{CC(A)} = V_{CC(B)} = 3.3 \text{ V}$	-	4.5	-	pF

[1] V_{CCO} is the supply voltage associated with the output port.

[2] For I/O ports, the parameter I_{OZ} includes the input leakage current.

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Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). [1]

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	data input					
		V _{CCI} = 0.8 V	0.70V _{CCI}	-	0.70V _{CCI}	-	V
		V _{CCI} = 1.1 V to 1.95 V	0.65V _{CCI}	-	0.65V _{CCI}	-	V
		V _{CCI} = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V _{CCI} = 3.0 V to 3.6 V	2	-	2	-	V
		nDIR, nOE input					
		V _{CC(A)} = 0.8 V	0.70V _{CC(A)}	-	0.70V _{CC(A)}	-	V
		V _{CC(A)} = 1.1 V to 1.95 V	0.65V _{CC(A)}	-	0.65V _{CC(A)}	-	V
		V _{CC(A)} = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V _{CC(A)} = 3.0 V to 3.6 V	2	-	2	-	V
V _{IL}	LOW-level input voltage	data input					
		V _{CCI} = 0.8 V	-	0.30V _{CCI}	-	0.30V _{CCI}	V
		V _{CCI} = 1.1 V to 1.95 V	-	0.35V _{CCI}	-	0.35V _{CCI}	V
		V _{CCI} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V _{CCI} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		nDIR, nOE input					
		V _{CC(A)} = 0.8 V	-	0.30V _{CC(A)}	-	0.30V _{CC(A)}	V
		V _{CC(A)} = 1.1 V to 1.95 V	-	0.35V _{CC(A)}	-	0.35V _{CC(A)}	V
		V _{CC(A)} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V _{CC(A)} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = -100 µA; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	V _{CCO} - 0.1	-	V _{CCO} - 0.1	-	V
		I _O = -3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	0.85	-	0.85	-	V
		I _O = -6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	1.05	-	1.05	-	V
		I _O = -8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	1.2	-	1.2	-	V
		I _O = -9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	1.75	-	1.75	-	V
		I _O = -12 mA; V _{CC(A)} = V _{CC(B)} = 3.0 V	2.3	-	2.3	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 100 µA; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I _O = 3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	-	0.25	-	0.25	V
		I _O = 6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	-	0.35	-	0.35	V
		I _O = 8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	-	0.45	-	0.45	V
		I _O = 9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	-	0.55	-	0.55	V
		I _O = 12 mA; V _{CC(A)} = V _{CC(B)} = 3.0 V	-	0.7	-	0.7	V

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Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_I	input leakage current	nDIR, $\overline{nOE}$ input; $V_I = 0\text{ V}$ or 3.6 V ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$ to 3.6 V	-	± 1	-	± 5	μA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0\text{ V}$ or V_{CCO} ; $V_{CC(A)} = V_{CC(B)} = 3.6\text{ V}$ [2]	-	± 5	-	± 30	μA
		suspend mode A port; $V_O = 0\text{ V}$ or V_{CCO} ; $V_{CC(A)} = 3.6\text{ V}$; $V_{CC(B)} = 0\text{ V}$ [2]	-	± 5	-	± 30	μA
		suspend mode B port; $V_O = 0\text{ V}$ or V_{CCO} ; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 3.6\text{ V}$ [2]	-	± 5	-	± 30	μA
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0\text{ V}$ to 3.6 V ; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 0.8\text{ V}$ to 3.6 V	-	± 5	-	± 30	μA
		B port; V_I or $V_O = 0\text{ V}$ to 3.6 V ; $V_{CC(B)} = 0\text{ V}$; $V_{CC(A)} = 0.8\text{ V}$ to 3.6 V	-	± 5	-	± 30	μA
I_{CC}	supply current	A port; $V_I = 0\text{ V}$ or V_{CCI} ; $I_O = 0\text{ A}$					
		$V_{CC(A)} = 0.8\text{ V}$ to 3.6 V ; $V_{CC(B)} = 0.8\text{ V}$ to 3.6 V	-	30	-	125	μA
		$V_{CC(A)} = 1.1\text{ V}$ to 3.6 V ; $V_{CC(B)} = 1.1\text{ V}$ to 3.6 V	-	25	-	100	μA
		$V_{CC(A)} = 3.6\text{ V}$; $V_{CC(B)} = 0\text{ V}$	-	25	-	100	μA
		$V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 3.6\text{ V}$	-5	-	-20	-	μA
		B port; $V_I = 0\text{ V}$ or V_{CCI} ; $I_O = 0\text{ A}$					
		$V_{CC(A)} = 0.8\text{ V}$ to 3.6 V ; $V_{CC(B)} = 0.8\text{ V}$ to 3.6 V	-	30	-	125	μA
		$V_{CC(A)} = 1.1\text{ V}$ to 3.6 V ; $V_{CC(B)} = 1.1\text{ V}$ to 3.6 V	-	25	-	100	μA
		$V_{CC(A)} = 3.6\text{ V}$; $V_{CC(B)} = 0\text{ V}$	-5	-	-20	-	μA
		$V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 3.6\text{ V}$	-	25	-	100	μA
		A plus B port ($I_{CC(A)} + I_{CC(B)}$); $I_O = 0\text{ A}$; $V_I = 0\text{ V}$ or V_{CCI} ; $V_{CC(A)} = 0.8\text{ V}$ to 3.6 V ; $V_{CC(B)} = 0.8\text{ V}$ to 3.6 V	-	55	-	185	μA
		A plus B port ($I_{CC(A)} + I_{CC(B)}$); $I_O = 0\text{ A}$; $V_I = 0\text{ V}$ or V_{CCI} ; $V_{CC(A)} = 1.1\text{ V}$ to 3.6 V ; $V_{CC(B)} = 1.1\text{ V}$ to 3.6 V	-	45	-	150	μA

[1] V_{CCI} is the supply voltage associated with the data input port; V_{CCO} is the supply voltage associated with the output port.

[2] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 8. Typical total supply current ($I_{CC(A)} + I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA

10. Dynamic characteristics

Table 9. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25\text{ °C}$

Voltages are referenced to GND (ground = 0 V). [1][2]

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C_{PD}	power dissipation capacitance	A port: (direction nAn to nBn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nAn to nBn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nBn to nAn); output enabled	9	9.7	9.8	10.3	11.7	13.7	pF
		A port: (direction nBn to nAn); output disabled	0.6	0.6	0.6	0.7	0.7	0.7	pF
		B port: (direction nAn to nBn); output enabled	9	9.7	9.8	10.3	11.7	13.7	pF
		B port: (direction nAn to nBn); output disabled	0.6	0.6	0.6	0.7	0.7	0.7	pF
		B port: (direction nBn to nAn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction nBn to nAn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz;

C_L = load capacitance in pF; V_{CC} = supply voltage in V;

N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] $f_i = 10\text{ MHz}$; $V_i = \text{GND to } V_{CC}$; $t_r = t_f = 1\text{ ns}$; $C_L = 0\text{ pF}$; $R_L = \infty\text{ }\Omega$.

Table 10. Typical dynamic characteristics at $V_{CC(A)} = 0.8\text{ V}$ and $T_{amb} = 25\text{ °C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6; for wave forms see Fig. 4 and Fig. 5. [1]

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		nBn to nAn	14.4	12.4	12.1	11.9	11.8	11.8	ns
t_{dis}	disable time	nOE to nAn	16.2	16.2	16.2	16.2	16.2	16.2	ns
		nOE to nBn	17.6	10.0	9.0	9.1	8.7	9.3	ns
t_{en}	enable time	nOE to nAn	21.9	21.9	21.9	21.9	21.9	21.9	ns
		nOE to nBn	22.2	11.1	9.8	9.4	9.4	9.6	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ;

t_{dis} is the same as t_{PLZ} and t_{PHZ} ;

t_{en} is the same as t_{PZL} and t_{PZH} .

Table 11. Typical dynamic characteristics at $V_{CC(B)} = 0.8\text{ V}$ and $T_{amb} = 25\text{ °C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6; for wave forms see Fig. 4 and Fig. 5. [1]

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		nBn to nAn	14.4	7.0	6.2	6.0	5.9	6.0	ns
t_{dis}	disable time	nOE to nAn	16.2	5.9	4.4	4.2	3.1	3.5	ns
		nOE to nBn	17.6	14.2	13.7	13.6	13.3	13.1	ns
t_{en}	enable time	nOE to nAn	21.9	6.4	4.4	3.5	2.6	2.3	ns
		nOE to nBn	22.2	17.7	17.2	17.0	16.8	16.7	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ;

t_{dis} is the same as t_{PLZ} and t_{PHZ} ;

t_{en} is the same as t_{PZL} and t_{PZH} .

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Table 12. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6; for wave forms see Fig. 4 and Fig. 5. [1]

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V _{CC(A)} = 1.1 V to 1.3 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.2	0.5	6.9	0.5	6.0	0.5	5.1	0.5	4.9	ns
		nBn to nAn	0.5	9.2	0.5	8.7	0.5	8.5	0.5	8.2	0.5	8.0	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	1.5	11.6	1.5	11.6	1.5	11.6	1.5	11.6	1.5	11.6	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.5	1.5	9.7	1.5	9.5	1.0	8.1	1.0	8.9	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.0	14.5	1.0	14.5	1.0	14.5	1.0	14.5	1.0	14.5	ns
		n $\overline{\text{OE}}$ to nBn	1.1	14.9	1.1	11.0	1.1	9.6	1.0	8.1	1.0	7.7	ns
V _{CC(A)} = 1.4 V to 1.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.7	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	ns
		nBn to nAn	0.5	6.9	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	ns
		n $\overline{\text{OE}}$ to nBn	1.5	11.4	1.5	8.7	1.5	7.5	1.0	6.5	1.0	6.3	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.0	10.1	1.0	10.1	1.0	10.1	1.0	10.1	1.0	10.1	ns
		n $\overline{\text{OE}}$ to nBn	1.0	13.5	1.0	10.1	0.5	8.1	0.5	5.9	0.5	5.2	ns
V _{CC(A)} = 1.65 V to 1.95 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.5	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	ns
		nBn to nAn	0.5	6.0	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	ns
		n $\overline{\text{OE}}$ to nBn	1.5	11.1	1.5	8.4	1.5	7.1	1.0	5.9	1.0	5.7	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	ns
		n $\overline{\text{OE}}$ to nBn	1.0	13.0	1.0	9.2	0.5	7.4	0.5	5.3	0.5	4.5	ns
V _{CC(A)} = 2.3 V to 2.7 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.2	0.5	5.6	0.5	4.6	0.5	3.3	0.5	2.8	ns
		nBn to nAn	0.5	5.1	0.5	4.1	0.5	3.7	0.5	3.4	0.5	3.2	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	1.0	6.1	1.0	6.1	1.0	6.1	1.0	6.1	1.0	6.1	ns
		n $\overline{\text{OE}}$ to nBn	1.0	10.6	1.0	7.9	1.0	6.6	1.0	6.1	1.0	5.2	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
		n $\overline{\text{OE}}$ to nBn	0.5	12.5	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	ns
V _{CC(A)} = 3.0 V to 3.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.0	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	ns
		nBn to nAn	0.5	4.9	0.5	3.7	0.5	3.3	0.5	2.9	0.5	2.7	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	ns
		n $\overline{\text{OE}}$ to nBn	1.0	10.3	1.0	7.7	1.0	6.5	1.0	5.2	0.5	5.0	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	0.5	4.3	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4.0	ns
		n $\overline{\text{OE}}$ to nBn	0.5	12.4	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4.0	ns

- [1] t_{pd} is the same as t_{PLH} and t_{PHL};
t_{dis} is the same as t_{PLZ} and t_{PHZ};
t_{en} is the same as t_{PZL} and t_{PZH}.

16-bit dual supply translating transceiver with configurable voltage translation; 3-state

Table 13. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6; for wave forms see Fig. 4 and Fig. 5. [1]

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V _{CC(A)} = 1.1 V to 1.3 V													
t _{pd}	propagation delay	nAn to nBn	0.5	10.2	0.5	7.6	0.5	6.6	0.5	5.7	0.5	5.4	ns
		nBn to nAn	0.5	10.2	0.5	9.6	0.5	9.4	0.5	9.1	0.5	8.8	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	1.5	12.8	1.5	12.8	1.5	12.8	1.5	12.8	1.5	12.8	ns
		n $\overline{\text{OE}}$ to nBn	1.5	13.8	1.5	10.7	1.5	10.5	1.0	9.0	1.5	9.8	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.0	16.0	1.0	16.0	1.0	16.0	1.0	16.0	1.0	16.0	ns
		n $\overline{\text{OE}}$ to nBn	1.1	16.4	1.1	12.1	1.1	10.6	1.0	9.0	1.0	8.5	ns
V _{CC(A)} = 1.4 V to 1.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.6	0.5	6.9	0.5	5.8	0.5	4.6	0.5	4.1	ns
		nBn to nAn	0.5	7.6	0.5	6.9	0.5	6.5	0.5	6.2	0.5	6.1	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	1.5	10.1	1.5	10.1	1.5	10.1	1.5	10.1	1.5	10.1	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.6	1.5	9.6	1.5	8.3	1.0	7.2	1.0	7.0	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.0	11.2	1.0	11.2	1.0	11.2	1.0	11.2	1.0	11.2	ns
		n $\overline{\text{OE}}$ to nBn	1.0	14.9	1.0	11.2	0.5	9.0	0.5	6.5	0.5	5.8	ns
V _{CC(A)} = 1.65 V to 1.95 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.4	0.5	6.5	0.5	5.3	0.5	4.1	0.5	3.7	ns
		nBn to nAn	0.5	6.6	0.5	5.8	0.5	5.3	0.5	5.0	0.5	4.9	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.3	1.5	9.3	1.5	7.9	1.0	6.5	1.0	6.3	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	1.0	8.6	1.0	8.6	1.0	8.6	1.0	8.6	1.0	8.6	ns
		n $\overline{\text{OE}}$ to nBn	1.0	14.3	1.0	10.2	0.5	8.2	0.5	5.9	0.5	5.0	ns
V _{CC(A)} = 2.3 V to 2.7 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.1	0.5	6.2	0.5	5.1	0.5	3.7	0.5	3.1	ns
		nBn to nAn	0.5	5.7	0.5	4.6	0.5	4.1	0.5	3.8	0.5	3.6	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	ns
		n $\overline{\text{OE}}$ to nBn	1.0	11.7	1.0	8.7	1.0	7.3	1.0	6.8	1.0	5.8	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	0.5	5.9	0.5	5.9	0.5	5.9	0.5	5.9	0.5	5.9	ns
		n $\overline{\text{OE}}$ to nBn	0.5	13.8	0.5	10.4	0.5	8.1	0.5	5.7	0.5	5.0	ns
V _{CC(A)} = 3.0 V to 3.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.8	0.5	6.1	0.5	4.9	0.5	3.6	0.5	3.0	ns
		nBn to nAn	0.5	5.4	0.5	4.1	0.5	3.7	0.5	3.2	0.5	3.0	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nAn	0.5	5.5	0.5	5.5	0.5	5.5	0.5	5.5	0.5	5.5	ns
		n $\overline{\text{OE}}$ to nBn	1.0	11.4	1.0	8.5	1.0	7.2	1.0	5.8	0.5	5.5	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nAn	0.5	4.8	0.5	4.8	0.5	4.7	0.5	4.6	0.5	4.4	ns
		n $\overline{\text{OE}}$ to nBn	0.5	13.7	0.5	10.3	0.5	8.0	0.5	5.4	0.5	4.4	ns

- [1] t_{pd} is the same as t_{PLH} and t_{PHL};
t_{dis} is the same as t_{PLZ} and t_{PHZ};
t_{en} is the same as t_{PZL} and t_{PZH}.

10.1. Waveforms and test circuit

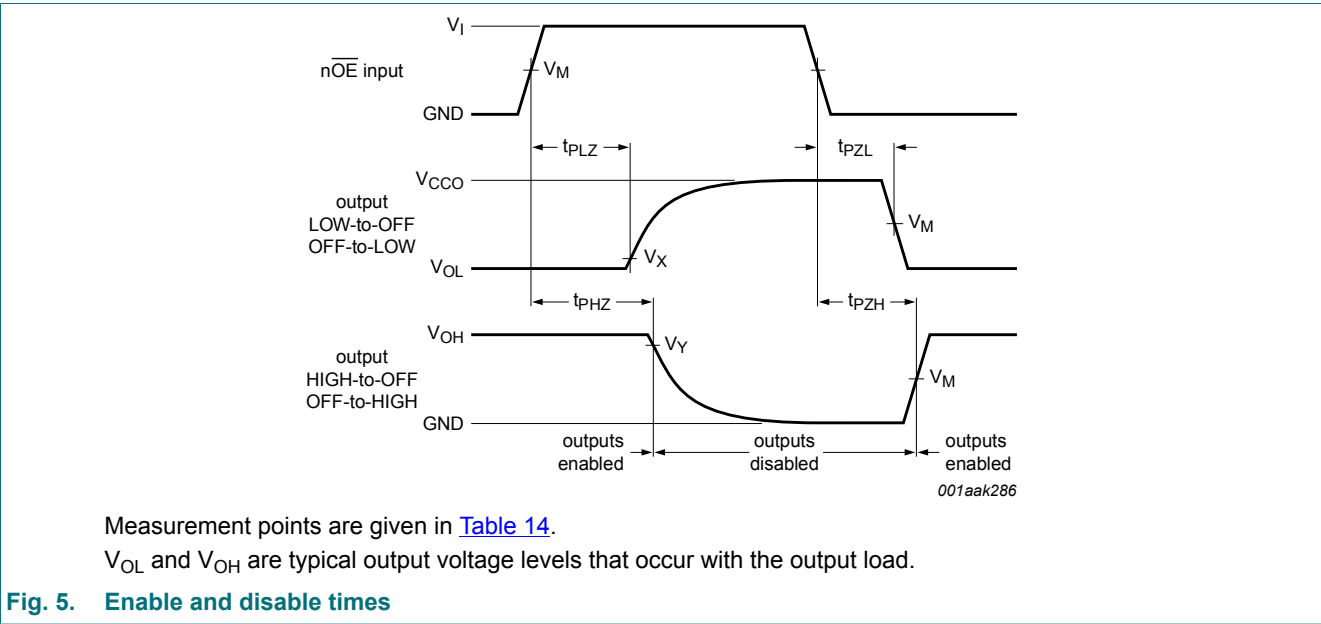
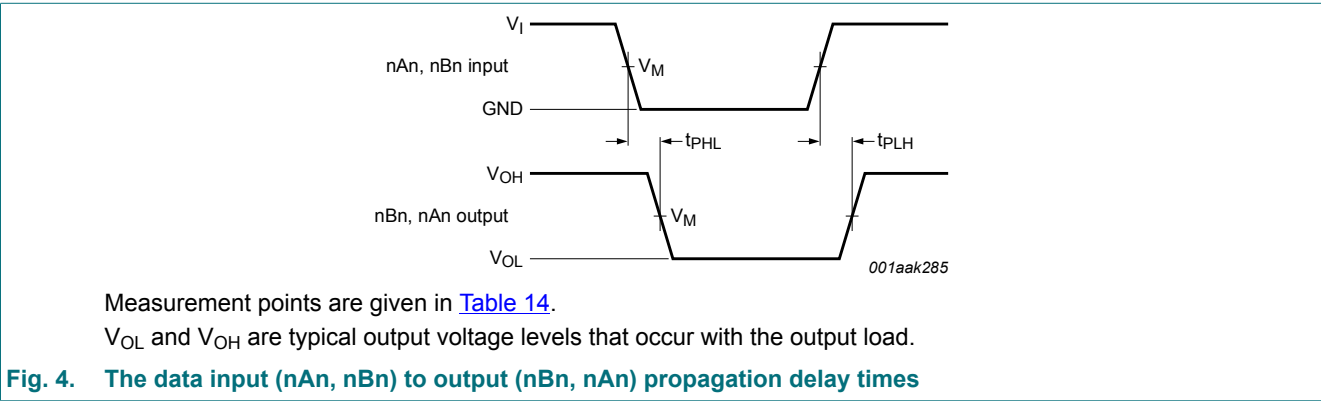


Table 14. Measurement points

Supply voltage	Input [1]	Output [2]		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1\text{ V}$	$V_{OH} - 0.1\text{ V}$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

[1] V_{CCI} is the supply voltage associated with the data input port.
[2] V_{CCO} is the supply voltage associated with the output port.

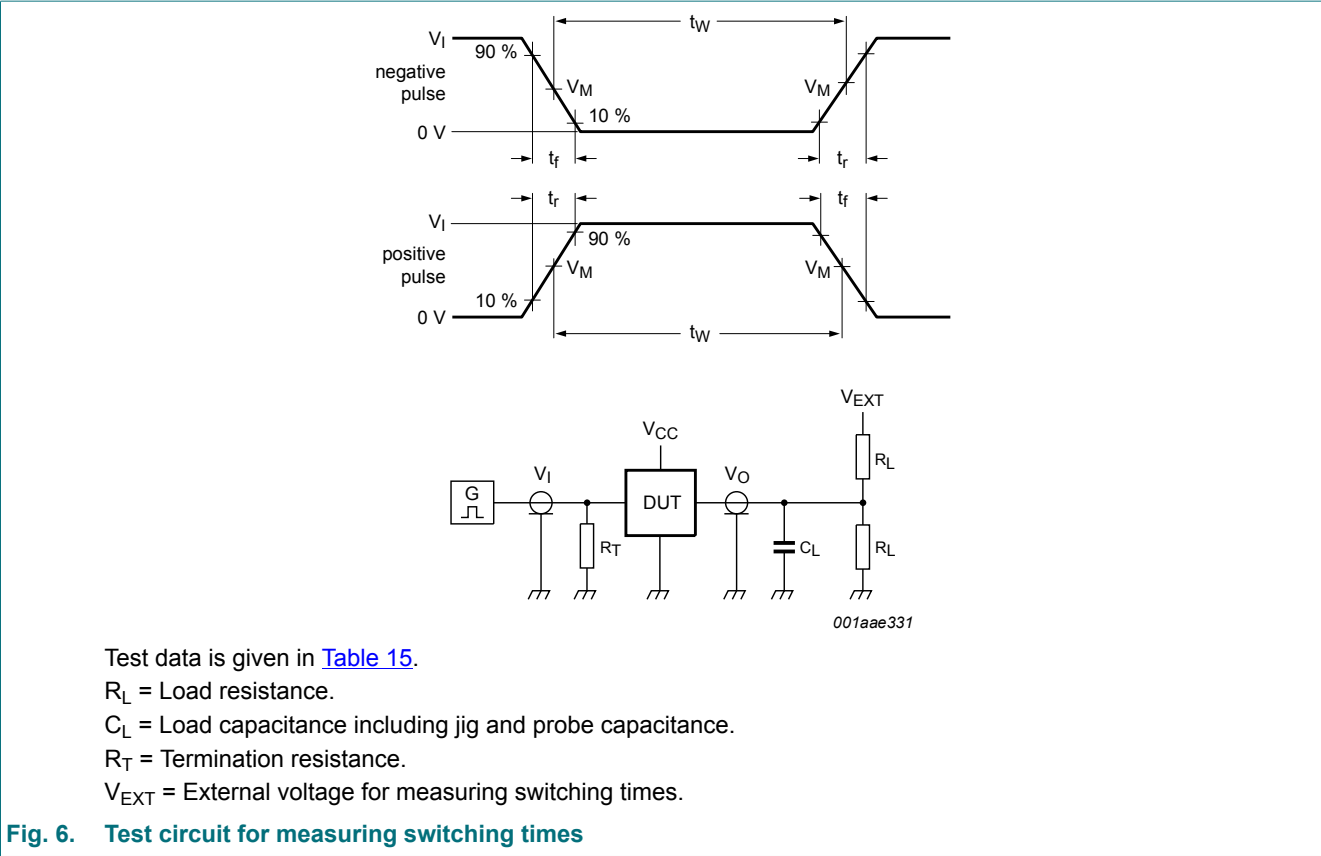


Table 15. Test data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	V_I [1]	$\Delta t/\Delta V$ [2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [3]
0.8 V to 1.6 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] $dV/dt \geq 1.0 \text{ V/ns}$

[3] V_{CCO} is the supply voltage associated with the output port.

11. Typical propagation delay characteristics

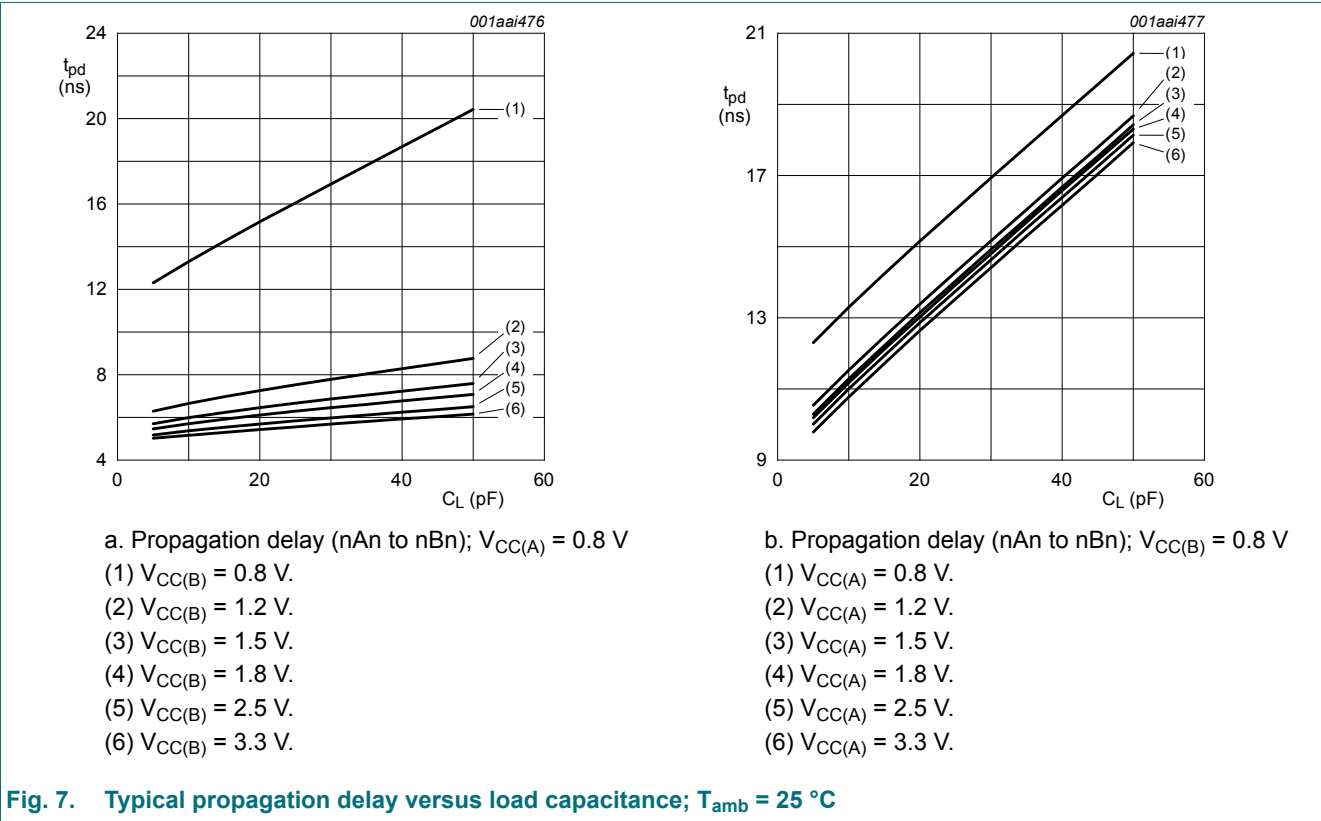
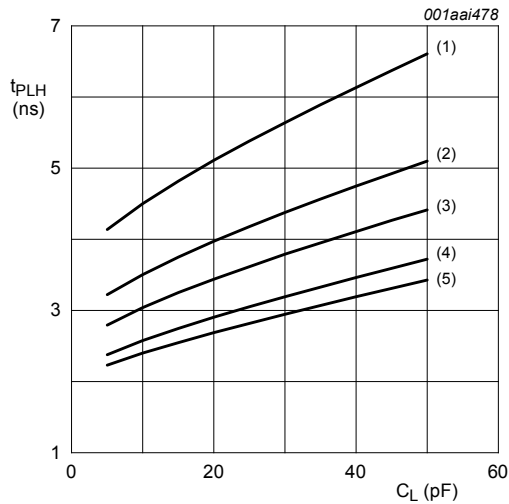
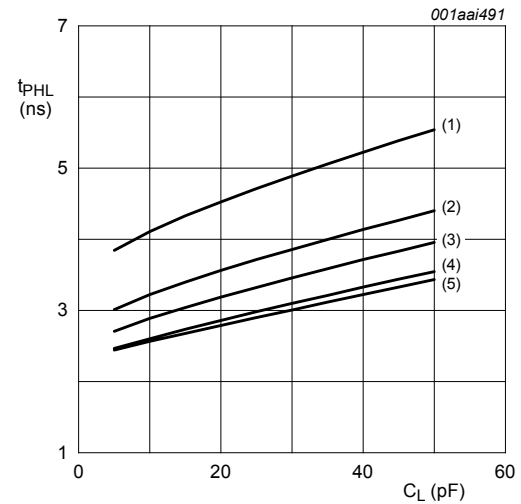


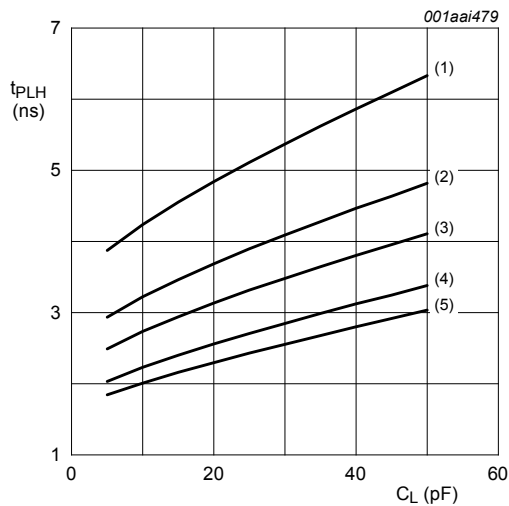
Fig. 7. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ }^{\circ}\text{C}$



a. LOW to HIGH propagation delay (nAn to nBn);
 $V_{CC(A)} = 1.2 \text{ V}$

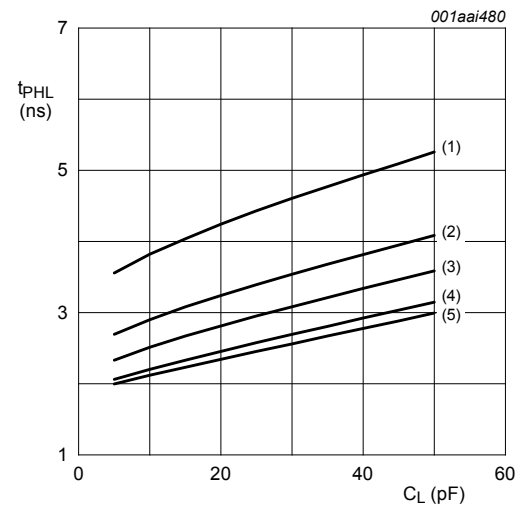


b. HIGH to LOW propagation delay (nAn to nBn);
 $V_{CC(A)} = 1.2 \text{ V}$



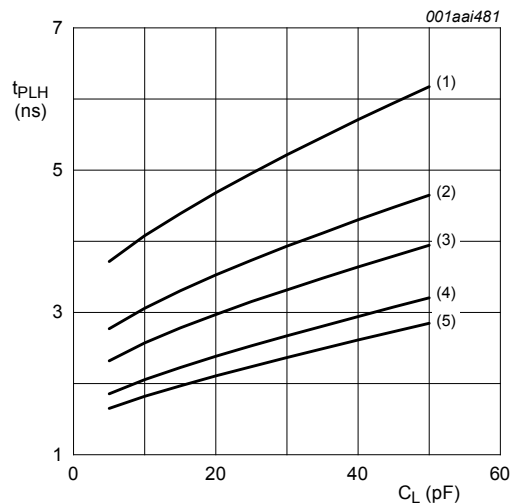
c. LOW to HIGH propagation delay (nAn to nBn);
 $V_{CC(A)} = 1.5 \text{ V}$

- (1) $V_{CC(B)} = 1.2 \text{ V}$.
- (2) $V_{CC(B)} = 1.5 \text{ V}$.
- (3) $V_{CC(B)} = 1.8 \text{ V}$.
- (4) $V_{CC(B)} = 2.5 \text{ V}$.
- (5) $V_{CC(B)} = 3.3 \text{ V}$.

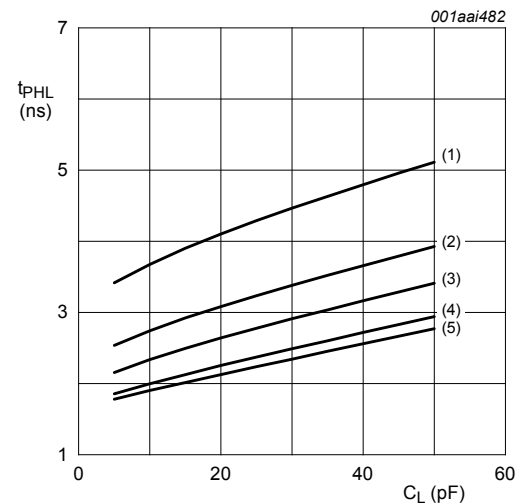


d. HIGH to LOW propagation delay (nAn to nBn);
 $V_{CC(A)} = 1.5 \text{ V}$

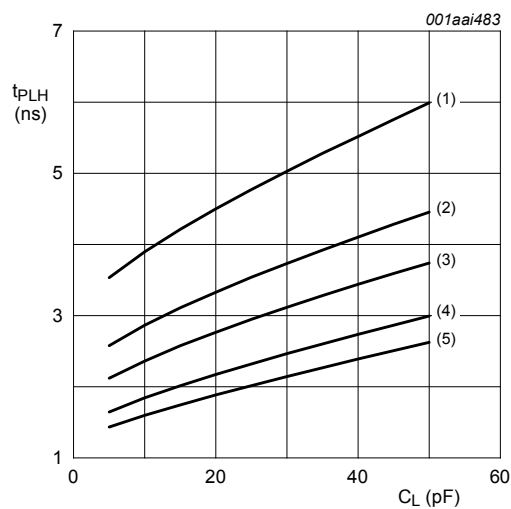
Fig. 8. Typical propagation delay versus load capacitance; $T_{amb} = 25^\circ\text{C}$



a. LOW to HIGH propagation delay (nAn to nBn);
 $V_{CC(A)} = 1.8 \text{ V}$

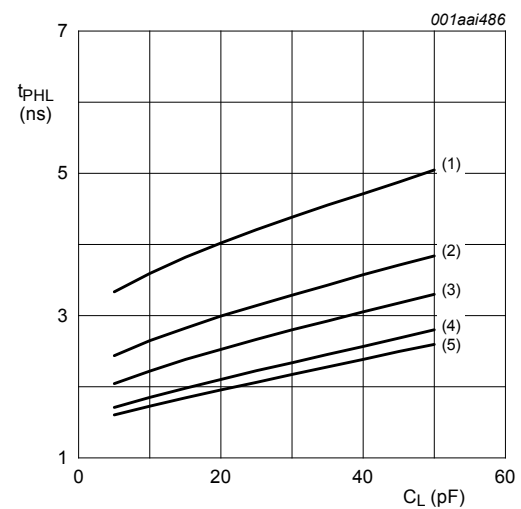


b. HIGH to LOW propagation delay (nAn to nBn);
 $V_{CC(A)} = 1.8 \text{ V}$



c. LOW to HIGH propagation delay (nAn to nBn);
 $V_{CC(A)} = 2.5 \text{ V}$

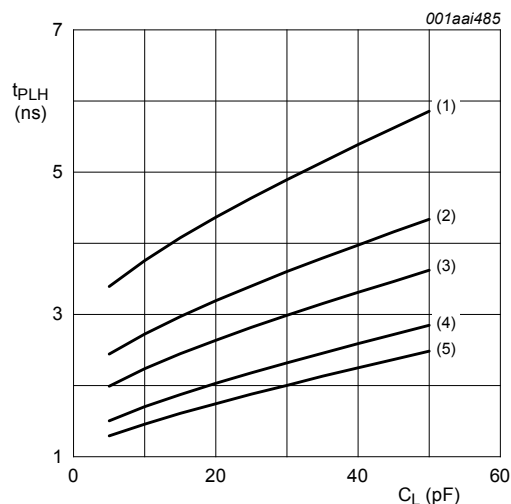
- (1) $V_{CC(B)} = 1.2 \text{ V}$.
- (2) $V_{CC(B)} = 1.5 \text{ V}$.
- (3) $V_{CC(B)} = 1.8 \text{ V}$.
- (4) $V_{CC(B)} = 2.5 \text{ V}$.
- (5) $V_{CC(B)} = 3.3 \text{ V}$.



d. HIGH to LOW propagation delay (nAn to nBn);
 $V_{CC(A)} = 2.5 \text{ V}$

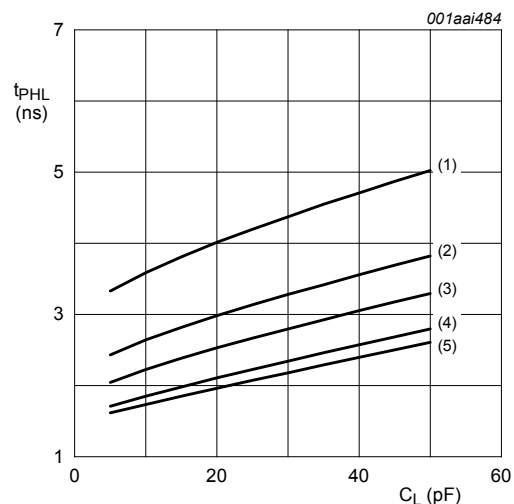
Fig. 9. Typical propagation delay versus load capacitance; $T_{amb} = 25^\circ\text{C}$

16-bit dual supply translating transceiver with configurable voltage translation; 3-state



a. LOW to HIGH propagation delay (nAn to nBn);
 $V_{CC(A)} = 3.3 \text{ V}$

- (1) $V_{CC(B)} = 1.2 \text{ V}$.
- (2) $V_{CC(B)} = 1.5 \text{ V}$.
- (3) $V_{CC(B)} = 1.8 \text{ V}$.
- (4) $V_{CC(B)} = 2.5 \text{ V}$.
- (5) $V_{CC(B)} = 3.3 \text{ V}$.



b. HIGH to LOW propagation delay (nAn to nBn);
 $V_{CC(A)} = 3.3 \text{ V}$

Fig. 10. Typical propagation delay versus load capacitance; $T_{amb} = 25^\circ\text{C}$

12. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm SOT362-1

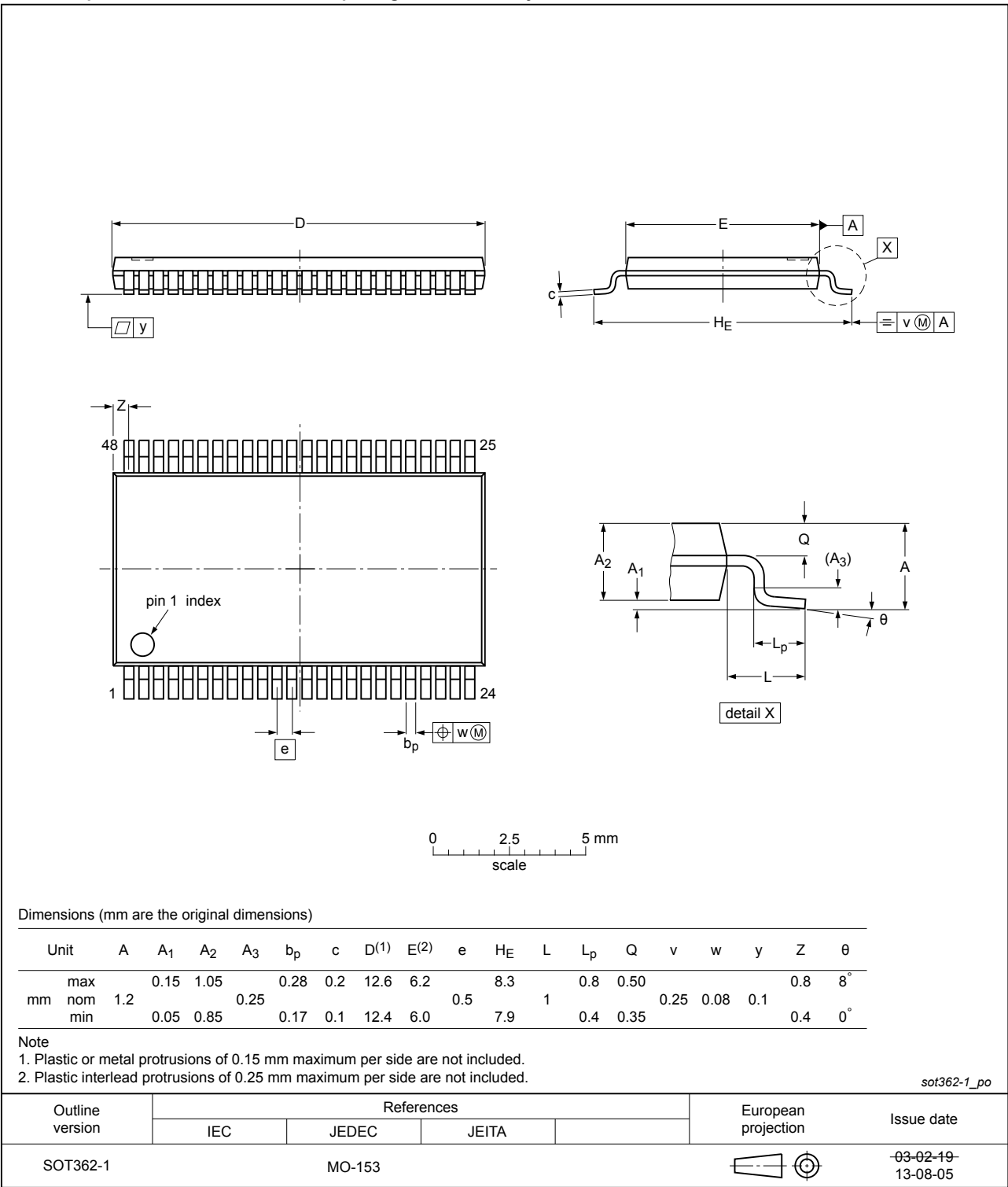


Fig. 11. Package outline SOT362-1 (TSSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads;
body width 4.4 mm; lead pitch 0.4 mm

SOT480-1

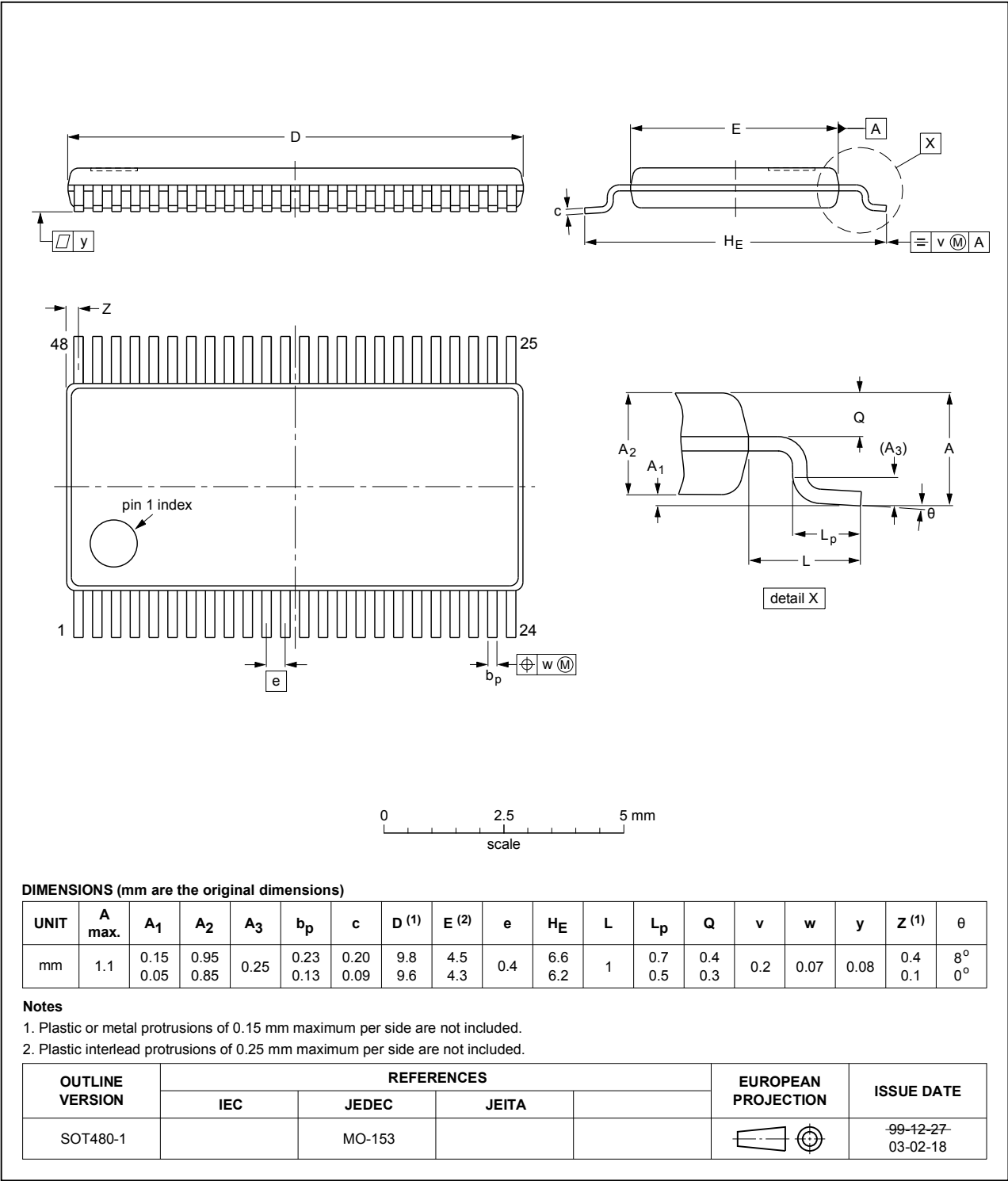


Fig. 12. Package outline SOT480-1 (TSSOP48)

13. Abbreviations

Table 16. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC16T245 v.7	20190114	Product data sheet	-	74AVC16T245 v.6
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type numbers 74AVC16T245EV (SOT702-1) and 74AVC16T245BX (SOT1134-2) removed.			
74AVC16T245 v.6	20130909	Product data sheet	-	74AVC16T245 v.5
Modifications:	Table 4: conditions I_{CC} and I_{GND} changed (errata).			
74AVC16T245 v.5	20120309	Product data sheet	-	74AVC16T245 v.4
Modifications:	For type number 74AVC16T245BX the sot code has changed to SOT1134-2.			
74AVC16T245 v.4	20111208	Product data sheet	-	74AVC16T245 v.3
Modifications:	Legal pages updated.			
74AVC16T245 v.3	20110609	Product data sheet	-	74AVC16T245 v.2
74AVC16T245 v.2	20100330	Product data sheet	-	74AVC16T245 v.1
74AVC16T245 v.1	20091001	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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