W83977F/ AF Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	n.a.	01/20/97	0.50		First publication
2	2,3,6,8,9,10, 122,126,128-132,134,138,168	01/27/97	0.51		Spec. Correction; typo correction
3	117-125,127	01/30/97	0.52		Register Correction; pages rearranging.
4	9,10,120-122	02/13/97	0.53		Spec. Correction; typo correction
5	127,135,136,169	03/03/97	0.54		Spec. Correction; typo correction
6	VIII,IX,166-169	05/24/97	0.55		Add section 15.0; pages rearranging.
7	P118	7/15/97	0.56		CR24: Pin 22→Pin1
8	53,54,58,61,62, 63,65,124,125	11/17/97	0.57		Register Correction
9	1,3,11,52,91,105, 109,110,111,113, 114,115,119,124, 130,131,148	03/10/98	0.58		Typo correction and data calibrated
10	n.a.	05/02/06	0.6		Add lead-free package version

Table of Contents-

1. GENERAL DESCRIPTION

This data sheet covers two products: W83977F/G, and W83977AF/AG whose pin assignment, and most of the functions are the same. W83977AF/AG is an advanced version of W83977F/G featuring the FIR function.

W83977F/G, W83977AF/AG are evolving products from Winbond's most popular I/O chip W83877F --- which integrates the disk drive adapter, serial port (UART), IrDA 1.0 SIR, parallel port, configurable plug-and-play registers in one chip --- plus additional powerful features: **ACPI**, 8042 keyboard controller with PS/2 mouse support, Real Time Clock, 14 general purpose I/O ports, full 16-bit address decoding, TV remote IR (Consumer IR, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols). In addition, W83977AF/AG provides the functions of **IrDA 1.1** (MIR for 1.152M bps or FIR for 4M bps).

The disk drive adapter functions of W83977F/G, W83977AF/AG include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt/ DMA logic. The wide range of functions integrated onto the W83977F/G, W83977AF/AG greatly reduces the number of components required for interfacing with floppy disk drives. The W83977F/G, W83977AF/AG supports up to four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83977F/G, W83977AF/AG provide two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate 115.2k and provide advanced speed with baud rate **230k**, **460k**, and **921k bps** which support higher speed modems. W83977AF/AG alone provides independent **3rd UART** (32-byte FIFO) dedicated for IR function.

The W83977F/G, W83977AF/AG supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95^{TM}, which makes system resource allocation more efficient than ever.

W83977F/G, W83977AF/AG provides functions that comply with **ACPI** (*Advanced Configuration and Power Interface*), which includes support of legacy and ACPI power management through SMI or SCI function pins. W83977F/G, W83977AF/AG also has auto power management to reduce power consumption.

The keyboard controller is based on 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware is available with optional AMIKEY^{TM} -2, Phoenix MultiKey/42^{TM}, or customer code.

The W83977F/G, W83977AF/AG provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a pre-defined alternate function.

W83977F/G, W83977AF/AG is made to fully comply with **Microsoft^{TM} PC97 Hardware Design Guide**. IRQs, DMAs, and I/O space resource are flexible to adjust to meet ISA PnP requirement. Full 16-bit address decoding is also provided. Moreover W83977F/G, W83977AF/AG is made to meet the specification of PC97's requirement in the power management: **ACPI** and **DPM** (Device Power Management).

2. FEATURES

General

- Plug & Play 1.0A Compliant
- Support 13 IRQs, 4 DMA channels, full 16-bit addresses decoding
- Capable of ISA Bus IRQ Sharing
- Compliant with Microsoft PC97 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- 24 or 14.318 Mhz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support **3-mode FDD, and its Win95 driver**

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- 3rd UART with 32-byte send/receive FIFO is supported for IR function [W83977AF/AG only]
- MIDI compatible
- Fully programmable serial-interface characteristics:
  - --- 5, 6, 7 or 8-bit characters
  - --- Even, odd or no parity bit generation/detection
  - --- 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  - --- Loop-back controls for communications link fault isolation
  - --- Break, parity, overrun, framing error simulation
- Programmable baud generator allows division of 1.8461 Mhz and 24 Mhz by 1 to (216-1)
- Maximum baud rate up to **921k bps** for 14.769 Mhz and 1.5M bps for 24 Mhz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support IrDA version 1.1 MIR (1.152M bps) and FIR (4M bps) protocol *[W83977AF/AG only]*

--- Single DMA channel for transmitter or receiver

--- 3rd UART with 32-byte FIFO is supported in both TX/RX transmission *[W83977AF/AG only]*

--- 8-byte status FIFO is supported to store received frame status (such as overrun CRC error, etc.)

- Support auto-config SIR and FIR *[W83977AF/AG only]*

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Advanced Power Management (APM) Controlling

- Power turned on when RTC reaches a preset date and time
- Power turned on when a ring pulse or pulse train is detected on the PHRI, or when a high to low transition on PWAKIN1, or PWAKIN2 input signals
- Power turned on when PANSW input signal indicates a switch on event
- Power turned off when PANSW input signal indicates a switch off event
- Power turned off when a fail-safe event occurs (power-save mode detected but system is hung up)
- Power turned off when software issues a power off command

Keyboard Controller

- 8042 based with optional F/W from AMIKKEY^{TM}-2, Phoenix MultiKey/42^{TM} or customer code
- with 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042 and PC87911 microcontrollers
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- **Fast Gate A20 and Hardware Keyboard Reset**
- 8 Bit Timer/ Counter; support binary and BCD arithmetic
- 6, 8, 12, or 16 Mhz operating frequency (16 Mhz available only if input clock rate = 14.318 Mhz)

Real Time Clock

- 27 bytes of clock, **On-Now**, and control/status register (14 bytes in Bank 0 and 13 bytes in Bank 2); 242 bytes of general purpose RAM
- BCD or Binary representation of time, calendar, and alarm registers
- Counts seconds, minutes, hours, days of week, days of month, month, year, and century
- 12-hour/ 24-hour clock with AM/PM in 12-hour mode
- Daylight saving time option; automatic leap-year adjustment
- Dedicated alarm (Alarm B) for **On-Now** function
- Programmable delay-time between panel switch off and power supply control
- Software control power-off; various and maskable events to activate system Power-On
- System Management Interrupt ($\overline{\text{SMI}}$) for panel switch power-off event

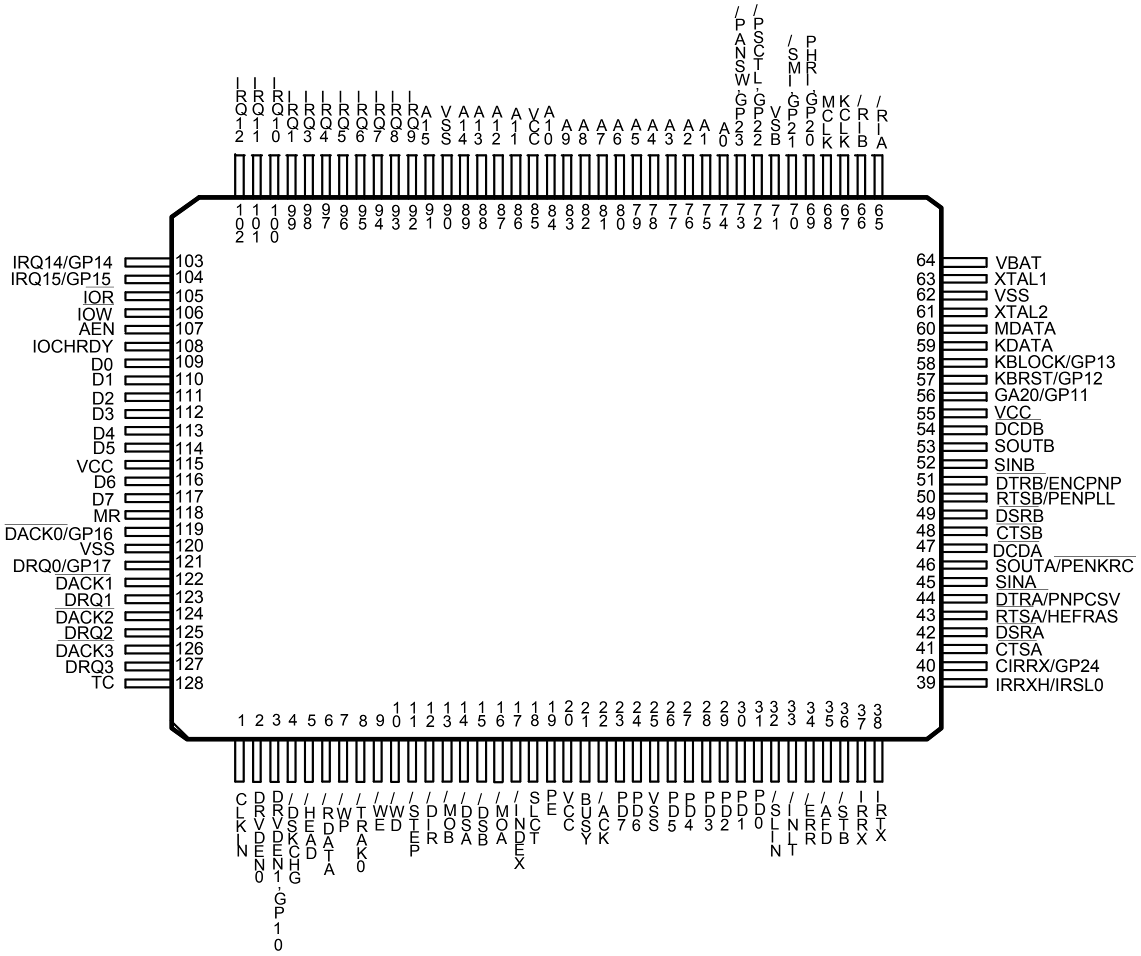
General Purpose I/O Ports

- 14 programmable general purpose I/O ports; 6 dedicate, 8 optional
- General purpose I/O ports can serve as simple I/O ports, interrupt steering inputs, watching dog timer output, power LED output, infrared I/O pins, general purpose address decoder, KBC control I/O pins.

Package

- 128-pin PQFP

3. PIN CONFIGURATION



4. PIN DESCRIPTION

Note: Please refer to Section 11.2 DC CHARACTERISTICS for details.

I/O6t - TTL level bi-directional pin with 6 mA source-sink capability

I/O8t - TTL level bi-directional pin with 8 mA source-sink capability

I/O8 - CMOS level bi-directional pin with 8 mA source-sink capability

I/O12t - TTL level bi-directional pin with 12 mA source-sink capability

I/O12 - CMOS level bi-directional pin with 12 mA source-sink capability

I/O16u - CMOS level bi-directional pin with 16 mA source-sink capability with internal pull-up resistor

I/OD16u - CMOS level bi-directional pin open drain output with 16 mA sink capability with internal pull-up resistor

I/O24t - TTL level bi-directional pin with 24 mA source-sink capability

OUT8t - TTL level output pin with 8 mA source-sink capability

OUT12t - TTL level output pin with 12 mA source-sink capability

OD12 - Open-drain output pin with 12 mA sink capability

OD24 - Open-drain output pin with 24 mA sink capability

INt - TTL level input pin

INc - CMOS level input pin

INcu - CMOS level input pin with internal pull-up resitor

INcs - CMOS level Schmitt-triggered input pin

INts - TTL level Schmitt-triggered input pin

INtsu - TTL level Schmitt-triggered input pin with internal pull-up resistor

4.1 Host Interface

SYMBOL	PIN	I/O	FUNCTION
A0–A10	74-84	IN$_t$	System address bus bits 0-10
A11-A14	86-89	IN$_t$	System address bus bits 11-14
A15	91	IN$_t$	System address bus bit 15
D0–D5	109-114	I/O$_{12t}$	System data bus bits 0-5
D6–D7	116-117	I/O$_{12t}$	System data bus bits 6-7
$\overline{\text{IOR}}$	105	IN$_{ts}$	CPU I/O read signal
$\overline{\text{IOW}}$	106	IN$_{ts}$	CPU I/O write signal
AEN	107	IN$_t$	System address bus enable
IOCHRDY	108	OD$_{24}$	In EPP Mode, this pin is the IO Channel Ready output to extend the host read/write cycle.
MR	118	IN$_{ts}$	Master Reset. Active high. MR is low during normal operations.

Host Interface, continued.

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{DACK0}}$ GP16 (WDTO) P15 $\overline{\text{RTSC}}$	119	IN_{ts} I/O_{12t} I/O_{12t} OUT_{12t}	CR2C bit5, 4= 00 (default): DMA Channel 0 Acknowledge signal. CR2C bit5, 4= 01: General purpose I/O port 1 bit 6. It can be configured as a watchdog timer output. CR2C bit5, 4= 10: Keyboard P15 I/O port. CR2C bit5, 4= 11: $\overline{\text{RTS}}$ output of UART C. *[W83977AF only]*
DRQ0 GP17 (PLEDO) P14 $\overline{\text{DTRC}}$	121	OUT_{12t} I/O_{12t} I/O_{12t} OUT_{12t}	CR2C bit7, 6= 00 (default): DMA Channel 0 request signal. CR2C bit7, 6= 01: General purpose I/O port 1, bit 7. It can be configured as power LED output. CR2C bit7, 6= 10: Keyboard P14 I/O port. CR2C bit7, 6= 11: $\overline{\text{DTR}}$ output of UART C. *[W83977AF only]*
$\overline{\text{DACK1}}$	122	IN_{ts}	DMA Channel 1 Acknowledge signal
DRQ1	123	OUT_{12t}	DMA Channel 1 request signal
$\overline{\text{DACK2}}$	124	IN_{ts}	DMA Channel 2 Acknowledge signal
DRQ2	125	OUT_{12t}	DMA Channel 2 request signal
$\overline{\text{DACK3}}$	126	IN_{ts}	DMA Channel 3 Acknowledge signal
DRQ3	127	OUT_{12t}	DMA Channel 3 request signal
TC	128	IN_{ts}	Terminal Count. When active, this pin indicates termination of a DMA transfer.
IRQ1	99	OUT_{12t}	Interrupt request 1
IRQ3	98	OUT_{12t}	Interrupt request 3
IRQ4	97	OUT_{12t}	Interrupt request 4
IRQ5	96	OUT_{12t}	Interrupt request 5
IRQ6	95	OUT_{12t}	Interrupt request 6
IRQ7	94	OUT_{12t}	Interrupt request 7
IRQ8/ nIRQ8	93	OUT_{12t}	Interrupt request 8; default is nIRQ8 for RTC
IRQ9	92	OUT_{12t}	Interrupt request 9
IRQ10	100	OUT_{12t}	Interrupt request 10
IRQ11	101	OUT_{12t}	Interrupt request 11
IRQ12	102	OUT_{12t}	Interrupt request 12

Host Interface, continued.

SYMBOL	PIN	I/O	FUNCTION
IRQ14 GP14 ($\overline{\text{GPACS}}$) PLED IRSL1	103	OUT_{12t} I/O_{12t} OUT_{12t} OUT_{12t}	CR2C bit1, 0= 00 (default): Interrupt request 14 CR2C bit1, 0= 01: General purpose I/O port 1, bit 4. It can be configured as a general purpose address decode output. CR2C bit1, 0= 10: Power LED output. CR2C bit1, 0= 11: IR module select signal 1. *[W83977AF only]*
IRQ15 GP15 ($\overline{\text{GPAWE}}$) WDT IRSL2	104	OUT_{12t} I/O_{12t} OUT_{12t} OUT_{12t}	CR2C bit3, 2= 00 (default): Interrupt request 15 CR2C bit3, 2= 01: General purpose I/O port 1, bit 5. It can be configured as a general purpose address write enable output. CR2C bit3, 2= 10: Watch-Dog timer output. CR2C bit3, 2= 11: IR module select signal 2. *[W83977AF only]*
CLKIN	1	IN_t	14.318/ 24 Mhz clock input, selectable through bit 5 of CR24.

4.2 Advanced Power Management

SYMBOL	PIN	I/O	FUNCTION
PHRI GP20 (KBRST)	69	IN_t I/O_{12t}	CR2B bit2, 1=00 (default): Advanced Power Management (APM) phone ring indicator. Detection of an active PHRI pulse or pulse train activates the $\overline{\text{PSCTL}}$ signal. CR2B bit2, 1=01: General purpose I/O port 2, bit 0. It can be configured as keyboard reset (Keyboard P20).
POFIRQ GP21 (P13) P16 $\overline{\text{RIC}}$	70	OUT_{12t} I/O_{12t} I/O_{12t} IN_t	CR2B bit4, 3=00 (default): Advanced Power Management (APM) power off interrupt request. CR2B bit4, 3=01: General purpose I/O port 2, bit 1. It can be configured as Keyboard P13 I/O port. CR2B bit4, 3=10: Keyboard P16 I/O port. CR2B bit4, 3=11: $\overline{\text{RI}}$ input of UART C. *[W83977AF only]*
VSB	71	-	Advanced Power Management (APM) standby current source
$\overline{\text{PSCTL}}$ GP22 (P14)	72	OUT_{12t} I/O_{12t}	CR2B bit5=0 (default): On/Off control for Advanced Power Management (APM). This signal tells the main power supply whether power should be turned on. CR2B bit5=1: General purpose I/O port 2, bit 2. It can be configured as Keyboard P14 I/O port.
$\overline{\text{PANSW}}$	73	IN_t	CR2B bit7, 6=00 (default): On/Off switch for Advanced Power Management (APM). This signal indicates a request to switch the power on or off. When the VDD of the chip is disrupted, a high to low transition on this pin indicates a switch on request. When VDD returns, a high to low transition on this pin indicates a switch off request.

Advanced Power Management, continued.

SYMBOL	PIN	I/O	FUNCTION
GP23 (P15)		I/O_{12t}	CR2B bit7, 6=01: General purpose I/O port 2, bit 3. It can be configured as Keyboard P15 I/O port.
$\overline{\text{DCDC}}$		IN_t	CR2B bit7, 6=11: $\overline{\text{DCD}}$ input of UART C. *[W83977AF only]*

4.3 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{CTSA}}$ $\overline{\text{CTSB}}$	41 48	IN_t	Clear To Send is the modem control input. The function of these pins can be tested by reading Bit 4 of the handshake status register.
$\overline{\text{DSRA}}$ $\overline{\text{DSRB}}$	42 49	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
$\overline{\text{RTSA}}$ HEFRAS	43	I/O_{8t}	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 370H as configuration I/O port address)
$\overline{\text{RTSB}}$ nPENPLL	50	I/O_{8t}	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as nPENPLL, which provides the power-on value for CR24 bit 5 (ENPLL) and bit 6. A 4.7 kΩ is recommended if intends to pull up. (PLL is disabled)
$\overline{\text{DTRA}}$ $\overline{\text{PNPCSV}}$	44	I/O_{8t}	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as $\overline{\text{PNPCSV}}$, which provides the power-on value for CR24 bit 0 ($\overline{\text{PNPCSV}}$). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PTR)
$\overline{\text{DTRB}}$ ENCPNP	51	I/O_{8t}	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as ENCPNP, which provides the power-on value for CR24 bit 1 (ENPNP). A 4.7 kΩ is recommended if intends to pull up. (enable comply PnP mode)
SINA SINB	45, 52	IN_t	Serial Input. Used to receive serial data through the communication link.

Serial Port Interface, continued.

SYMBOL	PIN	I/O	FUNCTION
SOUTA PENKRC	46	I/O$_{8t}$	UART A Serial Output. Used to transmit serial data out to the communication link. During power-on reset, this pin is pulled down internally and is defined as PENKRC, which provides the power-on value for CR24 bit 2 (ENKBRTC). A 4.7 kΩ is recommended if intends to pull up. (enable KBC and RTC)
SOUTB	53	I/O$_{8t}$	UART B Serial Output. Used to transmit serial data out to the communication link.
$\overline{DCDA}$ $\overline{DCDB}$	47 54	IN$_{t}$	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
$\overline{RIA}$ $\overline{RIB}$	65 66	IN$_{t}$	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

4.4 Infrared Interface

SYMBOL	PIN	I/O	FUNCTION
IRRX (SINC)	37	IN$_{cs}$	Infrared Receiver input. It functions as SIN input if UART C is configured as a simple serial port. *[W83977AF only]*
IRTX (SOUTC)	38	OUT$_{12t}$	Infrared Transmitter Output. It functions as SOUT output if UART C is configured as a simple serial port. *[W83977AF only]*
IRRXH IRSL0 GP25 (GA20) $\overline{CTSC}$	39	I/O$_{12t}$ OUT$_{12t}$ I/O$_{12t}$ IN$_{t}$	CR2A bit3, 2=00 (default): High speed IR receiving terminal. CR2A bit3, 2=01: IR module select 0. CR2A bit3, 2=10: General purpose I/O port 2, bit 5. It can be configured as GATE A20 (Keyboard P21). CR2A bit3, 2=11: $\overline{CTS}$ input of UART C. *[W83977AF only]*
CIRRX GP24 (P16) P13	40	IN$_{t}$ I/O$_{12t}$ I/O$_{12t}$	CR2A bit5, 4=00 (default): Consumer IR receiving terminal. CR2A bit5, 4=01: General purpose I/O port 2, bit 4. It can be configured as Keyboard P16 I/O port. CR2A bit5, 4=10: Keyboard P13 I/O

4.5 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT	18	$\mathrm{IN_t}$	PRINTER MODE: SLCT An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		$\mathrm{OD_{12}}$	EXTENSION FDD MODE: $\overline{\mathrm{WE2}}$ This pin is for Extension FDD B; its function is the same as the $\overline{\mathrm{WE}}$ pin of FDC.
		$\mathrm{OD_{12}}$	EXTENSION 2FDD MODE: $\overline{\mathrm{WE2}}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{\mathrm{WE}}$ pin of FDC.
PE	19	$\mathrm{IN_t}$	PRINTER MODE: PE An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		$\mathrm{OD_{12}}$	EXTENSION FDD MODE: $\overline{\mathrm{WD2}}$ This pin is for Extension FDD B; its function is the same as the $\overline{\mathrm{WD}}$ pin of FDC.
		$\mathrm{OD_{12}}$	EXTENSION 2FDD MODE: $\overline{\mathrm{WD2}}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{\mathrm{WD}}$ pin of FDC.
BUSY	21	$\mathrm{IN_t}$	PRINTER MODE: BUSY An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		$\mathrm{OD_{12}}$	EXTENSION FDD MODE: $\overline{\mathrm{MOB2}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\mathrm{MOB}}$ pin of FDC.
		$\mathrm{OD_{12}}$	EXTENSION 2FDD MODE: $\overline{\mathrm{MOB2}}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{\mathrm{MOB}}$ pin of FDC.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{ACK}}$	22	IN_t	PRINTER MODE: $\overline{\text{ACK}}$ An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{\text{DSB2}}$ This pin is for the Extension FDD B; its functions is the same as the $\overline{\text{DSB}}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{\text{DSB2}}$ This pin is for Extension FDD A and B; it functions is the same as the $\overline{\text{DSB}}$ pin of FDC.
$\overline{\text{ERR}}$	34	IN_t	PRINTER MODE: $\overline{\text{ERR}}$ An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{\text{HEAD2}}$ This pin is for Extension FDD B; its function is the same as the $\overline{\text{HEAD}}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{\text{HEAD2}}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{\text{HEAD}}$ pin of FDC.
$\overline{\text{SLIN}}$	32	OD_{12}	PRINTER MODE: $\overline{\text{SLIN}}$ Output line for detection of printer selection. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{\text{STEP2}}$ This pin is for Extension FDD B; its function is the same as the $\overline{\text{STEP}}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{\text{STEP2}}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{\text{STEP}}$ pin of FDC.
$\overline{\text{INIT}}$	33	OD_{12}	PRINTER MODE: $\overline{\text{INIT}}$ Output line for the printer initialization. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{\text{DIR2}}$ This pin is for Extension FDD B; its function is the same as the $\overline{\text{DIR}}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{\text{DIR2}}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{\text{DIR}}$ pin of FDC.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{AFD}}$	35	OD$_{12}$ OD$_{12}$ OD$_{12}$	PRINTER MODE: $\overline{\text{AFD}}$ An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC. EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.
$\overline{\text{STB}}$	36	OD$_{12}$ - -	PRINTER MODE: $\overline{\text{STB}}$ An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: This pin is a tri-state output.
PD0	31	I/O$_{24t}$ IN$_t$ IN$_t$	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: $\overline{\text{INDEX2}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\text{INDEX}}$ pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: $\overline{\text{INDEX2}}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{\text{INDEX}}$ pin of FDC. It is pulled high internally.
PD1	30	I/O$_{24t}$ IN$_t$ IN$_t$	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. . EXTENSION FDD MODE: $\overline{\text{TRAK02}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\text{TRAK0}}$ pin of FDC. It is pulled high internally.. EXTENSION. 2FDD MODE: $\overline{\text{TRAK02}}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{\text{TRAK0}}$ pin of FDC. It is pulled high internally.
PD2	29	I/O$_{24t}$ IN$_t$ IN$_t$	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.. EXTENSION FDD MODE: $\overline{\text{WP2}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\text{WP}}$ pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE: $\overline{\text{WP2}}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{\text{WP}}$ pin of FDC. It is pulled high internally.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
PD3	28	I/O$_{24t}$ IN$_t$ IN$_t$	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: $\overline{\text{RDATA2}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\text{RDATA}}$ pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: $\overline{\text{RDATA2}}$ This pin is for Extension FDD A and B; this function of this pin is the same as the $\overline{\text{RDATA}}$ pin of FDC. It is pulled high internally.
PD4	27	I/O$_{24t}$ IN$_t$ IN$_t$	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: $\overline{\text{DSKCHG2}}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{\text{DSKCHG}}$ pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: $\overline{\text{DSKCHG2}}$ This pin is for Extension FDD A and B; this function of this pin is the same as the $\overline{\text{DSKCHG}}$ pin of FDC. It is pulled high internally.
PD5	26	I/O$_{24t}$ - -	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6	24	I/O$_{24t}$ - OD$_{24}$	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION. 2FDD MODE: $\overline{\text{MOA2}}$ This pin is for Extension FDD A; its function is the same as the $\overline{\text{MOA}}$ pin of FDC.
PD7	23	I/O$_{24t}$ - OD$_{24}$	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: $\overline{\text{DSA2}}$ This pin is for Extension FDD A; its function is the same as the $\overline{\text{DSA}}$ pin of FDC.

4.6 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	2	OD_{24}	Drive Density Select bit 0.
DRVDEN1 GP10 (IRQIN1) P12 $\overline{\text{DSRC}}$	3	OD_{24}	Drive Density Select bit 1. Alternate Function 1: General purpose I/O port 1, bit 0. It can be configured as an interrupt channel. Alternate Function 2: Keyboard P12 I/O port. Alternate Function 3: $\overline{\text{DSR}}$ input of UART C *[W83977AF only]*
$\overline{\text{HEAD}}$	5	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0; Logic 0 = side 1
$\overline{\text{WE}}$	9	OD_{24}	Write enable. An open drain output.
$\overline{\text{WD}}$	10	OD_{24}	Write data. This logic low open drain writes precompensation serial data to the selected FDD. An open drain output.
$\overline{\text{STEP}}$	11	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
$\overline{\text{DIR}}$	12	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion; Logic 0 = inward motion
$\overline{\text{MOB}}$	13	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
$\overline{\text{DSA}}$	14	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
$\overline{\text{DSB}}$	15	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
$\overline{\text{MOA}}$	16	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
$\overline{\text{DSKCHG}}$	4	IN_{cs}	Diskette change. This signal is active low at power on and when the diskette is removed. This input pin is pulled up internally by a 1 K resistor, which can can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{\text{RDATA}}$	6	IN_{cs}	The read data input signal from the FDD. This input pin is pulled up internally by a 1 K resistor, which can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{\text{WP}}$	7	IN_{cs}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 K resistor, which can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{\text{TRAK0}}$	8	IN_{cs}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 K resistor, which can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{\text{INDEX}}$	17	IN_{cs}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 K resistor, which can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

4.7 KBC Interface

SYMBOL	PIN	I/O	FUNCTION
KDATA	59	I/OD$_{16u}$	Keyboard Data
MDATA	60	I/OD$_{16u}$	PS2 Mouse Data
KCLK	67	I/OD$_{16u}$	Keyboard Clock
MCLK	68	I/OD$_{16u}$	PS2 Mouse Clock
GA20 GP11 (IRQIN2)	56	OUT$_{12t}$ I/O$_{12t}$	CR2A bit6= 0 (default): Keyboard GATE A20 (P21) Output. CR2A bit6= 1: General purpose I/O port 1, bit 1. It can be configured as an interrupt channel.
KBRST GP12 (WDTO, IRRX)	57	OUT$_{12t}$ I/O$_{12t}$	CR2A bit7= 0 (default): Keyboard Reset (P20) Output. CR2A bit7= 1: General purpose I/O port 1, bit 2. It can be configured as watchdog timer output or IRRX (SINC if UART C is used as a simple serial port *[W83977AF only]*) input.
KBLOCK GP13 (PLEDO, IRTX)	58	IN$_{16tu}$ I/O$_{16tu}$	CR2B bit0= 0 (default): Keyboard KINH (P17) Input. CR2B bit0= 1: General purpose I/O port 1, bit 3. It can be configured as watchdog timer output or IRTX (SOUTC if UART C is used as a simple serial port *[W83977AF only]*) output.

4.8 RTC Interface

SYMBOL	PIN	I/O	FUNCTION
VBAT	64		RTC battery voltage input
XTAL1	63	IN$_C$	RTC 32.768Khz Clock Input
XTAL2	61	O$_{8t}$	RTC 32.768Khz Clock Output

4.9 POWER PINS

VCC	20,55, 85,115	+5V power supply for the digital circuitry
GND	25,62, 90,120	Ground

5. FDC FUNCTIONAL DESCRIPTION

5.1 W83977F/G and W83977AF/AG FDC

The floppy disk controller of the W83977F/G, W83977AF/AG integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution. All programmable options default to compatible values. The FIFO provides better system performance in multi-master systems. The digital data separator supports up to 2 M bits/sec data rate.

The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core.

5.1.1 AT interface

The interface consists of the standard asynchronous signals: $\overline{RD}$, $\overline{WR}$, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers. This interface can be switched between PC/AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC/AT.

5.1.2 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command. The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk errors. The following tables give several examples of the delays with a FIFO. The data are based upon the following formula:

THRESHOLD # × (1/DATA/RATE) *8 - 1.5 µS = DELAY

FIFO THRESHOLD	MAXIMUM DELAY TO SERVICING AT 500K BPS
	Data Rate
1 Byte	1 × 16 µS - 1.5 µS = 14.5 µS
2 Byte	2 × 16 µS - 1.5 µS = 30.5 µS
8 Byte	8 × 16 µS - 1.5 µS = 6.5 µS
15 Byte	15 × 16 µS - 1.5 µS = 238.5 µS

FIFO THRESHOLD	MAXIMUM DELAY TO SERVICING AT 1M BPS
	Data Rate
1 Byte	1 × 8 µS - 1.5 µS = 6.5 µS
2 Byte	2 × 8 µS - 1.5 µS = 14.5 µS
8 Byte	8 × 8 µS - 1.5 µS = 62.5 µS
15 Byte	15 × 8 µS - 1.5 µS = 118.5 µS

At the start of a command the FIFO is always disabled and command parameters must be sent based upon the RQM and DIO bit settings in the main status register. When the FDC enters the command execution phase, it clears the FIFO of any data to ensure that invalid data are not transferred.

An overrun and underrun will terminate the current command and the data transfer. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled with the SPECIFY command and are initiated by the FDC by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting $\overline{\text{DACK}}$ and addresses need not be valid.

Note that if the DMA controller is programmed to function in verify mode a pseudo read is performed by the FDC based only on $\overline{\text{DACK}}$. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled the above operation is performed by using the new VERIFY command. No DMA operation is needed.¡@

5.1.3 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When a lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The DDS circuit cycles once every 12 clock cycles ideally. Any data pulse input will be synchronized and then adjusted by immediate error adjustment. The control logic will generate RDD and RWD for every pulse input. During any cycle where no data pulse is present, the DDS cycles are based on speed. A digital integrator is used to keep track of the speed changes in the input data stream.

5.1.4 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and is dependent on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late relative to the surrounding bits.

5.1.5 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires a 1 Mbps data rate for the FDC. At this data rate the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk.

5.1.6 FDC Core

The W83977F/G, W83977AF/AG FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information is provided to the microprocessor.

5.1.7 FDC Commands

Command Symbol Descriptions:

C:	Cylinder number 0 - 256
D:	Data Pattern

DIR:	Step Direction
	DIR = 0, step out
	DIR = 1, step in

DS0:	Disk Drive Select 0
DS1:	Disk Drive Select 1
DTL:	Data Length
EC:	Enable Count
EOT:	End of Track
EFIFO:	Enable FIFO
EIS:	Enable Implied Seek
EOT:	End of track
FIFOTHR:	FIFO Threshold
GAP:	Gap length selection
GPL:	Gap Length
H:	Head number
HDS:	Head number select
HLT:	Head Load Time
HUT:	Head Unload Time
LOCK:	Lock EFIFO, FIFOTHR, PTRTRK bits prevent affected by software reset
MFM:	MFM or FM Mode
MT:	Multitrack
N:	The number of data bytes written in a sector
NCN:	New Cylinder Number

ND:	Non-DMA Mode
OW:	Overwritten
PCN:	Present Cylinder Number
POLL:	Polling Disable
PRETRK:	Precompensation Start Track Number
R:	Record
RCN:	Relative Cylinder Number
R/W:	Read/Write
SC:	Sector/per cylinder
SK:	Skip deleted data address mark
SRT:	Step Rate Time
ST0:	Status Register 0
ST1:	Status Register 1
ST2:	Status Register 2
ST3:	Status Register 3
WG:	Write gate alters timing of WE

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------------------- C ------------------------								Sector ID information prior to command execution
	W	---------------------- H ------------------------								
	W	---------------------- R ------------------------								
	W	---------------------- N ------------------------								
	W	-------------------- EOT -----------------------								
	W	-------------------- GPL -----------------------								
	W	-------------------- DTL -----------------------								
Execution										Data transfer between the FDD and system
Result	R	-------------------- ST0 -----------------------								Status information after command execution
	R	-------------------- ST1 -----------------------								
	R	-------------------- ST2 -----------------------								
	R	---------------------- C ------------------------								Sector ID information after command execution
	R	---------------------- H ------------------------								
	R	---------------------- R ------------------------								
	R	---------------------- N ------------------------								

(2) Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------------------- C ------------------------								Sector ID information prior to command execution
	W	---------------------- H ------------------------								
	W	---------------------- R ------------------------								
	W	---------------------- N ------------------------								
	W	-------------------- EOT -----------------------								
	W	-------------------- GPL -----------------------								
	W	-------------------- DTL -----------------------								
Execution										Data transfer between the FDD and system
Result	R	-------------------- ST0 -----------------------								Status information after command execution
	R	-------------------- ST1 -----------------------								
	R	-------------------- ST2 -----------------------								
	R	---------------------- C ------------------------								Sector ID information after command execution
	R	---------------------- H ------------------------								
	R	---------------------- R ------------------------								
	R	---------------------- N ------------------------								

(3) Read A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------------------- C ------------------------								Sector ID information prior to command execution
	W	---------------------- H ------------------------								
	W	---------------------- R ------------------------								
	W	---------------------- N ------------------------								
	W	-------------------- EOT -----------------------								
	W	-------------------- GPL -----------------------								
	W	-------------------- DTL -----------------------								
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT
Result	R	-------------------- ST0 -----------------------								Status information after command execution
	R	-------------------- ST1 -----------------------								
	R	-------------------- ST2 -----------------------								
	R	---------------------- C ------------------------								Sector ID information after command execution
	R	---------------------- H ------------------------								
	R	---------------------- R ------------------------								
	R	---------------------- N ------------------------								

(4) Read ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in Data Register
Result	R	-------------------- ST0 -----------------------								Status information after command execution
	R	-------------------- ST1 -----------------------								
	R	-------------------- ST2 -----------------------								
	R	---------------------- C ------------------------								Disk status after the command has been completed
	R	---------------------- H ------------------------								
	R	---------------------- R ------------------------								
	R	---------------------- N ------------------------								

(5) Verify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	---------------------- C ------------------------								Sector ID information prior to command execution
	W	---------------------- H ------------------------								
	W	---------------------- R ------------------------								
	W	---------------------- N ------------------------								
	W	-------------------- EOT -----------------------								
	W	-------------------- GPL -----------------------								
		-------------------- DTL/SC --------------------								
Execution										No data transfer takes place
Result	R	-------------------- ST0 -----------------------								Status information after command execution
	R	-------------------- ST1 -----------------------								
	R	-------------------- ST2 -----------------------								
	R	---------------------- C ------------------------								Sector ID information after command execution
	R	---------------------- H ------------------------								
	R	---------------------- R ------------------------								
	R	---------------------- N ------------------------								

(6) Version

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

(7) Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------------------- C ------------------------								Sector ID information prior to Command execution
	W	---------------------- H ------------------------								
	W	---------------------- R ------------------------								
	W	---------------------- N ------------------------								
	W	-------------------- EOT -----------------------								
	W	-------------------- GPL -----------------------								
	W	-------------------- DTL -----------------------								
Execution										Data transfer between the FDD and system
Result	R	-------------------- ST0 -----------------------								Status information after Command execution
	R	-------------------- ST1 -----------------------								
	R	-------------------- ST2 -----------------------								
	R	---------------------- C ------------------------								Sector ID information after Command execution
	R	---------------------- H ------------------------								
	R	---------------------- R ------------------------								
	R	---------------------- N ------------------------								

(8) Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------------------- C ------------------------								Sector ID information prior to command execution
	W	---------------------- H ------------------------								
	W	---------------------- R ------------------------								
	W	---------------------- N ------------------------								
	W	-------------------- EOT -----------------------								
	W	-------------------- GPL -----------------------								
	W	-------------------- DTL -----------------------								
Execution										Data transfer between the FDD and system
Result	R	-------------------- ST0 -----------------------								Status information after command execution
	R	-------------------- ST1 -----------------------								
	R	-------------------- ST2 -----------------------								
	R	---------------------- C ------------------------								Sector ID information after command execution
	R	---------------------- H ------------------------								
	R	---------------------- R ------------------------								
	R	---------------------- N ------------------------								

(9) Format A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------------------- N ------------------------								Bytes/Sector
	W	--------------------- SC -----------------------								Sectors/Cylinder
	W	--------------------- GPL ---------------------								Gap 3
	W	---------------------- D ------------------------								Filler Byte
Execution for Each Sector Repeat:	W	---------------------- C ------------------------								Input Sector Parameters
	W	---------------------- H ------------------------								
	W	---------------------- R ------------------------								
	W	---------------------- N ------------------------								
Result	R	-------------------- ST0 -----------------------								Status information after command execution
	R	-------------------- ST1 -----------------------								
	R	-------------------- ST2 -----------------------								
	R	---------------- Undefined -------------------								
	R	---------------- Undefined -------------------								
	R	---------------- Undefined -------------------								
	R	---------------- Undefined -------------------								

(10) Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt

(11) Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	---------------- ST0 -------------------------								Status information at the end of each seek operation
	R	---------------- PCN -------------------------								

(12) Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	| ---------SRT ----------- |				--------- HUT ---------- |				
	W	|------------ HLT ---------------------------------|							ND	

(13) Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------------------- NCN -----------------------								
Execution	R									Head positioned over proper cylinder on diskette

(14) Configure

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	| ------ FIFOTHR ----|				
	W	| --------------------PRETRK ----------------------- |								
Execution										Internal registers written

(15) Relative Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	| -------------------- RCN ---------------------------- |								

(16) Dumpreg

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	Registers placed in FIFO
Result	R	----------------------- PCN-Drive 0--------------------								
	R	----------------------- PCN-Drive 1 -------------------								
	R	----------------------- PCN-Drive 2--------------------								
	R	----------------------- PCN-Drive 3 -------------------								
	R	--------SRT ------------------ |				--------- HUT --------				
	R	----------- HLT ----------------------------------|							ND	
	R	------------------------ SC/EOT ----------------------								
	R	LOCK	0	D3	D2	D1	D0	GAP	WG	
	R	0	EIS	EFIFO	POLL	| ------ FIFOTHR --------				
	R	-----------------------PRETRK -------------------------								

(17) Perpendicular Mode

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Code
	W	OW	0	D3	D2	D1	D0	GAP	WG	

(18) Lock

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	

(19) Sense Drive Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------------- ST3 ------------------------								Status information about disk drive

(20) Invalid

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	------------- Invalid Codes -----------------								Invalid codes (no operation- FDC goes to standby state)
Result	R	-------------------- ST0 ----------------------								ST0 = 80H

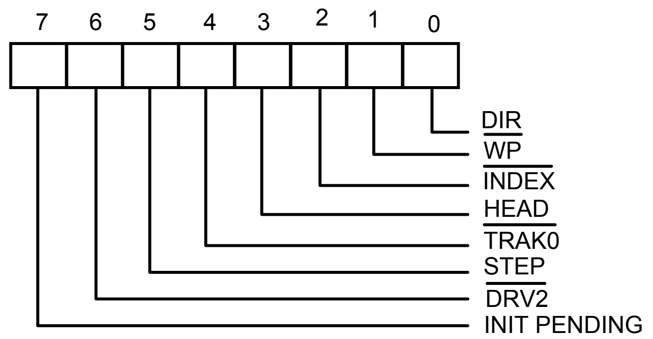
5.2 Register Descriptions

There are several status, data, and control registers in W83977F/G, W83977AF/AG. These registers are defined below:

ADDRESS	REGISTER	
OFFSET	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

5.2.1 Status Register A (SA Register) (Read base address + 0)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

$\overline{\text{DRV2}}$ (Bit 6):

0 A second drive has been installed

1 A second drive has not been installed

STEP (Bit 5):

This bit indicates the complement of $\overline{\text{STEP}}$ output.

$\overline{\text{TRAK0}}$ (Bit 4):

This bit indicates the value of $\overline{\text{TRAK0}}$ input.

HEAD (Bit 3):

This bit indicates the complement of $\overline{\text{HEAD}}$ output.

0 side 0

1 side 1

$\overline{\text{INDEX}}$ (Bit 2):

This bit indicates the value of $\overline{\text{INDEX}}$ output.

$\overline{\text{WP}}$ (Bit 1):

0disk is write-protected

1disk is not write-protected

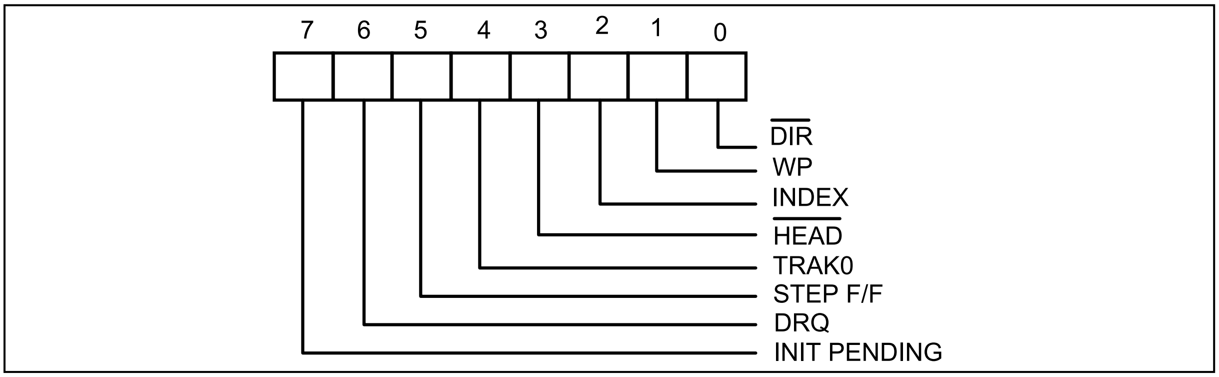
DIR (Bit 0)

This bit indicates the direction of head movement.

0 outward direction

1 inward direction

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRQ (Bit 6):

This bit indicates the value of DRQ output pin.

STEP F/F (Bit 5):

This bit indicates the complement of latched $\overline{\text{STEP}}$ output.

TRAK0 (Bit 4):

This bit indicates the complement of $\overline{\text{TRAK0}}$ input.

$\overline{\text{HEAD}}$ (Bit 3):

This bit indicates the value of $\overline{\text{HEAD}}$ output.

0	side 1
1	side 0

INDEX (Bit 2):

This bit indicates the complement of $\overline{\text{INDEX}}$ output.

WP (Bit 1):

0	disk is not write-protected
1	disk is write-protected

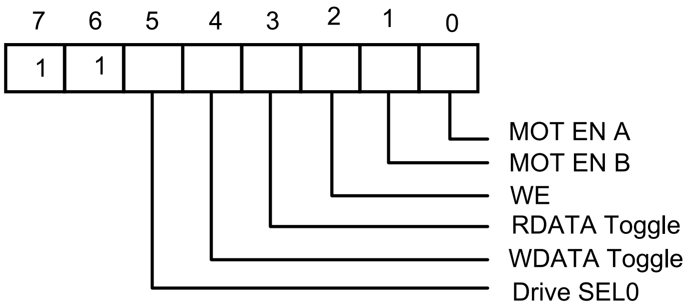
$\overline{\text{DIR}}$ (Bit 0)

This bit indicates the direction of head movement.

0	inward direction
1	outward direction

5.2.2 Status Register B (SB Register) (Read base address + 1)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



Drive SEL0 (Bit 5):

This bit indicates the status of DO REGISTER bit 0 (drive select bit 0).

WDATA Toggle (Bit 4):

This bit changes state at every rising edge of the $\overline{\text{WD}}$ output pin.

RDATA Toggle (Bit 3):

This bit changes state at every rising edge of the $\overline{\text{RDATA}}$ output pin.

WE (Bit 2):

This bit indicates the complement of the $\overline{\text{WE}}$ output pin.

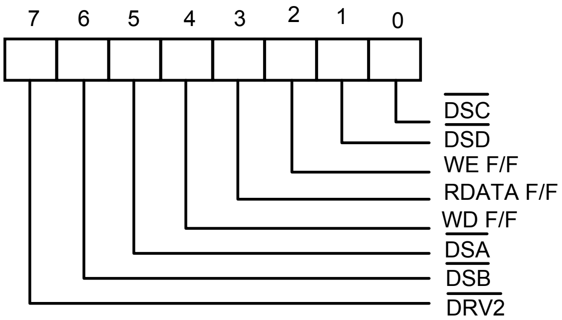
MOT EN B (Bit 1)

This bit indicates the complement of the $\overline{\text{MOB}}$ output pin.

MOT EN A (Bit 0)

This bit indicates the complement of the $\overline{\text{MOA}}$ output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



$\overline{\text{DRV2}}$ (Bit 7):

0 A second drive has been installed

1 A second drive has not been installed

$\overline{\text{DSB}}$ (Bit 6):

This bit indicates the status of $\overline{\text{DSB}}$ output pin.

$\overline{\text{DSA}}$ (Bit 5):

This bit indicates the status of $\overline{\text{DSA}}$ output pin.

WD F/F(Bit 4):

This bit indicates the complement of the latched $\overline{\text{WD}}$ output pin at every rising edge of the $\overline{\text{WD}}$ output pin.

RDATA F/F(Bit 3):

This bit indicates the complement of the latched $\overline{\text{RDATA}}$ output pin .

WE F/F (Bit 2):

This bit indicates the complement of latched $\overline{\text{WE}}$ output pin.

$\overline{\text{DSD}}$ (Bit 1):

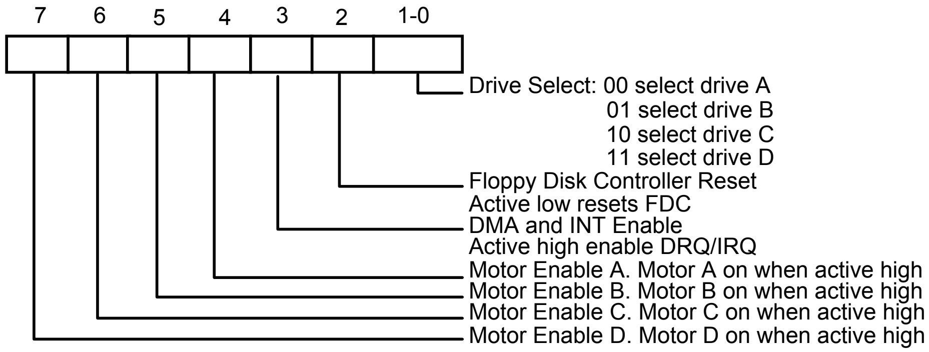
0 Drive D has been selected
1 Drive D has not been selected

$\overline{\text{DSC}}$ (Bit 0):

0 Drive C has been selected
1 Drive C has not been selected

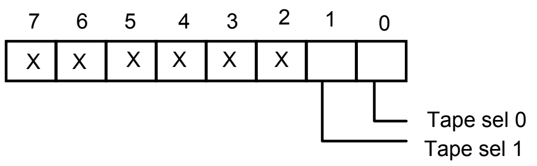
5.2.3 Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register controlling drive motors, drive selection, DRQ/IRQ enable, and FDC resetting. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:

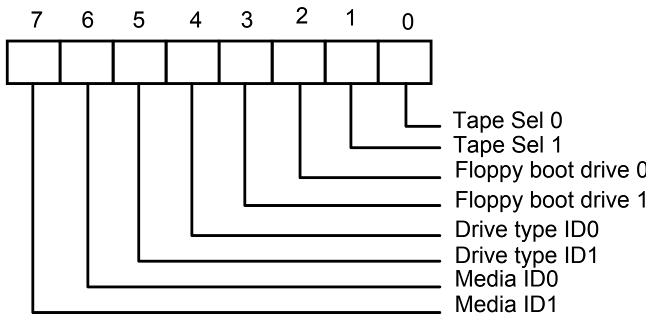

7
6
5
4
3
2
1-0
Drive Select: 00 select drive A
01 select drive B
10 select drive C
11 select drive D
Floppy Disk Controller Reset
Active low resets FDC
DMA and INT Enable
Active high enable DRQ/IRQ
Motor Enable A. Motor A on when active high
Motor Enable B. Motor B on when active high
Motor Enable C. Motor C on when active high
Motor Enable D. Motor D on when active high

5.2.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information of the floppy disk drive. In normal floppy mode, this register includes only bit 0 and 1. The bit definitions are as follows:



If three mode FDD function is enabled (EN3MODE = 1 in Logical Device 0 CRF0 bit:0), the bit definitions are as follows:



Media ID1 Media ID0 (Bit 7, 6):

These two bits are read only. These two bits reflect the value of Logical Device 0 CRF1 bit 4,5.

Drive type ID1 Drive type ID0 (Bit 5, 4):

These two bits reflect two of the bits of Logical Device 0 CRF2. Which two bits are reflected depends on the last drive selected in the DO REGISTER.

Floppy Boot drive 1, 0 (Bit 3, 2):

These two bits reflect the value of Logical Device 0 CRF1 bit 7,6.

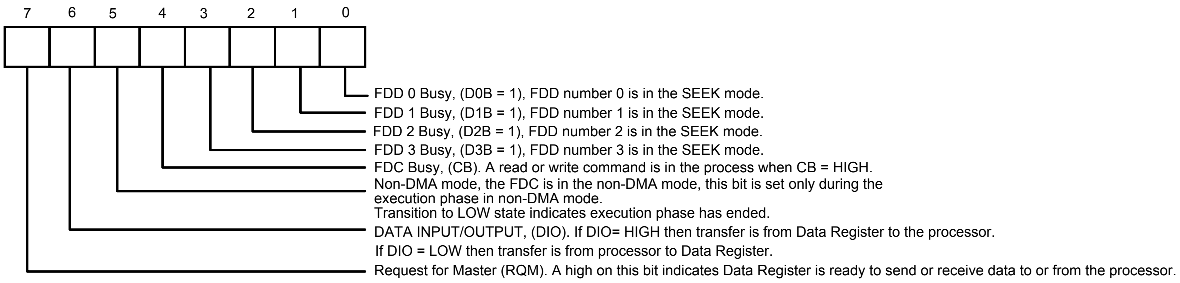
Tape Sel 1, Tape Sel 0 (Bit 1, 0):

These two bits assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive.

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

5.2.5 Main Status Register (MS Register) (Read base address + 4)

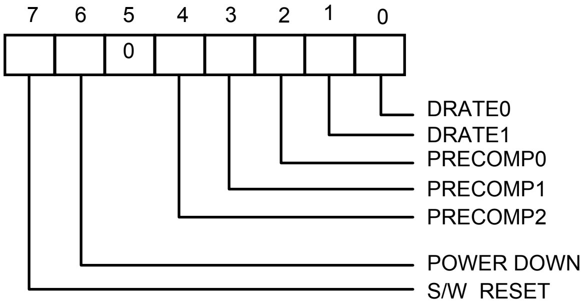
The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:



FDD 0 Busy, (D0B = 1), FDD number 0 is in the SEEK mode.
FDD 1 Busy, (D1B = 1), FDD number 1 is in the SEEK mode.
FDD 2 Busy, (D2B = 1), FDD number 2 is in the SEEK mode.
FDD 3 Busy, (D3B = 1), FDD number 3 is in the SEEK mode.
FDC Busy, (CB). A read or write command is in the process when CB = HIGH.
Non-DMA mode, the FDC is in the non-DMA mode, this bit is set only during the execution phase in non-DMA mode.
Transition to LOW state indicates execution phase has ended.
DATA INPUT/OUTPUT, (DIO). If DIO= HIGH then transfer is from Data Register to the processor.
If DIO = LOW then transfer is from processor to Data Register.
Request for Master (RQM). A high on this bit indicates Data Register is ready to send or receive data to or from the processor.

5.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. The data rate of the FDC is programmed by the CC REGISTER for PC-AT and PS/2 Model 30 and PS/2 mode, and not by the DR REGISTER. The real data rate is determined by the most recent write to either of the DR REGISTER or CC REGISTER.



S/W RESET (Bit 7):

This bit is the software reset bit.

POWER-DOWN (Bit 6):

0 FDC in normal mode
1 FDC in power-down mode

PRECOMP2 PRECOMP1 PRECOMP0 (Bit 4, 3, 2):

These three bits select the value of write precompensation. The following tables show the precompensation values for the combination of these bits.

PRECOMP 2 1 0	PRECOMPENSATION DELAY 250K - 1 Mbps	 2 Mbps Tape drive
0 0 0	Default Delays	Default Delays
0 0 1	41.67 nS	20.8 nS
0 1 0	83.34 nS	41.17 nS
0 1 1	125.00 nS	62.5nS
1 0 0	166.67 nS	83.3 nS
1 0 1	208.33 nS	104.2 nS
1 1 0	250.00 nS	125.00 nS
1 1 1	0.00 nS (disabled)	0.00 nS (disabled)

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 nS
300 KB/S	125 nS
500 KB/S	125 nS
1 MB/S	41.67nS
2 MB/S	20.8 nS

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC and reduced write current control.

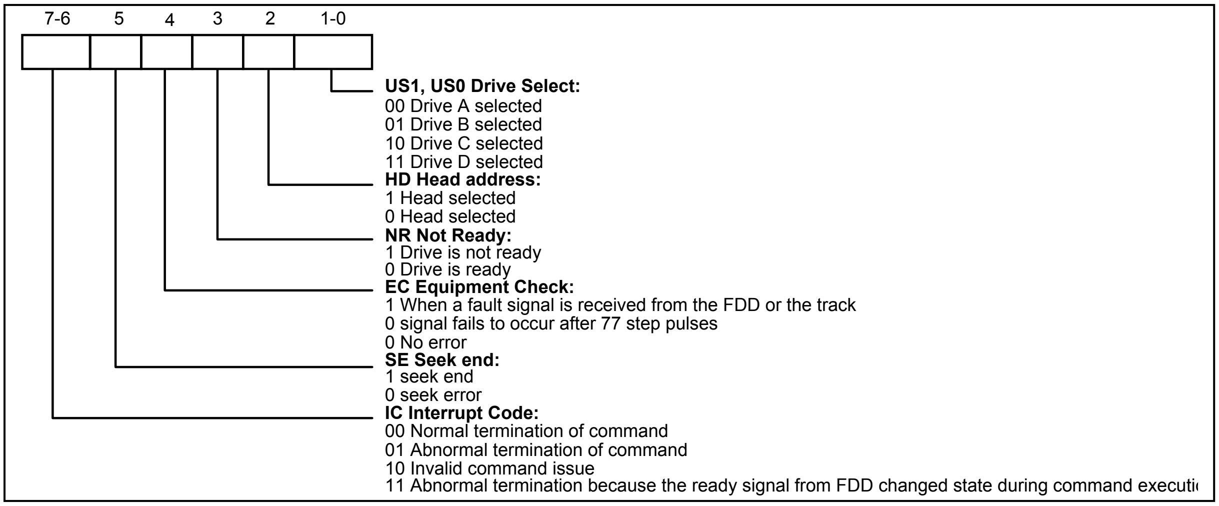
00 500 KB/S (MFM), 250 KB/S (FM), $\overline{\text{RWC}}$ = 1
01 300 KB/S (MFM), 150 KB/S (FM), $\overline{\text{RWC}}$ = 0
10 250 KB/S (MFM), 125 KB/S (FM), $\overline{\text{RWC}}$ = 0
11 1 MB/S (MFM), Illegal (FM), $\overline{\text{RWC}}$ = 1

The 2 MB/S data rate for Tape drive is only supported by setting 01 to DRATE1 and DRATE0 bits, as well as setting 10 to DRT1 and DRT0 bits which are two of the Configure Register CRF4 or CRF5 bits in logic device 0. Please refer to the function description of CRF4 or CRF5 and data rate table for individual data rates setting.

5.2.7 FIFO Register (R/W base address + 5)

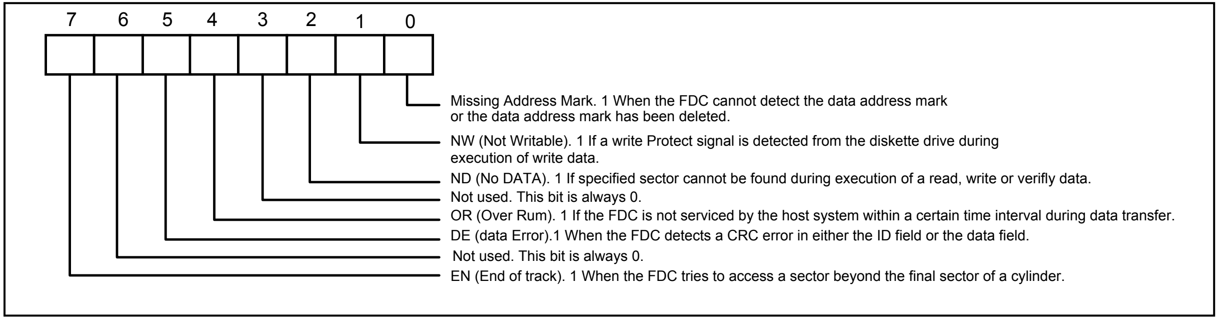
The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. This register stores data, commands, and parameters and provides diskette-drive status information. Data bytes are passed through the data register to program or obtain results after a command. In the W83977F/ AF, this register defaults to FIFO disabled mode after reset. The FIFO can change its value and enable its operation through the CONFIGURE command.

Status Register 0 (ST0)



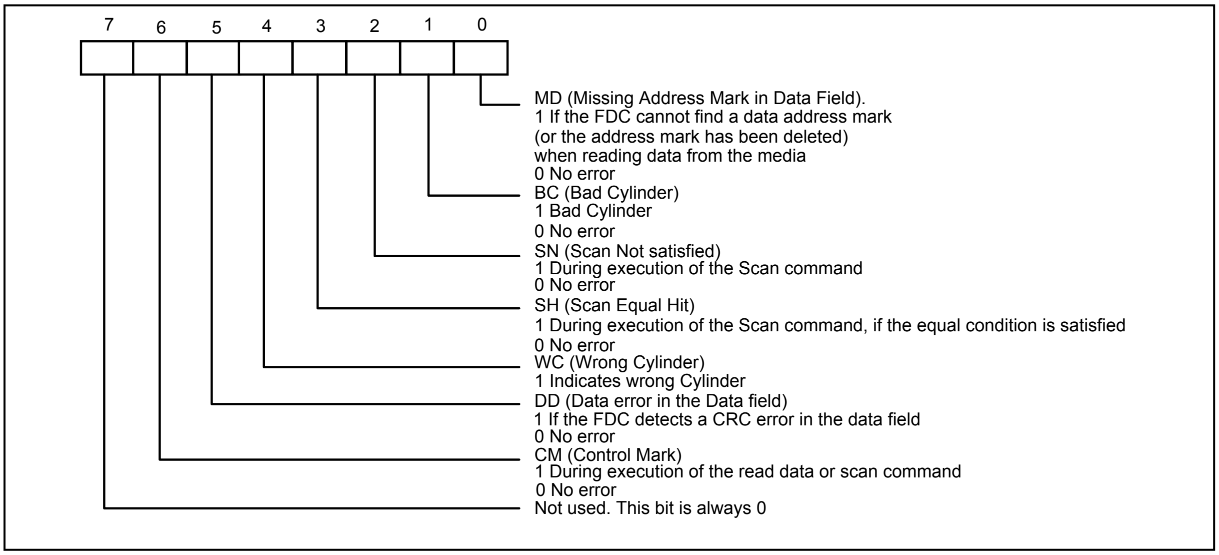
US1, US0 Drive Select:
00 Drive A selected
01 Drive B selected
10 Drive C selected
11 Drive D selected
HD Head address:
1 Head selected
0 Head selected
NR Not Ready:
1 Drive is not ready
0 Drive is ready
EC Equipment Check:
1 When a fault signal is received from the FDD or the track
0 signal fails to occur after 77 step pulses
0 No error
SE Seek end:
1 seek end
0 seek error
IC Interrupt Code:
00 Normal termination of command
01 Abnormal termination of command
10 Invalid command issue
11 Abnormal termination because the ready signal from FDD changed state during command executi

Status Register 1 (ST1)



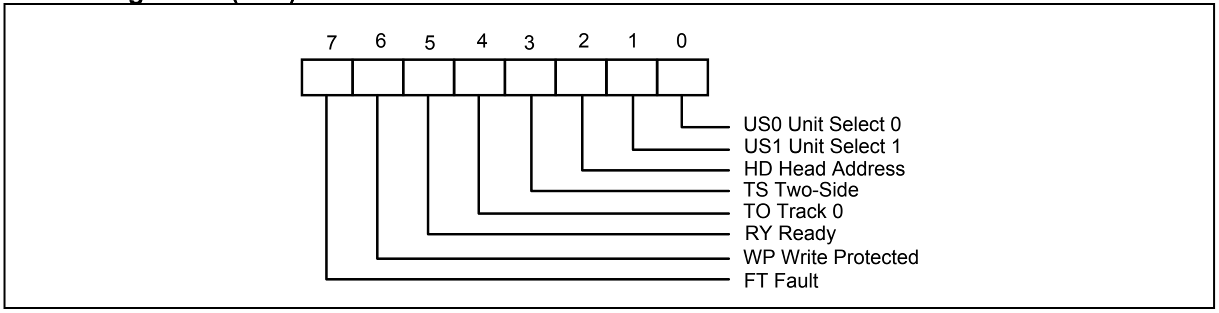
Missing Address Mark. 1 When the FDC cannot detect the data address mark or the data address mark has been deleted.
NW (Not Writable). 1 If a write Protect signal is detected from the diskette drive during execution of write data.
ND (No DATA). 1 If specified sector cannot be found during execution of a read, write or verifly data.
Not used. This bit is always 0.
OR (Over Rum). 1 If the FDC is not serviced by the host system within a certain time interval during data transfer.
DE (data Error).1 When the FDC detects a CRC error in either the ID field or the data field.
Not used. This bit is always 0.
EN (End of track). 1 When the FDC tries to access a sector beyond the final sector of a cylinder.

Status Register 2 (ST2)



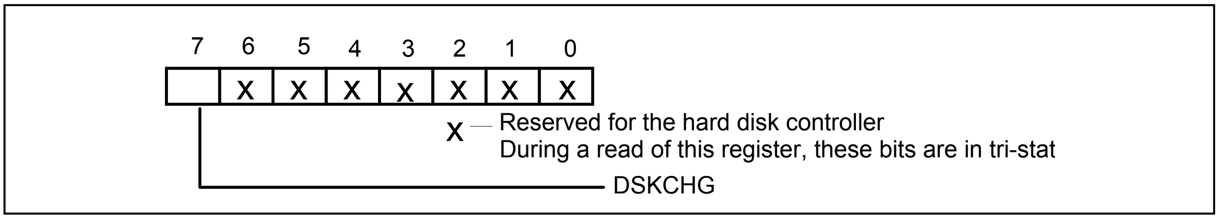
MD (Missing Address Mark in Data Field).
1 If the FDC cannot find a data address mark
(or the address mark has been deleted)
when reading data from the media
0 No error
BC (Bad Cylinder)
1 Bad Cylinder
0 No error
SN (Scan Not satisfied)
1 During execution of the Scan command
0 No error
SH (Scan Equal Hit)
1 During execution of the Scan command, if the equal condition is satisfied
0 No error
WC (Wrong Cylinder)
1 Indicates wrong Cylinder
DD (Data error in the Data field)
1 If the FDC detects a CRC error in the data field
0 No error
CM (Control Mark)
1 During execution of the read data or scan command
0 No error
Not used. This bit is always 0

Status Register 3 (ST3)

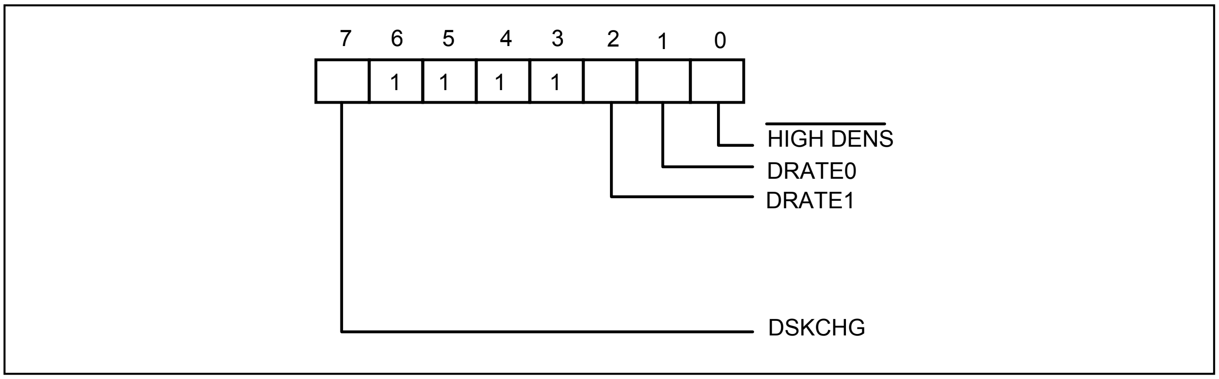


5.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit read-only register used for diagnostic purposes. In a PC/XT or AT only Bit 7 is checked by the BIOS. When the register is read, Bit 7 shows the complement of $\overline{\text{DSKCHG}}$, while other bits of the data bus remain in tri-state. Bit definitions are as follows:


7
6
5
4
3
2
1
0
X
X
X
X
X
X
X
X — Reserved for the hard disk controller
During a read of this register, these bits are in tri-stat
DSKCHG

In the PS/2 mode, the bit definitions are as follows:



DSKCHG (Bit 7):

This bit indicates the complement of the $\overline{\text{DSKCHG}}$ input.

Bit 6-3: These bits are always a logic 1 during a read.

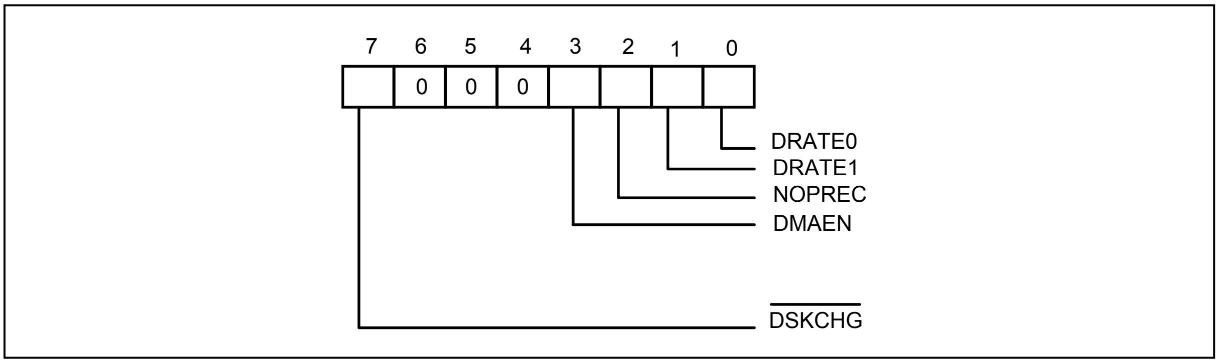
DRATE1 DRATE0 (Bit 2, 1):

These two bits select the data rate of the FDC. Refer to the DR register bits 1 and 0 for the settings corresponding to the individual data rates.

$\overline{\text{HIGH DENS}}$ (Bit 0):

0	500 KB/S or 1 MB/S data rate (high density FDD)
1	250 KB/S or 300 KB/S data rate

In the PS/2 Model 30 mode, the bit definitions are as follows:



DSKCHG (Bit 7):
This bit indicates the status of $\overline{\text{DSKCHG}}$ input.

Bit 6-4: These bits are always a logic 1 during a read.

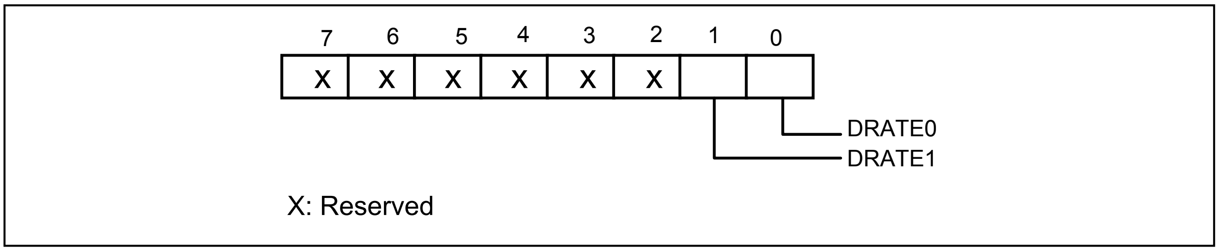
DMAEN (Bit 3):
This bit indicates the value of DO REGISTER bit 3.

NOPREC (Bit 2):
This bit indicates the value of CC REGISTER NOPREC bit.

DRATE1 DRATE0 (Bit 1, 0):
These two bits select the data rate of the FDC.

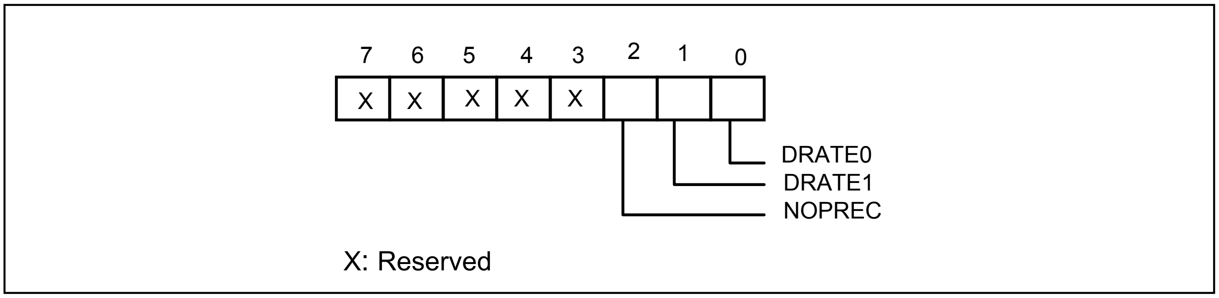
5.2.9 Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In the PC/AT and PS/2 mode, the bit definitions are as follows:



Bit 7-2: Reserved. These bits should be set to 0.

DRATE1 DRATE0 (Bit 1, 0):
These two bits select the data rate of the FDC.
In the PS/2 Model 30 mode, the bit definitions are as follows:



Bit 7-3: Reserved. These bits should be set to 0.

NOPREC (Bit 2):
This bit indicates no precompensation. It has no function and can be set by software.

DRATE1 DRATE0 (Bit 1, 0):
These two bits select the data rate of the FDC.

6. UART PORT

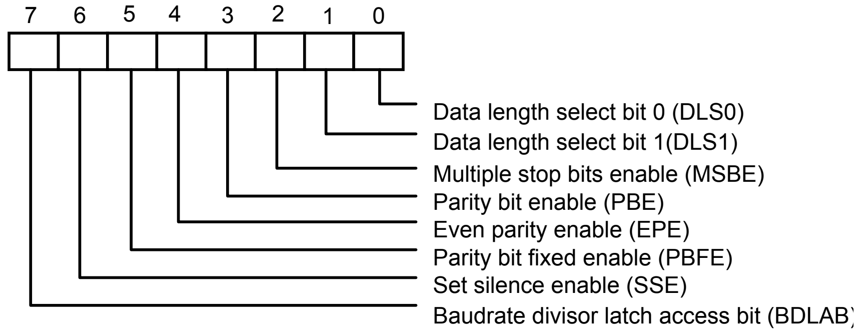
6.1 Universal Asynchronous Receiver/Transmitter (UART A, UART B)

The UARTs are used to convert parallel data into serial format on the transmit side and convert serial data to parallel format on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include complete modem control capability and a processor interrupt system that may be software trailed to the computing time required to handle the communication link. The UARTs have a FIFO mode to reduce the number of interrupts presented to the CPU. In each UART, there are 16-byte FIFOs for both receive and transmit mode.

6.2 Register Address

6.2.1 UART Control Register (UCR) (Read/Write)

The UART Control Register controls and defines the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.


7
6
5
4
3
2
1
0
Data length select bit 0 (DLS0)
Data length select bit 1(DLS1)
Multiple stop bits enable (MSBE)
Parity bit enable (PBE)
Even parity enable (EPE)
Parity bit fixed enable (PBFE)
Set silence enable (SSE)
Baudrate divisor latch access bit (BDLAB)

Bit 7: BDLAB. When this bit is set to a logical 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baudrate generator during a read or write operation. When this bit is reset, the Receiver Buffer Register, the Transmitter Buffer Register, or the Interrupt Control Register can be accessed.

Bit 6: SSE. A logical 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.

Bit 5: PBFE. When PBE and PBFE of UCR are both set to a logical 1,

(1) if EPE is logical 1, the parity bit is fixed as logical 0 to transmit and check.

(2) if EPE is logical 0, the parity bit is fixed as logical 1 to transmit and check.

TABLE 6-1 UART Register Bit Map

BIT NUMBER										
REGISTER ADDRESS BASE			**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 Mode.

Bit 4: EPE. This bit describes the number of logic 1's in the data word bits and parity bit only when bit 3 is programmed. When this bit is set, an even number of logic 1's are sent or checked. When the bit is reset, an odd number of logic 1's are sent or checked.

Bit 3: PBE. When this bit is set, the position between the last data bit and the stop bit of the SOUT will be stuffed with the parity bit at the transmitter. For the receiver, the parity bit in the same position as the transmitter will be detected.

Bit 2: MSBE. This bit defines the number of stop bits in each serial character that is transmitted or received.

(1) If MSBE is set to a logical 0, one stop bit is sent and checked.

(2) If MSBE is set to a logical 1, and data length is 5 bits, one and a half stop bits are sent and checked.

(3) If MSBE is set to a logical 1, and data length is 6, 7, or 8 bits, two stop bits are sent and checked.

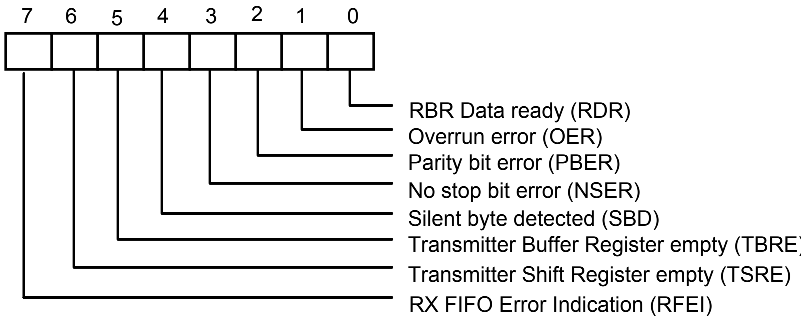
Bits 0 and 1: DLS0, DLS1. These two bits define the number of data bits that are sent or checked in each serial character.

TABLE 6-2 WORD LENGTH DEFINITION

DLS1	**DLS0**	**DATA LENGTH**
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

6.2.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of the data transfer during communication.


7 6 5 4 3 2 1 0
RBR Data ready (RDR)
Overrun error (OER)
Parity bit error (PBER)
No stop bit error (NSER)
Silent byte detected (SBD)
Transmitter Buffer Register empty (TBRE
Transmitter Shift Register empty (TSRE)
RX FIFO Error Indication (RFEI)

Bit 7: RFEI. In 16450 mode, this bit is always set to a logic 0. In 16550 mode, this bit is set to a logic 1 when there is at least one parity bit error, no stop bit error or silent byte detected in the FIFO. In 16550 mode, this bit is cleared by reading from the USR if there are no remaining errors left in the FIFO.

Bit 6: TSRE. In 16450 mode, when TBR and TSR are both empty, this bit will be set to a logical 1. In 16550 mode, if the transmit FIFO and TSR are both empty, it will be set to a logical 1. Other thanthese two cases, this bit will be reset to a logical 0.

Bit 5: TBRE. In 16450 mode, when a data character is transferred from TBR to TSR, this bit will be set to a logical 1. If ETREI of ICR is a logical 1, an interrupt will be generated to notify the CPU to write the next data. In 16550 mode, this bit will be set to a logical 1 when the transmit FIFO is empty. It will be reset to a logical 0 when the CPU writes data into TBR or FIFO.

Bit 4: SBD. This bit is set to a logical 1 to indicate that received data are kept in silent state for a full word time, including start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 3: NSER. This bit is set to a logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

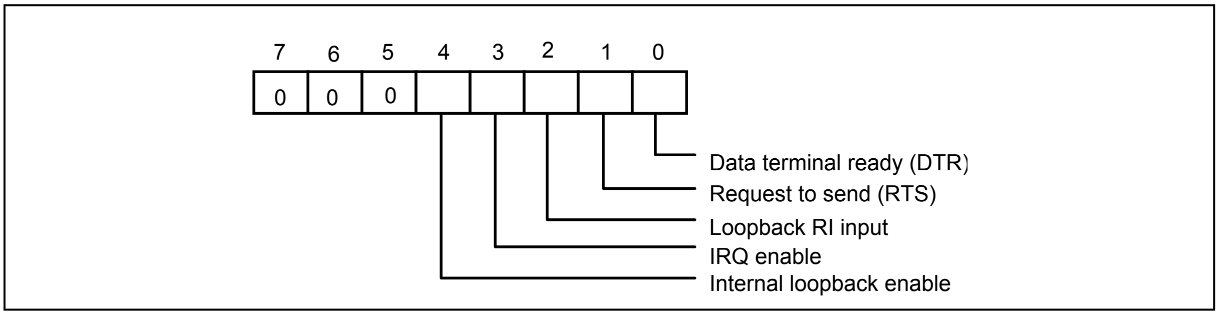
Bit 2: PBER. This bit is set to a logical 1 to indicate that the parity bit of received data is wrong. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 1: OER. This bit is set to a logical 1 to indicate received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition instead of FIFO full. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 0: RDR. This bit is set to a logical 1 to indicate received data are ready to be read by the CPU in the RBR or FIFO. After no data are left in the RBR or FIFO, the bit will be reset to a logical 0.

6.2.3 Handshake Control Register (HCR) (Read/Write)

This register controls the pins of the UART used for handshaking peripherals such as modem, and controls the diagnostic mode of the UART.



Bit 4: When this bit is set to a logical 1, the UART enters diagnostic mode by an internal loopback, as follows:

(1) SOUT is forced to logical 1, and SIN is isolated from the communication link instead of the TSR.

(2) Modem output pins are set to their inactive state.

(3) Modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) → $\overline{\text{DSR}}$, RTS (bit 1 of HCR) → $\overline{\text{CTS}}$, Loopback RI input (bit 2 of HCR) → $\overline{\text{RI}}$ and IRQ enable (bit 3 of HCR) → $\overline{\text{DCD}}$.

Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.

Bit 3: The UART interrupt output is enabled by setting this bit to a logic 1. In the diagnostic mode this bit is internally connected to the modem control input $\overline{\text{DCD}}$.

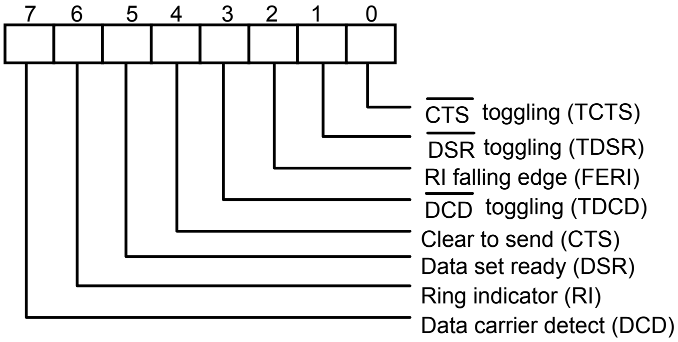
Bit 2: This bit is used only in the diagnostic mode. In the diagnostic mode this bit is internally connected to the modem control input $\overline{\text{RI}}$.

Bit 1: This bit controls the $\overline{\text{RTS}}$ output. The value of this bit is inverted and output to $\overline{\text{RTS}}$.

Bit 0: This bit controls the $\overline{\text{DTR}}$ output. The value of this bit is inverted and output to $\overline{\text{DTR}}$.

6.2.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins for handshake peripherals such as a modem and records changes on these pins.


7
6
5
4
3
2
1
0
$\overline{\text{CTS}}$ toggling (TCTS)
$\overline{\text{DSR}}$ toggling (TDSR)
RI falling edge (FERI)
$\overline{\text{DCD}}$ toggling (TDCD)
Clear to send (CTS)
Data set ready (DSR)
Ring indicator (RI)
Data carrier detect (DCD)

Bit 7: This bit is the opposite of the $\overline{\text{DCD}}$ input. This bit is equivalent to bit 3 of HCR in loopback mode.

Bit 6: This bit is the opposite of the $\overline{\text{RI}}$ input. This bit is equivalent to bit 2 of HCR in loopback mode.

Bit 5: This bit is the opposite of the $\overline{\text{DSR}}$ input. This bit is equivalent to bit 0 of HCR in loopback mode.

Bit 4: This bit is the opposite of the $\overline{\text{CTS}}$ input. This bit is equivalent to bit 1 of HCR in loopback mode.

Bit 3: TDCD. This bit indicates that the $\overline{\text{DCD}}$ pin has changed state after HSR was read by the CPU.

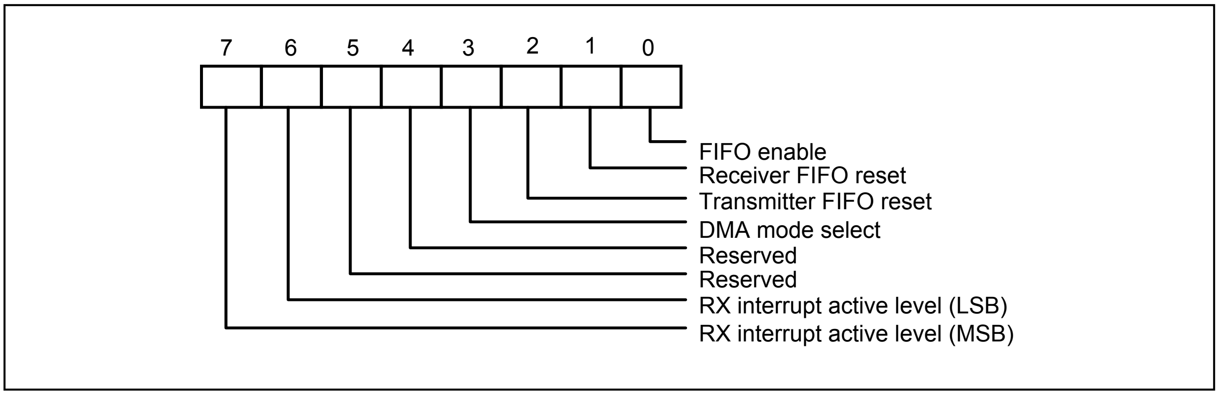
Bit 2: FERI. This bit indicates that the $\overline{\text{RI}}$ pin has changed from low to high state after HSR was read by the CPU.

Bit 1: TDSR. This bit indicates that the $\overline{\text{DSR}}$ pin has changed state after HSR was read by the CPU.

Bit 0: TCTS. This bit indicates that the $\overline{\text{CTS}}$ pin has changed state after HSR was read.

6.2.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.



Bit 6, 7: These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes, once there are more than 4 data characters in the receiver FIFO, the interrupt will be activated to notify the CPU to read the data from the FIFO.

TABLE 6-3 FIFO TRIGGER LEVEL

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

Bit 4, 5: Reserved

Bit 3: When this bit is programmed to logic 1, the DMA mode will change from mode 0 to mode 1 if UFR bit 0 = 1.

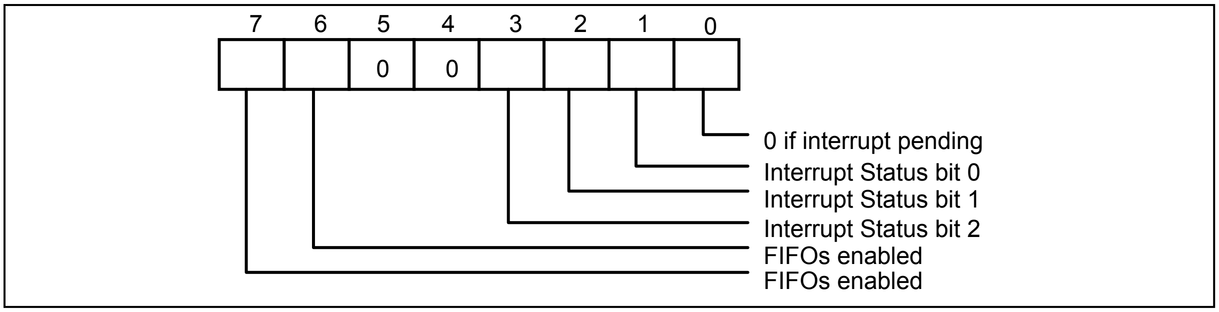
Bit 2: Setting this bit to a logical 1 resets the TX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 1: Setting this bit to a logical 1 resets the RX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 0: This bit enables the 16550 (FIFO) mode of the UART. This bit should be set to a logical 1 before other bits of UFR are programmed.

6.2.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status, which is encoded by different interrupt sources into 3 bits.



Bit 7, 6: These two bits are set to a logical 1 when UFR bit 0 = 1.

Bit 5, 4: These two bits are always logic 0.

Bit 3: In 16450 mode, this bit is 0. In 16550 mode, both bit 3 and 2 are set to a logical 1 when a time-out interrupt is pending.

Bit 2, 1: These two bits identify the priority level of the pending interrupt, as shown in the table below.

Bit 0: This bit is a logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit will be set to a logical 0.

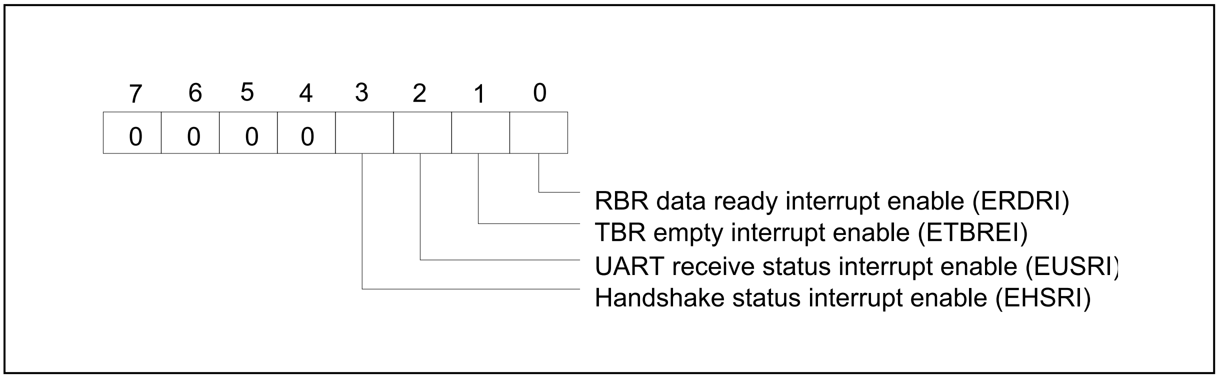
TABLE 6-4 INTERRUPT CONTROL FUNCTION

ISR				**INTERRUPT SET AND FUNCTION**			
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Interrupt priority**	**Interrupt Type**	**Interrupt Source**	**Clear Interrupt**
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

6.2.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register allows the five types of controller interrupts to activate the interrupt output signal separately. The interrupt system can be totally disabled by resetting bits 0 through 3 of the Interrupt Control Register (ICR). A selected interrupt can be enabled by setting the appropriate bits of this register to a logical 1.


7 6 5 4 3 2 1 0
0 0 0 0
RBR data ready interrupt enable (ERDRI)
TBR empty interrupt enable (ETBREI)
UART receive status interrupt enable (EUSRI)
Handshake status interrupt enable (EHSRI)

Bit 7-4: These four bits are always logic 0.

Bit 3: EHSRI. Setting this bit to a logical 1 enables the handshake status register interrupt.

Bit 2: EUSRI. Setting this bit to a logical 1 enables the UART status register interrupt.

Bit 1: ETBREI. Setting this bit to a logical 1 enables the TBR empty interrupt.

Bit 0: ERDRI. Setting this bit to a logical 1 enables the RBR data ready interrupt.

6.2.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divides it by a divisor from 1 to 2^{16}-1. The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table in the next page illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (refer to CR0C bit7 and CR0C bit6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. In high-speed mode, the data transmission rate can be as high as 1.5M bps.

6.2.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

TABLE 6-5 BAUD RATE TABLE

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461M HZ	**PRE-DIV:1.625 14.769M HZ**	**PRE-DIV: 1.0 24M HZ**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERCENTAGE BETWEEN DESIRED AND ACTUAL**
50	400	650	**2304**	**
75	600	975	**1536**	**
110	880	1430	**1047**	0.18%
134.5	1076	1478.5	**857**	0.099%
150	1200	1950	**768**	**
300	2400	3900	**384**	**
600	4800	7800	**192**	**
1200	9600	15600	**96**	**
1800	14400	23400	**64**	**
2000	16000	26000	**58**	0.53%
2400	19200	31200	**48**	**
3600	28800	46800	**32**	**
4800	38400	62400	**24**	**
7200	57600	93600	**16**	**
9600	76800	124800	**12**	**
19200	153600	249600	**6**	**
38400	307200	499200	**3**	**
57600	460800	748800	**2**	**
115200	921600	1497600	**1**	**

** The percentage error for all baud rates, except where indicated otherwise, is 0.16%.

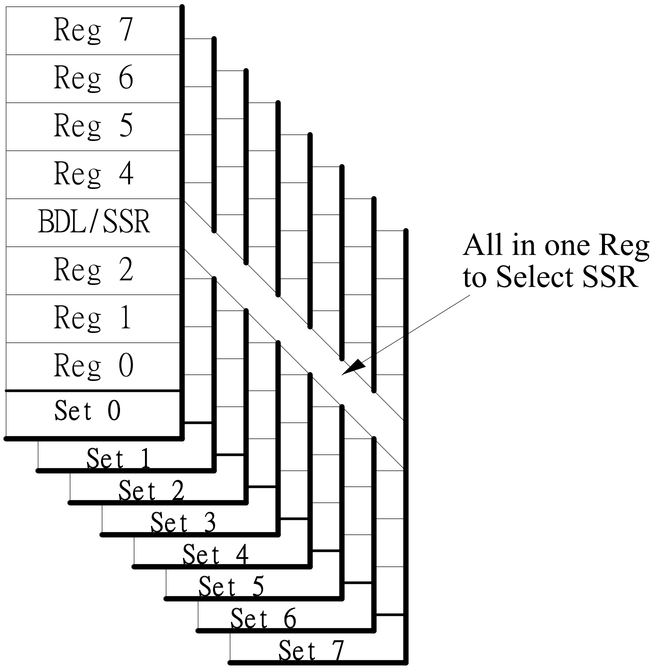
Note. Pre-Divisor is determined by CRF0 of UART A and B.

7. INFRARED (IR) PORT

The Infrared (IR) function provides point-to-point (or multi-point to multi-point) wireless communication which can operate under various transmission protocols including IrDA 1.0 SIR, IrDA 1.1 MIR (1.152 Mbps), IrDA 1.1 FIR (4 Mbps), SHARP ASK-IR, and remote control (NEC, RC-5, advanced RC-5, and RECS-80 protocol).

7.1 IR Register Description

When bank select enable bit (ENBNKSEL, the bit 0 in CRF0 of logic device 6) is set, legacy IR will be switched to Advanced IR, and eight Register Sets can then be accessible. These Register Sets control enhanced IR, SIR, MIR, or FIR. Also a superior traditional SIR function can be used with enhanced features such as 32-byte transmitter/receiver FIFOs, non-encoding IRQ identify status register, and automatic flow control. The MIR/FIR and remote control registers are also defined in these Register Sets. Structure of these Register Sets is shown as follows.



*Set 0, 1 are legacy/Advanced UART Registers
*Set 2~7 are Advanced UART Registers

Each of these register sets has a common register, namely *Sets Select Register* (SSR), in order to switch to another register set. The summary description of these *Sets* is shown in the following.

SET	SETS DESCRIPTION
0	Legacy/Advanced IR Control and Status Registers.
1	Legacy Baud Rate Divisor Register.
2	Advanced IR Control and Status Registers.
3	Version ID and Mapped Control Registers.
4	Transmitter/Receiver/Timer Counter Registers and IR Control Registers.
5	Flow Control and IR Control and Frame Status FIFO Registers.
6	IR Physical Layer Control Registers
7	Remote Control and IR front-end Module Selection Registers.

7.2 Set0-Legacy/Advanced IR Control and Status Registers

ADDRESS OFFSET	REGISTER NAME	REGISTER DESCRIPTION
0	**RBR/TBR**	Receiver/Transmitter Buffer Registers
1	**ICR**	Interrupt Control Register
2	**ISR/UFR**	Interrupt Status or IR FIFO Control Register
3	**UCR/SSR**	IR Control or Sets Select Register
4	**HCR**	Handshake Control Register
5	**USR**	IR Status Register
6	**HSR**	Handshake Status Register
7	**UDR/ESCR**	User Defined Register

7.2.1 Set0.Reg0 - Receiver/Transmitter Buffer Registers (RBR/TBR) (Read/Write)

Receiver Buffer Register is read only and Transmitter Buffer Register is write only. When operate in the PIO mode, the port is used to Receive/Transmit 8-bit data.

When function as a legacy IR, this port only supports PIO mode. If set in the advanced IR mode and configured as MIR/FIR/Remote IR, this port can support DMA transmission. Two DMA channels can be used simultaneously, one for TX DMA and the other for RX DMA. Therefore, single DMA channel is also supported when set the bit of D_CHSW (DMA Channel Swap, in Set2.Reg2.Bit3) and the TX/RX DMA channel is swapped. Note that two DMA channel can be defined in configure register CR2A which selects DMA channel or disables DMA channel. If only RX DMA channel is enabled while TX DMA channel is disabled, then the single DMA channel will be selected.

7.2.2 Set0.Reg1 - Interrupt Control Register (ICR)

MODE	B7	B6	B5	B4	B3	B2	B1	B0
Legacy IR	0	0	0	0	0	EUSRI	ETBREI	ERDRI
Advanced IR	ETMRI	EFSFI	ETXTHI	EDMAI	0	EUSRI/ TXURI	ETBREI	ERBRI

The advanced IR functions including Advanced SIR/ASK-IR, MIR, FIR, or Remote IR are described as follows.

Bit 7: *Legacy IR Mode:*

Not used. A read will return 0.

Advanced IR Mode:

ETMRI - Enable Timer Interrupt

A write to 1 will enable timer interrupt.

Bit 6: *Legacy IR Mode:*

Not used. A read will return 0.

MIR, FIR mode:

EFSFI - Enable Frame Status FIFO Interrupt

A write to 1 will enable frame status FIFO interrupt.

Advanced SIR/ASK-IR, Remote IR:

Not used.

Bit 5: *Legacy IR Mode:*

Not used. A read will return 0.

Advanced SIR/ASK-IR, MIR, FIR, Remote IR:

ETXTHI - Enable Transmitter Threshold Interrupt

A write to 1 will enable transmitter threshold interrupt.

Bit 4: *Legacy IR Mode:*

Not used. A read will return 0.

MIR, FIR, Remote IR:

EDMAI - Enable DMA Interrupt.

A write to 1 will enable DMA interrupt.

Bit 3: Reserved. A read will return 0.

Bit 2: *Legacy IR Mode:*

EUSRI - Enable USR (IR Status Register) Interrupt

A write to 1 will enable IR status register interrupt.

Advanced SIR/ASK-IR:

EUSRI - Enable USR (IR Status Register) Interrupt

A write to 1 will enable IR status register interrupt.

MIR, FIR, Remote Controller:

EHSRI/ETXURI - Enable USR Interrupt *or* Enable Transmitter Underrun Interrupt

A write to 1 will enable USR interrupt or enable transmitter underrun interrupt.

Bit 1: **ETBREI - Enable TBR (Transmitter Buffer Register) Empty Interrupt**

A write to 1 will enable the transmitter buffer register empty interrupt.

Bit 0: **ERBRI - Enable RBR (Receiver Buffer Register) Interrupt**

A write to 1 will enable receiver buffer register interrupt.

7.2.3 Set0.Reg2 - Interrupt Status Register/IR FIFO Control Register (ISR/UFR)

7.2.3.1 Interrupt Status Register (Read Only)

MODE	B7	B6	B5	B4	B3	B2	B1	B0
Legacy IR	FIFO Enable	FIFO Enable	0	0	IID2	IID1	IID0	IP
Advanced IR	TMR_I	FSF_I	TXTH_I	DMA_I	HS_I	USR_I/ FEND_I	TXEMP_I	RXTH_I
Reset Value	0	0	1	0	0	0	1	0

Legacy IR:

This register reflects the Legacy IR interrupt status, which is encoded by different interrupt sources into 3 bits.

Bit 7, 6: These two bits are set to a logical 1 when UFR bit 0 = 1.

Bit 5, 4: These two bits are always logical 0.

Bit 3: When not in FIFO mode, this bit is always 0. In FIFO mode, both bit 3 and 2 are set to logical 1 when a time-out interrupt is pending.

Bit 2, 1: These bits identify the priority level of the pending interrupt, as shown in the table below.

Bit 0: This bit is a logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit will be set to logical 0.

TABLE: INTERRUPT CONTROL FUNCTION

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	IR Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Time-out	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)

** Bit 3 of ISR is enabled when bit 0 of UFR is a logical 1.

Advanced IR:

Bit 7: **TMR_I - Timer Interrupt.**

Set to 1 when timer count to logical 0. This bit is valid when: (1) the timer registers are defined in Set4.Reg0 and Set4.Reg1; (2) EN_TMR(Enable Timer, in Set4.Reg2.Bit0) is set to 1; (3) ENTMR_I (Enable Timer Interrupt, in Set0.Reg1.Bit7) is set to 1.

Bit 6: *MIR, FIR modes:*

FSF_I - Frame Status FIFO Interrupt.

Set to 1 when Frame Status FIFO is equal or larger than the threshold level *or* Frame Status FIFO time-out occurs. Cleared to 0 when Frame Status FIFO is below the threshold level.

Advanced SIR/ASK-IR, Remote IR modes: Not used.

Bit 5: **TXTH_I - Transmitter Threshold Interrupt.**

Set to 1 if the TBR (Transmitter Buffer Register) FIFO is below the threshold level. Cleared to 0 if the TBR (Transmitter Buffer Register) FIFO is above the threshold level.

Bit 4: *MIR, FIR, Remote IR Modes:*

DMA_I - DMA Interrupt.

Set to 1 if the DMA controller 8237A sends a TC (Terminal Count) to I/O device which might be a Transmitter TC or a Receiver TC. Cleared to 0 when this register is read.

Bit 3: **HS_I - Handshake Status Interrupt.**

Set to 1 when the Handshake Status Register has a toggle. Cleared to 0 when Handshake Status Register (HSR) is read. Note that in all IR modes including SIR, ASK-IR, MIR, FIR, and Remote Control IR, this bit defaults to be inactive unless IR Handshake Status Enable (IRHS_EN) is set to 1.

Bit 2: *Advanced SIR/ASK-IR modes:*

USR_I - IR Status Interrupt.

Set to 1 when overrun error, parity error, stop bit error, or silent byte error detected and registered in the IR Status Register (USR). Cleared to 0 when USR is read.

MIR, FIR modes:

FEND_I - Frame End Interrupt.

Set to 1 when (1) a frame has a grace end to be detected where the frame signal is defined in the physical layer of IrDA version 1.1; (2) abort signal or illegal signal has been detected during receiving valid data. Cleared to 0 when this register is read.

Remote Controller Mode: Not used.

Bit 1: **TXEMP_I - Transmitter Empty.**

Set to 1 when transmitter (or, say, FIFO + Transmitter) is empty. Cleared to 0 when this register is read.

Bit 0: **RXTH_I - Receiver Threshold Interrupt.**

Set to 1 when (1) the Receiver Buffer Register (RBR) is equal *or* larger than the threshold level; or (2) RBR time-out occurs if the receiver buffer register has valid data and below the threshold level. Cleared to 0 when RBR is less than threshold level after reading RBR.

7.2.3.2 IR FIFO Control Register (UFR):

MODE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Legacy IR	RXFTL1 (MSB)	RXFTL0 (LSB)	0	0	0	TXF_RST	RXF_RST	EN_FIFO
Advanced IR	RXFTL1 (MSB)	RXFTL0 (LSB)	TXFTL1 (MSB)	TXFTL0 (LSB)	0	TXF_RST	RXF_RST	EN_FIFO
Reset Value	0	0	0	0	0	0	0	0

Legacy IR:

This register is used to control FIFO functions of the IR.

Bit 6, 7: These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes and there are more than 4 data characters in the receiver FIFO, the interrupt will be activated to notify CPU to read the data from FIFO.

TABLE: FIFO TRIGGER LEVEL

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

Bit 4, 5: Reserved

Bit 3: When this bit is programmed to logic 1, the DMA mode will change from mode 0 to mode 1 if UFR bit 0 = 1.

Bit 2: Setting this bit to a logical 1 resets the TX FIFO counter logic to its initial state. This bit will be cleared to logical 0 by itself after being set to logical 1.

Bit 1: Setting this bit to logical 1 resets the RX FIFO counter logic to its initial state. This bit will be cleared to a logical 0 by itself after being set to logical 1.

Bit 0: This bit enables the 16550 (FIFO) mode of the IR. This bit should be set to logical 1 before other bits of UFR can be programmed.

Advanced IR:

Bit 7, 6: **RXFTL1, 0 - Receiver FIFO Threshold Level**

Its definition is the same as Legacy IR. RXTH_I becomes 1 when the Receiver FIFO Threshold Level is equal or larger than the defined value shown as follow.

RXFTL1, 0 (BIT 7, 6)	RX FIFO THRESHOLD LEVEL (FIFO SIZE: 16-BYTE)	RX FIFO THRESHOLD LEVEL (FIFO SIZE: 32-BYTE)
00	1	1
01	4	4
10	8	16
11	14	26

Note that the FIFO Size is selectable in SET2.Reg4.

Bit 5, 4: **TXFTL1, 0 - Transmitter FIFO Threshold Level**

TXTH_I (Transmitter Threshold Level Interrupt) is set to 1 when the Transmitter Threshold Level is less than the programmed value shown as follows.

TXFTL1, 0 (BIT 5, 4)	TX FIFO THRESHOLD LEVEL (FIFO SIZE: 16-BYTE)	TX FIFO THRESHOLD LEVEL (FIFO SIZE: 32-BYTE)
00	1	1
01	3	7
10	9	17
11	13	25

Bit 3 ~0 **Same as in Legacy IR Mode**

7.2.4 Set0.Reg3 - IR Control Register/Set Select Register (UCR/SSR):

These two registers share the same address. In all Register Sets, *Set Select Register (SSR)* can be programmed to select a desired Set but IR Control Register can only be programmed in Set 0 and Set 1. In other words, writing to Reg3 in Sets other than Set 0 and Set 1 will not affect IR Control Register. The mapping of entry Set and programming value is shown as follows.

SSR BITS									**SELECTED**
7	6	5	4	3	2	1	0	Hex Value	**Set**
0	¡Ñ	¡Ñ	¡Ñ	¡Ñ	¡Ñ	¡Ñ	¡Ñ	¡Ð	**Set 0**
1	Any combination except those used in SET 2~7							¡Ð	**Set1**
1	1	1	0	0	0	0	0	**0xE0**	**Set 2**
1	1	1	0	0	1	0	0	**0xE4**	**Set 3**
1	1	1	0	1	0	0	0	**0xE8**	**Set 4**
1	1	1	1	1	1	0	0	**0xEC**	**Set 5**
1	1	1	1	0	0	0	0	**0xF0**	**Set 6**
1	1	1	1	0	1	0	0	**0xF4**	**Set 7**

7.2.5 Set0.Reg4 - Handshake Control Register (HCR)

MODE	B7	B6	B5	B4	B3	B2	B1	B0
Legacy IR	0	0	0	XLOOP	EN_IRQ	0	0	0
Advanced IR	AD_MD2	AD_MD1	AD_MD0	SIR_PLS	TX_WT	EN_DMA	0	0
Reset Value	0	1	1	0	0	0	0	0

Legacy IR Register:

This register controls the pins of IR used for handshaking with peripherals such as modem, and controls the diagnostic mode of IR.

Bit 4: When this bit is set to logical 1, the legacy IR enters diagnostic mode by an internal loopback: IRTX is forced to logical 0, and IRRX is isolated from the communication link instead of the TSR.

Bit 3: The legacy IR interrupt output is enabled by setting this bit to logic 1.

Advanced IR Register:

Bit 7~5 *Advanced SIR/ASK-IR, MIR, FIR, Remote Controller Modes:*

AD_MD2~0 - Advanced IR/Infrared Mode Select.

These registers are active when Advanced IR Select (ADV_SL, in Set2.Reg2.Bit0) is set to 1. Operational mode selection is defined as follows. When backward operation occurs, these registers will be reset to 0 and fall back to legacy IR mode.

AD_MD2~0 (BIT 7, 6, 5)	SELECTED MODE
000	Reserved
001	Low speed **MIR** (0.576M bps)
010	Advanced **ASK-IR**
011	Advanced **SIR**
100	High Speed **MIR** (1.152M bps)
101	**FIR** (4M bps)
110	**Consumer IR**
111	Reserved

Bit 4: *MIR, FIR Modes:*

SIR_PLS - Send Infrared Pulse

Writing 1 to this bit will send a 2 μs long infrared pulse after physical frame end. This is to signal to SIR that the high speed infrared is still in. This bit will be auto cleared by hardware.

Other Modes: Not used.

Bit 3: *MIR, FIR modes:*

TX_WT - Transmission Waiting

If this bit is set to 1, the transmitter will wait for TX FIFO reaching threshold level or transmitter time-out before it begins to transmit data which prevents short queues of data bytes from transmitting prematurely. This is to avoid Underrun.

Other Modes: Not used.

Bit 2: *MIR, FIR modes:*

EN_DMA - Enable DMA

Enable DMA function for transmitting or receiving. Before using this, the DMA channel should be selected first. If only RX DMA channel is set and TX DMA channel is disabled, then the single DMA channel is used. In the single channel system, the bit of D_CHSW (DMA channel swap, in Set 2.Reg2.Bit3) will determine if it is RX_DMA or TX_DMA channel.

Other modes: Not used.

Bit 1, 0: **RTS, DTR**

Functional definitions is the same as in legacy IR mode.

7.2.6 Set0.Reg5 - IR Status Register (USR)

MODE	B7	B6	B5	B4	B3	B2	B1	B0
Legacy IR	RFEI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
Advanced IR	LB_INFR	TSRE	TBRE	MX_LEX	PHY_ERR	CRC_ERR	OER	RDR
Reset Value	0	0	0	0	0	0	0	0

Legacy IR Register: These registers are defined the same as previous description.

Advanced IR Register:

Bit 7: *MIR, FIR Modes:*

LB_INFR - Last Byte In Frame End

Set to 1 when last byte of a frame is in the bottom of FIFO. This bit separates one frame from another when RX FIFO has more than one frame.

Bit 6, 5: Same as legacy IR description.

Bit 4: *MIR, FIR modes:*

MX_LEX - Maximum Frame Length Exceed

Set to 1 when the length of a frame from the receiver has exceeded the programmed frame length defined in SET4.Reg6 and Reg5. If this bit is set to 1, the receiver will not receive any data to RX FIFO.

Bit 3: *MIR, FIR modes:*

PHY_ERR - Physical Layer Error

Set to 1 when an illegal data symbol is received. The illegal data symbol is defined in physical layer of IrDA version 1.1. When this bit is set to 1, the decoder of receiver will be aborted and a frame end signal is set to 1.

Bit 2: *MIR, FIR Modes:*

CRC_ERR - CRC Error

Set to 1 when an attached CRC is erroneous.

Bit 1, 0: **OER - Overrun Error, RDR - RBR Data Ready**

Definitions are the same as legacy IR.

7.2.7 Set0.Reg6 - Reserved

7.2.8 Set0.Reg7 - User Defined Register (UDR/AUDR)

MODE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Legacy IR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced IR	FLC_ACT	UNDRN	RX_BSY/ RX_IP	LST_FE/ RX_PD	S_FEND	0	LB_SF	RX_TO
Reset Value	0	0	0	0	0	0	0	0

Legacy IR Register:

This is a temporary register that can be accessed and defined by the user.

Advanced IR Register:

Bit 7 *MIR, FIR Modes:*

FLC_ACT - Flow Control Active

Set to 1 when the flow control occurs. Cleared to 0 when this register is read. Note that this will be affected by Set5.Reg2 which controls the SIR mode switches to MIR/FIR mode *or* MIR/FIR mode operated in DMA function switches to SIR mode.

Bit 6 *MIR, FIR Modes:*

UNDRN - Underrun

Set to 1 when transmitter is empty *and* S_FEND (bit 3 of this register) is not set in PIO mode or no TC (Terminal Count) in DMA mode. Cleared to 0 after a write to 1.

Bit 5 *MIR, FIR Modes:*

RX_BSY - Receiver Busy

Set to 1 when receiver is busy or active in process.

Remote IR mode:

RX_IP - Receiver in Process

Set to 1 when receiver is in process.

Bit 4: *MIR, FIR modes:*

LST_FE - Lost Frame End

Set to 1 when a frame end in a entire frame is lost. Cleared to 0 when this register is read.

Remote IR Modes:

RX_PD - Receiver Pulse Detected

Set to 1 when one or more remote pulses are detected. Cleared to 0 when this register is read.

Bit 3 *MIR, FIR Modes:*

S_FEND - Set a Frame End

Set to 1 when trying to terminate the frame, that is, the procedure of PIO command is

An Entire Frame = Write Frame Data (First) + Write S_FEND (Last)

This bit should be set to 1, if use in PIO mode, to avoid transmitter underrun. Note that setting S_FEND to 1 is equivalent to TC (Terminal Count) in DMA mode. Therefore, this bit should be set to 0 in DMA mode.

Bit 2: Reserved.

Bit 1: *MIR, FIR Modes:*

LB_SF - Last Byte Stay in FIFO

A 1 in this bit indicates one or more frame ends still stay in receiver FIFO.

Bit 0: *MIR, FIR, Remote IR Modes:*

RX_TO - Receiver FIFO or Frame Status FIFO time-out

Set to 1 when receiver FIFO *or* frame status FIFO time-out occurs

7.3 Set1 - Legacy Baud Rate Divisor Register

ADDRESS OFFSET	REGISTER NAME	REGISTER DESCRIPTION
0	**BLL**	Baud Rate Divisor Latch (Low Byte)
1	**BHL**	Baud Rate Divisor Latch (High Byte)
2	**ISR/UFR**	Interrupt Status *or* IR FIFO Control Register
3	**UCR/SSR**	IR Control *or* Sets Select Register
4	**HCR**	Handshake Control Register
5	**USR**	IR Status Register
6	**HSR**	Handshake Status Register
7	**UDR/ESCR**	User Defined Register

7.3.1 Set1.Reg0~1 - Baud Rate Divisor Latch (BLL/BHL)

These two registers of BLL and BHL are baud rate divisor latch in the legacy SIR/ASK-IR mode. Accessing these registers in Advanced IR mode will cause backward operation, that is, UART will fall back to legacy SIR mode and clear some register values as shown in the following table.

SET & REGISTER	ADVANCED MODE DIS_BACK=¡Ñ	LEGACY MODE DIS_BACK=0
Set 0.Reg 4	Bit 7~5	-
Set 2.Reg 2	Bit 0, 5, 7	Bit 5, 7
Set 4.Reg 3	Bit 2, 3	-

Note that DIS_BACK=1 (Disable Backward operation) in legacy SIR/ASK-IR mode will not affect any register which is meaningful in legacy SIR/ASK-IR.

7.3.2 Set1.Reg 2~7

These registers are defined as the same as Set 0 registers.

7.4 Set2 - Interrupt Status or IR FIFO Control Register (ISR/UFR)

These registers are only used in advanced modes.

ADDRESS OFFSET	REGISTER NAME	REGISTER DESCRIPTION
0	**ABLL**	Advanced Baud Rate Divisor Latch (Low Byte)
1	**ABHL**	Advanced Baud Rate Divisor Latch (High Byte)
2	**ADCR1**	Advanced IR Control Register 1
3	**SSR**	Sets Select Register
4	**ADCR2**	Advanced IR Control Register 2
5	**Reserved**	-
6	**TXFDTH**	Transmitter FIFO Depth
7	**RXFDTH**	Receiver FIFO Depth

7.4.1 Reg0, 1 - Advanced Baud Rate Divisor Latch (ABLL/ABHL)

These two registers are the same as legacy IR baud rate divisor latch in SET 1.Reg0~1. In advanced SIR/ASK-IR mode, user should program these registers to set baud rate. This is to prevent backward operation from occurring.

7.4.2 Reg2 - Advanced IR Control Register 1 (ADCR1)

MODE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Advanced IR	BR_OUT	-	EN_LOUT	ALOOP	D_CHSW	DMATHL	DMA_F	ADV_SL
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **BR_OUT - Baud Rate Clock Output**

When written to 1, the programmed baud rate clock will be output to DTR pin. This bit is only used to test baud rate divisor.

Bit 6: **Reserved,** write 0.

Bit 5: **EN_LOUT - Enable Loopback Output**

A write to 1 will enable transmitter to output data to IRTX pin when loopback operation. Internal data can be verified through an output pin by setting this bit.

Bit 4: **ALOOP - All Mode Loopback**

A write to 1 will enable loopback in all modes.

Bit 3: **D_CHSW - DMA TX/RX Channel Swap**

If only one DMA channel operates in MIR/FIR mode, then the DMA channel can be swapped.

D_CHSW	DMA Channel Selected
0	Receiver (Default)
1	Transmitter

A write to 1 will enable output data when ALOOP=1.

Bit 2: **DMATHL - DMA Threshold Level**

Set DMA threshold level as shown in the following table.

DMATHL	TX FIFO THRESHOLD		RX FIFO THRESHOLD
	16-BYTE	32-BYTE	(16/32-BYTE)
0	13	13	4
1	23	7	10

Bit 1: **DMA_F - DMA Fairness**

DMA_F	Function Description
0	DMA request (DREQ) is forced inactive after 10.5us
1	No effect DMA request.

Bit 0: **ADV_SL - Advanced Mode Select**

A write to 1 selects advanced mode.

7.4.3 Reg3 - Sets Select Register (SSR)

Reading this register returns E0H. Writing a value selects Register Set.

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Refault Value	1	1	1	0	0	0	0	0

7.4.4 Reg4 - Advanced IR Control Register 2 (ADCR2)

MODE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Advanced IR	DIS_BACK	-	PR_DIV1	PR_DIV0	RX_FSZ1	RX_FSZ0	TX_FSZ1	TXFSZ0
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **DIS_BACK - Disable Backward Operation**

A write to 1 disables backward legacy IR mode. When operate in legacy SIR/ASK-IR mode, this bit should be set to 1 to avoid backward operation.

Bit 6: **Reserved,** write 0.

Bit 5, 4: **PR_DIV1~0 - Pre-Divisor 1~0.**

These bits select pre-divisor for external input clock 24M Hz. The clock goes through the pre-divisor then input to baud rate divisor of IR.

PR_DIV1~0	PRE-DIVISOR	MAX. BAUD RATE
00	13.0	**115.2K** bps
01	1.625	**921.6K** bps
10	6.5	**230.4K** bps
11	1	**1.5M** bps

Bit 3, 2: **RX_FSZ1~0 - Receiver FIFO Size 1~0**

These bits setup receiver FIFO size when FIFO is enable.

RX_FSZ1~0	RX FIFO SIZE
00	**16**-Byte
01	**32**-Byte
1X	Reserved

Bit 1, 0: **TX_FSZ1~0 - Transmitter FIFO Size 1~0**

These bits setup transmitter FIFO size when FIFO is enable.

TX_FSZ1~0	TX FIFO SIZE
00	**16**-Byte
01	**32**-Byte
1X	Reserved

TABLE: SIR Baud Rate

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461M HZ	PRE-DIV:1.625 14.769M HZ	PRE-DIV: 1.0 24M HZ	DECIMAL DIVISOR USED TO GENERATE 16X CLOCK	ERROR PERCENTAGE BETWEEN DESIRED AND ACTUAL
50	400	650	**2304**	**
75	600	975	**1536**	**
110	880	1430	**1047**	0.18%
134.5	1076	1478.5	**857**	0.099%
150	1200	1950	**768**	**
300	2400	3900	**384**	**
600	4800	7800	**192**	**
1200	9600	15600	**96**	**
1800	14400	23400	**64**	**
2000	16000	26000	**58**	0.53%
2400	19200	31200	**48**	**
3600	28800	46800	**32**	**
4800	38400	62400	**24**	**
7200	57600	93600	**16**	**
9600	76800	124800	**12**	**
19200	153600	249600	**6**	**
38400	307200	499200	**3**	**
57600	460800	748800	**2**	**
115200	921600	1497600	**1**	**

** The percentage error for all baud rates, except where indicated otherwise, is 0.16%.

7.4.5 Reg6 - Transmitter FIFO Depth (TXFDTH) (Read Only)

MODE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Advanced IR	0	0	TXFD5	TXFD4	TXFD3	TXFD2	TXFD1	TXFD1
Reset Value	0	0	0	0	0	0	0	0

Bit 7~6: **Reserved,** Read 0.

Bit 5~0: Reading these bits returns the current transmitter FIFO depth, that is, the number of bytes left in the transmitter FIFO.

7.4.6 Reg7 - Receiver FIFO Depth (RXFDTH) (Read Only)

MODE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Advanced IR	0	0	RXFD5	RXFD4	RXFD3	RXFD2	RXFD1	RXFD1
Reset Value	0	0	0	0	0	0	0	0

Bit 7~6: **Reserved,** Read 0.

Bit 5~0: Reading these bits returns the current receiver FIFO depth, that is, the number of bytes left in the receiver FIFO.

7.5 Set3 - Version ID and Mapped Control Registers

ADDRESS OFFSET	REGISTER NAME	REGISTER DESCRIPTION
0	**AUID**	Advanced IR ID
1	**MP_UCR**	Mapped IR Control Register
2	**MP_UFR**	Mapped IR FIFO Control Register
3	**SSR**	Sets Select Register
4	**Reversed**	-
5	**Reserved**	-
6	**Reserved**	-
7	**Reserved**	-

7.5.1 Reg0 - Advanced IR ID (AUID)

This register is read only. It stores advanced IR version ID. Reading it returns 1XH.

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	0	0	0	1	X	X	X	X

7.5.2 Reg1 - Mapped IR Control Register (MP_UCR)

This register is read only. Reading this register returns IR Control Register value of Set 0.

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	0	0	0	0	0	0	0	0

7.5.3 Reg2 - Mapped IR FIFO Control Register (MP_UFR)

This register is read only. Reading this register returns IR FIFO Control Register (UFR) value of SET 0.

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	0	0	0	0	0	0	0	0

7.5.4 Reg3 - Sets Select Register (SSR)

Reading this register returns E4H. Writing a value selects a Register Set.

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	1	1	1	0	0	1	0	0

7.6 Set4 - TX/RX/Timer counter registers and IR control registers.

ADDRESS OFFSET	REGISTER NAME	REGISTER DESCRIPTION
0	**TMRL**	Timer Value Low Byte
1	**TMRH**	Timer Value High Byte
2	**IR_MSL**	Infrared Mode Select
3	**SSR**	Sets Select Register
4	**TFRLL**	Transmitter Frame Length Low Byte
5	**TFRLH**	Transmitter Frame Length High Byte
6	**RFRLL**	Receiver Frame Length Low Byte
7	**RFRLH**	Receiver Frame Length High Byte

7.6.1 Set4.Reg0, 1 - Timer Value Register (TMRL/TMRH)

This is a 12-bit timer whose resolution is 1ms, that is, the maximum programmable time is 2^{12}-1 ms. The timer is a down-counter and starts counting down when EN_TMR (Enable Timer) of Set4.Reg2 is set to 1. When the timer counts down to *zero* and EN_TMR=1, the TMR_I is set to 1 and a new initial value will be loaded into counter.

7.6.2 Set4.Reg2 - Infrared Mode Select (IR_MSL)

MODE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Advanced IR	-	-	-	-	IR_MSL1	IR_MSL0	TMR_TST	EN_TMR
Reset Value	0	0	0	0	0	0	0	0

Bit 7~4: **Reserved**, write to 0.

Bit 3, 2: **IR_MSL1, 0 - Infrared Mode Select**

Select legacy IR, SIR, or ASK-IR mode. Note that in legacy SIR/ASK-IR user should set DIS_BACK=1 to avoid backward when programming baud rate.

IR_MSL1, 0	OPERATION MODE SELECTED
00	Legacy **IR**
01	CIR
10	Legacy **ASK-IR**
11	Legacy **SIR**

Bit 1: **TMR_TST - Timer Test**

When set to 1, reading the TMRL/TMRH returns the programmed values of TMRL/TMRH instead of the value of down counter. This bit is for testing timer register.

Bit 0: **EN_TMR - Enable Timer**

A write to 1 will enable the timer.

7.6.3 Set4.Reg3 - Set Select Register (SSR)

Reading this register returns E8H. Writing this register selects Register Set.

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	1	1	1	1	1	0	0	0

7.6.4 Set4.Reg4, 5 - Transmitter Frame Length (TFRLL/TFRLH)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TFRLL	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
Reset Value	0	0	0	0	0	0	0	0
TFRLH	-	-	-	bit 12	bit 11	bit 10	bit 9	bit 8
Reset Value	-	-	-	0	0	0	0	0

These are combined to be a 13-bit register. Writing these registers programs the transmitter frame length of a package. These registers are only valid when APM=1 (automatic package mode, Set5.Reg4.bit5). When APM=1, the physical layer will split data stream to a programmed frame length if the transmitted data is larger than the programmed frame length. When these registers are read, they will return the number of bytes which is not transmitted from a frame length programmed.

7.6.5 Set4.Reg6, 7 - Receiver Frame Length (RFRLL/RFRLH)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RFRLL	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reset Value	0	0	0	0	0	0	0	0
RFRLH	-	-	-	bit 12	bit 11	bit 10	bit 9	bit 8
Reset Value	-	-	-	0	0	0	0	0

These are combined to be a 13-bit registers and up counter. The length of receiver frame will be limited to the programmed frame length. If the received frame length is larger than the programmed receiver frame length, the bit of MX_LEX (Maximum Length Exceed) will be set to 1. Simultaneously, the receiver will not receive any more data to RX FIFO until the next start flag of the next frame, which is defined in the physical layer IrDA 1.1. Reading these registers returns the number of received data bytes of a frame from the receiver.

7.7 Set 5 - Flow control and IR control and Frame Status FIFO registers

ADDRESS OFFSET	REGISTER NAME	REGISTER DESCRIPTION
0	**FCBLL**	Flow Control Baud Rate Divisor Latch Register (Low Byte)
1	**FCBHL**	Flow Control Baud Rate Divisor Latch Register (High Byte)
2	**FC_MD**	Flow Control Mode Operation
3	**SSR**	Sets Select Register
4	**IRCFG1**	Infrared Configure Register
5	**FS_FO**	Frame Status FIFO Register
6	**RFRLFL**	Receiver Frame Length FIFO Low Byte
7	**RFRLFH**	Receiver Frame Length FIFO High Byte

7.7.1 Set5.Reg0, 1 - Flow Control Baud Rate Divisor Latch Register (FCDLL/ FCDHL)

If flow control is enforced when UART switches mode from MIR/FIR to SIR, then the pre-programmed baud rate of FCBLL/FCBHL are loaded into advanced baud rate divisor latch (ADBLL/ADBHL).

7.7.2 Set5.Reg2 - Flow Control Mode Operation (FC_MD)

These registers control flow control mode operation as shown in the following table.

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FC_MD	FC_MD2	FC_MD1	FC_MD0	-	FC_DSW	EN_FD	EN_BRFC	EN_FC
Reset Value	0	0	0	0	0	0	0	0

Bit 7~5 **FC_MD2 - Flow Control Mode**

When flow control is enforced, these bits will be loaded into AD_MD2~0 of advanced HSR (Handshake Status Register). These three bits are defined as same as AD_MD2~0.

Bit 4: **Reserved**, write 0.

Bit 3: **FC_DSW - Flow Control DMA Channel Swap**

A write to 1 allow user to swap DMA channel for transmitter or receiver when flow control is enforced.

FC_DSW	Next Mode After Flow Control Occurred
0	Receiver Channel
1	Transmitter Channel

Bit 2: **EN_FD - Enable Flow DMA Control**

A write to 1 enables UART to use DMA channel when flow control is enforced.

Bit 1: **EN_BRFC - Enable Baud Rate Flow Control**

A write to 1 enables FC_BLL/FC_BHL (Flow Control Baud Rate Divider Latch, in Set5.Reg1~0) to be loaded into advanced baud rate divisor latch (ADBLL/ADBHL, in Set2.Reg1~0).

Bit 0: **EN_FC - Enable Flow Control**

A write to 1 enables flow control function and bit 7~1 of this register.

7.7.3 Set5.Reg3 - Sets Select Register (SSR)

Writing this register selects Register Set. Reading this register returns ECH.

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	1	1	1	0	1	1	0	0

7.7.4 Set5.Reg4 - Infrared Configure Register 1 (IRCFG1)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRCFG1	-	FSF_TH	FEND_M	AUX_RX	-	-	IRHSSL	IR_FULL
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **Reserved**, write 0.

Bit 6: **FSF_TH - Frame Status FIFO Threshold**

Set this bit to determine the frame status FIFO threshold level and to generate the FSF_I. The threshold level values are defined as follows.

FSF_TH	STATUS FIFO THRESHOLD LEVEL
0	2
1	4

Bit 5: **FEND_MD - Frame End Mode**

A write to 1 enables hardware to split data stream into equal length frame automatically as defined in Set4.Reg4 and Set4.Reg5, i.e., TFRLL/TFRLH.

Bit 4: **AUX_RX - Auxiliary Receiver Pin**

A write to 1 selects IRRX input pin. (Refer to Set7.Reg7.Bit5)

Bit 3~2: **Reserved**, write 0.

Bit 1: **IRHSSL - Infrared Handshake Status Select**

When set to 0, the HSR (Handshake Status Register) operates as same as defined in IR mode. A write to 1 will disable HSR, and reading HSR returns 30H.

Bit 0: **IR_FULL - Infrared Full Duplex Operation**

When set to 0, IR module operates in half duplex. A write to 1 makes IR module operate in full duplex.

7.7.5 Set5.Reg5 - Frame Status FIFO Register (FS_FO)

This register shows the bottom byte of frame status FIFO.

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FS_FO	FSFDR	LST_FR	-	MX_LEX	PHY_ERR	CRC_ERR	RX_OV	FSF_OV
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **FSFDR - Frame Status FIFO Data Ready**

Indicate that a data byte is valid in frame status FIFO bottom.

Bit 6: **LST_FR - Lost Frame**

Set to 1 when one or more frames have been lost.

Bit 5: **Reserved**.

Bit 4: **MX_LEX - Maximum Frame Length Exceed**

Set to 1 when incoming data exceeds programmed maximum frame length defined in Set4.Reg6 and Set4.Reg7. This bit is in frame status FIFO bottom and is valid only when FSFDR=1 (Frame Status FIFO Data Ready).

Bit 3: **PHY_ERR - Physical Error**

When receiving data, any physical layer error as defined in IrDA 1.1 will set this bit to 1. This bit is in frame status FIFO bottom and is valid only when FSFDR=1 (Frame Status FIFO Data Ready).

Bit 2: **CRC_ERR - CRC Error**

Set to 1 when receive a bad CRC in a frame. This CRC belongs to physical layer as defined in IrDA 1.1. This bit is in frame status FIFO bottom and is valid only when FSFDR=1 (Frame Status FIFO Data Ready).

Bit 1: **RX_OV - Received Data Overrun**

Set to 1 when receiver FIFO overruns.

Bit 0: **FSF_OV - Frame Status FIFO Overrun**

Set to 1 When frame status FIFO overruns.

7.7.6 Set5.Reg6, 7 - Receiver Frame Length FIFO (RFLFL/RFLFH) or Lost Frame Number (LST_NU)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RFLFL/ LST_NU	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset Value	0	0	0	0	0	0	0	0
RFLFH	-	-	-	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset Value	0	0	0	0	0	0	0	0

Receiver Frame Length FIFO (RFLFL/RFLFH):

These are combined to be a 13-bit register. Reading these registers returns received byte count for the frame. When read, the register of *RFLFH* will pop-up another frame status and frame length if FSFDR=1 (Set5.Reg4.Bit7).

Lost Frame Number (LST_NU):

When LST_FR=1 (Set5.Reg4.Bit6), Reg6 stands for LST_NU which is a 8-bit register holding the number of frames lost in succession.

7.8 Set6 - IR Physical Layer Control Registers

ADDRESS OFFSET	REGISTER NAME	REGISTER DESCRIPTION
0	**IR_CFG2**	Infrared Configure Register 2
1	**MIR_PW**	MIR (1.152M bps or 0.576M bps) Pulse Width
2	**SIR_PW**	SIR Pulse Width
3	**SSR**	Sets Select Register
4	**HIR_FNU**	High Speed Infrared Flag Number
5	**Reserved**	-
6	**Reserved**	-
7	**Reserved**	-

7.8.1 Set6.Reg0 - Infrared Configure Register 2 (IR_CFG2)

This register controls ASK-IR, MIR, FIR operations.

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IR_CFG2	SHMD_N	SHDM_N	FIR_CRC	MIR_CRC	-	INV_CRC	DIS_CRC	-
Reset Value	0	0	1	0	0	0	0	0

Bit 7: **SHMD_N - ASK-IR Modulation Disable**

SHMD_N	Modulation Mode
0	IRTX modulate 500K Hz Square Wave
1	Re-rout IRTX

Bit 6: **SHDM_N - ASK-IR Demodulation Disable**

SHDM_N	Demodulation Mode
0	Demodulation 500K Hz
1	Re-rout IRRX

Bit 5: **FIR_CRC - FIR (4M bps) CRC Type**

FIR_CRC	CRC Type
0	16-bit CRC
1	32-bit CRC

Note that the 16/32-bit CRC are defined in IrDA 1.1 physical layer.

Bit 4: **MIR_CRC - MIR (1.152M/0.576M bps) CRC Type**

MIR_CRC	CRC Type
0	16-bit CRC
1	32-bit CRC

Bit 2: **INV_CRC - Inverting CRC**

When set to 1, the CRC is inversely output in physical layer.

Bit 1: **DIS_CRC - Disable CRC**

When set to 1, the transmitter does not transmit CRC in physical layer.

Bit 0: **Reserved**, write 1.

7.8.2 Set6.Reg1 - MIR (1.152M/0.576M bps) Pulse Width

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MIR_PW	-	-	-	M_PW4	M_PW3	M_PW2	M_PW1	M_PW0
Reset Value	0	0	0	0	1	0	1	0

This 5-bit register sets MIR output pulse width.

M_PW4~0	MIR PULSE WIDTH (1.152M BPS)	MIR OUTPUT WIDTH (0.576M BPS)
00000	**0** ns	**0** ns
00001	**20.83** ns	**41.66** ns
00010	**41.66** (==20.83*2) ns	**83.32** (==41.66*2) ns
...	**...**	**...**
k_{10}	**20.83***k_{10} ns	**41.66***k_{10} ns
...	**...**	**...**
11111	**645** ns	**1290** ns

7.8.3 Set6.Reg2 - SIR Pulse Width

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SIR_PW	-	-	-	S_PW4	S_PW3	S_PW2	S_PW1	S_PW0
Reset Value	0	0	0	0	0	0	0	0

This 5-bit register sets SIR output pulse width.

S_PW4~0	SIR OUTPUT PULSE WIDTH
00000	**3/16 bit time** of IR
01101	**1.6** us
Others	**1.6** us

7.8.4 Set6.Reg3 - Set Select Register

Select Register Set by writing a set number to this register. Reading this register returns F0H.

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	1	1	1	1	0	0	0	0

7.8.5 Set6.Reg4 - High Speed Infrared Beginning Flag Number (HIR_FNU)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HIR_FNU	M_FG3	M_FG2	M_FG1	M_FG0	F_FL3	F_FL2	F_FL1	F_FL0
Reset Value	0	0	1	0	1	0	1	0

Bit 7~4: **M_FG3~0 - MIR beginning Flag Number**

These bits define the number of transmitter *Start Flag* of MIR. Note that the number of MIR start flag should be equal or more than *two* which is defined in IrDA 1.1 physical layer. The default value is 2.

M_FG3~0	BEGINNING FLAG NUMBER	M_FG3~0	BEGINNING FLAG NUMBER
0000	Reserved	**1000**	10
0001	1	**1001**	12
0010	**2** (Default)	**1010**	16
0011	3	**1011**	20
0100	4	**1100**	24
0101	5	**1101**	28
0110	6	**1110**	32
0111	8	**1111**	Reserved

Bit 3~0: **F_FG3~0 - FIR Beginning Flag Number**

These bits define the number of transmitter *Preamble Flag* in FIR. Note that the number of FIR start flag should be equal to *sixteen* which is defined in IrDA 1.1 physical layer. The default value is 16.

M_FG3~0	BEGINNING FLAG NUMBER	M_FG3~0	BEGINNING FLAG NUMBER
0000	Reserved	**1000**	10
0001	1	**1001**	12
0010	2	**1010**	**16** (Default)
0011	3	**1011**	20
0100	4	**1100**	24
0101	5	**1101**	28
0110	6	**1110**	32
0111	8	**1111**	Reserved

7.9 Set7 - Remote control and IR module selection registers

ADDRESS OFFSET	REGISTER NAME	REGISTER DESCRIPTION
0	**RIR_RXC**	Remote Infrared Receiver Control
1	**RIR_TXC**	Remote Infrared Transmitter Control
2	**RIR_CFG**	Remote Infrared Config Register
3	**SSR**	Sets Select Register
4	**IRM_SL1**	Infrared Module (Front End) Select 1
5	**IRM_SL2**	Infrared Module Select 2
6	**IRM_SL3**	Infrared Module Select 3
7	**IRM_CR**	Infrared Module Control Register

7.9.1 Set7.Reg0 - Remote Infrared Receiver Control (RIR_RXC)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RIR_RXC	RX_FR2	RX_FR1	RX_FR0	RX_FSL4	RX_FSL3	RX_FSL2	RX_FSL1	RX_FSL0
Default Value	0	0	1	0	1	0	0	1

This register defines frequency range of receiver of remote IR.

Bit 7~5: **RX_FR2~0 - Receiver Frequency Range 2~0.**

These bits select the input frequency range of the receiver. It is implemented through a band pass filter, i.e., only the input signals whose frequency lies in the range defined in this register will be received.

Bit 4~0: **RX_FSL4~0 - Receiver Frequency Select 4~0.**

Select the operation frequency of receiver.

Table: Low Frequency range select of receiver.

	RX_FR2~0 (LOW FREQUENCY)					
	001		**010**		**011**	
RX_FSL4~0	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**
00010	26.1	29.6	24.7	31.7	23.4	34.2
00011	28.2	32.0	26.7	34.3	25.3	36.9
00100	29.4	33.3	27.8	35.7	26.3	38.4
00101	30.0	34.0	28.4	36.5	26.9	39.3
00110	31.4	35.6	29.6	38.1	28.1	41.0
00111	32.1	36.4	30.3	39.0	28.7	42.0
01000	32.8	37.2	31.0	39.8	29.4	42.9
01001	***33.6****	***38.1****	31.7	40.8	30.1	44.0
01011	34.4	39.0	32.5	41.8	30.8	45.0
01100	36.2	41.0	34.2	44.0	32.4	47.3
01101	37.2	42.1	35.1	45.1	33.2	48.6
01111	38.2	43.2	36.0	46.3	34.1	49.9
10000	40.3	45.7	38.1	49.0	36.1	52n.7
10010	41.5	47.1	39.2	50.4	37.2	54.3
10011	42.8	48.5	40.4	51.9	38.3	56.0
10101	44.1	50.0	41.7	53.6	39.5	57.7
10111	45.5	51.6	43.0	55.3	40.7	59.6
11010	48.7	55.2	46.0	59.1	43.6	63.7
11011	50.4	57.1	47.6	61.2	45.1	65.9
11101	54.3	61.5	51.3	65.9	48.6	71.0

Note that those unassigned combinations are reserved.

Table: High Frequency range select of receiver

	RX_FR2~0 (HIGH FREQUENCY)	
	001	
RX_FSL4~0	Min.	Max.
00011	355.6	457.1
01000	380.1	489.8
01011	410.3	527.4

Note that those unassigned combinations are reserved.

Table: SHARP ASK-IR receiver frequency range select.

RX_FSL4~0 (SHARP ASK-IR)												
RX_FR2~0	**001**		**010**		**011**		**100**		**101**		**110**	
-	***480.0****	***533.3****	457.1	564.7	436.4	600.0	417.4	640.0	400.0	685.6	384.0	738.5

Note that those unassigned combinations are reserved.

7.9.2 Set7.Reg1 - Remote Infrared Transmitter Control (RIR_TXC)

REG.	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
RIR_TXC	TX_PW2	TX_PW1	TX_PW0	TX_FSL4	TX_FSL3	TX_FSL2	TX_FSL1	TX_FSL0
Default Value	0	1	1	0	1	0	0	1

This Register defines the transmitter frequency and pulse width of remote IR.

Bit 7~5: **TX_PW2~0 - Transmitter Pulse Width 2~ 0.**

Select the transmission pulse width.

TX_PW2~0	**LOW FREQUENCY**	**HIGH FREQUENCY**
010	6 μs	0.7 μs
011	7 μs	0.8 μs
100	9 μs	0.9 μs
101	10.6 μs	1.0 μs

Note that those unassigned combinations are reserved.

Bit 4~0: **TX_FSL4~0 - Transmitter Frequency Select 4~0.**

Select the transmission frequency.

Table: Low frequency selected.

TX_FSL4~0	LOW FREQUENCY
00011	30K Hz
00100	31K HZ
...	...
11101	56K Hz

Note that those unassigned combinations are reserved.

Table: High frequency selected.

TX_FSL4~0	HIGH FREQUENCY
00011	400K Hz
01000	450K Hz
01011	480K Hz

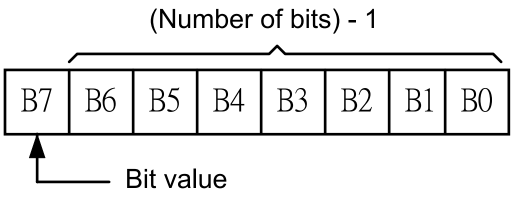
Note that those unassigned combinations are reserved.

7.9.3 Set7.Reg2 - Remote Infrared Config Register (RIR_CFG)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RIR_CFG	P_PNB	SMP_M	RXCFS	-	TX_CFS	RX_DM	TX_MM1	TX_MM0
Default Value	0	0	0	0	0	0	0	0

Bit 7: **P_PNB: Programming Pulse Number Coding.**

Write a 1 to select programming pulse number coding. The code format is defined as follows.



If the bit value is set to 0, the high pulse will be transmitted/received. If the bit value is set to 1, then no energy will be transmitted/received.

Bit 6: **SMP_M - Sampling Mode.**

To select receiver sampling mode.

When set to 0 then uses T-period sampling, that the T-period is programmed IR baud rate.

When set to 1, programmed baud rate will be used to do oversampling.

Bit 5: **RXCFS - Receiver Carry Frequency Select**

RXCFS	Selected Frequency
0	30K ~ 56K Hz
1	400K ~ 480K Hz

Bit 4: **Reserved,** write 0.

Bit 3: **TX_CFS - Transmitter Carry Frequency Select.**

Select low speed or high speed transmitter carry frequency.

TX_FCS	Selected Frequency
0	30K ~ 56K Hz
1	400K ~ 480K Hz

Bit 2: **RX_DM - Receiver Demodulation Mode.**

RX_DM	Demodulation Mode
0	Enable internal decoder
1	Disable internal decoder

Bit 1~0: **TX_MM1~0 - Transmitter Modulation Mode 1~0**

TX_MM1~0	TX Modulation Mode
00	Continuously send pulse for logic 0
01	**8 pulses** for logic 0 and no pulse for logic 1.
10	**6 pulses** for logic 0 and no pulse for logic 1
11	Reserved.

7.9.4 Set7.Reg3 - Sets Select Register (SSR)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SSR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default Value	1	1	1	1	0	1	0	0

Reading this register returns F4H. Select Register Set by writing a set number to this register.

7.9.5 Set7.Reg4 - Infrared Module (Front End) Select 1 (IRM_SL1)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRM_SL1	IR_MSP	SIR_SL2	SIR_SL1	SIR_SL0	-	AIR_SL2	AIR_SL1	AIR_SL0
Default Value	0	0	0	0	0	0	0	0

Bit 7: **IR_MSP - IR Mode Select Pulse**

When set to 1, the transmitter (IRTX) will send a 64 μs pulse to setup a special IR front-end operational mode. When IR front-end module uses *mode select pin (MD)* and *transmitter IR pulse (IRTX)* to switch between high speed IR (such as FIR or MIR) and low speed IR (SIR or ASK-IR), this bit should be used.

Bit 6~4: **SIR_SL2~0 - SIR (Serial IR) mode select.**

These bits are used to program the operational mode of the SIR front-end module. These values of SIR_SL2~0 will be automatically loaded to pins of IR_SL2~0, respectively, when (1) AM_FMT=1 (Automatic Format, in Set7.Reg7.Bit7); (2) the mode of Advanced IR is set to SIR (AD_MD2~0, in Set0.Reg4.Bit7~0).

Bit 3: **Reserved,** write 0.

Bit 2~0: **AIR_SL2~0 - ASK-IR Mode Select.**

These bits setup the operational mode of ASK-IR front-end module when AM_FMT=1 and AD_MD2~0 are configured to ASK-IR mode. These values will be automatically loaded to IR_SL2~0, respectively.

7.9.6 Set7.Reg5 - Infrared Module (Front End) Select 2 (IRM_SL2)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRM_SL2	-	FIR_SL2	FIR_SL1	FIR_SL0	-	MIR_SL2	MIR_SL1	MIR_SL0
Default Value	0	0	0	0	0	0	0	0

Bit 7: **Reserved,** write 0.

Bit 6~4: **FIR_SL2~0 - FIR mode select.**

These bits setup the operational mode of FIR front-end module when AM_FMT=1 and AD_MD2~0 are configured to FIR mode. These values will be automatically loaded to IR_SL2~0, respectively.

Bit 3: **Reserved,** write 0.

Bit 2~0: **MIR_SL2~0 - MIR Mode Select.**

These bits setup the MIR operational mode when AM_FMT=1 *and* AD_MD2~0 are configured to MIR mode. These values will be automatically loaded to IR_SL2~0, respectively.

7.9.7 Set7.Reg6 - Infrared Module (Front End) Select 3 (IRM_SL3)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRM_SL3	-	LRC_SL2	LRC_SL1	LRC_SL0	-	HRC_SL2	HRC_SL1	HRC_SL0
Default Value	0	0	0	0	0	0	0	0

Bit 7: **Reserved,** write 0.

Bit 6~4: **LRC_SL2~0 - Low Speed Remote IR mode select.**

These bits setup the operational mode of *low speed* remote IR front-end module when AM_FMT=1 and AD_MD2~0 are configured to Remote IR mode. These values will be automatically loaded to IR_SL2~0, respectively.

Bit 3: **Reserved,** write 0.

Bit 2~0: **HRC_SL2~0 - High Speed Remote IR Mode Select.**

These bits setup the operational mode of *high speed* remote IR front-end module when AM_FMT=1 and .AD_MD2~0 are configured to Remote IR mode. These values will be automatically loaded to IR_SL2~0, respectively.

7.9.8 Set7.Reg7 - Infrared Module Control Register (IRM_CR)

REG.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRM_CR	AM_FMT	IRX_MSL	IRSL0D	RXINV	TXINV	-	-	-
Default Value	0	0	0	0	0	0	0	0

Bit 7: **AM_FMT - Automatic Format**

A write to 1 will enable automatic format IR front-end module. These bit will affect the output of IR_SL2~0 which is referred by IR front-end module selection (Set7.Reg4~6)

Bit 6: **IRX_MSL - IR Receiver Module Select**

Select the receiver input path from the IR front end module if IR module has the separated high speed and low speed receiver path. If the IR module has only one receiving path, then this bit should be set to 0.

IRX_MSL	Receiver Pin selected
0	IRRX (Low/High Speed)
1	IRRXH (High Speed)

Bit 5: **IRSL0D - Direction of IRSL0 Pin**

Select function for IRRXH or IRSL0 because they share common pin and have different input/output direction.

IRSL0_D	Function
0	IRRXH (I/P)
1	IRSL0 (O/P)

Table: IR receiver input pin selection

IRSL0D	IRX_MSL	AUX_RX	HIGH SPEED IR	SELECTED IR PIN
0	0	0	X	**IRRX**
0	0	1	X	**IRRXH**
0	1	X	0	**IRRX**
0	1	X	1	**IRRXH**
1	0	0	X	**IRRX**
1	0	1	X	Reserved
1	1	X	0	**IRRX**
1	1	X	1	Reserved

Note: that (1) AUX_RX is defined in Set5.Reg4.Bit4, (2) high speed IR includes MIR (1.152M or 0.576M bps) and FIR (4M bps), (3) IRRX is the input of the low speed or high speed IR receiver, IRRXH is the input of the high speed IR receiver.

Bit 4: **RXINV - Receiving Signal Invert**

A write to 1 will Invert the receiving signal.

Bit 3: **TXINV - Transmitting Signal Invert**

A write to 1 will Invert the transmitting signal.

Bit 2~0: **Reserved,** write 0.

8. PARALLEL PORT

8.1 Printer Interface Logic

The parallel port of the W83977F/G, W83977AF/AG makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL level. The W83977F/G, W83977AF/AG supports an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP), Extension FDD mode (EXTFDD), Extension 2FDD mode (EXT2FDD) on the parallel port. Refer to the configuration registers for more information on disabling, power-down, and on selecting the mode of operation.

Table 8-1 shows the pin definitions for different modes of the parallel port.

TABLE 8-1-1 PARALLEL PORT CONNECTOR AND PIN DEFINITIONS

HOST CONNECTOR	PIN NUMBER OF W83977F/ AF	PIN ATTRIBUTE	SPP	EPP	ECP
1	36	O	nSTB	nWrite	nSTB, HostClk[2]
2-9	31-26, 24-23	I/O	PD<0:7>	PD<0:7>	PD<0:7>
10	22	I	nACK	Intr	nACK, PeriphClk[2]
11	21	I	BUSY	nWait	BUSY, PeriphAck[2]
12	19	I	PE	PE	PEerror, nAckReverse[2]
13	18	I	SLCT	Select	SLCT, Xflag[2]
14	35	O	nAFD	nDStrb	nAFD, HostAck[2]
15	34	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	33	O	nINIT	nInit	nINIT[1], nReverseRqst[2]
17	32	O	nSLIN	nAStrb	nSLIN[1] , ECPMode[2]

Notes:

n<name > : Active Low

1. Compatible Mode
2. High Speed Mode
3. For more information, refer to the IEEE 1284 standard.

TABLE 8-1-2 PARALLEL PORT CONNECTOR AND PIN DEFINITIONS

HOST CONNECTOR	PIN NUMBER OF W83977F/AF	PIN ATTRIBUTE	SPP	PIN ATTRIBUTE	EXT2FDD	PIN ATTRIBUTE	EXTFDD
1	36	O	nSTB	---	---	---	---
2	31	I/O	PD0	I	$\overline{\text{INDEX2}}$	I	$\overline{\text{INDEX2}}$
3	30	I/O	PD1	I	$\overline{\text{TRAK02}}$	I	$\overline{\text{TRAK02}}$
4	29	I/O	PD2	I	$\overline{\text{WP2}}$	I	$\overline{\text{WP2}}$
5	28	I/O	PD3	I	$\overline{\text{RDATA2}}$	I	$\overline{\text{RDATA2}}$
6	27	I/O	PD4	I	$\overline{\text{DSKCHG2}}$	I	$\overline{\text{DSKCHG2}}$
7	26	I/O	PD5	---	---	---	---
8	24	I/O	PD6	OD	$\overline{\text{MOA2}}$	---	---
9	23	I/O	PD7	OD	$\overline{\text{DSA2}}$	---	---
10	22	I	nACK	OD	$\overline{\text{DSB2}}$	OD	$\overline{\text{DSB2}}$
11	21	I	BUSY	OD	$\overline{\text{MOB2}}$	OD	$\overline{\text{MOB2}}$
12	19	I	PE	OD	$\overline{\text{WD2}}$	OD	$\overline{\text{WD2}}$
13	18	I	SLCT	OD	$\overline{\text{WE2}}$	OD	$\overline{\text{WE2}}$
14	35	O	nAFD	OD	$\overline{\text{RWC2}}$	OD	$\overline{\text{RWC2}}$
15	34	I	nERR	OD	$\overline{\text{HEAD2}}$	OD	$\overline{\text{HEAD2}}$
16	33	O	nINIT	OD	$\overline{\text{DIR2}}$	OD	$\overline{\text{DIR2}}$
17	32	O	nSLIN	OD	$\overline{\text{STEP2}}$	OD	$\overline{\text{STEP2}}$

8.2 Enhanced Parallel Port (EPP)

TABLE 8-2 PRINTER MODE AND EPP REGISTER ADDRESS

A2	A1	A0	REGISTER	NOTE
0	0	0	Data port (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

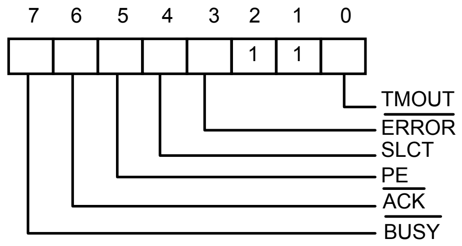
1. These registers are available in all modes.
2. These registers are available only in EPP mode.

8.2.1 Data Swapper

The system microprocessor can read the contents of the printer's data latch by reading the data swapper.

8.2.2 Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the printer status buffer. The bit definitions are as follows:



Bit 7: This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's $\overline{\text{ACK}}$ signal. A 0 means the printer has received a character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before $\overline{\text{BUSY}}$ stops.

Bit 5: Logical 1 means the printer has detected the end of paper.

Bit 4: Logical 1 means the printer is selected.

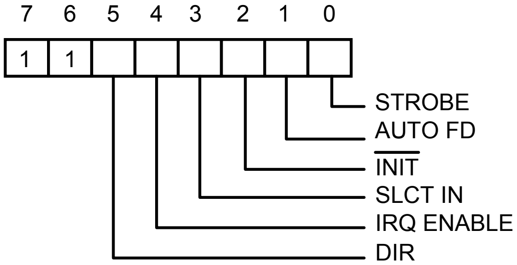
Bit 3: Logical 0 means the printer has encountered an error condition.

Bit 1, 2: These two bits are not implemented and are logic one during a read of the status register.

Bit 0: This bit is valid in EPP mode only. It indicates that a 10 µS time-out has occurred on the EPP bus. A logic 0 means that no time-out error has occurred; a logic 1 means that a time-out error has been detected. Writing a logic 1 to this bit will clear the time-out status bit; writing a logic 0 has no effect.

8.2.3 Printer Control Latch and Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the printer control swapper. Bit definitions are as follows:



Bit 7, 6: These two bits are a logic one during a read. They can be written.

Bit 5: Direction control bit

When this bit is a logic 1, the parallel port is in input mode (read); when it is a logic 0, the parallel port is in output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.

Bit 4: A 1 in this position allows an interrupt to occur when $\overline{\text{ACK}}$ changes from low to high.

Bit 3: A 1 in this bit position selects the printer.

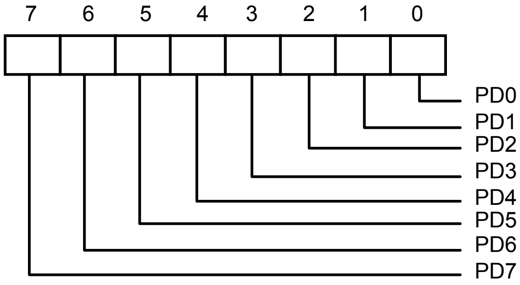
Bit 2: A 0 starts the printer (50 microsecond pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

8.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

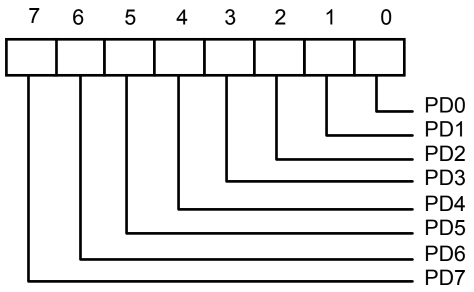


The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of $\overline{\text{IOW}}$ causes an EPP address write cycle to be performed, and the trailing edge of $\overline{\text{IOW}}$ latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of $\overline{\text{IOR}}$ causes an EPP address read cycle to be performed and the data to be output to the host CPU.

8.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. Bit definitions of each data port are as follows:



When accesses are made to any EPP data port, the contents of DB0-DB7 are buffered (non-inverting) and output to the ports PD0-PD7 during a write operation. The leading edge of $\overline{\text{IOW}}$ causes an EPP data write cycle to be performed, and the trailing edge of $\overline{\text{IOW}}$ latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of $\overline{\text{IOR}}$ causes an EPP read cycle to be performed and the data to be output to the host CPU.

8.2.6 Bit Map of Parallel Port and EPP Registers

REGISTER	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	$\overline{\text{BUSY}}$	$\overline{\text{ACK}}$	PE	SLCT	$\overline{\text{ERROR}}$	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	$\overline{\text{INIT}}$	$\overline{\text{AUTOFD}}$	$\overline{\text{STROBE}}$
Control Latch (Write)	1	1	DIR	IRQ	SLIN	$\overline{\text{INIT}}$	$\overline{\text{AUTOFD}}$	$\overline{\text{STROBE}}$
EPP Address Port R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

8.2.7 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
nWrite	O	Denotes an address or data read or write operation.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
nWait	I	Inactive to acknowledge that data transfer is completed. Active to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer selected status; same as SPP mode.
nDStrb	O	This signal is active low. It denotes a data read or write operation.
nError	I	Error; same as SPP mode.
nInits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
nAStrb	O	This signal is active low. It denotes an address read or write operation.

8.2.8 EPP Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. The PDx bus is in the standard or bi-directional mode when no EPP read, write, or address cycle is currently being executed. In this condition all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 µS have elapsed from the start of the EPP cycle to the time $\overline{\text{WAIT}}$ is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in Status bit 0.

8.2.8.1 EPP Operation

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

8.2.8.2 EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If the nWait is active low, when the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, the read/write cycle proceeds normally and will be completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle will not start. It must wait until nWait changes to active low, at which time it will start as described above.

8.2.8.3 EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it will not terminate until nWait changes from active low to inactive high.

8.3 Extended Capabilities Parallel (ECP) Port

This port is software and hardware compatible with existing parallel ports, so it may be used as a standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host to peripheral) and reverse (peripheral to host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port supports run-length-encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Hardware support for compression is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

8.3.1 ECP Register and Mode Definitions

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR23, which are determined by configuration register or hardware setting.

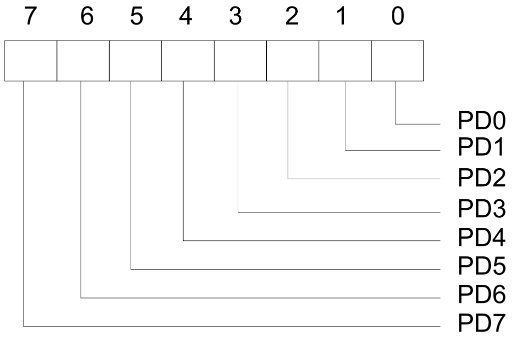
MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CR9 and CR0 to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

Note: The mode selection bits are bit 7-5 of the Extended Control Register.

8.3.2 Data and ecpAFifo Port

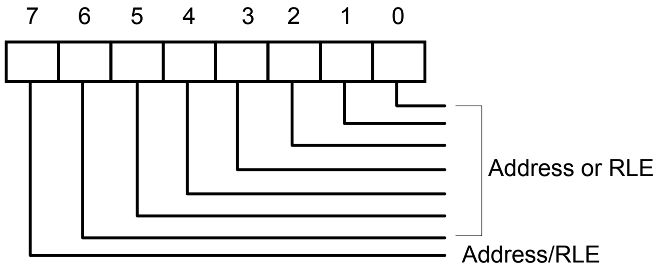
Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input. The contents of this register are output to the PD0-PD7 ports. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:



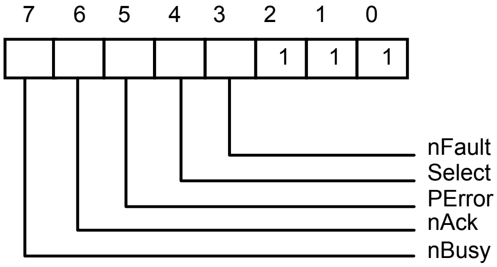
Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is defined only for the forward direction. The bit definitions are as follows:



8.3.3 Device Status Register (DSR)

These bits are at low level during a read of the Printer Status Register. The bits of this status register are defined as follows:



Bit 7: This bit reflects the complement of the Busy input.

Bit 6: This bit reflects the nAck input.

Bit 5: This bit reflects the PError input.

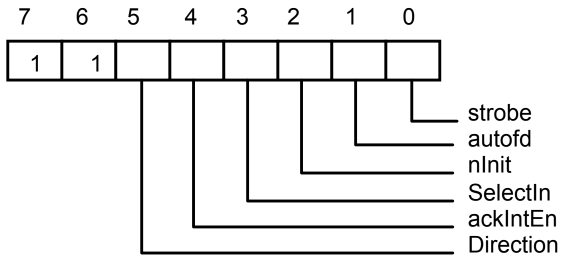
Bit 4: This bit reflects the Select input.

Bit 3: This bit reflects the nFault input.

Bit 2-0: These three bits are not implemented and are always logic one during a read.

8.3.4 Device Control Register (DCR)

The bit definitions are as follows:



Bit 6, 7: These two bits are logic one during a read and cannot be written.

Bit 5: This bit has no effect and the direction is always out if mode = 000 or mode = 010. Direction is valid in all other modes.

0	the parallel port is in output mode.
1	the parallel port is in input mode.

Bit 4: Interrupt request enable. When this bit is set to a high level, it may be used to enable interrupt requests from the parallel port to the CPU due to a low to high transition on the $\overline{\text{ACK}}$ input.

Bit 3: This bit is inverted and output to the $\overline{\text{SLIN}}$ output.

0	The printer is not selected.
1	The printer is selected.

Bit 2: This bit is output to the $\overline{\text{INIT}}$ output.

Bit 1: This bit is inverted and output to the $\overline{\text{AFD}}$ output.

Bit 0: This bit is inverted and output to the $\overline{\text{STB}}$ output.

8.3.5 cFifo (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. The standard parallel port protocol is used by a hardware handshake to the peripheral to transmit bytes written or DMAed from the system to this FIFO. Transfers to the FIFO are byte aligned.

8.3.6 ecpDFifo (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

When the direction bit is 1, data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

8.3.7 tFifo (Test FIFO Mode) Mode = 110

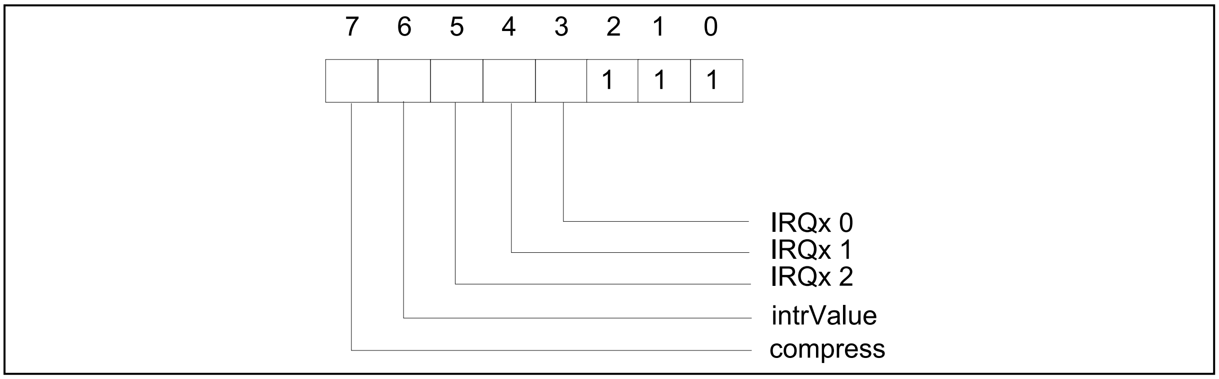
Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO will not be transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

8.3.8 cnfgA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates to the system that this is an 8-bit implementation.

8.3.9 cnfgB (Configuration Register B) Mode = 111

The bit definitions are as follows:



Bit 7: This bit is read-only. It is at low level during a read. This means that this chip does not support hardware RLE compression.

Bit 6: Returns the value on the ISA IRQ line to determine possible conflicts.

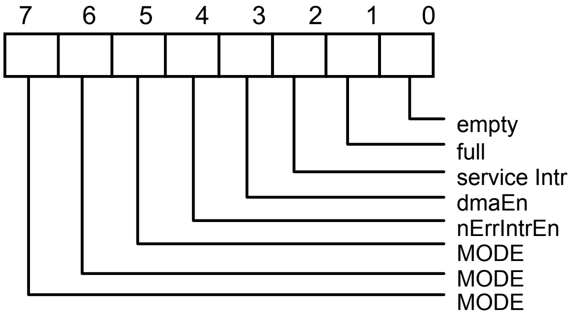
Bit 5-3: Reflect the IRQ resource assigned for ECP port.

cnfgB[5:3]	IRQ resource
000	reflect other IRQ resources selected by PnP register (default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

Bit 2-0: These five bits are at high level during a read and can be written.

8.3.10 ecr (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:



Bit 7-5: These bits are read/write and select the mode.

000	Standard Parallel Port mode. The FIFO is reset in this mode.
001	PS/2 Parallel Port mode. This is the same as 000 except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register.
010	Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.
011	ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and auto transmitted to the peripheral using ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
100	Selects EPP Mode. In this mode, EPP is activated if the EPP mode is selected.
101	Reserved.
110	Test Mode. The FIFO may be written and read in this mode, but the data will not be transmitted on the parallel port.
111	Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.

Bit 4: Read/Write (Valid only in ECP Mode)

1	Disables the interrupt generated on the asserting edge of nFault.
0	Enables an interrupt pulse on the high to low edge of nFault. If nFault is asserted (interrupt) an interrupt will be generated and this bit is written from a 1 to 0.

Bit 3: Read/Write

1	Enables DMA.
0	Disables DMA unconditionally.

Bit 2: Read/Write

1	Disables DMA and all of the service interrupts.
0	Enables one of the following cases of interrupts. When one of the service interrupts has occurred, the serviceIntr bit is set to a 1 by hardware. This bit must be reset to 0 to re-enable the interrupts. Writing a 1 to this bit will not cause an interrupt. (a) dmaEn = 1: During DMA this bit is set to a 1 when terminal count is reached. (b) dmaEn = 0 direction = 0: This bit is set to 1 whenever there are writeIntr Threshold or more bytes free in the FIFO. (c) dmaEn = 0 direction = 1: This bit is set to 1 whenever there are readIntr Threshold or more valid bytes to be read from the FIFO.

Bit 1: Read only

0	The FIFO has at least 1 free byte.
1	The FIFO cannot accept another byte or the FIFO is completely full.

Bit 0: Read only

0	The FIFO contains at least 1 byte of data.
1	The FIFO is completely empty.

8.3.11 Bit Map of ECP Port Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dsr	nBusy	nAck	PError	Select	nFault	1	1	1	1
dcr	1	1	Directio	ackIntEn	SelectIn	nInit	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

8.3.12 ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe (HostClk)	O	The nStrobe registers data or address into the slave on the asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contains address or data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. It indicates whether the data lines contain ECP command information or data in the reverse direction. When in reverse direction, normal data are transferred when Busy (PeriphAck) is high and an 8-bit command is transferred when it is low.
PError (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on line.
nAutoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. This signal indicates whether the data lines contain ECP address or data in the forward direction. When in forward direction, normal data are transferred when nAutoFd (HostAck) is high and an 8-bit command is transferred when it is low.
nFault (nPeriphRequest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP Mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

8.3.13 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits. The following are required:

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

(c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

8.3.13.1 Mode Switching

Software will execute P1284 negotiation and all operations prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can be changed only in mode 001.

When in extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001.

8.3.13.2 Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

8.3.13.3 Data Compression

The W83977F/G, W83977AF/AG supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Note that the odd (RLE) compression in hardware is not supported. In order to transfer data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

8.3.14 FIFO Operation

The FIFO threshold is set in configuration register 5. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

8.3.15 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. The DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, which will disable the DMA.

8.3.16 Programmed I/O (NON-DMA) Mode

The ECP or parallel port FIFOs can also be operated using interrupt driven programmed I/O. Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. The host must set the direction, state, dmaEn = 0 and serviceIntr = 0 in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

8.4 Extension FDD Mode (EXTFDD)

In this mode, the W83977F/ AF changes the printer interface pins to FDC input/output pins, allowing the user to install a second floppy disk drive (FDD B) through the DB-25 printer connector. The pin assignments for the FDC input/output pins are shown in Table 5-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins $\overline{\text{MOB}}$ and $\overline{\text{DSB}}$ will be forced to inactive state.

(2) Pins $\overline{\text{DSKCHG}}$, $\overline{\text{RDATA}}$, $\overline{\text{WP}}$, $\overline{\text{TRAK0}}$, $\overline{\text{INDEX}}$ will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXTFDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

8.5 Extension 2FDD Mode (EXT2FDD)

In this mode, the W83977F/G, W83977AF/AG changes the printer interface pins to FDC input/output pins, allowing the user to install two external floppy disk drives through the DB-25 printer connector to replace internal floppy disk drives A and B. The pin assignments for the FDC input/output pins are shown in Table5-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins $\overline{\text{MOA}}$, $\overline{\text{DSA}}$, $\overline{\text{MOB}}$, and $\overline{\text{DSB}}$ will be forced to inactive state.

(2) Pins $\overline{\text{DSKCHG}}$, $\overline{\text{RDATA}}$, $\overline{\text{WP}}$, $\overline{\text{TRAK0}}$, and $\overline{\text{INDEX}}$ will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXT2FDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

9. REAL-TIME CLOCK (RTC) AND "ON-NOW" CONTROL

The RTC with 242 bytes of RAM is a low-power device that provides a time-of-day clock in various formats, and a calendar with century register. It has two alarms and three programmable interrupts. It is also equipped with external battery backup capability for keeping time and saving RAM data under power-failure situation.

The RTC software is compatible with the MC146818 Clock chip.

The **"On-Now"** Control enables PC to be powered on by several trigger events, a telephone ring for example. Also, it allows a safely controlled power-off procedure executed in an orderly fashion.

9.1 REGISTER ADDRESS MAP

Table 9.1.1, table 9.1.2, and table 9.1.3 show the register map of RTC and **"On-Now"**. These registers are separated into three banks: Bank 0, Bank 1, and Bank 2. Bank 0 contains 10 bytes of time, calendar, and alarm A data, four bytes of control/status registers, and 114 bytes of general purpose user RAM.

TABLE 9.1.1 **- REAL TIME CLOCK ADDRESS MAP BANK 0**

ADDRESS	REGISTER TYPE	REGISTER FUNCTION
00h	R/W	Register 00h : Seconds
01h	R/W	Register 01h : Seconds Alarm A
02h	R/W	Register 02h : Minutes
03h	R/W	Register 03h : Minutes Alarm A
04h	R/W	Register 04h : Hours
05h	R/W	Register 05h : Hours Alarm A
06h	R/W	Register 06h : Day of Week
07h	R/W	Register 07h : Date of Month
08h	R/W	Register 08h: Month
09h	R/W	Register 09h : Year
0Ah	R/W	Register 0Ah : Control Register
0Bh	R/W	Register 0Bh : Control Register (Bit 0 is Read only)
0Ch	R	Register 0Ch : Status Register
0Dh	R	Register 0Dh : Status Register
0Eh-7Fh	R/W	Register 0Eh-7Fh : User RAM

In Bank 1, there are 128 bytes of general purpose user RAM, as shown in table 9.1.2.

TABLE 9.1.2 - **REAL TIME CLOCK ADDRESS MAP BANK 1**

ADDRESS	REGISTER TYPE	REGISTER FUNCTION
00h-7Fh	R/W	Register 0h-7Fh : user RAM

Bank 2 has 13 registers, 1 Century register, 8 Alarm B registers and 4 control/status registers for "**On-Now**" function.

TABLE 9.1.3 - **REAL TIME CLOCK** "ON-NOW" **ADDRESS MAP BANK 2**

ADDRESS	REGISTER TYPE	REGISTER FUNCTION
40h	R/W	Register 40h : Centuries
41h	R/W	Register 41h : Seconds Alarm B
42h	R/W	Register 42h : Minutes Alarm B
43h	R/W	Register 43h : Hours Alarm B
44h	R/W	Register 44h : Day of Week Alarm B
45h	R/W	Register 45h : Date of Month Alarm B
46h	R/W	Register 46h : Month Alarm B
47h	R/W	Register 47h : Year Alarm B
48h	R/W	Register 48h : Century Alarm B
49h	R/W	Register 49h : "On-Now" Control Register 1
4Ah	R/W	Register 4Ah : "On-Now" Control Register 2
4Bh	R	Register 4Bh : "On-Now" Status Register 3
4Ch	R/W	Register 4Ch : "On-Now" Control/Status Register 4

Time, Calendar, Alarm A, and Alarm B data Modes

REGISTER LOCATION	FUNCTION	RANGE(DATA MODE)		EXAMPLE	
		BINARY	BCD	BINARY	BCD
Register 00h	Seconds	00h-3Bh	00h-59h	1Eh	30h
Register 01h	Sec. Alarm A	00h-3Bh	00h-59h	1Eh	30h
Register 02h	Minutes	00h-3Bh	00h-59h	1Eh	30h
Register 03h	Min. Alarm A	00h-3Bh	00h-59h	1Eh	30h
Register 04h	Hours	01h-0Ch(AM)	01h-12h(AM)	08h	08h
	(12-Hour Mode)	81h-8Ch(PM)	81h-92h(PM)		
	(24-Hour Mode)	00h-17h	00h-23h	08h	08h

Time, Calendar, Alarm A, and Alarm B data Modes continued

REGISTER LOCATION	FUNCTION	RANGE(DATA MODE)		EXAMPLE	
		BINARY	BCD	BINARY	BCD

Register 05h	Hours Alarm A
	(12-Hour Mode)
	(24-Hour Mode)
		01h-0Ch(AM)
		81h-8Ch(PM)
		00h-17h
			01h-12h(AM)
			81h-92h(PM)
			00h-23h
				08h
				
				08h
					08h
					
					08h

Register 06h	Day of Week	01h-07h	01h-07h	02h	02h
Register 07h	Date of Month	01h-1Fh	01h-31h	04h	04h
Register 08h	Month	01h-0Ch	01h-12h	07h	07h
Register 09h	Year	00h-63h	00h-99h	61h	97h
Register 40h	Century	00h-63h	00h-99h	13h	19h
Register 41h	Sec. Alarm B	00h-3Bh	00h-59h	1Eh	30h
Register 42h	Min. Alarm B	00h-3Bh	00h-59h	1Eh	30h

Register 43h	Hours Alarm B
	(12-Hour Mode)
	(24-Hour Mode)
		01h-0Ch(AM)
		81h-8Ch(PM)
		00h-17h
			01h-12h(AM)
			81h-92h(PM)
			00h-23h
				08h
				
				08h
					08h
					
					08h

Register 44h	Day of Week Alarm B	01h-07h	01h-07h	02h	02h
Register 45h	Date of Month Alarm B	01h-1Fh	01h-31h	04h	04h
Register 46h	Month Alarm B	01h-0Ch	01h-12h	07h	07h
Register 47h	Year Alarm B	00h-63h	00h-99h	61h	97h
Register 48h	Century Alarm B	00h-63h	00h-99h	13h	19h

9.2 Update Cycle

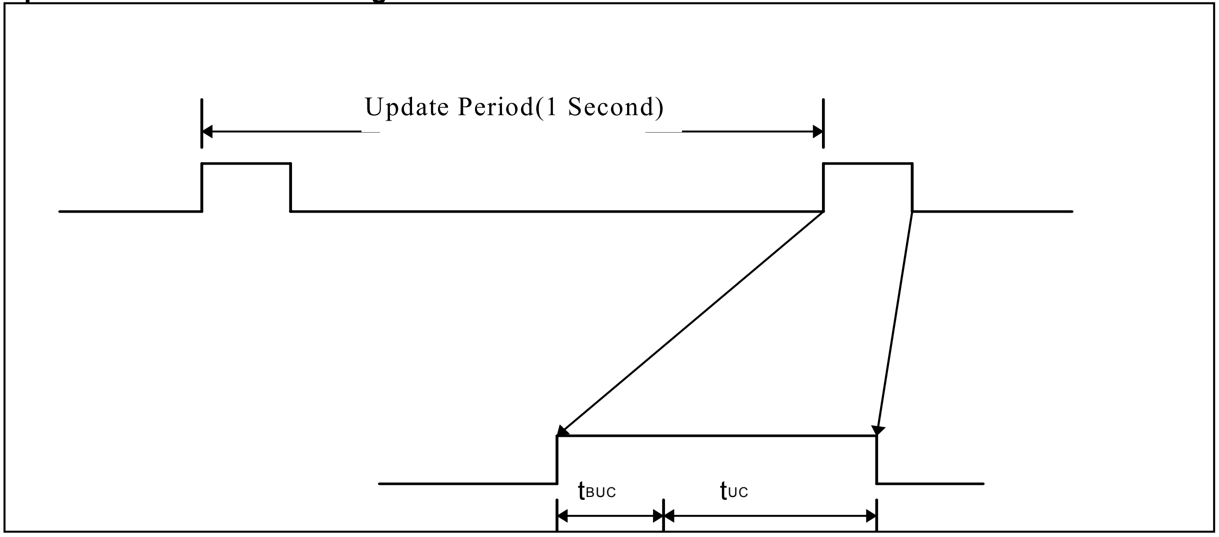
The RTC executes an update cycle once per second. It is in an update cycle when RTC updates the contents of the clock and calendar registers. In the meantime, RTC also compares each alarm byte with corresponding timer byte and generates an alarm flag if a match or a don't care condition (0C0h) is present in the alarm register.

The update-in-progress bit (UIP) in register A pulses high once per second. The update cycle occurs 244µS after the UIP bit goes high. This bit is cleared and the update-ended flag (UF) is set in the end of an update cycle.

UPDATE CYCLE TIME TABLE

UIP BIT	UPDATE CYCLE TIME (T_{UC})	BEFORE UPDATE CYCLE TIME (T_{BUC} MIN)
1	1984µS	-
0	-	244µS

Update Period and UIP Timing



9.3 REGISTERS

The RTC has four control/status registers. They are accessible at all times.

9.3.1 Register 0Ah

- All bits are unaffected by RESET.
- Register A is a read/write register except bit 7 (UIP is read only).

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP : (read only)

When UIP is 1, an update cycle is in progress. The UIP is cleared in the end of an update cycle and when the SET bit in register B is 1.

DV[2:0] : Divider Control

These three bits are used to control divider and 32KHz oscillator.

TIME-BASE FREQUENCY	DV2	DV1	DV0	OPERATION MODE	DIVIDER RESET
32.768KHZ	0	0	X	NO	-
32.768KHZ	0	1	0	YES	-
32.768KHZ	0	1	1	NO	-
32.768KHZ	1	0	X	NO	-
32.768KHZ	1	1	X	NO	YES

RS[3:0] : Periodic Interrupt Rate

PERIODIC INTERRUPT RATE TABLE

RS[3:0]	TIME BASE
0 0 0 0	None
0 0 0 1	3.90625mS / 256Hz
0 0 1 0	7.8125mS / 128Hz
0 0 1 1	122.070µS / 8.192KHz
0 1 0 0	244.141µS / 4.096KHz
0 1 0 1	488.281µS / 2.048KHz
0 1 1 0	976.562µS / 1.024KHz
0 1 1 1	1.953125mS / 512Hz
1 0 0 0	3.90625mS / 256Hz
1 0 0 1	7.8125mS / 128Hz
1 0 1 0	15.625ms / 64Hz
1 0 1 1	31.25ms / 32Hz
1 1 0 0	62.5ms / 16Hz
1 1 0 1	125ms / 8Hz
1 1 1 0	250ms / 4Hz
1 1 1 1	500ms / 2Hz

9.3.2 Register 0Bh (Read/Write)

BIT	7	6	5	4	3	2	1	0
NAME	SET	PE	AE	UE	Reserved	DM	12/24	DSE

SET

When the SET bit is set, any occurring update cycle is aborted and registers (Register 00h~09h, Register (40h~48h) may be modified without entering an update cycle. When this bit is cleared, the update cycle function occurs once per second. This bit is not affected by any other internal functions or by a RESET.

PE

A "1" on the periodic interrupt enable bit enables the periodic interrupt flag (PF) bit in Register 0Ch to assert an interrupt.

A "0" on this bit blocks the IRQ output from being driven by a periodic interrupt. This bit can not be modified by any internal function, but it may be cleared by a RESET.

AE

A "1" on the enable bit of **alarm A** enables the **alarm A** flag (AF) bit in Register 0Ch to assert an interrupt.

A "0" on this bit prohibits **alarm A** interrupt. The RESET signal clears AE to "0". This bit can not be modified by any internal function.

UE

A "1" on this bit enables the update-ended flag (UF) bit in register C to assert an interrupt.

A "0" on this bit prohibits update-ended interrupt. The UE bit is cleared by setting the SET bit or by a RESET.

DM

The data mode bit determines whether time and calendar updates are in binary format or in binary-coded-decimal (BCD) format.

A "1" on this bit means binary format.

A "0" on this bit means BCD format. This bit can not be modified by a RESET or any internal function.

24/12

A "1" on this bit selects 24-hour mode for the time-of-day function.

A "0" on this bit selects 12-hour mode. This bit can not be modified by a RESET or any internal function.

DSE

A "1" on this bit allows two special updates:

- On the last Sunday of April, the time increments from 1:59:59 AM to 3:00:00 AM.
- On the last Sunday of October, the time decrements from 1:59:59 AM to 1:00:00 AM.

A "0" on this bit disables these special updates. DSE can not be changed by any internal operation or a RESET.

(Note: RTC IRQ is ultimately controlled by Logical Device 4-CR70 and Logical Device 4-CR71. These two registers must be set properly if RTC IRQ is needed)

9.3.3 Register 0Ch (Read only)

BIT	7	6	5	4	3	2	1	0
NAME	IRQF	PF	AF	UF	0	0	0	0

IRQF

The interrupt request flag is set to a "1" if one or more of following cases are true:

PF*PE = "1"

AF*AE = "1"

UF*UE = "1"

(i.e., IRQF = PF*PE + AF*AE + UF*UE)

Any time the IRQF bit is a "1", the IRQ is asserted (provided LD4-CR70 and LD4-CR71 are set properly). All flags are cleared by reading the register or by a RESET.

PF

The periodic interrupt flag is set to "1" when a rising edge is detected on the selected tap of the divider chain(RS[3:0] of register A). PF is set to a "1" regardless of the state of PE bit. This bit is cleared by a RESET or when this register is read.

AF

A "1" on this bit indicates that the current time has reached the alarm time setting (alarm A). A RESET or a read of this register clears this bit.

UF

The update-ended interrupt flag bit is set after the end of each update cycle. This bit is cleared by a RESET or when this bit is read.

Bit 3 - Bit 0

These bits are reserved and all read "0".

9.3.4 Register D (Read only)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	VRT	0	0	0	0	0	0	0

VRT

The valid RAM and time bit. A "0" appears on this bit when the external battery is removed or at low-voltage during power-failure situation, indicating the data integrity of the real time clock, "**On-Now**" logic, and storage registers is not guaranteed. This bit can only be set by reading this register, and is not affected by a RESET.

9.4 "On-Now" Control

The **"On-Now"** Control function is built in RTC. It enables the PC to be powered on automatically from triggers of various events, and to be powered off in an orderly controlled fashion.

The **"On-Now"** works at all times even when the system power is switch-off or disconnected. It detects several external events to control system power supply On/Off properly (e.g. telephone ring, panel switch-off). It also controls the signal ($\overline{\text{PSCTRL}}$) to turn the power supply on or off.

9.5 Power-On Events

The "On-Now" Control turns on power supply when one of the following events occurs:

- Panel Switch **"turned on"**
- Telephone is ringing
- Ring-In detection signal comes from a modem
- Keyboard/Mouse is stroked/moved
- Power-wake-up input goes from high to low.
- $\overline{\text{PSCTRL}}$ active when power returns after a power-failure occurs.

(Note: Panel-Switch has a debounce circuit which is clocked by RTC 32.768KHz oscillator. The "**On-Now**" control will not function properly if this oscillator fails to work and PC can not be powered-on consequently)

9.6 Power-Off Events

- Panel Switch **"turned off"**
- Power-off under software control
- Power-failure event
- **Override Power off**: Panel switch is pushed for at least 4 seconds, then the system will be forced to turn off immediately

9.7 Registers

9.7.1 On-Now”” Register 1 (Bank2 Register 49h)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	PF	CLPOST	SPOFC	DPSCA	CLRSMI	SMIMD	PHRIDM	DPODTM

PF (Power Failure)

The PF is set when a power-failure occurs. This bit is cleared by writing a "1" to it.

CLPOST (Clear Panel-switch-off-Save Timer)

This bit is self-cleared after writing an "1" to it. If it is set, Panel-switch-off-Save timer is stopped and cleared.

SPOFC (Software Power-Off Command)

This bit is self-cleared after writing an "1" to it. If it is set, the $\overline{\text{PSCTRL}}$ goes inactive immediately.

DPSCA (Disable Power Supply Control Activation)

This bit is set as long as PF is set. When set, it disables all $\overline{\text{PSCTRL}}$ activation events except Panel-Switch- On event.

CLSMI (Clear $\overline{\text{SMI}}$)

This bit is self-cleared after writing an "1" to it. If it is set, $\overline{\text{SMI}}$ is cleared to its inactive state. This bit is used to clear $\overline{\text{SMI}}$ when SMIMD is set.

SMIMD ($\overline{\text{SMI}}$ Mode)

If it is set, $\overline{\text{SMI}}$ is level-sensitive. Once $\overline{\text{SMI}}$ goes active, it keeps active until CLSMI is set.

Writing a "0" to this bit sets $\overline{\text{SMI}}$ to be edge-triggered.

PHRIDM ($\overline{\text{PHRI}}$ Detection Mode)

A "1" on this bit sets $\overline{\text{PHRI}}$ detection mode to be on falling edge.

A "0" on this bit sets $\overline{\text{PHRI}}$ detection mode to be on a pulse train of frequency greater than 11Hz and lasts for 0.2 second.

DPODTM (Disable Power Off Delay Timer)
If set, Panel Switch Power-Off Delay Timer is stopped.
If reset, Panel Switch Power-Off Delay Timer counts down continuously.

9.7.2 On-Now_ Register 2 (Bank2 Register 4Ah)

BIT	7	6	5	4	3	2	1	0
NAME	MCLKE	KCLKE	RIBE	RIAE	PHRIE	PWAKI2E	PWAKI1E	ALARMBE

MCLKE (Mouse Clock Enable)

Logical *1* on this bit, a falling edge transition on MCLK asserts $\overline{\text{PSCTRL}}$.

KCLKE (Keyboard Clock Enable)

Logical *1* on this bit, a falling edge transition on KCLK asserts $\overline{\text{PSCTRL}}$.

RIBE (RI B Enable)

Logical *1* on this bit, a falling edge transition on $\overline{\text{RIB}}$ asserts $\overline{\text{PSCTRL}}$.

RIAE (RI A Enable)

Logical *1* on this bit, a falling edge transition on $\overline{\text{RIA}}$ asserts $\overline{\text{PSCTRL}}$.

PHRIE (PHRI Enable)

Logical *1* on this bit, a falling edge transition on $\overline{\text{PHRI}}$ asserts $\overline{\text{PSCTRL}}$.

PWAKI2E (Power Wake-up Input 2 Enable)

Logical *1* on this bit, a falling edge transition on $\overline{\text{PWAKIN2}}$ asserts $\overline{\text{PSCTRL}}$.

PWAKI1E (Power Wake-up Input 1 Enable)

Logical *1* on this bit, a falling edge transition on $\overline{\text{PWAKIN1}}$ asserts $\overline{\text{PSCTRL}}$.

ALARMBE (Alarm B Enable)

Logical *1* on this bit, the alarm B reaches its predetermined time asserts $\overline{\text{PSCTRL}}$.

9.7.3 "On-Now" Register 3 (Bank2 Register 4Bh)

BIT	7	6	5	4	3	2	1	0
NAME	PHRIST	Reserved	PSPOFD	PSPOFTD	RIBD	RIAD	PHRID	ALMBD

This register is read only except bit 5.

PHRIST ($\overline{\text{PHRI}}$ Status)

This bit holds the current value of $\overline{\text{PHRI}}$.

PSPOFD (Panel Switch Power-Off Detect)

Logical *1* on this bit, a Panel-Switch-Off event is detected.

Logical 0 on this bit, there is no Panel-Switch-Off event.

PSOFTD (Panel Switch Power-Off Delay Timer Detect)

This bit is set when Panel Switch Power-Off Delay Timer reaches its terminal count. This bit is cleared by reading this register.

RIBD (RI B Detect)

A falling edge transition on $\overline{\text{RIB}}$ asserts this bit. This bit is cleared by reading this register.

RIAD (RI A Detect)

A falling edge transition on $\overline{\text{RIA}}$ asserts this bit. This bit is cleared by reading this register.

PHRID (PHRI Detect)

A falling edge transition on $\overline{\text{PHRI}}$ asserts this bit. This bit is cleared by reading this register.

ALMBD (Alarm B Detect)

Logical *1* on this bit, the alarm B when reaching its preset time asserts this bit. This bit is cleared by reading this register.

9.7.4 "On-Now" Register 4 (Bank2 Register 4Ch)

BIT	7	6	5	4	3	2	1	0
NAME	PSOFDS1	PSOFDS0	INVSMI	Reserved	MCLKD	KCLKD	PWAKI2D	PWAKI1D

This register is read only except bits 5, 6 and 7.

PSOFDS1, PSOFDS0

These two bits decide the delay time between panel switch power off event and power supply off.

00 : 0 second.
01 : 5 seconds.
10 : 13 seconds.
11 : 21 seconds.

INVSMI

Logical *1* on this bit, nSMI is active low and goes high-Z when dis-asserted.

Logical *0* on this bit, nSMI is active high and goes high-Z when dis-asserted.

MCLKD (MCLK Detect)

A falling edge transition on $\overline{\text{MCLK}}$ asserts this bit. This bit is cleared by reading this register.

KCLKD (KCLK Detect)

A falling edge transition on $\overline{\text{KCLK}}$ asserts this bit. This bit is cleared by reading this register.

PWAKI2D (PWAKIN2 Detect)

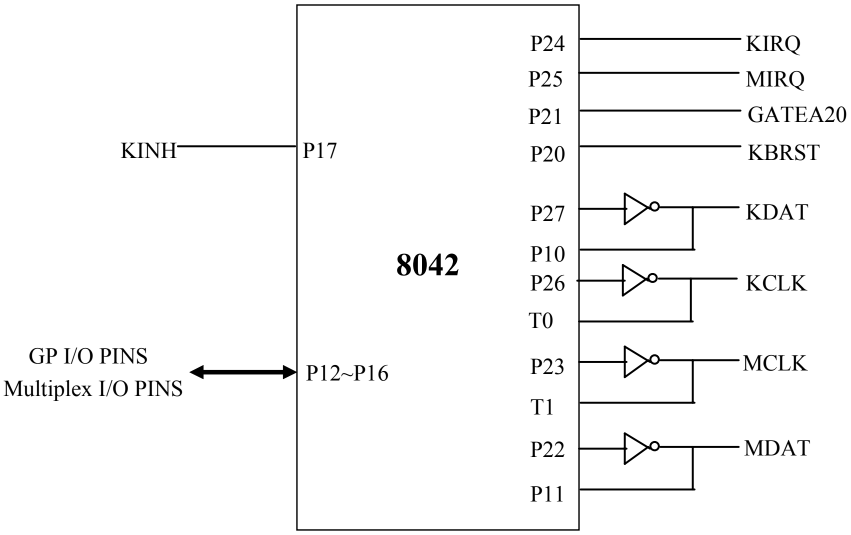
A falling edge transition on $\overline{\text{PWAKIN2}}$ asserts this bit. This bit is cleared by reading this register.

PWAKI1D (PWAKIN1 Detect)

A falling edge transition on $\overline{\text{PWAKIN1}}$ asserts this bit. This bit is cleared by reading this register.

10. KEYBOARD CONTROLLER

The KBC (8042 with licensed KB BIOS) circuit of W83977F/G, W83977AF/AG is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse, and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller will assert an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledge is received for the previous data byte.



Keyboard and Mouse Interface

10.1 Output Buffer

The output buffer is an 8-bit read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by commands to the system. The output buffer can only be read when the output buffer full bit in the register is "1".

10.2 Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60H or 64H (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60H sets a flag to indicate a data write; writing to address 64H sets a flag to indicate a command write. Data written to I/O address 60H is sent to keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit in the status register is _0_.

10.3 Status Register

The status register is an 8-bit read-only register at I/O address 64H (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63), that holds information about the status of the keyboard controller and interface. It may be read at any time.

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

10.4 Commands

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte of Keyboard Controller</td></tr>
<tr><td>60h</td><td>Write Command Byte of Keyboard Controller
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>6</td><td>IBM Keyboard Translate Mode</td></tr>
<tr><td>5</td><td>Disable Auxiliary Device</td></tr>
<tr><td>4</td><td>Disable Keyboard</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>2</td><td>System Flag</td></tr>
<tr><td>1</td><td>Enable Auxiliary Interrupt</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
</table></td></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a "0" is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>AAh</td><td>Self-test
Returns 055h if self test succeeds</td></tr>
</table>

Commands, continued

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>ABh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr>
</table></td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read Input Port(P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into STATUS register</td></tr>
<tr><td>D0h</td><td>Send Port2 value to the system</td></tr>
<tr><td>D1h</td><td>Only set/reset GateA20 line based on the system data bit 1</td></tr>
<tr><td>D2h</td><td>Send data back to the system as if it came from Keyboard</td></tr>
<tr><td>D3h</td><td>Send data back to the system as if it came from Auxiliary Device</td></tr>
<tr><td>D4h</td><td>Output next received byte of data from system to Auxiliary Device</td></tr>
<tr><td>E0h</td><td>Reports the status of the test inputs</td></tr>
<tr><td>FXh</td><td>Pulse only RC(the reset line) low for 6μS if Command byte is even</td></tr>
</table>

10.5 HARDWARE GATEA20/KEYBOARD RESET CONTROL LOGIC

The KBC implements a hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

10.5.1 KB Control Register (Logic Device 5, CR-F0)

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	Reserved	Reserved	Reserved	P92EN	HGA20	HKBRST

KCLKS1, KCLKS0

This 2 bits are for the KBC clock rate selection.

= 0 0	KBC clock input is 6 Mhz
= 0 1	KBC clock input is 8 Mhz
= 1 0	KBC clock input is 12 Mhz
= 1 1	KBC clock input is 16 Mhz

P92EN (Port 92 Enable)

A "1" on this bit enables Port 92 to control GATEA20 and KBRESET.

A "0" on this bit disables Port 92 functions.

HGA20 (Hardware GATE A20)

A "1" on this bit selects hardware GATEA20 control logic to control GATE A20 signal.

A "0" on this bit disables hardware GATEA20 control logic function.

HKBRST (Hardware Keyboard Reset)

A "1" on this bit selects hardware KB RESET control logic to control KBRESET signal.

A "0" on this bit disables hardware KB RESET control logic function.

When the KBC receives data that follows a "D1" command, the hardware control logic sets or clears GATE A20 according to the received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on the received data bit 0. When the KBC receives a "FE" command, the KBRESET is pulse low for 6µS(Min.) with 14µS(Min.) delay.

GATEA20 and KBRESET are controlled by either the software control or the hardware control logic and they are mutually exclusive. Then, GATEA20 and KBRESET are merged along with Port92 when P92EN bit is set.

10.5.2 Port 92 Control Register (Default Value = 0x24)

BIT	7	6	5	4	3	2	1	0
NAME	Res. (0)	Res. (0)	Res. (1)	Res. (0)	Res. (0)	Res. (1)	SGA20	PLKBRST

SGA20 (Special GATE A20 Control)

A "1" on this bit drives GATE A20 signal to high.

A "0" on this bit drives GATE A20 signal to low.

PLKBRST (Pull-Low KBRESET)

A "1" on this bit causes KBRESET to drive low for 6µS(Min.) with 14µS(Min.) delay. Before issuing another keyboard reset command, the bit must be cleared.

11. GENERAL PURPOSE I/O

W83977F/G, W83977AF/AG provides 14 Input/Output ports that can be individually configured to perform a simple basic I/O function or a pre-defined alternate function. Those 14 GP I/O ports are divided into two groups, the first group contains 8 ports, and the other group contains only 6 ports. Each port in the first group corresponds to a configuration register in logical device 7. Each port in the second group corresponds to a configuration register in logical device 8. Users can select those I/O ports functions by independently programming the configuration registers. Figure 8.1 and 8.2 respectively show the GP I/O port's structure of logical device 7 and device 8. Right after Power-on reset, those ports perform basic I/O functions.

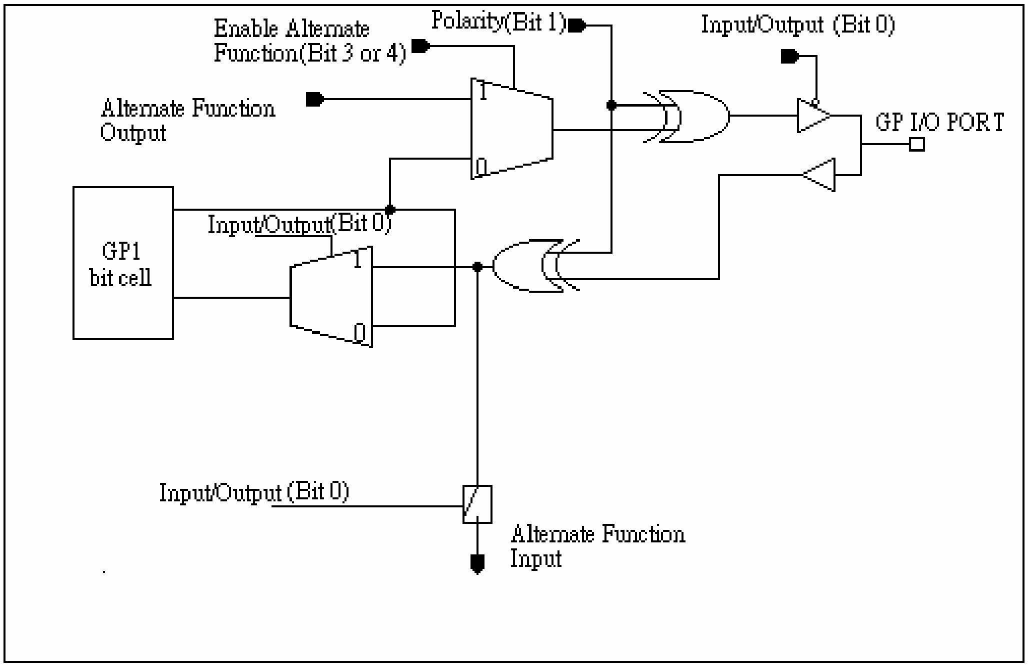


Figure 11.1

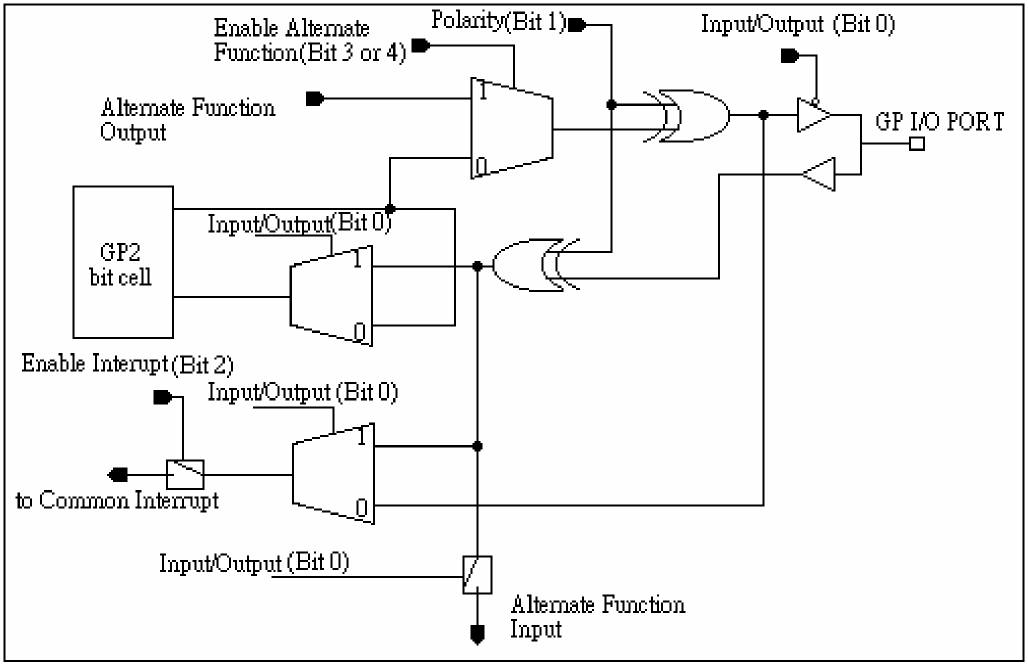


Figure 11.2

11.1 Basic I/O functions

The Basic I/O functions of W83977F/G, W83977AF/AG provide several I/O operations including driving a logic value to output port, latching a logic value from input port, inverting the input/output logic value, and steering Common Interrupt (only available in the second group of the GP I/O port). Common Interrupt is the ORed function of all interrupt channels in the second group of the GP I/O ports, and it also connects to a 1ms debounce filter which can reject a noise of 1 ms pulse width or less. There are two 8-bit registers, GP1 and GP2, which are directly connected to both groups of GP I/O ports. Each GP I/O port is represented as a bit in one of two 8-bit registers. Only 6 bits of GP2 are implemented. Table 11.1.1 shows their combinations of Basic I/O functions, and Table 11.1.2 shows the register bit assignments of GP1 and GP2.

Table 11.1.1

I/O BIT **0 = OUTPUT** **1 = INPUT**	**ENABLE INT BIT** **0 = DISABLE** **1 = ENABLE**	**POLARITY BIT** **0 = NON INVERT** **1 = INVERT**	**BASIC I/O OPERATIONS**
0	0	0	Basic non-inverting output
0	0	1	Basic inverting output
0	1	0	Non-inverted output bit value of GP2 drive to Common Interrupt
0	1	1	Inverted output bit value of GP2 drive to Common Interrupt
1	0	0	Basic non-inverting input
1	0	1	Basic inverting input
1	1	0	Non-inverted input drive to Common Interrupt
1	1	1	Inverted input drive to Common Interrupt

Table 11.1.2

GP I/O PORT ACCESSED REGISTER	**REGISTER BIT ASSIGNMENT**	**GP I/O PORT**
GP1	BIT 0	GP10
	BIT 1	GP11
	BIT 2	GP12
	BIT 3	GP13
	BIT 4	GP14
	BIT 5	GP15
	BIT 6	GP16
	BIT 7	GP17
GP2	BIT 0	GP20
	BIT 1	GP21
	BIT 2	GP22
	BIT 3	GP23
	BIT 4	GP24
	BIT 5	GP25

11.2 Alternate I/O Functions

W83977F/G, W83977AF/AG provides several alternate functions which are scattered among the GP I/O ports. Table 11.2.1 shows their assignments. Polarity bit can also be set to alter their polarity of alternate functions.

Table 11.2.1

GP I/O PORT	ALTERNATE FUNCTION
GP10	Interrupt Steering
GP11	Interrupt Steering
GP12	Watching Dog Timer Output/IRRX input
GP13	Power LED output/ IRTX output *[W83977AF only]*
GP14	General Purpose Address Decoder/ Keyboard Inhibit(P17)
GP15	General Purpose Write Strobe/ 8042 P12
GP16	Watching Dog Timer Output
GP17	Power LED output
GP20	Keyboard Reset (8042 P20)
GP21	8042 P13
GP22	8042 P14
GP23	8042 P15
GP24	8042 P16
GP25	GATE A20 (8042 P21)

11.2.1 Interrupt Steering

GP10 and GP11 can be programmed to map their own interrupt channels. The selection of IRQ channel can be done in configure registers CR70 and CR72 of logical device 7. Each interrupt channel also has its own 1 ms debounce filter that is used to reject any noise which is equal to or less than 1 ms wide.

11.2.2 Watch Dog Timer Output

Watch Dog Timer contains a one minutes resolution down counter, CRF2 of Logical Device 8, and two watch Dog control registers, WDT_CTRL0 and WDT_CTRL1 of Logical Device 8. The down counter can be programmed within the range from 1 to 255 minutes. Writing any new non-zero value to CRF2 or reset signal coming from a Mouse interrupt or Keyboard interrupt (CRF2 also contains non-zero value) will cause the Watch Dog Timer to reload and start to count down from the new value. As the counter reaches zero, (1) Watch Dog Timer time-out occurs and the bit 0 of WDT_CTRL1 will be set to logic 1; (2) Watch Dog interrupt output is asserted if the interrupt is enable in CR72 of logical device 8; and (3) Power LED starts to toggle output if the bit 3 of WDT_CTRL0 is enabled. WDT_CTRL1 also can be accessed through GP2 I/O base address + 1.

11.2.3 Power LED

The Power LED function provides 1 Hertz rate toggle pulse output with 50 percent duty cycle. Table 11.2.2 shows how to enable Power LED.

Table 11.2.2

WDT_CTRL1 BIT[1]	WDT_CTRL0 BIT[3]	WDT_CTRL1 BIT[0]	POWER LED STATE
1	X	X	1 Hertz Toggle pulse
0	0	X	Continuous high or low *
0	1	0	Continuous high or low *
0	1	1	1 Hertz Toggle pulse

* Note: Continuous high or low depends on the polarity bit of GP13 or GP17 configure registers.

11.2.4 General Purpose Address Decoder

General Purpose Address Decoder provides two address decode as AEN equal to logic 0. The address base is stored at CR62, CR63 of logical device 7. The decode output is normally active low. Users can alter its polarity through the polarity bit of the GP14's configuration register.

11.2.5 General Purpose Write Strobe

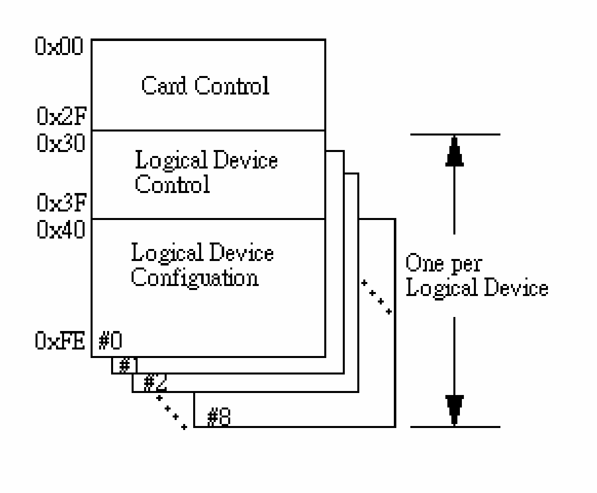
General Purpose Write Strobe is an address decoder that performs like General Purpose Address Decoder, but it has to be qualified by $\overline{\text{IOW}}$ and AEN. Its output is normally active low. Users can alter its polarity through the polarity bit of the GP15's configuration register.

12. PLUG AND PLAY CONFIGURATION

The W83977F/G, W83977AF/AG provides many configuration registers for setting up different types of configurations. There are two approaches to entering the configuration state and accessing these configuration registers, Comply PnP and Compatible PnP. The Comply PnP protocol is based on the Plug and Play ISA Specification. The Compatible PnP protocol is similar to previous Winbond I/O's protocol. The Power-On-Setting upon the Pin 51 ($\overline{\text{DTRB}}$) decides the method of entering the configuration mode. In W83977F/G, W83977AF/AG, there are nine Logical Devices (from Logical Device 0 to Logical Device 8) which correspond to nine individual functions: FDC, PRT, UART1, UART2, RTC, KBC, IR, GPIO1, GPIO2 in listed order. Each Logical Device has its own configuration registers (above CR30). Host can access those registers only after entering configuration mode.

12.1 Comply PnP

The protocol of Comply PnP is 100% compatible with the Plug and Play ISA Specification. W83977F/G, W83977AF provide built-in Plug and Play state machine to control the configuration flow. The state machine supports four states: **Wait for Key** state, **Sleep** state, **Isolation** state, and **Configure** State. According to Plug and Play ISA Specification, users can transit the four states by accessing the configuration registers, CR00 - CR07.



12.1.1 Wait for Key State

All cards enter this state after power-up reset or in response to the Reset and Wait for Key commands. No command is active in this state until the initiation key is detected on the ISA bus. The initiation key is a sequence of 32 hexadecimal number which will be shifted into LFSR (linear feedback shift register) built in W83977F/G, W83977AF/AG. The Wait for Key state is the default state for Plug and Play cards during normal system operation. After configuration and activation, software should return all cards to this state.

12.1.2 Sleep State

In this state, Plug and Play wait for a Wake[CSN] command. This command will selectively enable one or more cards to enter either the Isolation or Configure states based on the write data and the value of the CSN on each card. If the write data for the Wake[CSN] command is zero then all cards that have not been assigned a CSN will enter the Isolation state. If the write data for the Wake[CSN] command is not zero then the one card whose assigned CSN matches the parameter of the Wake[CSN] command will enter the Configure state.

12.1.3 Isolation State

In this state, Plug and Play cards respond to reads of the Serial Isolation registers according to Isolation protocol. An unique CSN is assigned after the card is isolated

12.1.4 Configure State

A card in the Configure state responds to all configuration commands including reading the card's resource configure information and programming the card's resource selections. Only one card may be in this state at a time.

12.2 Compatible PnP

12.2.1 Extended Function Registers

In Compatible PnP, there are two ways to enter Extended Function mode (which is same as Configure State in Comply PnP) and read or write the configuration registers. HEFRAS (CR26 bit 6) can be used to select one out of these two methods of entering the Extended Function mode as follows:

HEFRAS	ADDRESS AND VALUE
0	write 87h to the location 3F0h twice
1	write 87h to the location 370h twice

After Power-on reset, the value on $\overline{\text{RTSA}}$ (pin 43) is latched by HEFRAS of CR26. In Compatible PnP, a specific value (87h) must be written twice to the Extended Functions Enable Register (I/O port address 3F0h or 370h). Secondly, an index value (02h, 07h-FEh) must be written to the Extended Functions Index Register (I/O port address 3F0h or 370h same as Extended Functions Enable Register) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 3F1h or 371h).

After programming of the configuration register is finished, an additional value(AAh) should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration registers. The designer can also set bit 5 of CR26 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

12.2.2 Extended Functions Enable Registers (EFERs)

After a power-on reset, the W83977F/ AF enters the default operating mode. Before the W83977F/ AF enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 3F0h or 370h (as described in previous section).

12.2.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers (EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (02h, 07h-FEh) to access Configuration Register 0 (CR0), Configuration Register 7 (CR07) to Configuration Register FE (CRFE), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 3F0h or 370h (as described in section 12.2.1) on PC/AT systems; the EFDRs are read/write registers with port address 3F1h or 371h (as described in section 9.2.1) on PC/AT systems.

13. CONFIGURATION REGISTER

13.1 Chip (Global) Control Register

CR00 (only available in comply PnP mode)

Bit 7-0 : IORDPRA9 - IORDPRA2 --> Set RD_DATA Port A9-A2

CR01 (only available in comply PnP mode)

Bit7-0 : SISO 7-0 --> Serial Isolation

CR02 (Default 0x00)

Bit 7-3 : Reserved.
Bit 2: RSTCSN --> Reset CSN to 0. Only available in comply PnP mode.
Bit 1: RTUWAIT -- > Return to Wait for Key state. Only available in comply PnP mode.
Bit 0 : SWRST --> Soft Reset.

CR03 (only available in comply PnP mode)

Bit 7-0 : WAKCSN7 - WAKCSN0 --> Wake CSN

CR04 (only available in comply PnP mode)

Bit 7-0 : RSODAT7 - RSODAT 0 --> Resource Data

CR05 (only available in comply PnP mode)

Bit 7-1 : Reserved
Bit 0 : RSOSTAT -- > resource status bit

CR06 (only available in comply PnP mode)

Bit 7-0 : CSN7 -CSN0 --> Card Select Number 7 - 0

CR07

Bit 7-0 : LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

CR20

Bit 7-0 : DEVIDB7 - DEBIDB0 -- > Device ID Bit 7 - Bit 0 = 0x97 (read only).

CR21

Bit 7-0 : DEVREVB7 - DEBREVB0 -- > Device Rev Bit 7 - Bit 0 = 0x71 (read only).

CR22 (Default 0xff)

Bit 7-6 : Reserved.
Bit 5 : URBPWD
= 0 Power down
= 1 No Power down
Bit 4 : URAPWD
= 0 Power down
= 1 No Power down
Bit 3 : PRTPWD
= 0 Power down
= 1 No Power down
Bit 2 : IRPWD
= 0 Power down
= 1 No Power down
Bit 1 : Reserved.
Bit 0 : FDCPWD

= 0 Power down
= 1 No Power down

CR23 (Default 0x00)

Bit7-6 : Reserved
Bit 5-3 : APDTMS2 APDTMS1 APDTMS0
= 000 4 seconds count-down time of the APD mode.
= 001 8 seconds count-down time of the APD mode.
= 010 16 seconds count-down time of the APD mode.
= 011 32 seconds count-down time of the APD mode.
= 100 1 minute count-down time of the APD mode.
= 101 2 minutes count-down time of the APD mode.
= 110 4 minutes count-down time of the APD mode.
= 111 16 minutes count-down time of the APD mode.
Bit 2-0 : OSCS2, OSCS1, OSCS0.
= 000 Default power-on state after power on reset.
= 1xx Stop Clock supply to whole chip, but PLL circuit still in operation.
= 001 Stop Clock supply to whole chip and PLL circuit.
= 010 Standby for automatic power-down(APD).
= 011 Automatic power-down(APD) has been happened.

CR24 (Default 0b1ss00sss)

Bit 7 : EN16SA
= 0 12 bit Address Qualification
= 1 16 bit Address Qualification
Bit 6-5 : CLKSEL, ENPLL
= 00 The clock input on Pin 1 should be 14.31818 Mhz.
= 01 The clock input on Pin 1 should be 24 Mhz.
= 11 The clock input on Pin 1 should be 48 Mhz.
Bit 4 : RWPNPREG
= 0 Disable read/write PnP mode config registers by using the method of non-PnP mode
= 1 Enable read/write PnP mode config registers by using the method of non-PnP mode
Bit 3 : Reserved
Bit 2 : ENKBRTC
= 0 KBC and RTC are disabled after hardware reset.
= 1 KBC and RTC are active after hardware reset.
This bit is read only, and set/reset by hardware setting.
Bit 1 : ENPNP
= 0 Disable Comply PnP
= 1 Enable Comply PnP
Bit 0 : PNPCSV
= 0 The Compatible and Comply PnP has default value
= 1 The Compatible and Comply PnP has no default value

CR25 (Default 0x00)

Bit 7-6 : Reserved

Bit 5 : URBTRI
Bit 4 : URATRI
Bit 3 : PRTTRI
Bit 2 : IRTRI *[W83977AF only]*
Bit 1 : Reserved.
Bit 0 : FDCTRI.

CR26 (Default 0b0s000000)

Bit 7 : SEL4FDD
= 0 Select two FDD mode.
= 1 Select four FDD mode.
Bit 6 : HEFRAS
These two bits define how to enable Configuration mode.
HEFRAS Address and Value
= 0 Write 87h to the location 3F0h twice.
= 1 Write 87h to the location 370h twice.
Bit 5 : LOCKREG
= 0 Enable R/W Configuration Registers.
= 1 Disable R/W Configuration Registers.
Bit 4 : DSIRLGRQ *[W83977AF only]*
= 0 Enable IR legacy mode on IRQ and DRQ selection, then MCR register bit 3 is effective in selecting IRQ and DRQ.
= 1 Disable IR legacy mode on IRQ and DRQ selection, then MCR register bit 3 is not effective in selecting IRQ and DRQ.
Bit 3 : DSFDLGRQ
= 0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is effective in selecting IRQ
= 1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is not effective in selecting IRQ

Bit 2 : DSPRLGRQ
= 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ
= 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on selecting IRQ
Bit 1 : DSUALGRQ
= 0 Enable UART A legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ
= 1 Disable UART A legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ
Bit 0 : DSUBLGRQ
= 0 Enable UART B legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ
= 1 Disable UART B legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

CR28 (Default 0x00)

Bit 7-5: Reserved.
Bit 4 : IRQ Sharing selection.

= 0 Disable IRQ Sharing
= 1 Enable IRQ Sharing
Bit 3 :Reserved
Bit 2-0 : PRTMODS2 - PRTMODS0
= 0xx Parallel Port Mode
= 100 Reserved
= 101 External FDC Mode
= 110 Reserved
= 111 External two FDC Mode

CR29 *[W83977AF only]*
Bit 7-0 : CPSIDB7 - CPSIDB0 --> Comply PnP Serial ID Bit 7 - Bit 0.

CR2A (Default 0x00)
Bit 7 : PIN57S
= 0 KBRST
= 1 GP12
Bit 6 : PIN56S
= 0 GA20
= 1 GP11
Bit 5-4 : PIN40S1, PIN40S0
= 00 CIRRX *[W83977AF only]*
= 01 GP24
= 10 8042 P13
= 11 Reserved

Bit 3-2 : PIN39S1, PIN39S0
= 00 IRRXH *[W83977AF only]*
= 01 IRSL0 *[W83977AF only]*
= 10 GP25
= 11 $\overline{\text{CTSC}}$ *[W83977AF only]*
Bit 1-0 : PIN3S1, PIN3S0
= 00 DRVDEN1
= 01 GP10
= 10 8042 P12
= 11 nDSRC
CR2B (Default 0x00)
Bit 7-6 : PIN73S1, PIN73S0
= 00 PANSW
= 01 GP23
= 10 Reserved
= 11 $\overline{\text{DCDC}}$ *[W83977AF only]*
Bit 5 : PIN72S
= 0 $\overline{\text{PSCTRL}}$
= 1 GP22

Bit 4-3 : PIN70S1, PIN70S0
= 00 $\overline{\text{SMI}}$
= 01 GP21
= 10 8042 P16
= 11 $\overline{\text{RIC}}$ *[W83977AF only]*

Bit 2-1 : PIN69S1, PIN69S0
= 00 $\overline{\text{PHRI}}$
= 01 GP20
= 10 Reserved
= 11 Reserved

Bit 0 : PIN58S
= 0 KBLOCK
= 1 GP13

CR2C (Default 0x00)

Bit 7-6 : PIN121S1, PIN121S0
= 00 DRQ0
= 01 GP17
= 10 8042 P14
= 11 nDTRC *[W83977AF only]*

Bit 5-4 : PIN119S1, PIN119S0
= 00 NDACK0
= 01 GP16
= 10 8042 P15
= 11 nRTSC

Bit 3-2 : PIN104S1, PIN104S0
= 00 IRQ15
= 01 GP15
= 10 WDTO
= 11 IRSL2 *[W83977AF only]*

Bit 1-0 : PIN103S1, PIN103S0
= 00 IRQ14
= 01 GP14
= 10 PLEDO
= 11 IRSL1 *[W83977AF only]*

CR2D (Default 0x00)

Test Modes: Reserved for Winbond.

CR2E (Default 0x00)

Test Modes: Reserved for Winbond.

CR2F (Default 0x00)

Test Modes: Reserved for Winbond.

13.2 Logical Device 0 (FDC)

CR30 (Default 0x01)

Bit 7-1 : Reserved.
Bit 0 : = 1 Activates the logical device.
= 0 Logical device is inactive.

CR31

Bit 7-2 : Reserved.
Bit 1 : ENRNGCK -- > Enable I/O Range check
Bit 0 : FORIORD --> Forces LDN to respond I/O read

CR60, CR 61 (Default 0x03, 0xf0)

These two registers select FDC I/O base address [0x100:0xFF8] on 8 byte boundaries.

CR70 (Default 0x06)

Bit 7-4 : Reserved.
Bit 3-0 : These bits select IRQ resource for FDC.

CR71 (Default 0x02, read only)

Bit 7-2 : Reserved.
Bit 1 : IRQLEV -- > IRQ Level
= 1: High; = 0: Low
Bit 0 : IRQTYPE --> IRQ Type
= 1: Level trigger; = 0: Edge trigger

CR74 (Default 0x02)

Bit 7-3 : Reserved.
Bit 2-0 : These bits select DRQ resource for FDC.
= 0x00 DMA0
= 0x01 DMA1
= 0x02 DMA2
= 0x03 DMA3
= 0x04-0x07 No DMA active

CRF0 (Default 0x0E)

FDD Mode Register

Bit 7 : FIPURDWN

This bit controls the internal pull-up resistors of the FDC input pins RDATA, INDEX, TRAK0, DSKCHG, and WP.

= 0 The internal pull-up resistors of FDC are turned on.(Default)
= 1 The internal pull-up resistors of FDC are turned off.

Bit 6 : INTVERTZ

This bit determines the polarity of all FDD interface signals.

= 0 FDD interface signals are active low.
= 1 FDD interface signals are active high.

Bit 5 : DRV2EN (PS2 mode only)

When this bit is a logic 0, indicates a second drive is installed and is reflected in status register A.

Bit 4 : Swap Drive 0, 1 Mode

= 0 No Swap (Default)
= 1 Drive and Motor sel 0 and 1 are swapped.
Bit 3-2 Interface Mode
= 11 AT Mode (Default)
= 10 (Reserved)
= 01 PS/2
= 00 Model 30
Bit 1 : FDC DMA Mode
  = 0 Burst Mode is enabled
  = 1 Non-Burst Mode (Default)
Bit 0 : Floppy Mode
  = 0 Normal Floppy Mode (Default)
  = 1 Enhanced 3-Mode FDD

CRF1 (Default 0x00)

Bit 7-6 : Boot Floppy
  = 00 FDD A
  = 01 FDD B
  = 10 FDD C
  = 11 FDD D
Bit 5 : Media ID1 Polarity
= 0 Non-Inverse
= 1 Inverse
Bit 4 : Media ID0 Polarity
= 0 Non-Inverse
= 1 Inverse
Bit 3-2 : Density Select
= 00 Normal (Default)
= 01 Normal
= 10 1 (Forced to logic 1)
= 11 0 (Forced to logic 0)
Bit 1 : DISFDDWR
= 0 Enable FDD write.
= 1 Disable FDD write(forces pins WE, WD to stay high).
Bit 0 : SWWP
= 0 Normal, use WP to determine whether the FDD is write protected or not.
= 1 FDD is always write-protected.

CRF2 (Default 0xFF)

Bit 7-6 : FDD D Drive Type
Bit 5-4 : FDD C Drive Type
Bit 3-2 : FDD B Drive Type
Bit 1:0 : FDD A Drive Type

When FDD is in enhanced 3-mode(CRF0.bit0=1),these bits determine SELDEN value in TABLE A of CRF4 and CRF5 as follows.

DTYPE1	DPYTE0	DRATE1	DRATE0	SELDEN
0	0	1	1	1
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	1	X	X	0
1	0	X	X	1
1	1	0	1	0

Note: X means don't care.

CRF4 (Default 0x00)

FDD0 Selection:

Bit 7 : Reserved.

Bit 6 : Precomp. Disable.

= 1 Disable FDC Precompensation.

= 0 Enable FDC Precompensation.

Bit 5 : Reserved.

Bit 4-3 : DRTS1, DRTS0 : Data Rate Table select (Refer to TABLE A).

= 00 Select Regular drives and 2.88 format

= 01 Specifical application

= 10 2 Meg Tape

= 11 Reserved

Bit 2 : Reserved.

Bit 1:0 : DMOD0, DMOD1 : Drive Model select (Refer to TABLE B).

CRF5 (Default 0x00)

FDD1 Selection : Same as FDD0 of CRF4.

TABLE A

DRIVE RATE TABLE SELECT		DATA RATE		SELECTED DATA RATE		SELDEN
DRTS1	**DRTS0**	**DRATE1**	**DRATE0**	**MFM**	**FM**	**CRF0 BIT 0=0**
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

Note:Refer to CRF2 for SELDEN value in the cases when CRF0, bit0=1.

TABLE B

DMOD0	DMOD1	DRVDEN0(PIN 2)	DRVDEN1(PIN 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5”“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

13.3 Logical Device 1 (Parallel Port)

CR30 (Default 0x01 when PNPCSV=0 at POR)

Bit 7-1 : Reserved.

Bit 0 :

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR31

Bit 7-2 : Reserved.

Bit 1 : ENRNGCK -- > Enable I/O Range check

Bit 0 : FORIORD --> Forces LDN to respond I/O read

CR60, CR 61 (Default 0x03, 0x78 at PNPCSV=0)

These two registers select Parallel Port I/O base address.

[0x100:0xFFC] on 4 byte boundaries(EPP not supported) or

[0x100:0xFF8] on 8 byte boundaries(all modes supported, EPP is only available when the base address is on an 8byte boundary).

CR70 (Default 0x07 when PNPCSV=0 at POR)

Bit 7-4 : Reserved.

Bit [3:0] : These bits select IRQ resource for Parallel Port.

CR71 (Default 0x02, read only)

Bit 7-2 : Reserved.
Bit 1 : IRQLEV -- > IRQ Level
= 1: High; = 0: Low
Bit 0 : IRQTYPE --> IRQ Type
= 1: Level trigger; = 0: Edge trigger

CR74 (Default 0x04)

Bit 7-3 : Reserved.

Bit 2-0 : These bits select DRQ resource for Parallel Port.

0x00=DMA0

0x01=DMA1

0x02=DMA2

0x03=DMA3

0x04-0x07= No DMA active

CRF0 (Default 0x3F)

Bit 7 : PP Interrupt Type:

Not valid when the parallel port is in the printer Mode (100) or the standard & Bi-directional Mode (000).

= 1 Pulsed Low, released to high-Z .

= 0 IRQ follows nACK when parallel port in EPP Mode or [Printer, SPP, EPP] under ECP.

Bit [6:3] : ECP FIFO Threshold.

Bit 2-0 Parallel Port Mode (CR F1 PRTMODS2= logical 1)

= 100 Printer Mode (Default)

= 000 Standard and Bi-direction (SPP) mode

= 001 EPP-1.9 and SPP mode

= 101 EPP-1.7 and SPP mode

= 010 ECP mode

= 011 ECP and EPP-1.9 mode

= 111 ECP and EPP-1.7 mode.

13.4 Logical Device 2 (UART A)¢)

CR30 (Default 0x01 when PNPCSV=0 at POR)

Bit 7-1 : Reserved.

Bit 0 :

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR31

Bit 7-2 : Reserved.

Bit 1 : ENRNGCK -- > Enable I/O Range check

Bit 0 : FORIORD --> Forces LDN to respond I/O read

CR60, CR 61 (Default 0x03, 0xF8 when PNPCSV=0 at POR)

These two registers select Serial Port 1 I/O base address [0x100:0xFF8] on 8 byte boundaries.

CR70 (Default 0x04 when PNPCSV=0 at POR)

Bit 7-4 : Reserved.

Bit [3:0] : These bits select IRQ resource for Serial Port 1.

CR71(Default 0x02, read only)

Bit 7-2 : Reserved.
Bit 1 : IRQLEV -- > IRQ Level
= 1: High; = 0: Low
Bit 0 : IRQTYPE --> IRQ Type

= 1: Level trigger; = 0: Edge trigger

CRF0 (Default 0x00)

Bit 7-2 : Reserved.

Bit 1-0 : SUACLKB1, SUACLKB0

= 00 UART A clock source is 1.8462 Mhz (24MHz/13)

= 01 UART A clock source is 2 Mhz (24MHz/12)

= 10 UART A clock source is 24 Mhz (24MHz/1)

= 11 UART A clock source is 14.769 Mhz (24MHz/1.625)

13.5 Logical Device 3 (UART B)

CR30 (Default 0x01 when PNPCSV=0 at POR)

Bit 7-1 : Reserved.

Bit 0 :

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR31

Bit 7-2 : Reserved.

Bit 1 : ENRNGCK -- > Enable I/O Range check

Bit 0 : FORIORD --> Forces LDN to respond I/O read

CR60, CR 61 (Default 0x02, 0xF8 when PNPCSV=0 at POR)

These two registers select Serial Port 2 I/O base address [0x100:0xFF8] on 8 byte boundaries.

CR70 (Default 0x03 when PNPCSV=0 at POR)

Bit 7-4 : Reserved.

Bit [3:0] : These bits select IRQ resource for Serial Port 2.

CR71 (Default 0x02, read only)

Bit 7-2 : Reserved.
Bit 1 : IRQLEV -- > IRQ Level
= 1: High; = 0: Low
Bit 0 : IRQTYPE --> IRQ Type
= 1: Level trigger; 0: Edge trigger

CRF0 (Default 0x00)

Bit 7-2 : Reserved.

Bit 1-0 : SUBCLKB1, SUBCLKB0

= 00 UART B clock source is 1.8462 Mhz (24MHz/13)

= 01 UART B clock source is 2 Mhz (24MHz/12)

= 10 UART B clock source is 24 Mhz (24MHz/1)

= 11 UART B clock source is 14.769 Mhz (24MHz/1.625)

13.6 Logical Device 4 (Real Time Clock)

CR30 (Default 0x01 when PENKRC=1 at POR)

Bit 7-1 : Reserved.

Bit 0 :

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR31

Bit 7-2 : Reserved.

Bit 1 : ENRNGCK -- > Enable I/O Range check

Bit 0 : FORIORD --> Forces LDN to respond I/O read

CR60, CR 61 (Default 0x00, 0x70 when PENKRC=1 at POR)

These two registers select **Real Time Clock** I/O base address [0x100:0xFFE] on 2 byte boundaries.

CR70 (Default 0x08 when PENKRC=1 at POR)

Bit 7-4 : Reserved.

Bit [3:0] : These bits select IRQ resource for RTC.

CR71 (Default 0x00, read/write)

Bit 7-2 : Reserved.
Bit 1 : IRQLEV -- > IRQ Level
= 1: High; = 0: Low
Bit 0 : IRQTYPE --> IRQ Type

= 1: Level trigger; = 0: Edge trigger

CRF0 (Default 0x00)

RTC Mode Register

Bit 7-6 :

= 00 Select BANK0 of RAM

= 01 Select BANK1 of RAM

= 10 Select BANK2 of RAM

Bit 5-4 : Reserved.

Bit 3 : = 1 Lock CMOS RAM E0-FFh

Bit 2 : = 1 Lock CMOS RAM C0-DFh

Bit 1 : = 1 Lock CMOS RAM A0-BFh

Bit 0 : = 1 Lock CMOS RAM 80-9Fh

Note : Once set, bit[3:0] can not be cleared by a write; bit[3:0] is cleared only on Power-On Reset or upon a Hard Reset.

13.7 Logical Device 5 (KBC)

CR30 (Default 0x01 when PENKRC=1 at POR)

Bit 7-1 : Reserved.

Bit 0 :

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR31

Bit 7-2 : Reserved.

Bit 1 : ENRNGCK -- > Enables I/O Range check

Bit 0 : FORIORD --> Forces LDN to respond I/O read

CR60, CR 61 (Default 0x00, 0x60 when PENKRC=1 at POR)

These two registers select the first KBC I/O base address [0x100:0xFFF] on 1 byte boundaries.

CR62, CR 63 (Default 0x00, 0x64 when PENKRC=1 at POR)

These two registers select the second KBC I/O base address [0x100:0xFFF] on 1 byte boundaries.

CR70 (Default 0x01 when PENKRC=1 at POR)

Bit 7-4 : Reserved.

Bit [3:0] : These bits select IRQ resource for KINT(keyboard).

CR71 (Default 0x02, Read only)

Bit 7-2 : Reserved.
Bit 1 : IRQLEV -- > IRQ Level
= 1: High; = 0: Low
Bit 0 : IRQTYPE --> IRQ Type

= 1: Level trigger; = 0: Edge trigger

CR72 (Default 0x0C when PENKRC=1 at POR)

Bit 7-4 : Reserved.

Bit [3:0] : These bits select IRQ resource for MINT(PS2 Mouse)

CR73 (Default 0x02)

Bit 7-2 : Reserved.
Bit 1 : IRQLEV -- > IRQ Level
= 1: High; = 0: Low
Bit 0 : IRQTYPE --> IRQ Type

= 1: Level trigger; = 0: Edge trigger

CRF0 (Default 0x40)

Bit 7-6 : KBC clock rate selection

= 00 Select 6MHz as KBC clock input.

= 01 Select 8MHz as KBC clock input.

= 10 Select 12Mhz as KBC clock input.

= 11 Select 16Mhz as KBC clock input.

Bit 5-3 : Reserved.

Bit 2 :

= 0 Port 92 disable.

= 1 Port 92 enable.

Bit 1 :

= 0 Gate20 software control.

= 1 Gate20 hardware speed up.

Bit 0 :

= 0 KBRST software control.

= 1 KBRST hardware speed up.

13.8 Logical Device 6 (IR)

CR30 (Default 0x00)

Bit 7-1 : Reserved.

Bit 0 :

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR31

Bit 7-2 : Reserved.

Bit 1 : ENRNGCK -- > Enable I/O Range check

Bit 0 : FORIORD --> Forces LDN to respond I/O read

CR60, CR 61 (Default 0x00, 0x00)

These two registers select IR I/O base address [0x100:0xFF8] on 8 byte boundaries.

CR70 (Default 0x00)

Bit 7-4 : Reserved.

Bit [3:0] : These bits select IRQ resource for IR.

CR71 (Default 0x02, read only)

Bit 7-2 : Reserved.
Bit 1 : IRQLEV -- > IRQ Level
= 1: High; = 0: Low
Bit 0 : IRQTYPE --> IRQ Type
= 1: Level trigger; = 0: Edge trigger

CR74 (Default 0x04)

Bit 7-3 : Reserved.

Bit 2-0 : These bits select DRQ resource for RX of UART C.

= 0x00 DMA0

= 0x01 DMA1

= 0x02 DMA2

= 0x03 DMA3

= 0x04-0x07 No DMA active

CR75 (Default 0x04)

Bit 7-3 : Reserved.

Bit 2-0 : These bits select DRQ resource for TX of UART C.

= 0x00 DMA0

= 0x01 DMA1

= 0x02 DMA2

= 0x03 DMA3

= 0x04-0x07 No DMA active

CRF0 (Default 0x00)

Bit 7-4 : Reserved.

Bit 3 : RXW4C

= 0 No reception delay when SIR is changed from TX mode to RX mode.

= 1 Reception delays 4 characters-time(40 bit-time) when SIR is changed from TX mode to RX mode.

Bit 2 : TXW4C

= 0 No transmission delay when SIR is changed from RX mode to TX mode.

= 1 Transmission delays 4 characters-time(40 bit-time) when SIR is changed from RX mode to TX mode.

Bit 1 : APEDCRC

= 0 No append hardware CRC value as data in FIR/MIR mode.

= 1 Append hardware CRC value as data in FIR/MIR mode.

Bit 0 : ENBNKSEL; Bank select enable

= 0 Disable IR Bank selection.

= 1 Enable IR Bank selection.

13.9 Logical Device 7 (Auxiliary I/O Part I)

CR30 (Default 0x00)

Bit 7-1 : Reserved.

Bit 0 : = 1 Activates the logical device.

= 0 Logical device is inactive.

CR31

Bit 7-2 : Reserved.

Bit 1 : ENRNGCK -- > Enable I/O Range check

Bit 0 : FORIORD --> Forces LDN to respond I/O read

CR60, CR 61 (Default 0x00, 0x00)

These two registers select GP1 I/O base address [0x100:0xFFF] on 1 byte boundaries.

CR62, CR 63 (Default 0x00, 0x00)

These two registers select GP14 alternate function Primary I/O base address [0x100:0xFFE] on 2 byte boundaries; They are available as you setting GP14 to be an alternate function (General Purpose Address Decode).

CR64, CR 65 (Default 0x00, 0x00)

These two registers select GP15 alternate function Primary I/O base address [0x100:0xFFF] on 1 byte boundaries; They are available as you setting GP15 to be an alternate function (General Purpose Write Decode).

CR70 (Default 0x00)

Bit 7-4 : Reserved.

Bit 3-0 : These bits select IRQ resource for GP10 as you setting GP10 to be an alternate function (Interrupt Steering).

CR71 (Default 0x02, read only)

Bit 7-2 : Reserved.

Bit 1 : IRQLEV -- > IRQ Level

= 1: High; = 0: Low

Bit 0 : IRQTYPE --> IRQ Type

= 1: Level trigger; = 0: Edge trigger

CR72 (Default 0x00)

Bit 7-4 : Reserved.

Bit 3-0 : These bits select IRQ resource for GP11 as you setting GP10 to be an alternate function (Interrupt Steering).

CR73 (Default 0x02)

Bit 7-2 : Reserved.

Bit 1 : IRQLEV -- > IRQ Level

= 1: High; = 0: Low

Bit 0 : IRQTYPE --> IRQ Type

= 1: Level trigger; = 0: Edge trigger

CRE0 (GP10, Default 0x01)

Bit 7-5 : Reserved.
Bit 4 : IRQ Filter Select
= 1 Debounce Filter Enabled
= 0 Debounce Filter Bypassed
Bit 3 : Select Function.
= 1 Select Alternate Function : Interrupt Steering.
= 0 Select Basic I/O Function.
Bit 2 : Reserved.
Bit 1 : Polarity.
= 1 Invert.
= 0 No Invert.
Bit 0 : In/Out selection.
= 1 Input.
= 0 Output.

CRE1 (GP11, Default 0x01)

Bit 7-5 : Reserved.
Bit 4 : IRQ Filter Select
= 1 Debounce Filter Enabled
= 0 Debounce Filter Bypassed
Bit 3 : Select Function.
= 1 Select Alternate Function : Interrupt Steering.
= 0 Select Basic I/O Function.
Bit 2 : Reserved.
Bit 1 : Polarity.
= 1 Invert.
= 0 No Invert.
Bit 0 : In/Out selection.
= 1 Input.
= 0 Output.

CRE2 (GP12, Default 0x01)

Bit 7-5 : Reserved
Bit 4-3 : Select Function.
= 00 Select Basic I/O function.
= 01 Select 1st alternate function : Watching Dog Timer Output.
= 10 Reserved
= 11 Reserved
Bit 2 : Reserved.
Bit 1 : Polarity : 1 : Invert, 0 : No Invert
Bit 0 : In/Out : 1 : Input, 0 : Output

CRE3 (GP13, Default 0x01)

Bit 7-5 : Reserved.

Bit 4-3 : Select Function.

= 00 Select Basic I/O function.

= 01 Select 1st alternate function : Power LED output.

= 10 Reserved

= 11 Reserved

Bit 2 : Reserved.

Bit 1 : Polarity : 1 : Invert, 0 : No Invert

Bit 0 : In/Out : 1 : Input, 0 : Output

CRE4 (GP14, Default 0x01)

Bit 7-5 : Reserved.

Bit 4-3 : Select Function.

= 00 Select Basic I/O function.

= 01 Select 1st alternate function : General Purpose Address Decoder(Active Low when Bit 1 = 0, Decode two byte address).

= 10 Select 2nd alternate function : Keyboard Inhibit(P17).

= 11 Reserved

Bit 2 : Reserved.

Bit 1 : Polarity : 1 : Invert, 0 : No Invert

Bit 0 : In/Out : 1 : Input, 0 : Output

CRE5 (GP15, Default 0x01)

Bit 7-5 : Reserved.

Bit 4-3 : Select Function.

= 00 Select Basic I/O function.

= 01 General Purpose Write Strobe(Active Low when Bit 1 = 0).

= 10 8042 P12.

= 11 Reserved

Bit 2 : Reserved.

Bit 1 : Polarity : 1 : Invert, 0 : No Invert

Bit 0 : In/Out : 1 : Input, 0 : Output

CRE6 (GP16, Default 0x01)

Bit 7-5 : Reserved.

Bit 4-3 : Select Function.

= 00 Select Basic I/O function.

= 01 Select 1st alternate function : Watching Dog Timer Output.

= 1x Reserved

Bit 2 : Reserved.

Bit 1 : Polarity : 1 : Invert, 0 : No Invert

Bit 0 : In/Out : 1 : Input, 0 : Output

CRE7 (GP17, Default 0x01)

Bit 7-4 : Reserved.
Bit 4-3 : Select Function.
= 00 Select Basic I/O function.
= 01 Select 1st alternate function : Power LED output. Please refer to TABLE C
= 1x Reserved
Bit 2 : Reserved.
Bit 1 : Polarity : 1 : Invert, 0 : No Invert
Bit 0 : In/Out : 1 : Input, 0 : Output

TABLE C

WDT_CTRL1* BIT[1]*	WDT_CTRL0* BIT[3]	WDT_CTRL1 BIT[0]	POWER LED STATE
1	X	X	1 Hertz Toggle pulse
0	0	X	Continuous high or low*
0	1	0	Continuous high or low*
0	1	1	1 Hertz Toggle pulse

*Note: 1). Regarding to the contents of WDT_CTR1 and WDT_CTRL0, please refer to CRF3 and CRF4 in Logic Device 8.
2). Continuous high or low depends on the polarity bit of GP13 or GP17 configure registers.

CRF1 (Default 0x00)

General Purpose Read/Write Enable*
Bit 7-2 : Reserved
Bit 1 :
= 1 Enable General Purpose Write Strobe
= 0 Disable General Purpose Write Strobe
Bit 0 :
= 1 Enable General Purpose Address Decode
= 0 Disable General Purpose Address Decode

*Note : If the logical device activate bit is not set then bit 0 and 1 have no effect.

13.10 Logical Device 8 (Auxiliary I/O Part II)

CR30 (Default 0x00)

Bit 7-1 : Reserved.
Bit 0 :
= 1 Activates the logical device.
= 0 Logical device is inactive.

CR31

Bit 7-2 : Reserved.
Bit 1 : ENRNGCK -- > Enable I/O Range check
Bit 0 : FORIORD --> Forces LDN to respond I/O read

CR60, CR 61 (Default 0x00, 0x00)

These two registers select GP2 & Watch Dog I/O base address [0x100:0xFFE] on 2 byte boundaries. I/O base address + 1 : Watch Dog I/O base address.

CR70 (Default 0x00)

Bit 7-4 : Reserved.
Bit 3-0 : These bits select IRQ resource for Common IRQ of GP20~GP25 at Logic Device 9.

CR71 (Default 0x02)

Bit 7-2 : Reserved.
Bit 1 : IRQLEV -- > IRQ Level
= 1: High; = 0: Low
Bit 0 : IRQTYPE --> IRQ Type
= 1: Level trigger; 0: Edge trigger

CR72 (Default 0x00)

Bit 7-4 : Reserved.
Bit 3-0 : These bits select IRQ resource for Watch Dog.

CR73

Bit 7-2 : Reserved.
Bit 1 : IRQLEV -- > IRQ Level
= 1: High; = 0: Low
Bit 0 : IRQTYPE --> IRQ Type
= 1: Level trigger; = 0: Edge trigger

CRE8 (GP20, Default 0x01)

Bit 7-5 : Reserved.
Bit 4-3 : Select Function.
    = 00   Select basic I/O function
    = 01   Reserved
    = 10   Select alternate function : Keyboard Reset (connected to KBC P20)
    = 11   Reserved
Bit 2 : Int En
    = 1   Enable Common IRQ
    = 0   Disable Common IRQ
Bit 1 : Polarity : 1 : Invert, 0 : No Invert
Bit 0 : In/Out : 1 : Input, 0 : Output

CRE9 (GP21, Default 0x01)

Bit 7-5 : Reserved

Bit 4-3 : Select Function.
    = 00 Select Basic I/O function
    = 01 Reserved
    = 10 Select 2nd alternate function : Keyboard P13 I/O
    = 11 Reserved

Bit 2 : Int En
= 1 Enable Common IRQ
= 0 Disable Common IRQ

Bit 1 : Polarity : 1 : Invert, 0 : No Invert

Bit 0 : In/Out : 1 : Input, 0 : Output

CREA (GP22, Default 0x01)

Bit 7-5 : Reserved.

Bit 4-3 : Select Function.
= 00 Select Basic I/O function.
= 01 Reserved
= 10 Select 2nd alternate function : Keyboard P14 I/O.
= 11 Reserved

Bit 2 : Int En
= 1 Enable Common IRQ
= 0 Disable Common IRQ

Bit 1 : Polarity : 1 : Invert, 0 : No Invert

Bit 0 : In/Out : 1 : Input, 0 : Output

CREB (GP23, Default 0x01)

Bit 7-5 : Reserved.

Bit 4-3 : Select Function.
= 00 Select Basic I/O function
= 01 Reserved
= 10 Select 2nd alternate function : Keyboard P15 I/O
= 11 Reserved

Bit 2 : Int En
= 1 Enable Common IRQ
= 0 Disable Common IRQ

Bit 1 : Polarity : 1 : Invert, 0 : No Invert

Bit 0 : In/Out : 1 : Input, 0 : Output

CREC (GP24, Default 0x01)

Bit 7-5 : Reserved.

Bit 4-3 : Select Function.
= 00 Select Basic I/O function
= 01 Reserved
= 10 Select 2nd alternate function : Keyboard P16 I/O
= 11 Reserved

Bit 2 : Int En

= 1 Enable Common IRQ

= 0 Disable Common IRQ

Bit 1 : Polarity : 1 : Invert, 0 : No Invert

Bit 0 : In/Out : 1 : Input, 0 : Output

CRED (GP25, Default 0x01)

Bit 7-4 : Reserved.

Bit 3 : Select Function.

= 1 Select alternate function: GATE A20(Connect to KBC P21).

= 0 Select basic I/O function

Bit 2 : Int En

= 1 Enable Common IRQ

= 0 Disable Common IRQ

Bit 1 : Polarity : 1 : Invert, 0 : No Invert

Bit 0 : In/Out : 1 : Input, 0 : Output

CRF0 (Default 0x00)

Debounce Filter Enable or Disable for General Purpose I/O Combined Interrupt. The Debounce Filter can reject a pulse with 1ms width or less.

Bit 7-4 : Reserved

Bit 3 : GP Common IRQ Filter Select

= 1 Debounce Filter Enabled

= 0 Debounce Filter Bypassed

Bit 2-0 : Reserved

CRF1 (Reserved)

CRF2 (Default 0x00)

Watching Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watching Dog Counter and start to count down. If the Bit2 and Bit 1 are set, any Mouse Interrupt or Keyboard Interrupt happen will also cause to reload the non-zero value to Watching Dog Counter and count down. Read this register can not access Watching Dog Timer Time-out value, but can access the current value in Watching Dog Counter.

Bit 7-0 :

= 0x00 Time-out Disable

= 0x01 Time-out occurs after 1 minute

= 0x02 Time-out occurs after 2 minutes

= 0x03 Time-out occurs after 3 minutes

....

= 0xFF Time-out occurs after 255 minutes

CRF3 (WDT_CTRL0, Default 0x00)

Watching Dog Timer Control Register #0

Bit 7-4 : Reserved

Bit 3 : When Time-out occurs, Enable or Disable Power LED with 1 Hz and 50% duty cycle output.
= 1 Enable
= 0 Disable
Bit 2 : Mouse interrupt reset Enable or Disable
= 1 Watching Dog Timer is reset upon a Mouse interrupt
= 0 Watching Dog Timer is not affected by Mouse interrupt
Bit 1 : Keyboard interrupt reset Enable or Disable
= 1 Watching Dog Timer is reset upon a Keyboard interrupt
= 0 Watching Dog Timer is not affected by Keyboard interrupt
Bit 0 : Reserved.

CRF4 (WDT_CTRL1, Default 0x00)

Watching Dog Timer Control Register #1
Bit 7-4 : Reserved
Bit 3 : Enable the rising edge of Keyboard Reset(P20) to force Time-out event, R/W*
= 1 Enable
= 0 Disable
Bit 2 : Force Watching Dog Timer Time-out, Write only*
= 1 Force Watching Dog Timer time-out event; this bit is self-clearing.
Bit 1 : Enable Power LED 1Hz rate toggle pulse with 50% duty cycle , R/W
= 1 Enable
= 0 Disable
Bit 0 : Watching Dog Timer Status, R/W
= 1 Watching Dog Timer time-out occurred.
= 0 Watching Dog Timer counting

*Note : 1). Internal logic provides an 1us Debounce Filter to reject the width of P20 pulse less than 1us.

2). The P20 signal that coming from Debounce Filter is ORed with the signal generated by the Force Time-out bit and then connect to set the Bit 0(Watching Dog Timer Status). The ORed signal is self-clearing.

14. SPECIFICATIONS

14.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to VDD+0.5	V
RTC Battery Voltage VBAT	4.0 to 1.8	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

14.2 DC CHARACTERISTICS

(Ta = 0° C to 70° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	IBAT			2.4	uA	VBAT = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	IBAT			2.0	mA	VSB = 5.0 V, All ACPI pins are not connected.
I/O$_{8t}$ - TTL level bi-directional pin with source-sink capability of 8 mA						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	2.4			V	IOH = - 8 mA
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0V
I/O$_{6t}$ - TTL level bi-directional pin with source-sink capability of 6 mA						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 6 mA
Output High Voltage	VOH	2.4			V	IOH = - 6 mA
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0V

DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O$_8$ - CMOS level bi-directional pin with source-sink capability of 8 mA						
Input Low Voltage	VIL			0.3xVDD	V	
Input High Voltage	VIH	0.7xVDD			V	
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	3.5			V	IOH = - 8 mA
Input High Leakage	ILIH			+ 10	μA	VIN = VDD
Input Low Leakage	ILIL			- 10	μA	VIN = 0V
I/O$_{12}$ - CMOS level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	VIL			0.3xVDD	V	
Input High Voltage	VIH	0.7xVDD			V	
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	3.5			V	IOH = - 12 mA
Input High Leakage	ILIH			+ 10	μA	VIN = VDD
Input Low Leakage	ILIL			- 10	μA	VIN = 0V
I/O$_{16u}$ - CMOS level bi-directional pin with source-sink capability of 16 mA, with internal pull-up resistor						
Input Low Voltage	VIL			0.3xVDD	V	
Input High Voltage	VIH	0.7xVDD			V	
Output Low Voltage	VOL			0.4	V	IOL = 16 mA
Output High Voltage	VOH	3.5			V	IOH = - 16 mA
Input High Leakage	ILIH			+ 10	μA	VIN = VDD
Input Low Leakage	ILIL			- 10	μA	VIN = 0V
I/OD$_{16u}$ - CMOS level Open-Drain pin with source-sink capability of 16 mA, with internal pull-up resistor						
Input Low Voltage	VIL			0.3xVDD	V	
Input High Voltage	VIH	0.7xVDD			V	
Output Low Voltage	VOL			0.4	V	IOL = 16 mA
Output High Voltage	VOH	3.5			V	IOH = - 16 mA
Input High Leakage	ILIH			+ 10	μA	VIN = VDD
Input Low Leakage	ILIL			- 10	μA	VIN = 0V

DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O$_{12t}$ - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = - 12 mA
Input High Leakage	ILIH			+ 10	μA	VIN = VDD
Input Low Leakage	ILIL			- 10	μA	VIN = 0V
I/O$_{24t}$ - TTL level bi-directional pin with source-sink capability of 24 mA						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
Output High Voltage	VOH	2.4			V	IOH = - 24 mA
Input High Leakage	ILIH			+ 10	μA	VIN = VDD
Input Low Leakage	ILIL			- 10	μA	VIN = 0V
OUT$_{8t}$ - TTL level output pin with source-sink capability of 8 mA						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	2.4			V	IOH = - 8 mA
OUT$_{12t}$ - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
OD$_{12}$ - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
OD$_{24}$ - Open-drain output pin with sink capability of 24 mA						
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
IN$_{t}$ - TTL level input pin						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V

DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN$_{C}$- CMOS level input pin						
Input Low Voltage	VIL			0.3×VDD	V	
Input High Voltage	VIH	0.7×VDD			V	
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN$_{CS}$- CMOS level Schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	VDD = 5 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	VDD = 5 V
Hystersis	VTH	1.5	2		V	VDD = 5 V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN$_{CU}$ - CMOS level input pin with internal pull-up resistor						
Input Low Voltage	VIL			0.7xVDD	V	
Input High Voltage	VIH	0.7xVDD			V	
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN$_{ts}$- TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 5 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 5 V
Hystersis	VTH	0.5	1.2		V	VDD = 5 V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN$_{tsu}$- TTL level Schmitt-triggered input pin with internal pull-up resistor						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 5 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 5 V
Hystersis	VTH	0.5	1.2		V	VDD = 5 V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V

14.3 AC Characteristics

14.3.1 FDC: Data rate = 1 MB, 500 KB, 300 KB, 250 KB/sec.

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP. (NOTE 1)	MAX.	UNIT
SA9-SA0, AEN, $\overline{\text{DACK}}$, $\overline{\text{CS}}$, setup time to $\overline{\text{IOR}}$↓	TAR		25			nS
SA9-SA0, AEN, $\overline{\text{DACK}}$, hold time for $\overline{\text{IOR}}$↑	TAR		0			nS
$\overline{\text{IOR}}$ width	TRR		80			nS
Data access time from $\overline{\text{IOR}}$↓	TFD	CL = 100 pf			80	nS
Data hold from $\overline{\text{IOR}}$↓	TDH	CL = 100 pf	10			nS
SD to from $\overline{\text{IOR}}$ ↑	TDF	CL = 100 pf	10		50	nS
IRQ delay from $\overline{\text{IOR}}$↑	TRI				360/570 /675	nS
SA9-SA0, AEN, $\overline{\text{DACK}}$, setup time to $\overline{\text{IOW}}$↓	TAW		25			nS
SA9-SA0, AEN, $\overline{\text{DACK}}$, hold time for $\overline{\text{IOW}}$↑	TWA		0			nS
$\overline{\text{IOW}}$ width	TWW		60			nS
Data setup time to $\overline{\text{IOW}}$↑	TDW		60			nS
Data hold time from $\overline{\text{IOW}}$↑	TWD		0			nS
IRQ delay from $\overline{\text{IOW}}$↑	TWI				360/570 /675	nS
DRQ cycle time	TMCY		27			µS
DRQ delay time $\overline{\text{DACK}}$↓	TAM				50	nS
DRQ to $\overline{\text{DACK}}$ delay	TMA		0			nS
$\overline{\text{DACK}}$ width	TAA		260/430 /510			nS
$\overline{\text{IOR}}$ delay from DRQ	TMR		0			nS
$\overline{\text{IOW}}$ delay from DRQ	TMW		0			nS

FDC: Data rate = 1 MB, 500 KB, 300 KB, 250 KB/sec, continued.

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP. (NOTE 1)	MAX.	UNIT
$\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ response time from DRQ	TMRW			6/12 /20/24		µS
TC width	TTC		135/220 /260			nS
RESET width	TRST		1.8/3/3. 5			µS
$\overline{\text{INDEX}}$ width	TIDX		0.5/0.9 /1.0			µS
$\overline{\text{DIR}}$ setup time to $\overline{\text{STEP}}$	TDST		1.0/1.6 /2.0			µS
$\overline{\text{DIR}}$ hold time from $\overline{\text{STEP}}$	TSTD		24/40/4 8			µS
$\overline{\text{STEP}}$ pulse width	TSTP		6.8/11.5 /13.8	7/11.7 /14	7.2/11.9 /14.2	µS
$\overline{\text{STEP}}$ cycle width	TSC		Note 2	Note 2	Note 2	µS
$\overline{\text{WD}}$ pulse width	TWDD		100/185 /225	125/210 /250	150/235 /275	µS
Write precompensation	TWPC		100/138 /225	125/210 /250	150/235 /275	µS

Notes:

1. Typical values for T = 25° C and normal supply voltage.
2. Programmable from 2 mS through 32 mS in 2 mS increments.

14.3.2 UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{\text{IOR}}$ Reset Interrupt	TRINT	100 pf Loading		1	µS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from $\overline{\text{IOW}}$ to Reset interrupt	THR	100 pf Loading		175	nS
Delay from Initial $\overline{\text{IOW}}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			1/2	Baud Rate
Delay from $\overline{\text{IOR}}$ to Reset Interrupt	TIR	100 pF Loading		250	nS
Delay from $\overline{\text{IOR}}$ to Output	TMWO	100 pF Loading		200	nS
Set Interrupt Delay from Modem Input	TSIM			250	nS
Reset Interrupt Delay from $\overline{\text{IOR}}$	TRIM			250	nS
Interrupt Active Delay	TIAD	100 pF Loading		25	nS
Interrupt Inactive Delay	TIID	100 pF Loading		30	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

14.3.3 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS

14.3.4 EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOR}}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{\text{IOR}}$ Deasserted	t2	0		nS
$\overline{\text{IOR}}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{\text{IOR}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t4	40		
$\overline{\text{IOR}}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{\text{IOR}}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	μS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{\text{WRITE}}$ Deasserted to $\overline{\text{IOR}}$ Asserted	t13	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{IOR}}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		μS

14.3.5 EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{WRITE}}$ Deasserted and PD invalid	t22	0		nS

14.3.6 Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

14.3.7 ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

14.3.8 ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

14.3.9 KBC Timing Parameters

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	μS
T13	K/B Clock Period	20		μS
T14	K/B Clock Pulse Width	10		μS
T15	Data Valid Before Clock Falling (RECEIVE)	4		μS
T16	K/B ACK After Finish Receiving	20		μS
T17	RC Fast Reset Pulse Delay (8 Mhz)	2	3	μS
T18	RC Pulse Width (8 Mhz)	6		μS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		μS
T21	Input Clock Period (6–12 Mhz)	83	167	nS
T22	Duration of CLK inactive	30	50	μS
T23	Duration of CLK active	30	50	μS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	μS
T25	Time of inhibit mode	100	300	μS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	μS
T27	Duration of CLK inactive	30	50	μS
T28	Duration of CLK active	30	50	μS
T29	Time from DATA transition to falling edge of CLK	5	25	μS

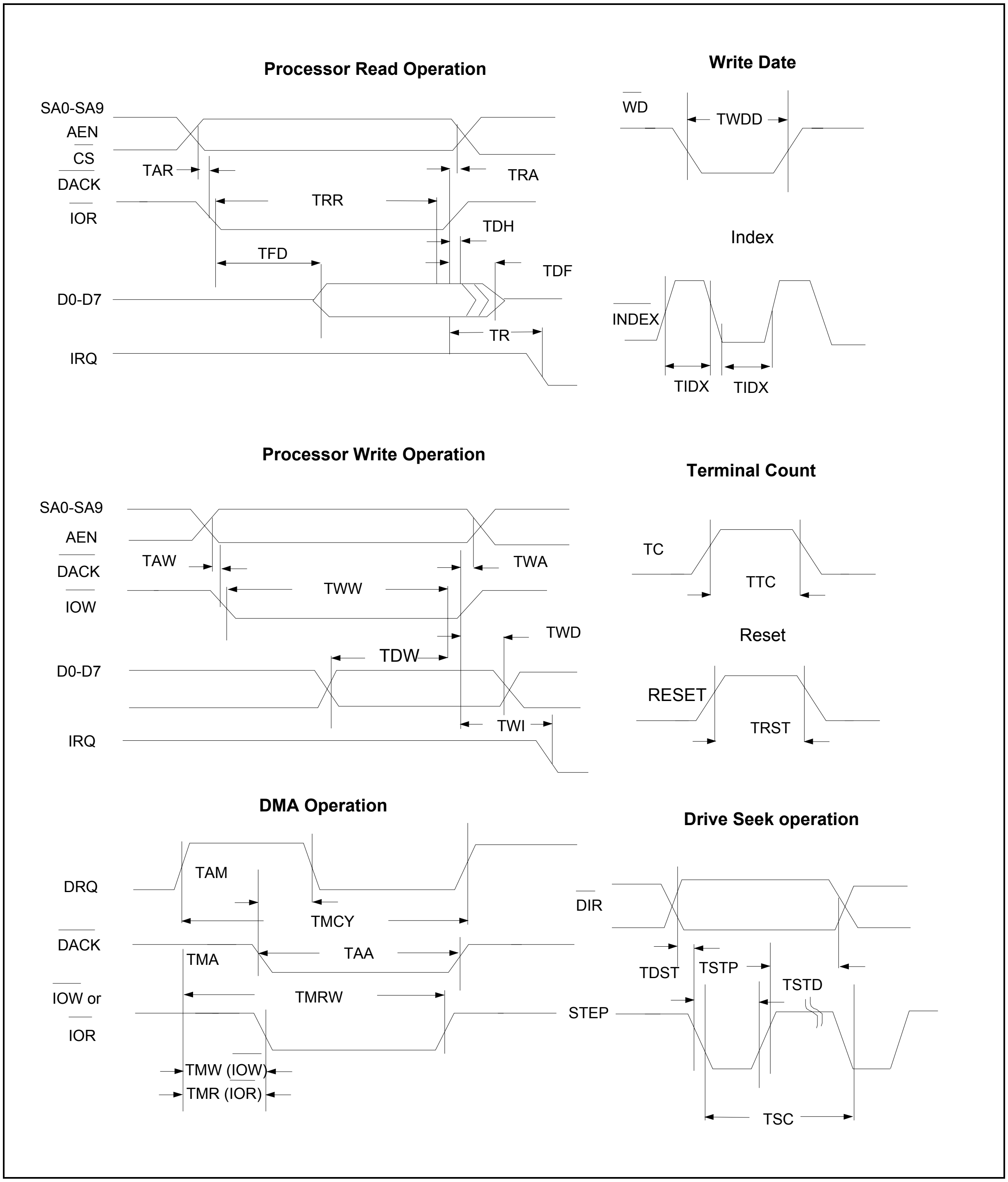
14.3.10 GPIO, ACPI, ROM Interface Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns
t_{SWP}	SWITCH pulse width	16		msec
t_{SWE}	Delay from SWITCH events to $\overline{\text{PSCTRL}}$, and from SWITCH Off event to $\overline{\text{SMI}}$	14	16	msec
t_{PORW}	$\overline{\text{SMI}}$ pulse width (edge mode)	30	90	µs
t_{POWR}	Delay from APCI Reg.1 write to $\overline{\text{SMI}}$ inactive (level mode)	-	25	nsec
t_{RIO}	Delay from $\overline{\text{RIA,B}}$ KCLK, MCLK, PWAKIN1, PWAKIN2 to $\overline{\text{PSCTRL}}$	-	25	nsec
t_{RPO}	Delay from $\overline{\text{PHRI}}$ pulse to $\overline{\text{PSCTRL}}$	-	25	sec
t_{RTO}	Delay from $\overline{\text{PHRI}}$ pulse train to $\overline{\text{PSCTRL}}$	0.125	0.190	sec
t_{RINW}	$\overline{\text{PHRI}}$ width (high and low time)	10	-	ns

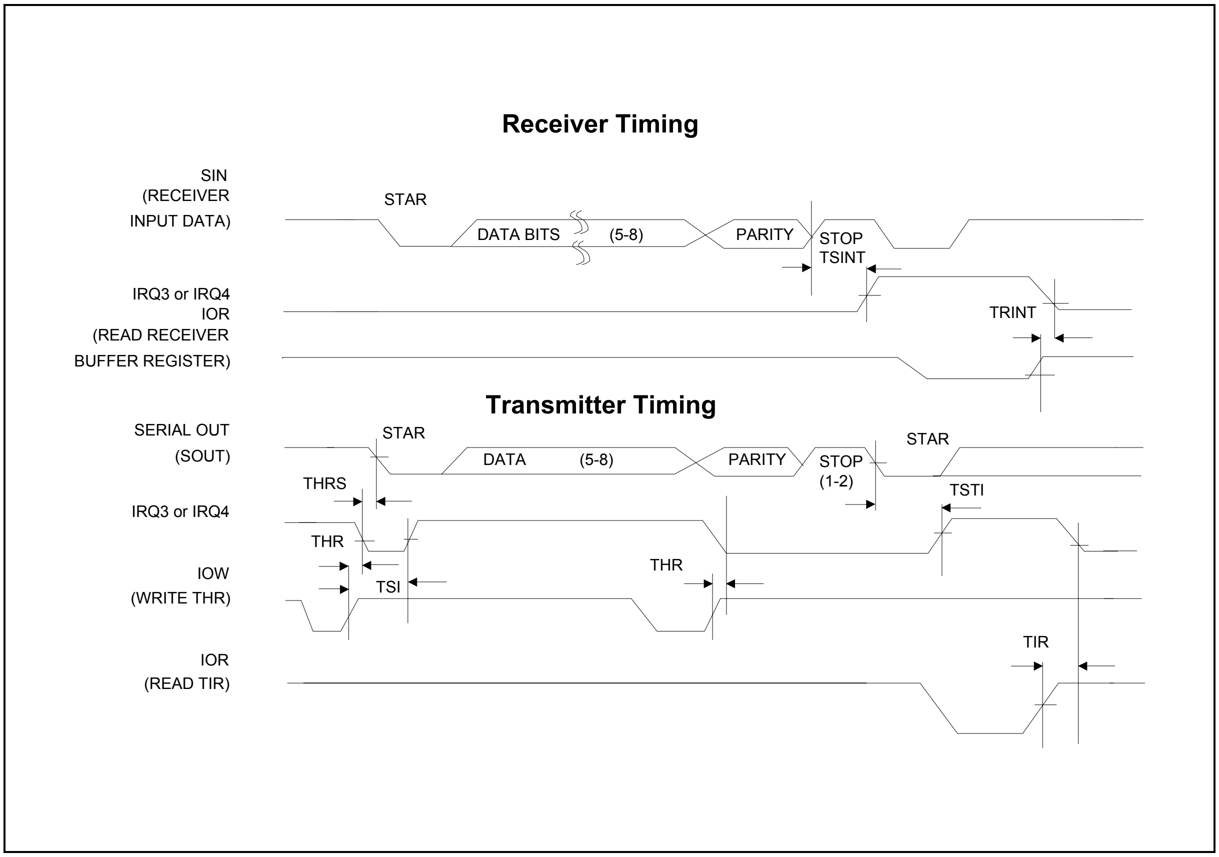
Note : Refer to Microprocessor Interface Timing for Read Timing.

15. TIMING WAVEFORMS

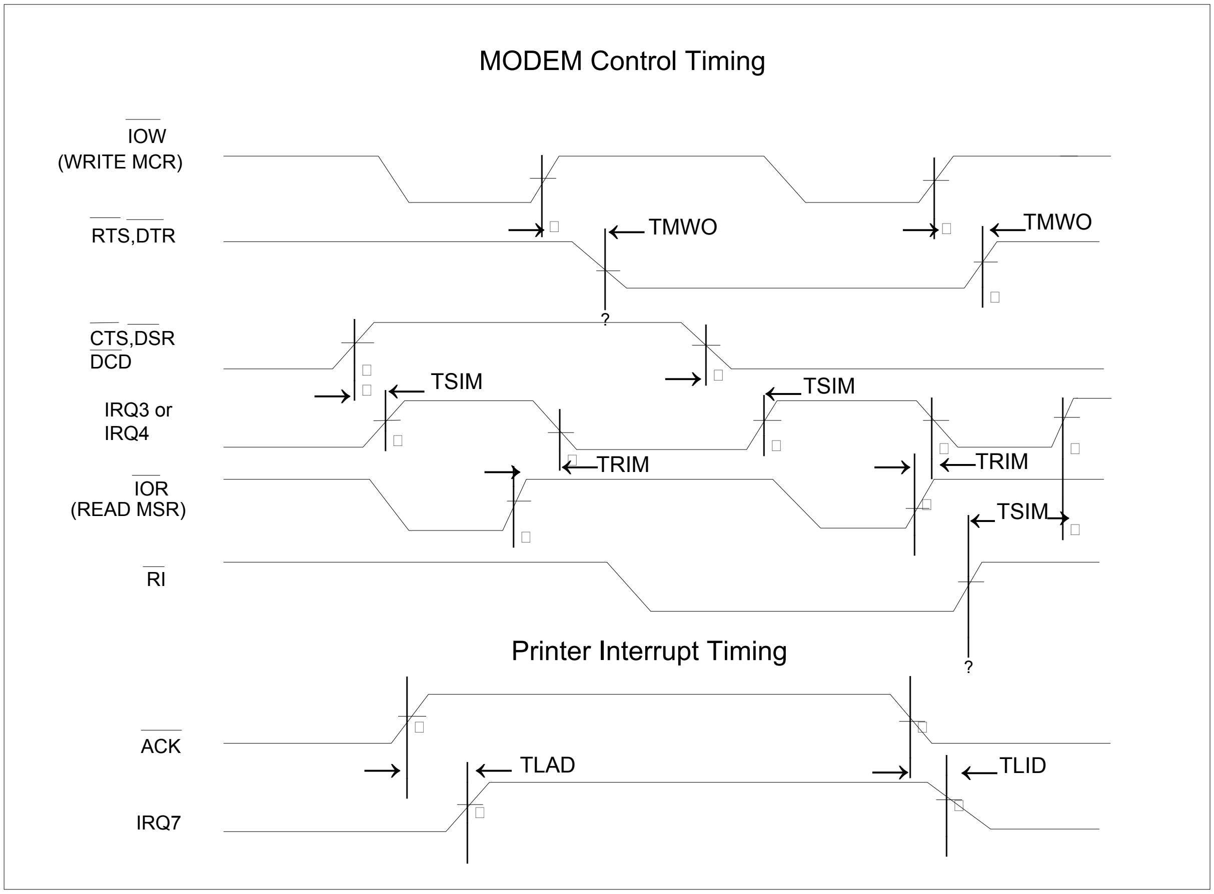
15.1 FDC



15.2 UART/Parallel

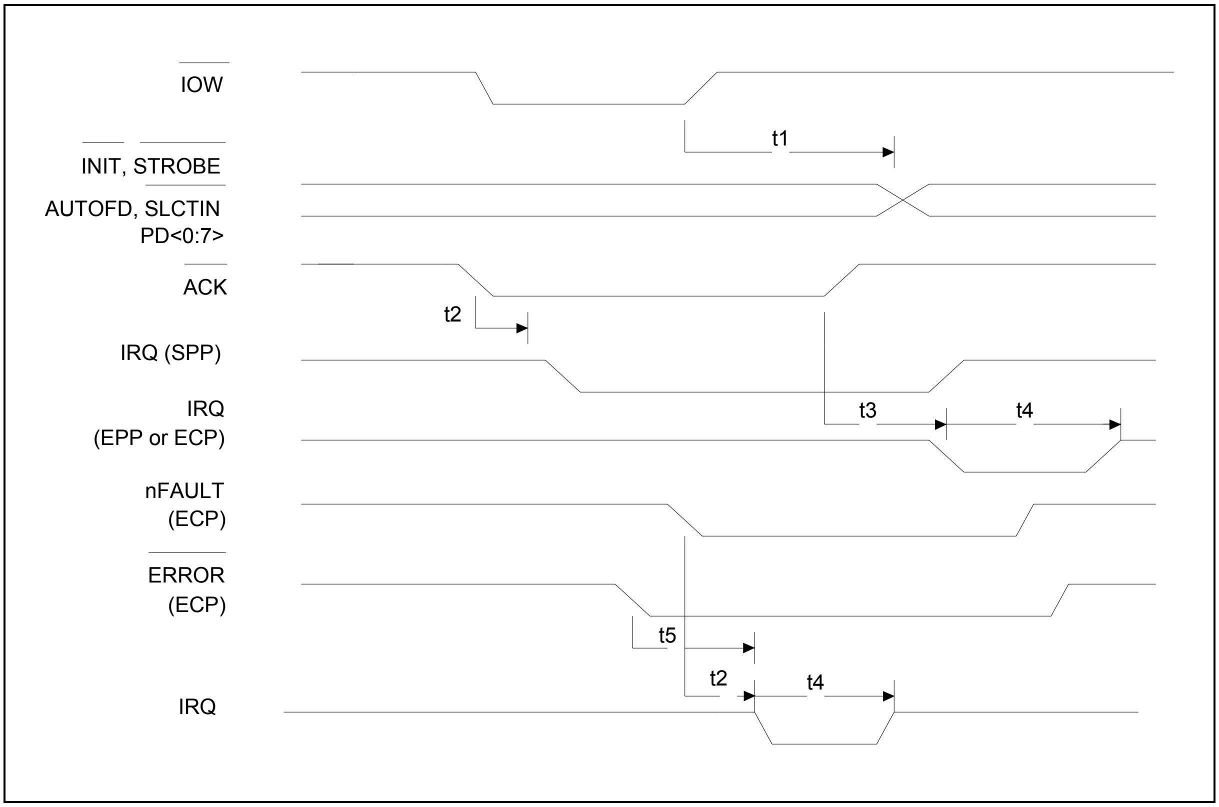


15.2.1 Modem Control Timing

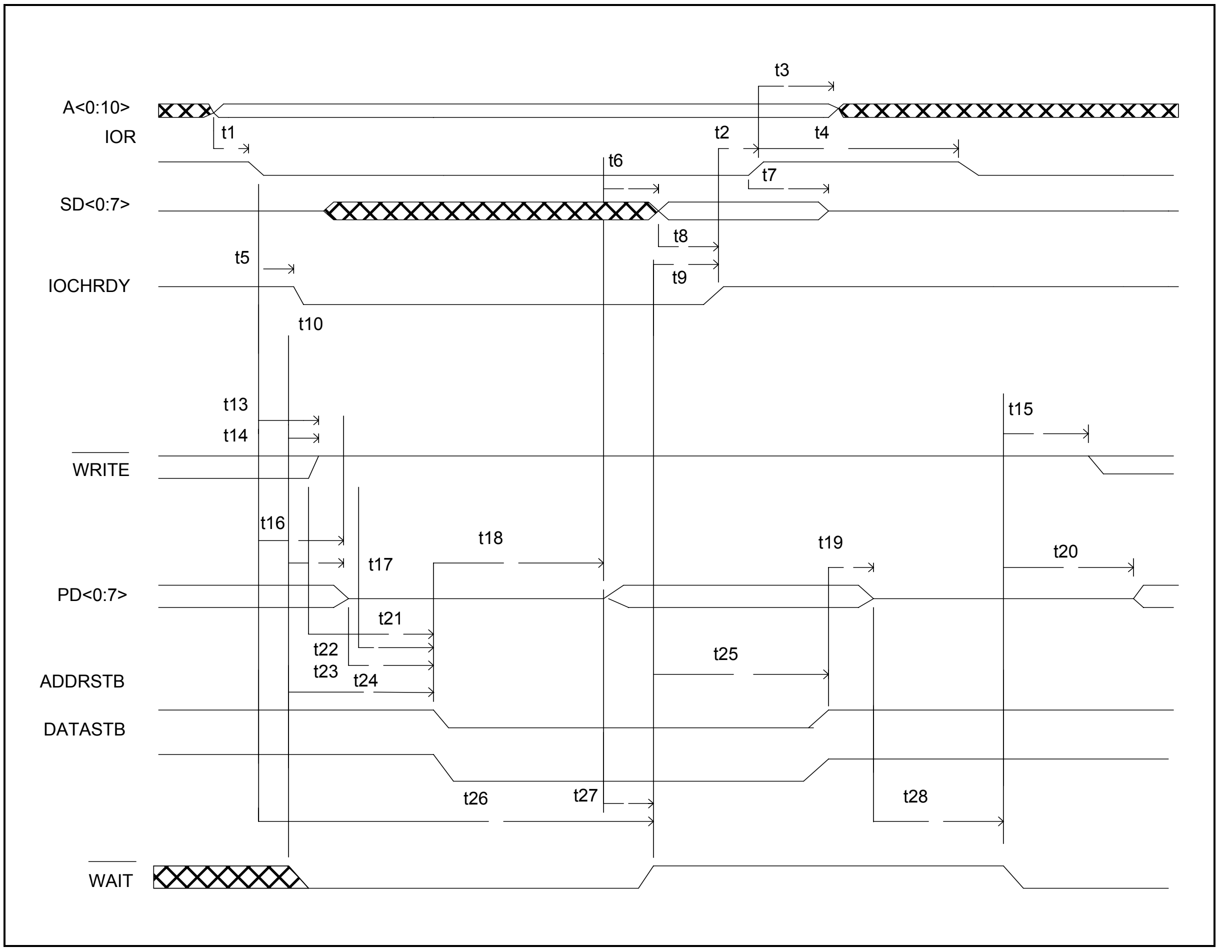


15.3 Parallel Port

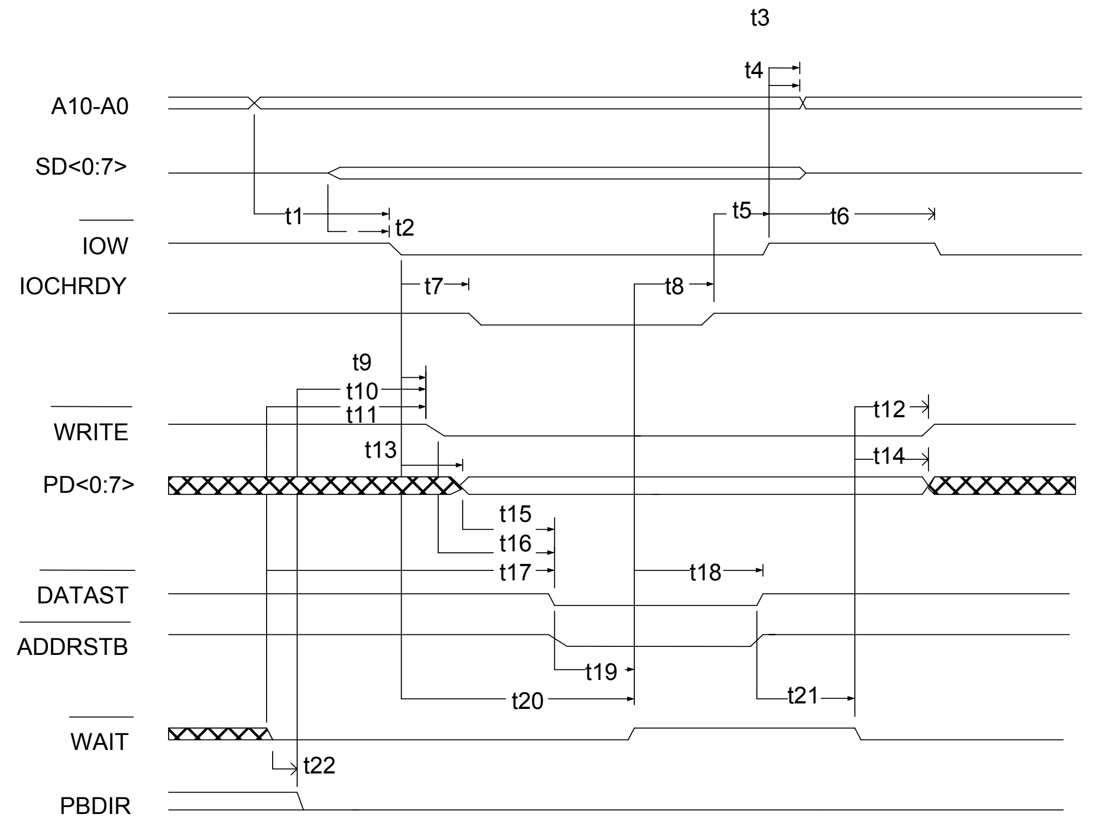
15.3.1 Parallel Port Timing



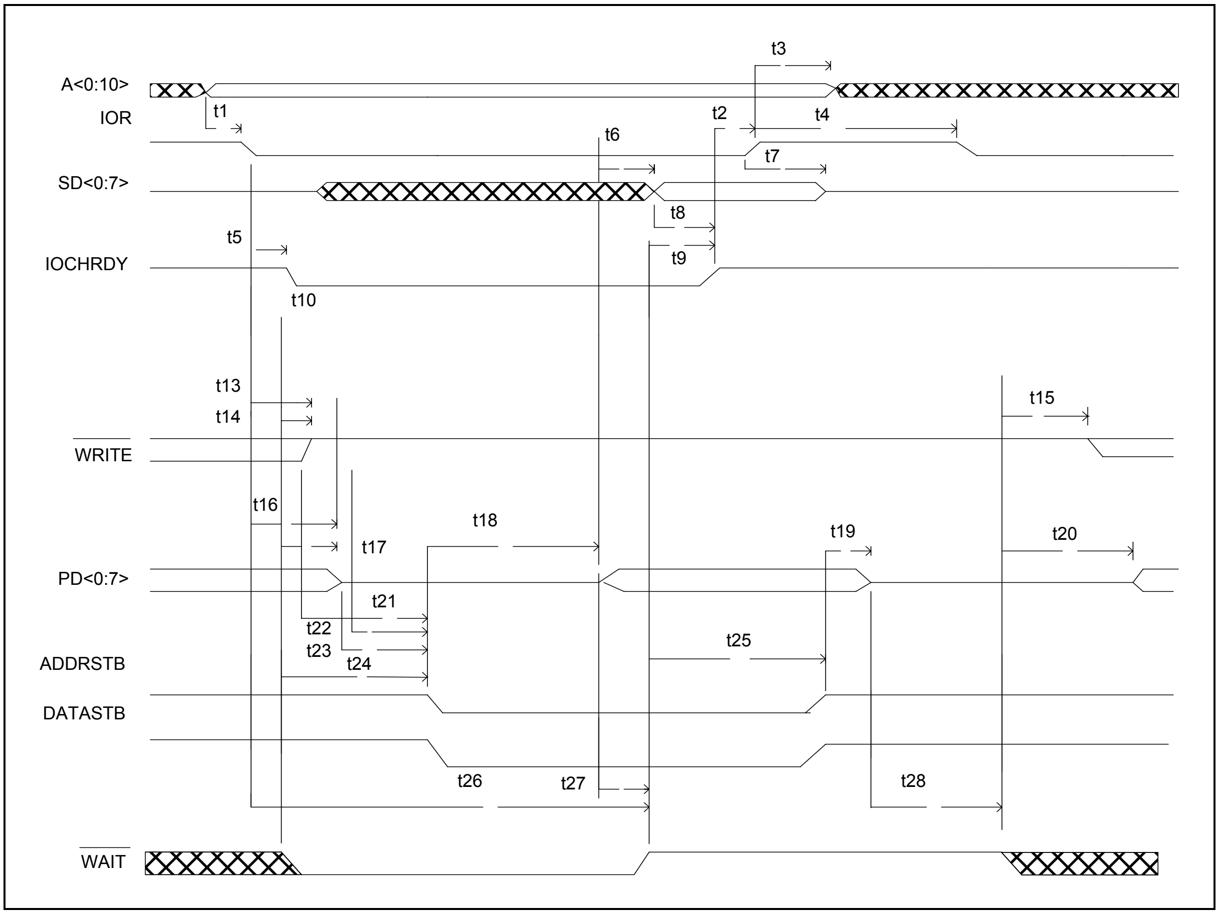
15.3.2 EPP Data or Address Read Cycle (EPP Version 1.9)



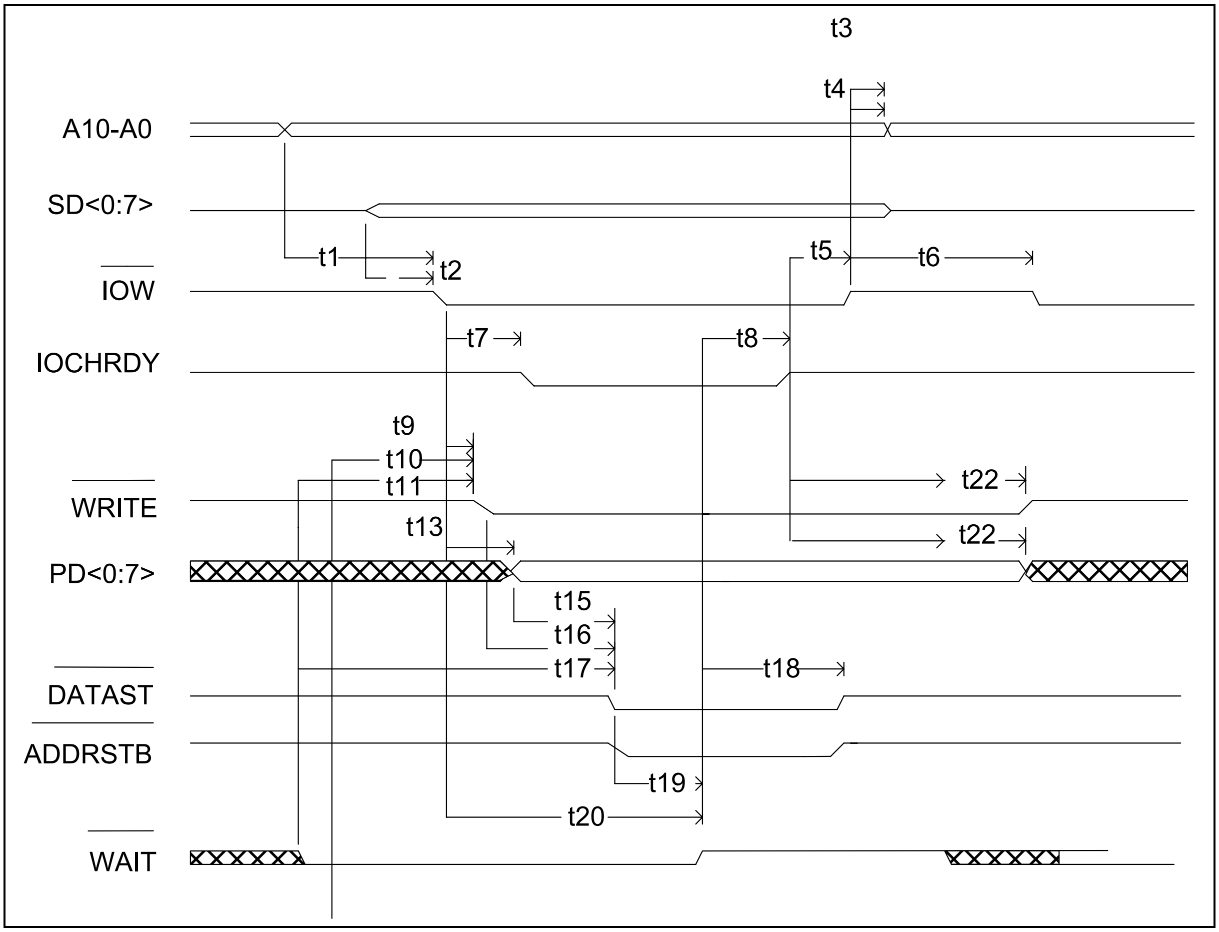
15.3.3 EPP Data or Address Write Cycle (EPP Version 1.9)



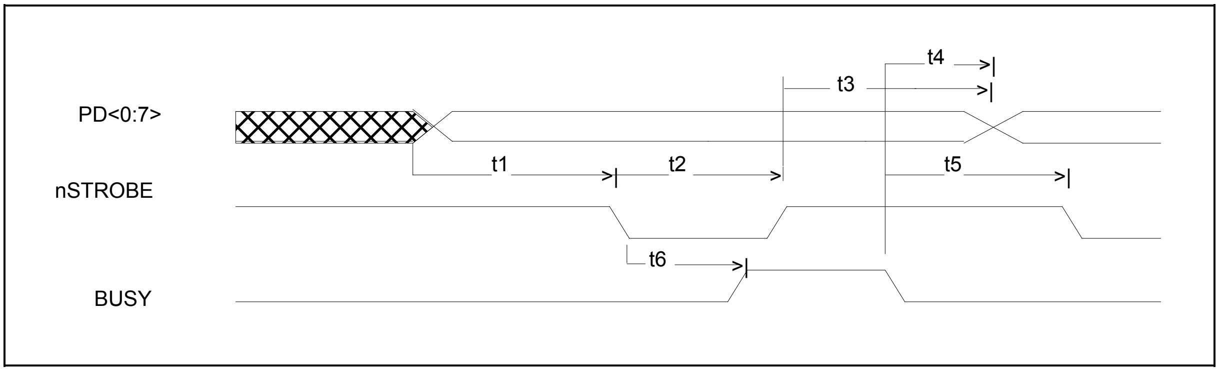
15.3.4 EPP Data or Address Read Cycle (EPP Version 1.7)



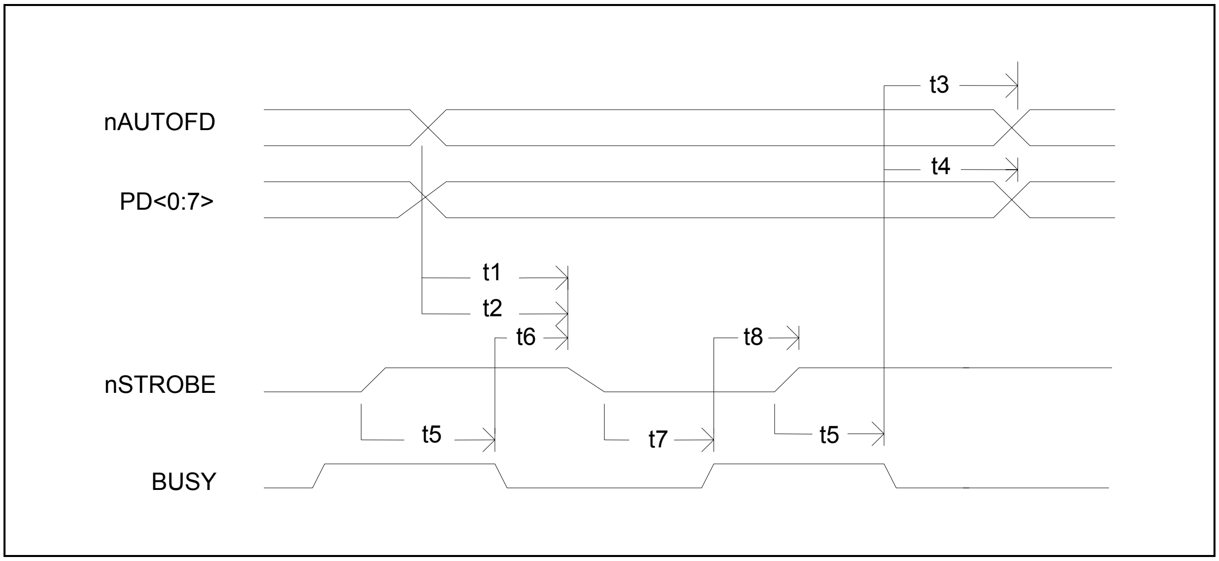
15.3.5 EPP Data or Address Write Cycle (EPP Version 1.7)



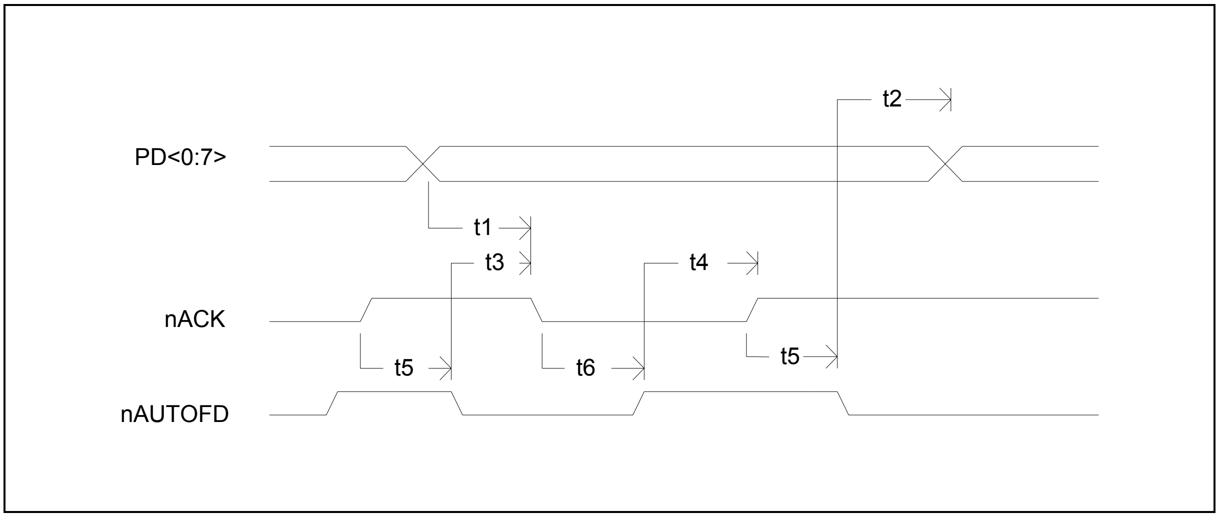
15.3.6 Parallel Port FIFO Timing



15.3.7 ECP Parallel Port Forward Timing

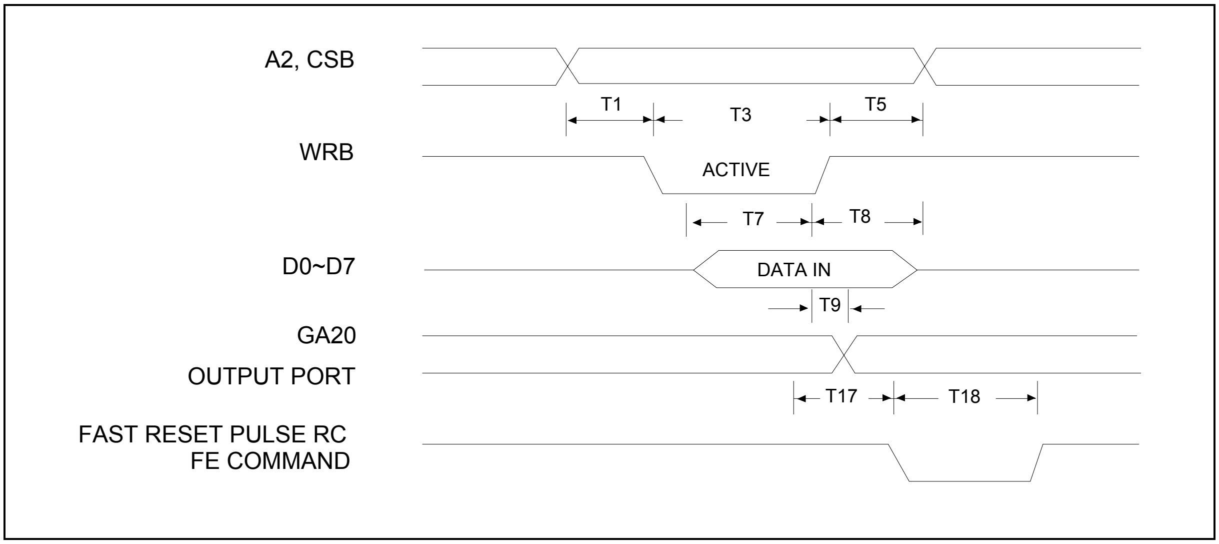


15.3.8 ECP Parallel Port Reverse Timing

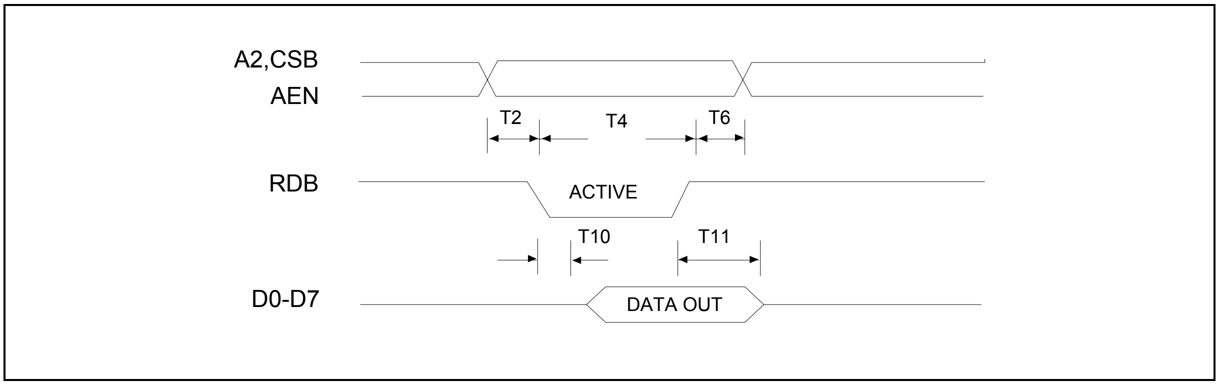


15.4 KBC

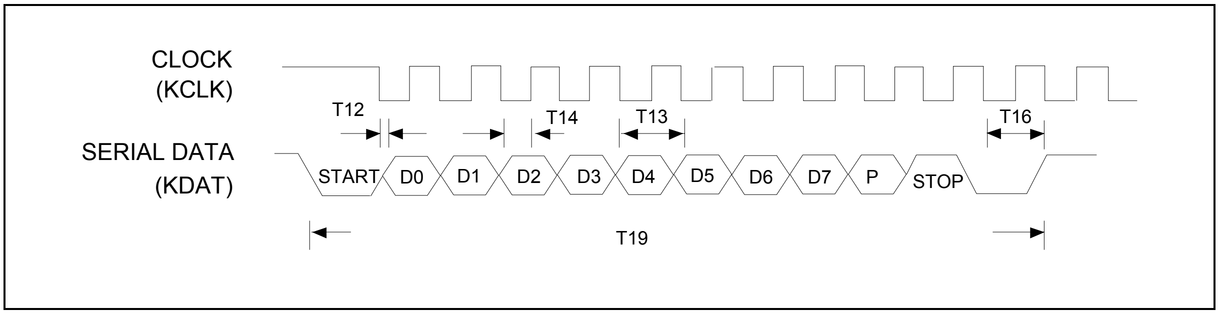
15.4.1 Write Cycle Timing



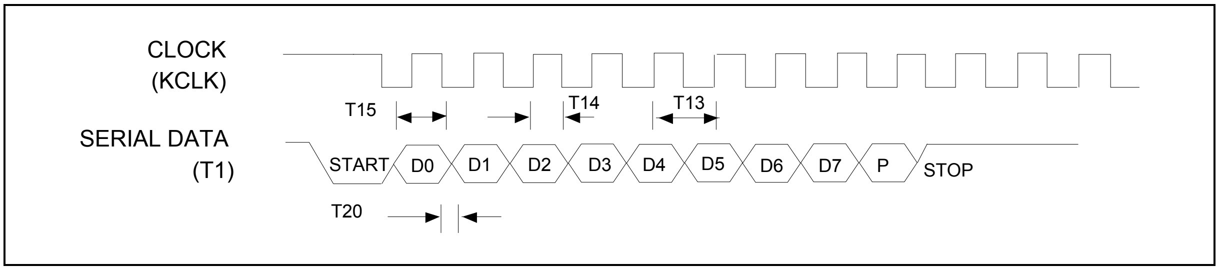
15.4.2 Read Cycle Timing



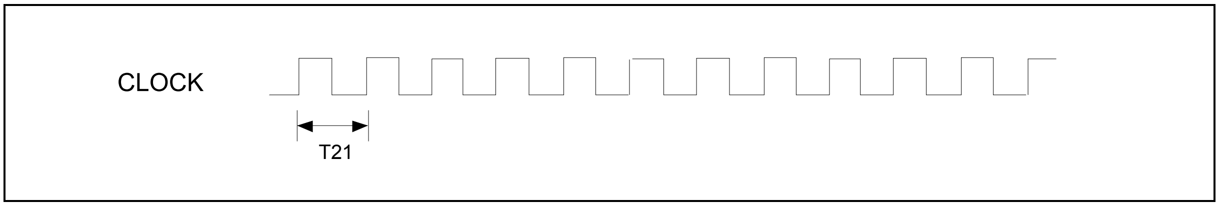
15.4.3 Send Data to K/B



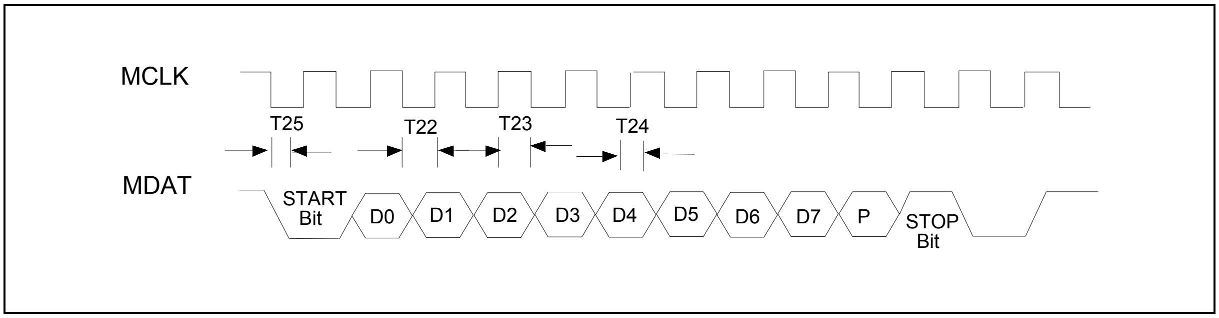
15.4.4 Receive Data from K/B



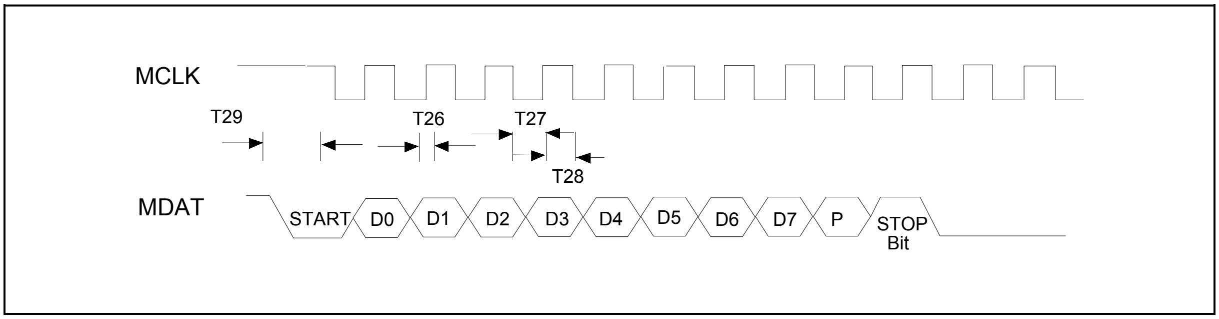
15.4.5 Input Clock



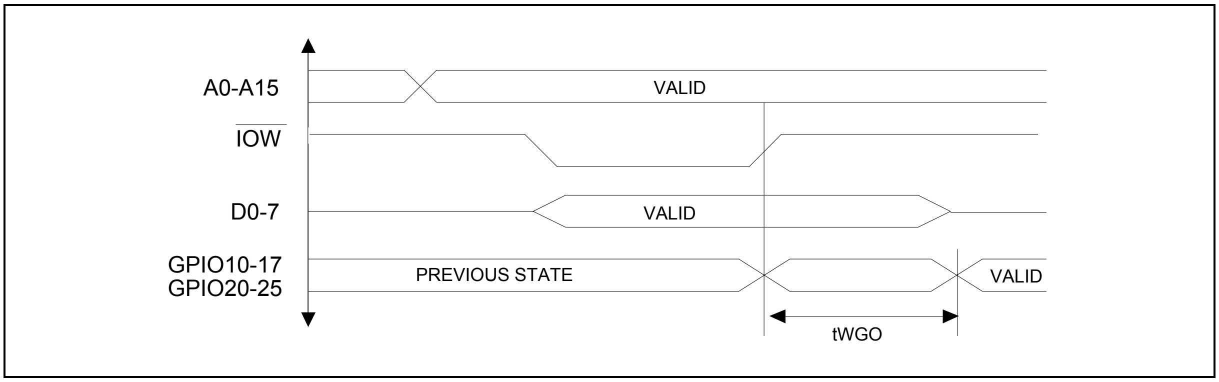
15.4.6 Send Data to Mouse



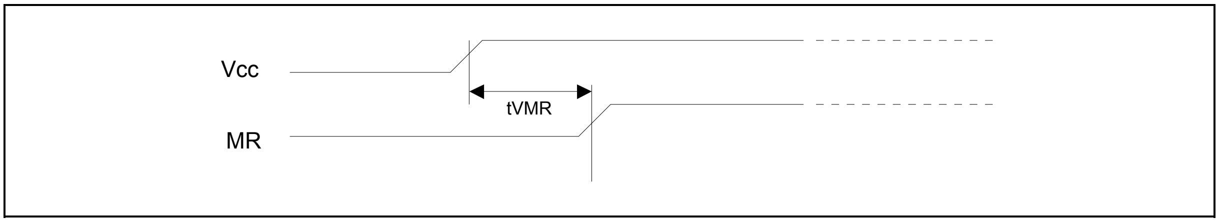
15.4.7 Receive Data from Mouse



15.5 GPIO Write Timing Diagram

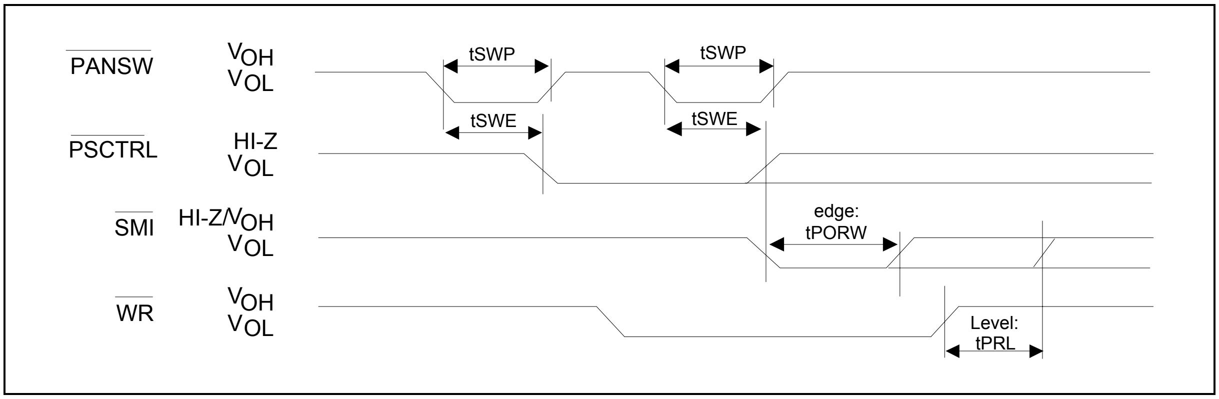


15.6 Master Reset (MR) Timing

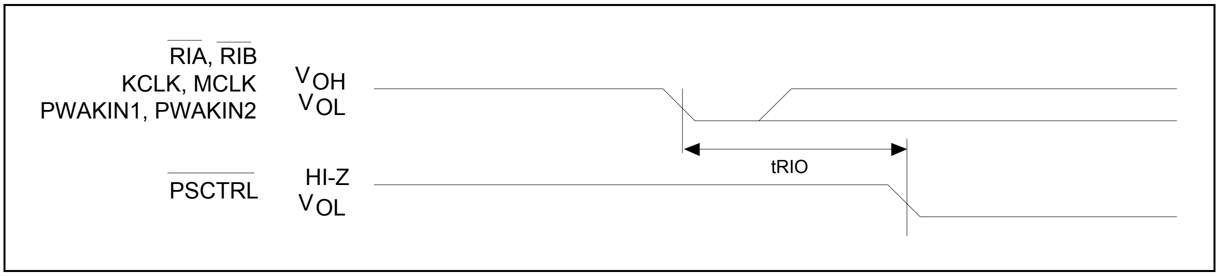


15.7 ACPI

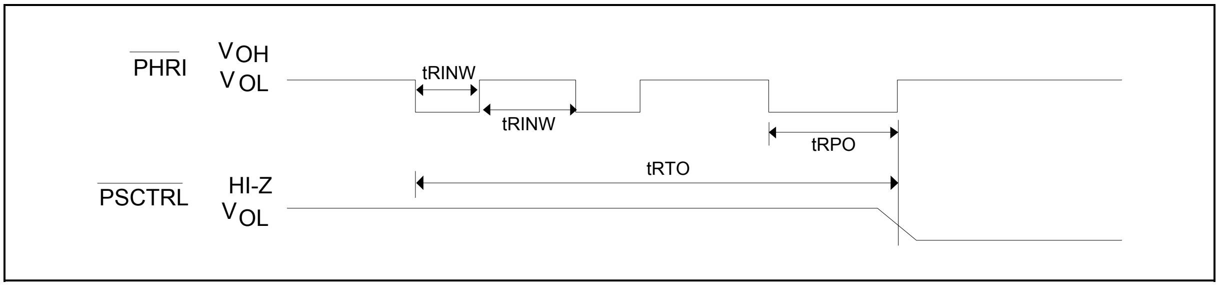
15.7.1 $\overline{PANSW}$ Trigger and $\overline{\text{PSCTRL}}$ Timing



15.7.2 $\overline{RIA}$, $\overline{RIB}$, KLCK, MCLK, PWAKIN1, PWAKIN2 Trigger and $\overline{\text{PSCTRL}}$ Timing

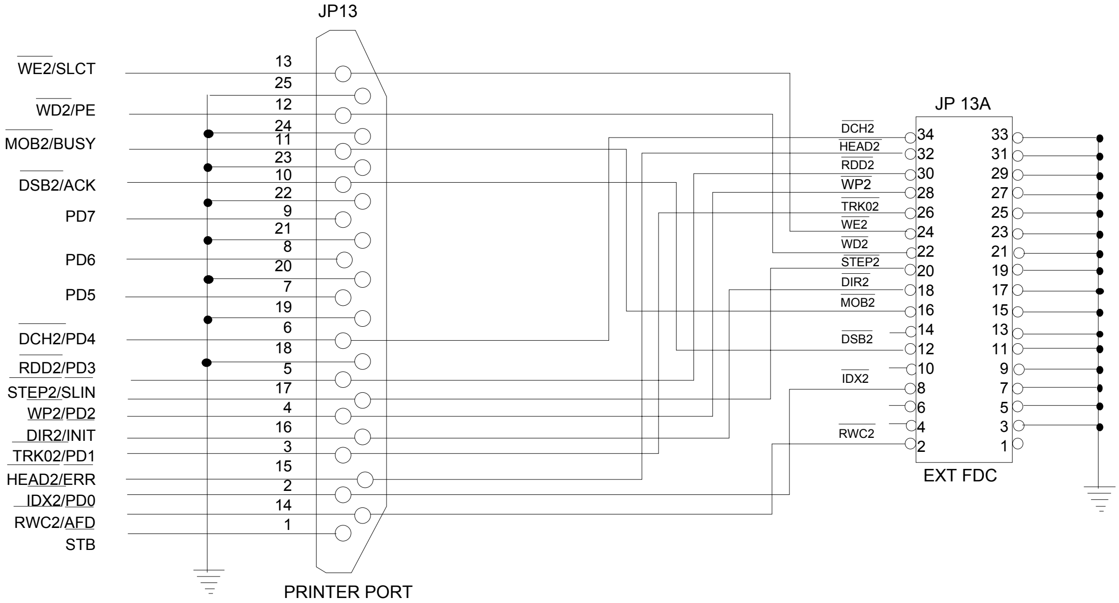


15.7.3 $\overline{PHRI}$ Trigger and $\overline{\text{PSCTRL}}$ Timing



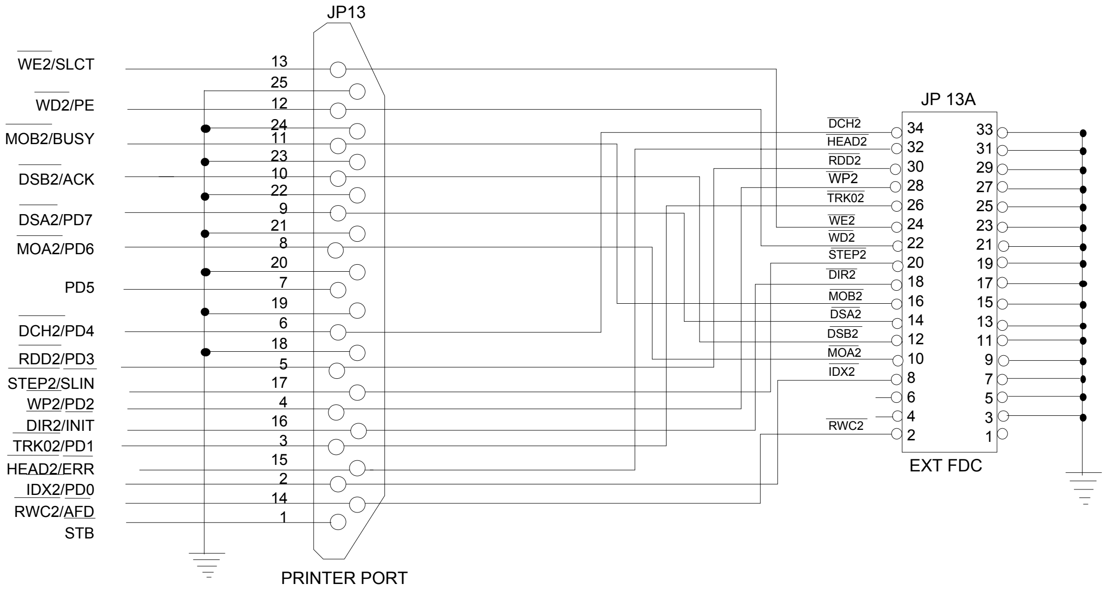
16. APPLICATION CIRCUITS

16.1 Parallel Port Extension FDD



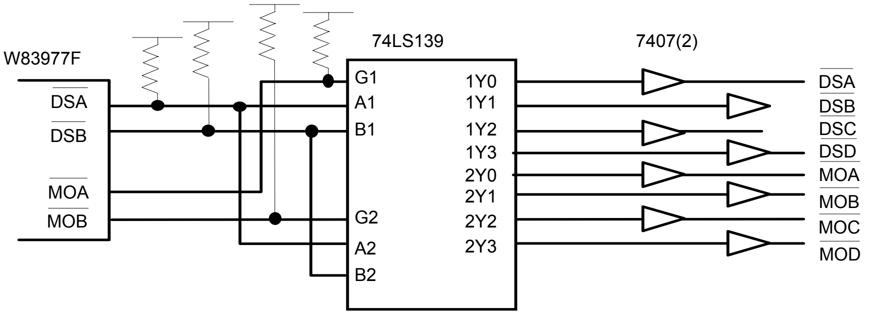
Parallel Port Extension FDD Mode Connection Diagram

16.2 Parallel Port Extension 2FDD



Parallel Port Extension 2FDD Connection Diagram

16.3 Four FDD Mode

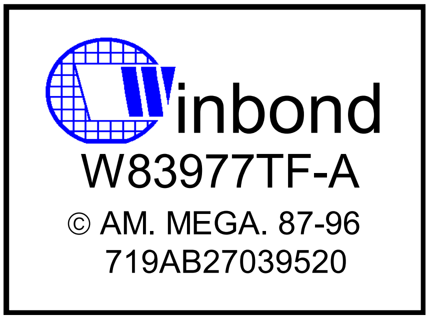


17. ORDERING INFORMATION

PART NO.	KBC FIRMWARE	REMARKS
W83977F-P	Phoenix MultiKey/42^{TM}	without FIR, 3rd UART
W83977F-A	AMIKEY-2^{TM}	without FIR, 3rd UART
W83977AF-P	Phoenix MultiKey/42^{TM}	with FIR, 3rd UART
W83977AF-A	AMIKEY-2^{TM}	with FIR, 3rd UART
W83977G-A	AMIKEY-2^{TM}	Lead-free version of W83977F-A
W83977AG-A	AMIKEY-2^{TM}	Lead-free version of W83977AF-A

18. HOW TO READ THE TOP MARKING

Example: The top marking of W83977F-A



1st line: Winbond logo

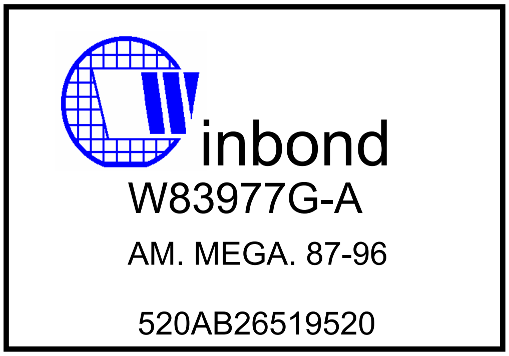
2nd line: the type number: W83977F-A

3rd line: the source of KBC F/W -- American Megatrends Incorporated™

4th line: Tracking code 719 A B 2 6519520

- **719**: packages made in '97, week 19
- **A**: assembly house ID; A means ASE, S means SPIL
- **B**: IC revision; B means version B, C means version C
- **2**: wafers manufactured in Winbond FAB 2
- **7039520**: wafer production series lot number

Example: The top marking of W83977G-A



1st line: Winbond logo

2nd line: the type number: W83977G-A

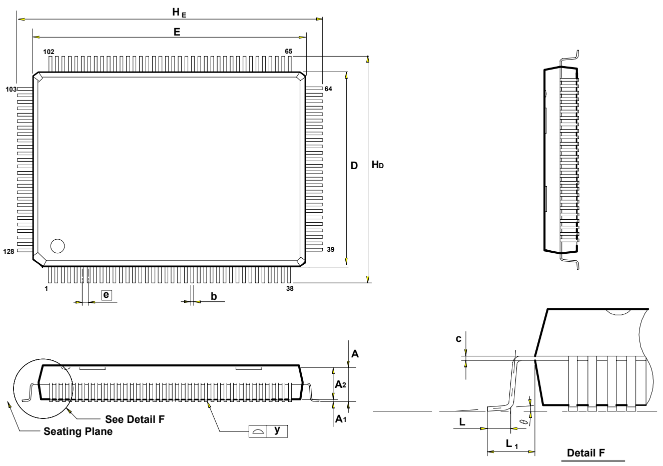
3rd line: the source of KBC F/W -- American Megatrends Incorporated™

4th line: Tracking code 709 A B 2 6519520

- **520**: packages made in '05, week 20
- **A**: assembly house ID; A means ASE, S means SPIL
- **B**: IC revision; B means version B, C means version C
- **2**: wafers manufactured in Winbond FAB 2
- **6519520**: wafer production series lot number

19. PACKAGE DIMENSIONS

(128-pin QFP)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
$\boxed{e}$	—	0.50	—	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	—	1.60	—	—	0.063	—
y	—	—	0.08	—	—	0.003
θ	0	—	7	0	—	7

Note:

1.Dimension D & E do not include interlead flash.

2.Dimension b does not include dambar protrusion/intrusion .

3.Controlling dimension : Millimeter

4.General appearance spec. should be based on final visual inspection spec.

5. PCB layout please use the "mm".

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.