

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{RRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM} MAXIMUM AT $T_J = 150\text{ }^{\circ}\text{C}$ mA
VSK.91	04	400	500	10
	06	600	700	
	08	800	900	
	10	1000	1100	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	

FORWARD CONDUCTION						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average forward current at case temperature	I _{F(AV)}	180° conduction, half sine wave			100	A
					100	°C
Maximum RMS forward current	I _{F(RMS)}	DC at 90 °C case temperature			157	A
Maximum peak, one-cycle forward, non-repetitive surge current	I _{FSM}	t = 10 ms	No voltage reappplied	Sinusoidal half wave, initial T _J = T _J maximum	2020	
		t = 8.3 ms			2110	
		t = 10 ms	100 % V _{RRM} reappplied		1700	
		t = 8.3 ms			1780	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reappplied		20.43	kA ² s
		t = 8.3 ms			18.65	
		t = 10 ms	100 % V _{RRM} reappplied		14.45	
		t = 8.3 ms			13.19	
Maximum I ² √t for fusing	I ² √t	t = 0.1 ms to 10 ms, no voltage reappplied			204.3	kA ² √s
Low level value of threshold voltage	V _{F(TO)1}	(16.7 % × π × I _{F(AV)} < I < π × I _{F(AV)}), T _J = T _J maximum			0.79	V
High level value of threshold voltage	V _{F(TO)2}	(I > π × I _{F(AV)}), T _J = T _J maximum			0.87	
Low level value of forward slope resistance	r _{f1}	(16.7 % × π × I _{F(AV)} < I < π × I _{F(AV)}), T _J = T _J maximum			1.78	mΩ
High level value of forward slope resistance	r _{f2}	(I > π × I _{F(AV)}), T _J = T _J maximum			1.57	
Maximum forward voltage drop	V _{FM}	I _{FM} = π × I _{F(AV)} , T _J = 25 °C, t _p = 400 μs square wave			1.45	V

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse leakage current	I_{RRM}	$T_J = 150\text{ }^{\circ}\text{C}$	10	mA
RMS insulation voltage	V_{INS}	50 Hz, circuit to base, all terminals shorted	3500 (1 s)	V

**THERMAL AND MECHANICAL SPECIFICATIONS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating and storage temperature range	T_J, T_{Stg}		- 40 to 150	°C
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.35	K/W
Typical thermal resistance, case to heatsink	R_{thCS}	Mounting surface flat, smooth and greased	0.1	
Mounting torque $\pm 10\%$ to heatsink busbar		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.	5	Nm
			4	
Approximate weight			110	g
			4	oz.
Case style		JEDEC	ADD-A-PAK (TO-240AA)	

 ΔR CONDUCTION PER JUNCTION

DEVICES	SINE HALF WAVE CONDUCTION					RECTANGULAR WAVE CONDUCTION					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSK.91	0.052	0.064	0.082	0.112	0.164	0.043	0.069	0.088	0.115	0.165	°C/W

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

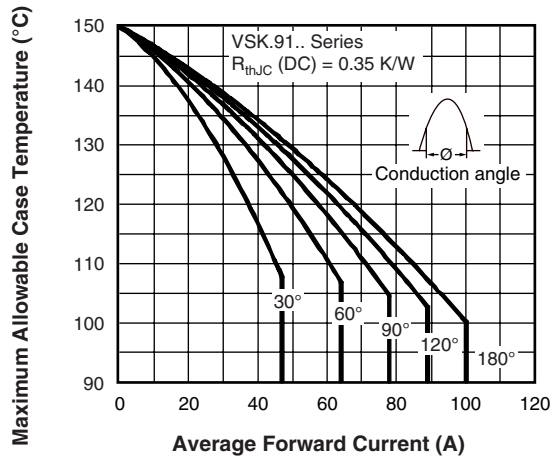


Fig. 1 - Current Ratings Characteristics

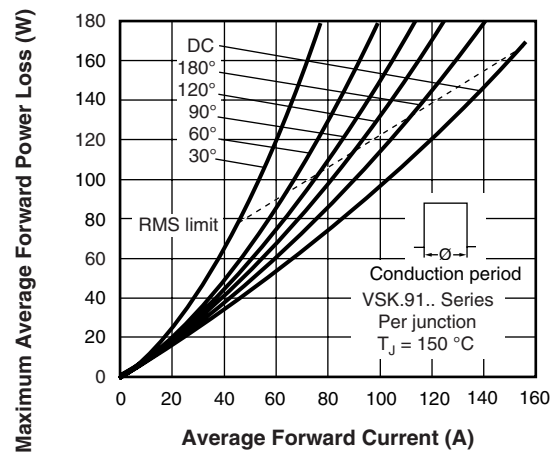


Fig. 4 - Forward Power Loss Characteristics

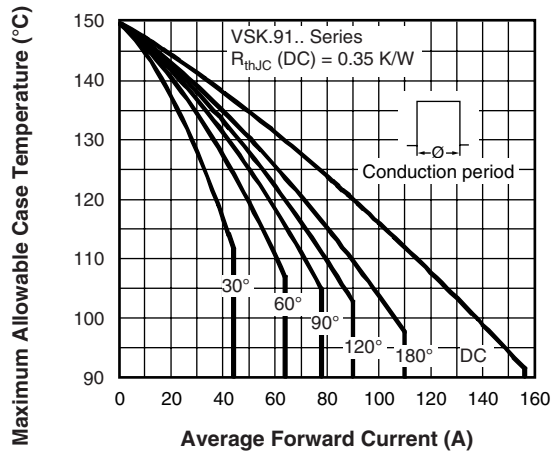


Fig. 2 - Current Ratings Characteristics

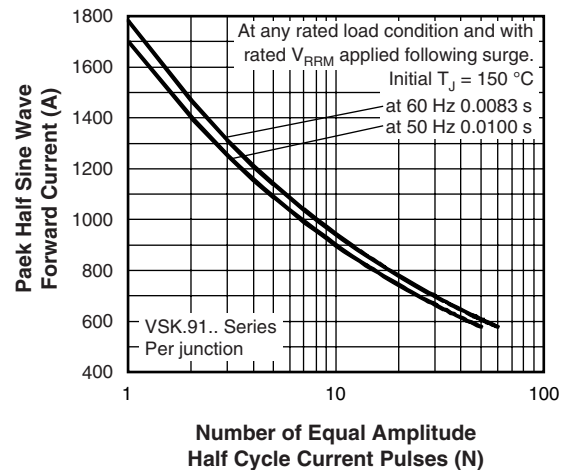


Fig. 5 - Maximum Non-Repetitive Surge Current

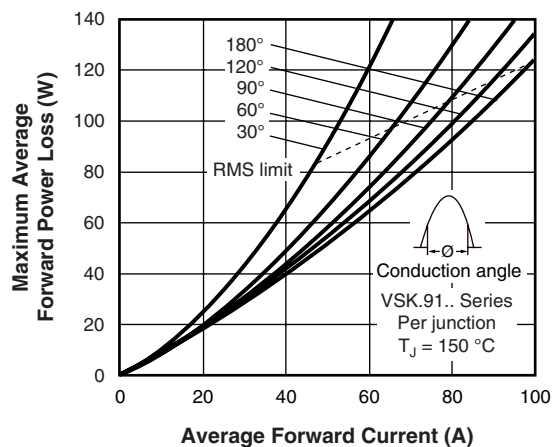


Fig. 3 - Forward Power Loss Characteristics

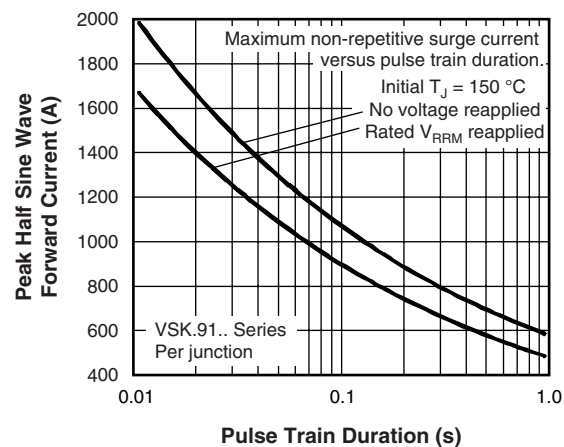


Fig. 6 - Maximum Non-Repetitive Surge Current

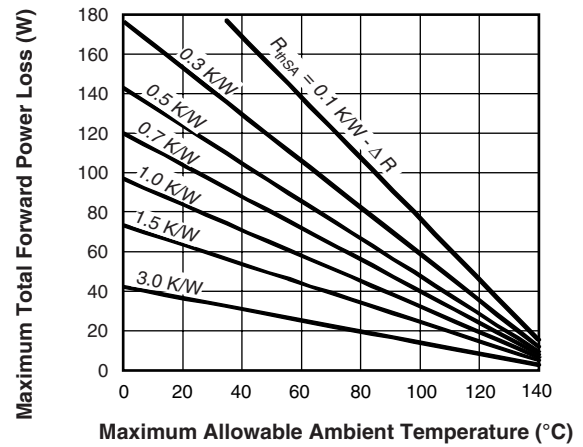
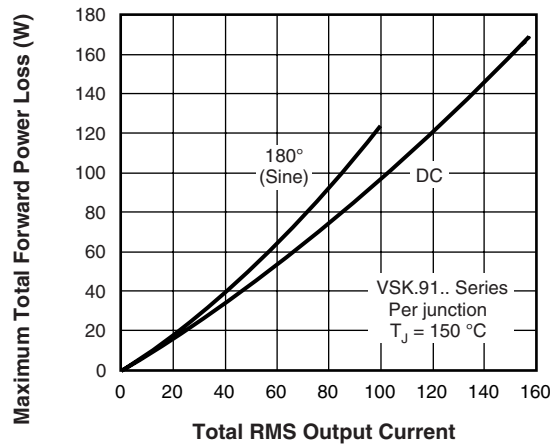


Fig. 7 - Forward Power Loss Characteristics

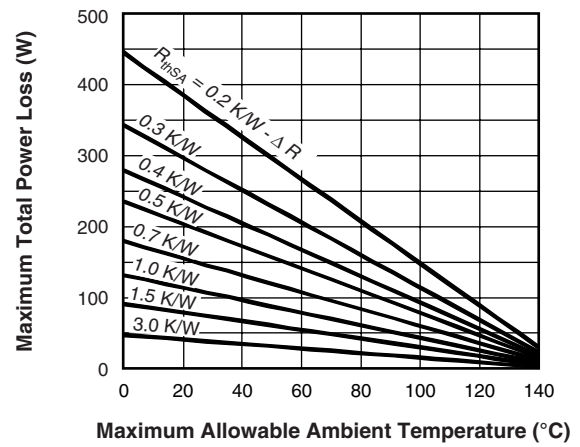
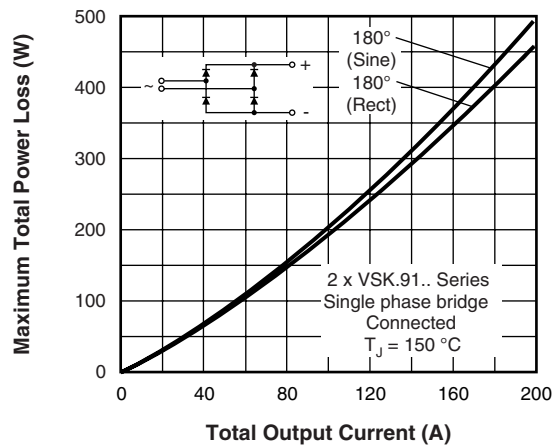


Fig. 8 - Forward Power Loss Characteristics

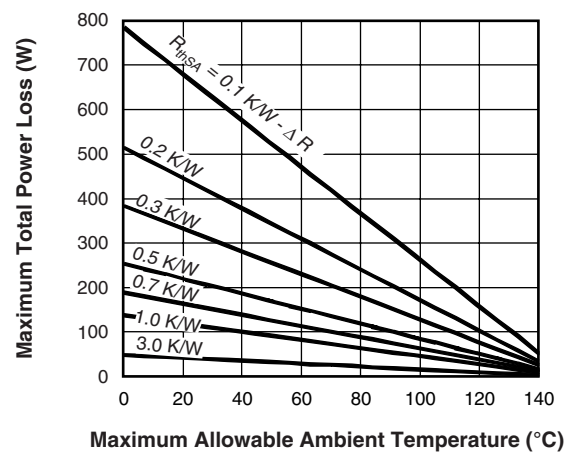
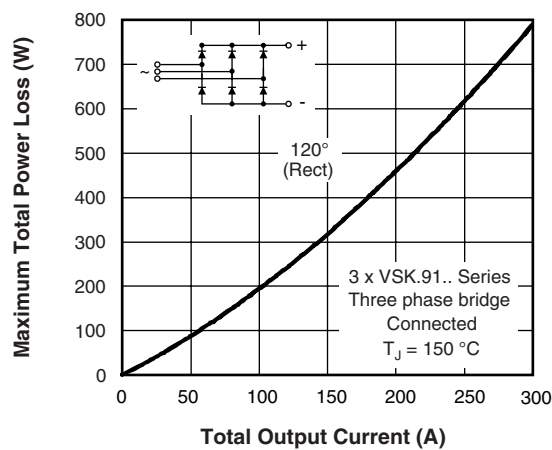


Fig. 9 - Forward Power Loss Characteristics

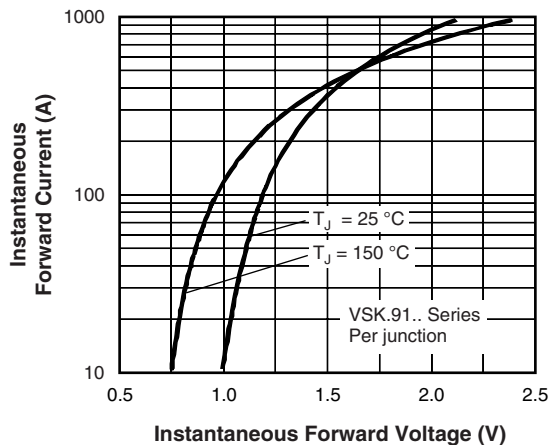


Fig. 10 - Forward Voltage Drop Characteristics

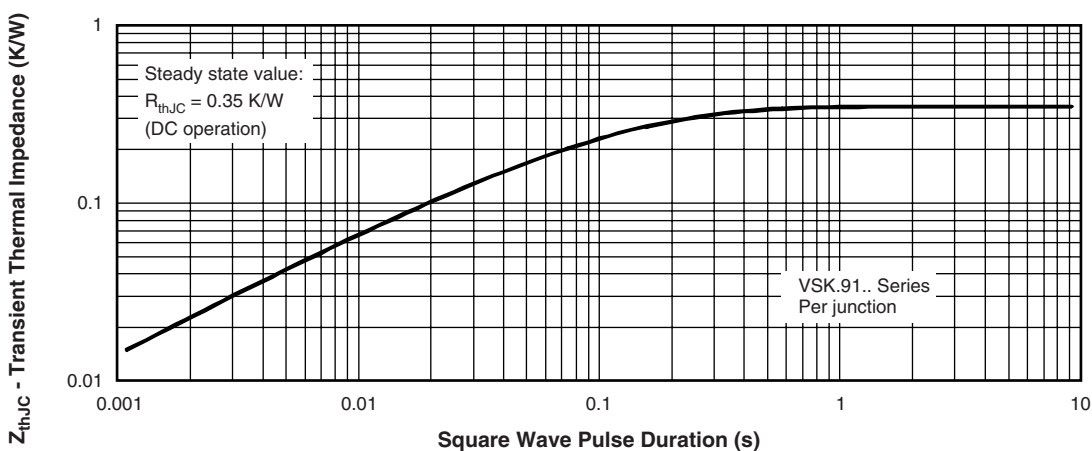


Fig. 11 - Thermal Impedance Z_{thJC} Characteristic

ORDERING INFORMATION TABLE

Device code

VSK	D	91	/	16	P
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1

2

3

4

5

1	-	Module type
2	-	Circuit configuration (see Circuit Configuration table)
3	-	Current code
4	-	Voltage code (see Voltage Ratings table)
5	-	P = Lead (Pb)-free

Note

- To order the optional hardware go to www.vishay.com/doc?95172

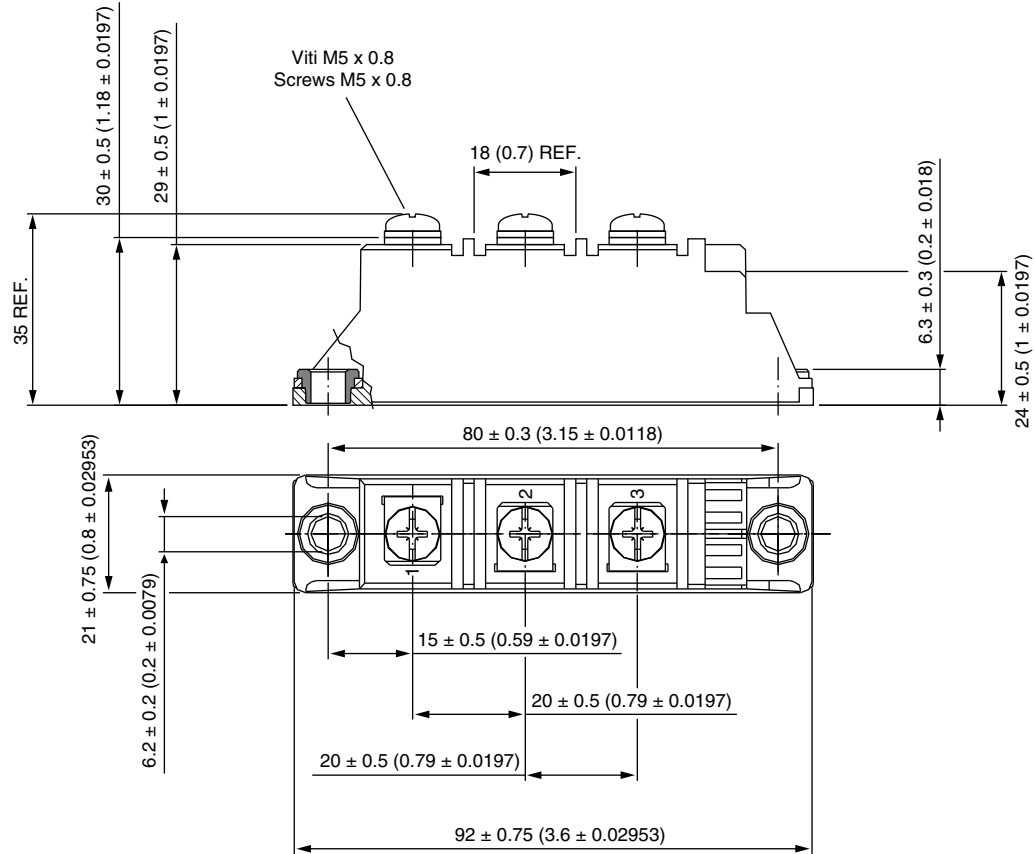


CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two diodes doubler circuit	D	<p>VSKD...</p> <p>Diagram showing two diodes connected in series. The first diode has its anode at terminal (1) and cathode at terminal (2). The second diode has its anode at terminal (2) and cathode at terminal (3). The input is AC at (1) and the output is at (3).</p>
Two diodes common cathodes	C	<p>VSKC...</p> <p>Diagram showing two diodes connected in common cathode configuration. The first diode has its anode at terminal (1) and cathode at terminal (2). The second diode has its anode at terminal (3) and cathode at terminal (2). The input is AC at (1) and the output is at (3).</p>
Two diodes common anodes	J	<p>VSKJ...</p> <p>Diagram showing two diodes connected in common anode configuration. The first diode has its cathode at terminal (1) and anode at terminal (2). The second diode has its cathode at terminal (3) and anode at terminal (2). The input is AC at (1) and the output is at (3).</p>
Single diode	E	<p>VSKE...</p> <p>Diagram showing a single diode connected. The anode is at terminal (2) and the cathode is at terminal (3). The input is AC at (2) and the output is at (3).</p>

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95015

ADD-A-PAK Diode

DIMENSIONS in millimeters (inches)





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