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1 Block diagram and pin configuration

Figure 1. Block diagram

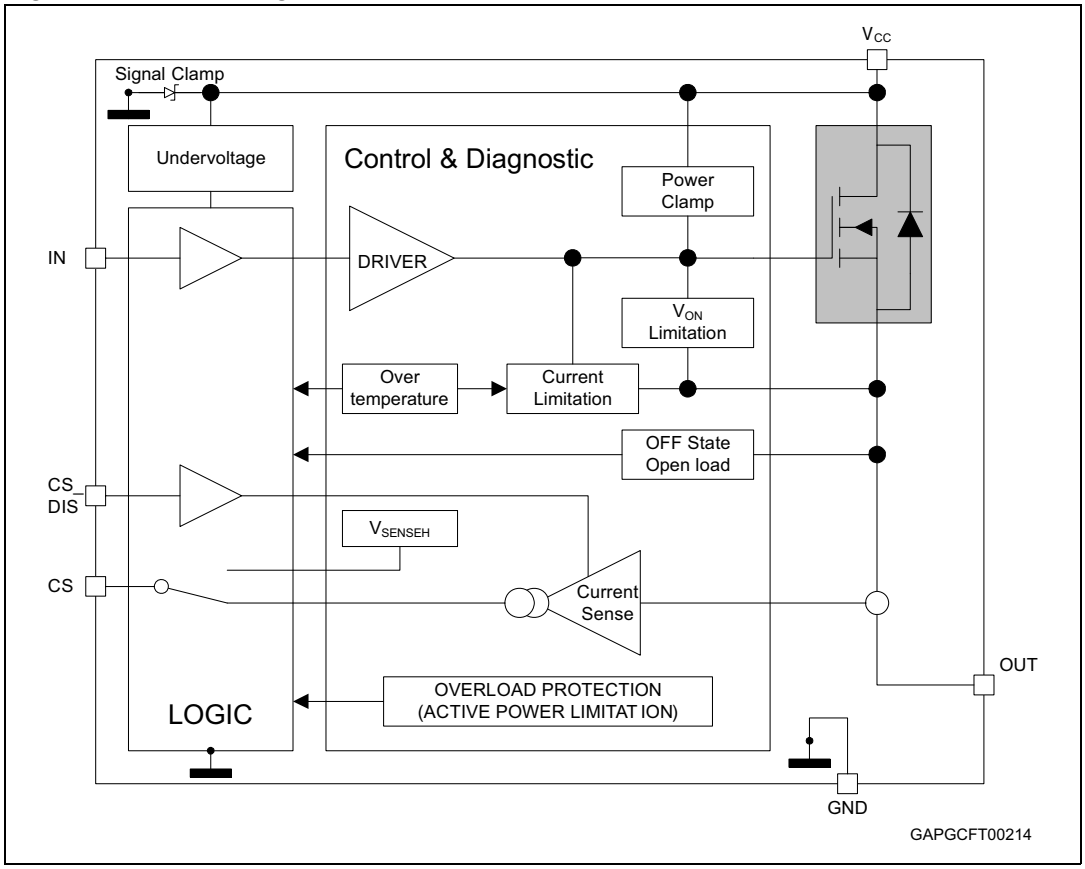

Table 1. Pin function

Name	Function
V_{CC}	Battery connection.
OUT	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
IN	Voltage-controlled input pin with hysteresis, CMOS compatible; it controls output switch state.
CS	Analog current sense pin; it delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

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Figure 2. Configuration diagram (top view)

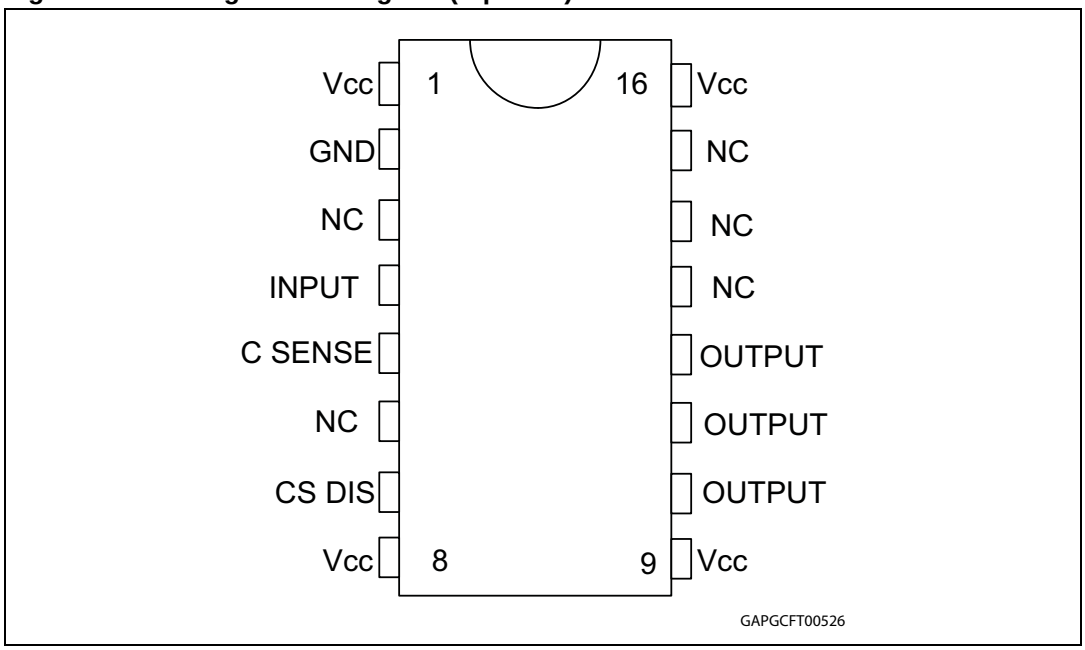

Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X(1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 10 kΩ resistor	Through 10 kΩ resistor

1. X: do not care.

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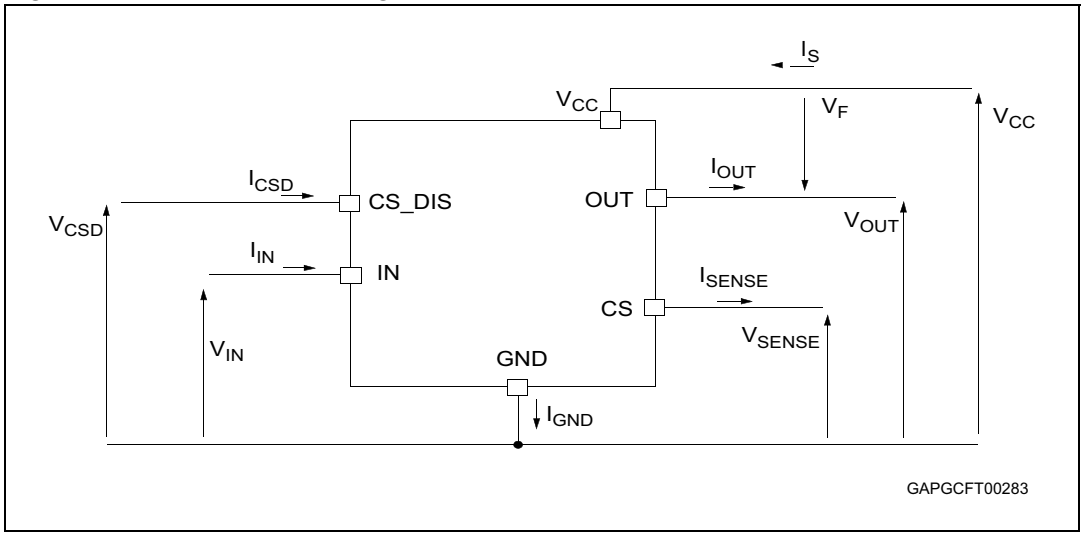
2 Electrical specifications

Figure 3. Current and voltage conventions



1. $V_F = V_{OUT} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the “absolute maximum ratings” table for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	6	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC} - 41 $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) (L = 8 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150°C; $I_{OUT} = I_{limL}$*(Typ.)*)	36	mJ

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Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF) – IN – CS – CS_DIS – OUT – V_{CC}	 4000 2000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typical value	Unit
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb(1)	18.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction - ambient on two layers pcb	See *Figure 36*	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction - ambient on two layers pcb(2)	38	°C/W

1. The measure is done in accordance with the JESD 51-8.
2. Four Layers PCB characteristics:

- Cu thickness: 70 um outer layers, 35 um inner layers
- Board finish thickness 1.6 mm +/- 10%
- Thermal vias separation 1.2 mm
- Thermal via diameter 0.3 mm +/- 0.08 mm
- Cu thickness on vias 0.025 mm
- Device soldered at about 2cm from the PCB edge with two sqcm of exposed copper.

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2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shut-down			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
R_{ON}	ON-state resistance	I_{OUT} = 1 A; T_j = 25°C		160		mΩ
		I_{OUT} = 1 A; T_j = 150°C			320	
		I_{OUT} = 1 A; V_{CC} = 5 V; T_j = 25°C			210	
V_{clamp}	Voltage clamp	I_S = 20 mA	41	46	52	V
I_S	Supply current	OFF-state: V_{CC} = 13 V; V_{IN} = V_{OUT} = 0 V; T_j = 25°C		2(1)	5(1)	µA
		ON-state: V_{IN} = 5 V; V_{CC} = 13 V; I_{OUT} = 0 A		1.9	3.5	mA
$I_{L(off1)}$	OFF-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125°C	0		5	
V_F	Output - V_{CC} diode voltage	-I_{OUT} = 1 A; T_j = 150°C			0.7	V

1. PowerMOS leakage included.

Table 6. Switching (V_{CC} = 13 V; T_j = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 13 Ω (see *Figure 6*)	—	10	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 13 Ω (see *Figure 6*)	—	10	—	µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 13 Ω	—	See *Figure 26*	—	V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 13 Ω	—	See *Figure 28*	—	V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 13 Ω (see *Figure 6*)	—	0.05	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 13 Ω (see *Figure 6*)	—	0.03	—	mJ

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Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage				0.9	V
I_{IL}	Low-level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	High-level input voltage		2.1			V
I_{IH}	High-level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Hysteresis input voltage		0.25			V
V_{ICL}	Input voltage clamp	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		
V_{CSDL}	Low-level CS_DIS voltage				0.9	V
I_{CSDL}	Low-level CS_DIS current	V_{CSD} = 0.9 V	1			µA
V_{CSDH}	High-level CS_DIS voltage		2.1			V
I_{CSDH}	High-level CS_DIS current	V_{CSD} = 2.1 V			10	µA
$V_{CSD(hyst)}$	Hysteresis CS_DIS voltage		0.25			V
V_{CSCL}	CS_DIS voltage clamp	I_{CSD} = 1 mA	5.5		7	V
		I_{CSD} = -1 mA		-0.7		

Table 8. Protection and diagnostics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	V_{CC} = 13 V	7	10	14	A
		5 V < V_{CC} < 28 V			14	A
I_{limL}	Short-circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		2.5		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 1 A; V_{IN} = 0, L = 20 mH	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.03 A (see *Figure 8*) T_j = -40 °C to +150 °C		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

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Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.025 A; V_{SENSE} = 0.5 V T_j = -40°C to 150°C	265	490	715	
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.35 A; V_{SENSE} = 0.5 V T_j = -40°C to 150°C T_j = 25°C to 150°C	355 385	465 465	575 545	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT} =0.35 A; V_{SENSE} = 0.5 V T_j = -40°C to 150°C	-11		+11	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 0.5 A; V_{SENSE} = 4 V T_j = -40°C to 150°C T_j = 25°C to 150°C	380 400	455 455	530 510	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT} = 0.5 A; T_j = -40°C to 150°C	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 1.5 A; V_{SENSE} = 4 V T_j = -40°C to 150°C T_j = 25°C to 150°C	420 420	455 455	490 480	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT} = 1.5 A; T_j = -40°C to 150°C	-4		+4	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 0 V; T_j = -40°C to 150°C	0		1	µA
		I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 0 V; V_{IN} = 5 V; T_j = -40°C to 150°C	0		2	
		I_{OUT} = 1 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 5 V; T_j = -40°C to 150°C	0		1	
V_{SENSE}	Max analog sense output voltage	R_{SENSE} = 10 KΩ I_{OUT} = 1 A;	5			V
V_{SENSEH} (2)	Analog sense output voltage in fault condition	V_{CC} = 13 V; R_{SENSE} = 3.9 KΩ		8		V
I_{SENSEH} (2)	Analog sense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V		9		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE} < 4 V; 0.025 A < I_{OUT} < 1.5 A I_{SENSE} = 90% of $I_{SENSE\ max}$ (see *Figure 4*)		40	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE} < 4 V; 0.025 A < I_{OUT} < 1.5 A I_{SENSE} = 10% of $I_{SENSE\ max}$ (see *Figure 4*)		5	20	µs

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Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE2H}$	Delay response time from rising edge of IN pin	V_{SENSE} < 4 V; 0.025 A < I_{OUT} < 1.5 A I_{SENSE}=90% of $I_{SENSE\ max}$ (see *Figure 4*)		30	160	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V; I_{SENSE} = 90% of $I_{SENSEMAX}$, I_{OUT} = 90% of I_{OUTMAX} I_{OUTMAX}=1.5A (see *Figure 7*)			110	µs
$t_{DSENSE2L}$	Delay response time from falling edge of IN pin	V_{SENSE} < 4 V; 0.025 A < I_{OUT} < 1.5 A I_{SENSE}=10% of $I_{SENSE\ max}$ (see *Figure 4*)		80	250	µs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open load OFF-state detection.

Table 10. Open-load detection (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	OFF-state open-load voltage detection threshold	V_{IN} = 0 V; 8 V < V_{CC} < 18 V	2		4	V
I_{OL}	ON-state open-load current detection threshold	V_{IN} = 5V; 8 V < V_{CC} < 18 V I_{SENSE} = 5 µA	0.5		5	mA
t_{DSTKON}	Output short-circuit to V_{CC} detection delay at turn-off	See *Figure 5*	180		1200	µs
$I_{L(off2)r}$	OFF-state output current at V_{OUT} = 4 V	V_{IN} = 0 V; V_{SENSE} = 0 V V_{OUT} rising from 0 V to 4 V	-120		0	µA
$I_{L(off2)f}$	OFF-state output current at V_{OUT} = 2 V	V_{IN} = 0 V; V_{SENSE} = V_{SENSEH} V_{OUT} falling from V_{CC} to 2 V	-50		90	
td_vol	Delay response from output rising edge to V_{SENSE} rising edge in open-load	V_{OUT} = 4 V; V_{IN} = 0 V V_{SENSE}= 90% of V_{SENSEH}			20	µs

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Figure 4. Current sense delay characteristics

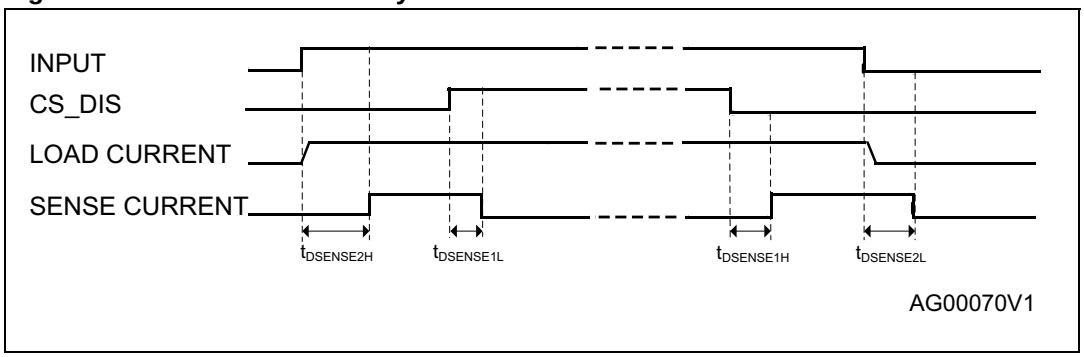

Figure 5. OFF-state open-load delay timing

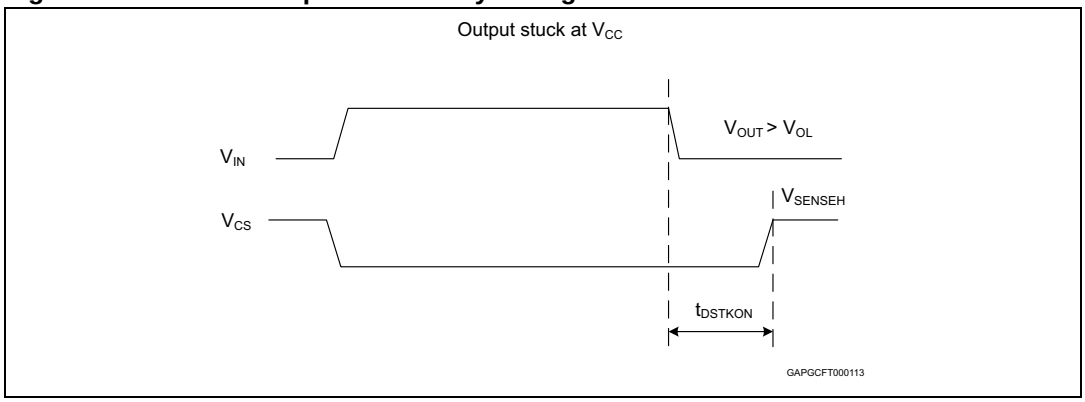

Figure 6. Switching characteristics

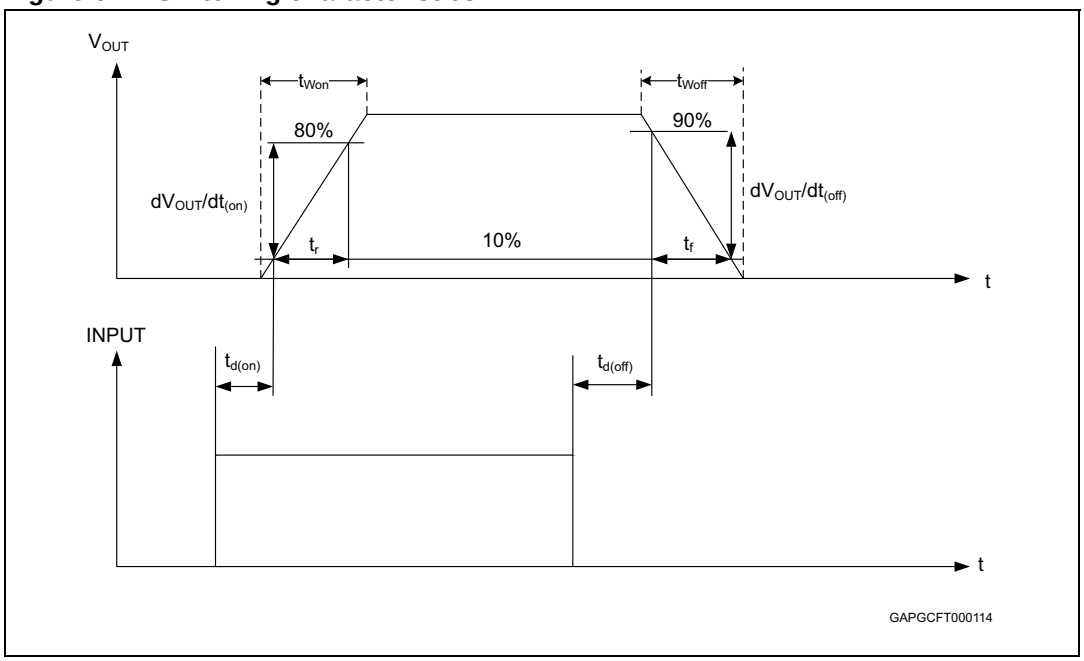

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Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

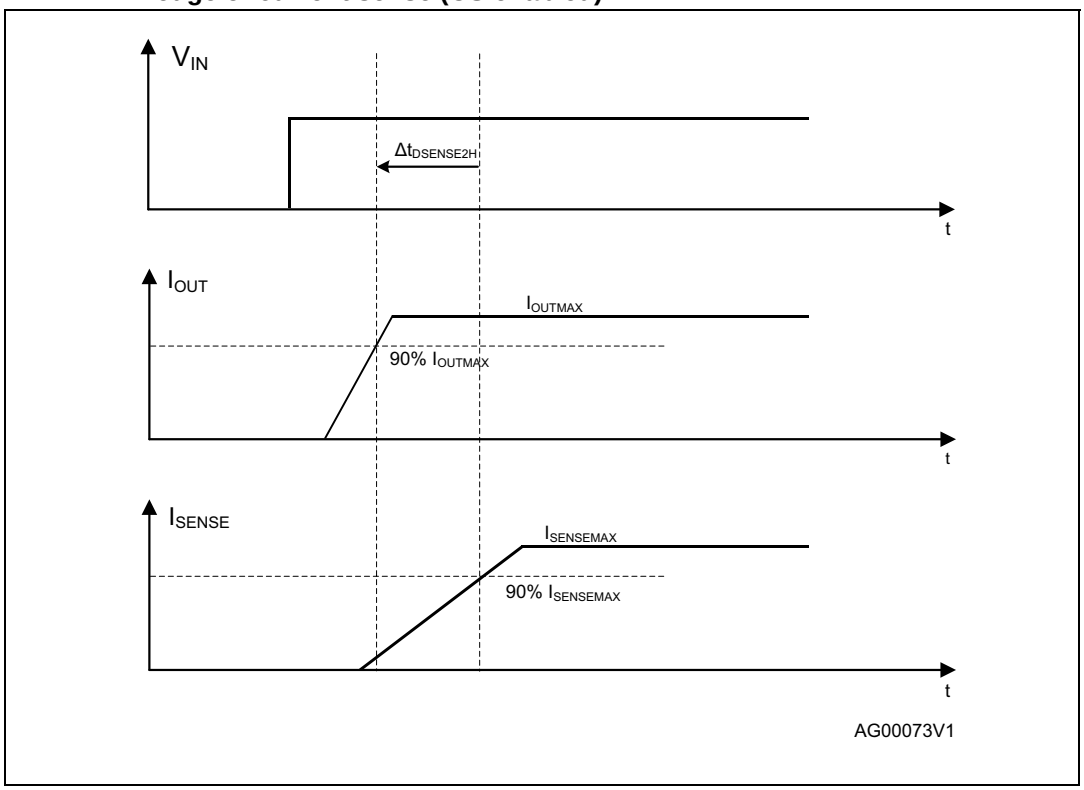

Figure 8. Output voltage drop limitation

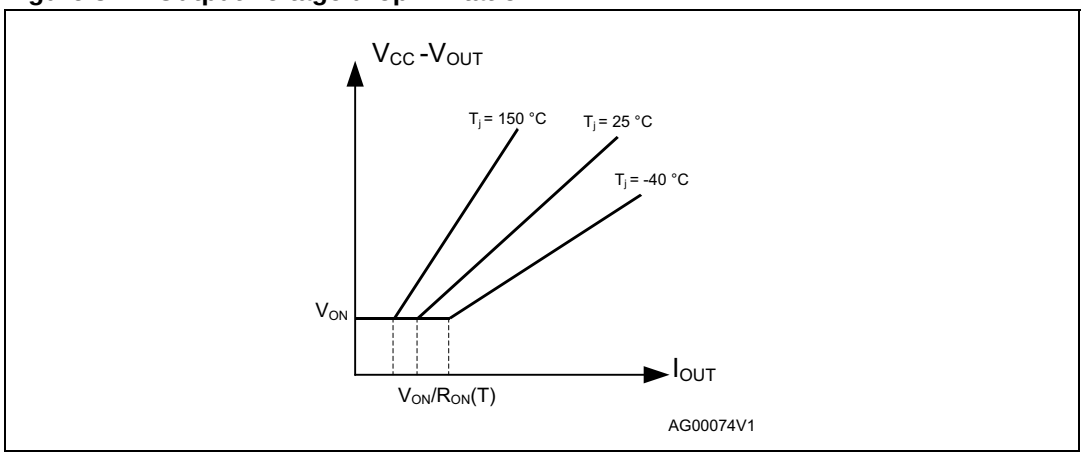

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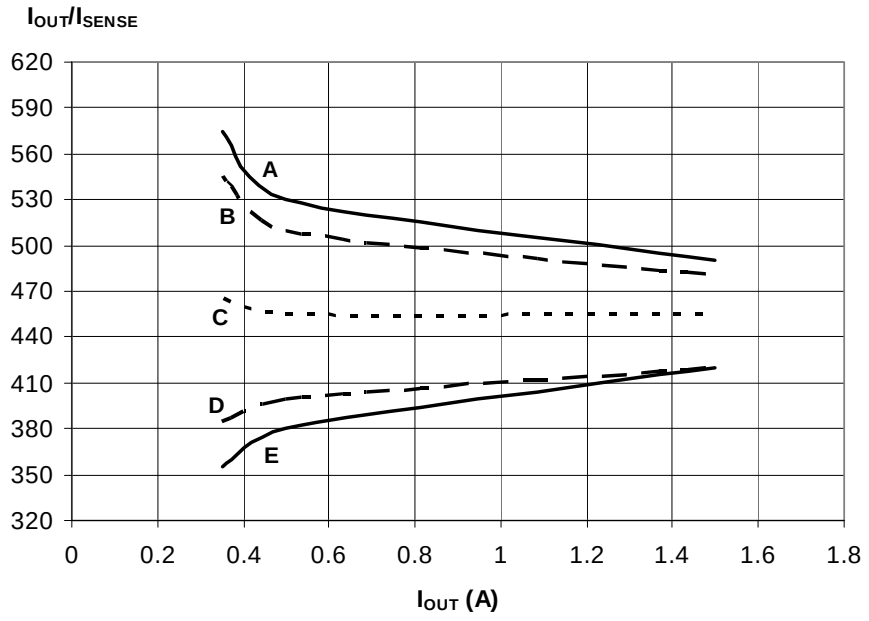
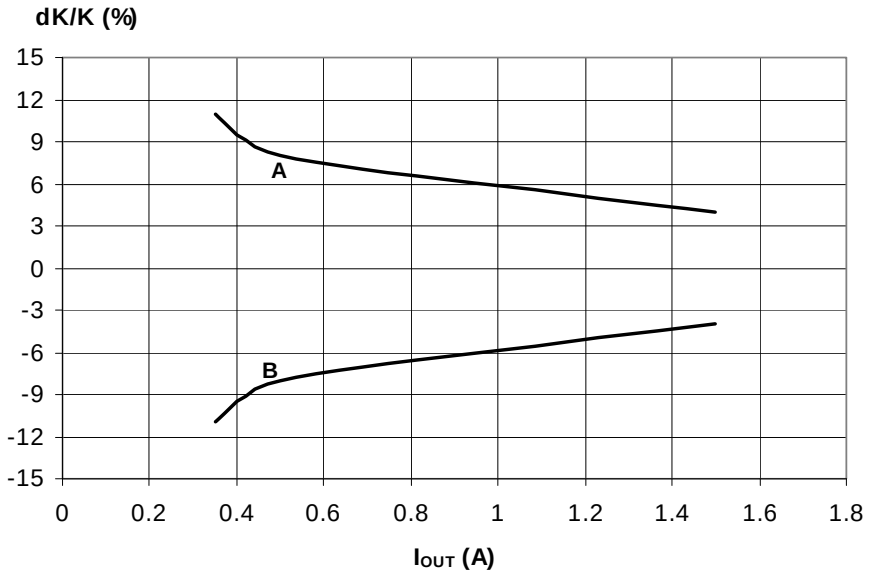
Figure 9. I_{OUT}/I_{SENSE} vs I_{OUT}



A: Max, T_j = -40°C to 150°C
B: Max, T_j = 25°C to 150°C
C: Typical, T_j = -40°C to 150°C
D: Min, T_j = 25°C to 150°C
E: Min, T_j = -40°C to 150°C

Figure 10. Maximum current sense ratio drift vs load current(1)



A: Max, T_j = -40°C to 150°C
B: Min, T_j = 25°C to 150°C

1. Parameter guaranteed by design; it is not tested.

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Table 11. Truth table

Conditions	IN	OUT	SENSE (V_{CSD} = 0 V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (Power limitation)	L H	L L	0 V_{SENSEH}
OFF-state open-load (with external pull-up)	L	H	V_{SENSEH}

1. If the V_{CSD} is high, the SENSE output is at high impedance, its potential depends on leakage currents and external circuit.

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Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+65 V	+87 V	1 pulse			400 ms, 2 Ω

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b
2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

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2.4 Waveforms

Figure 11. Normal operation

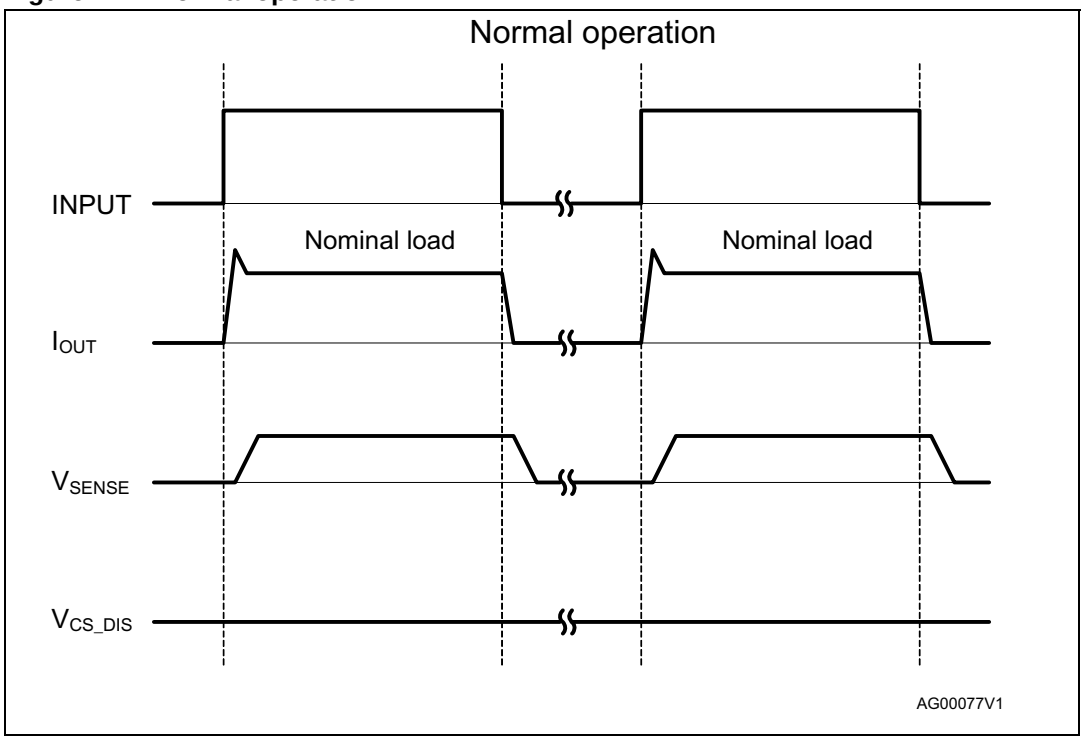

Figure 12. Overload or short to GND

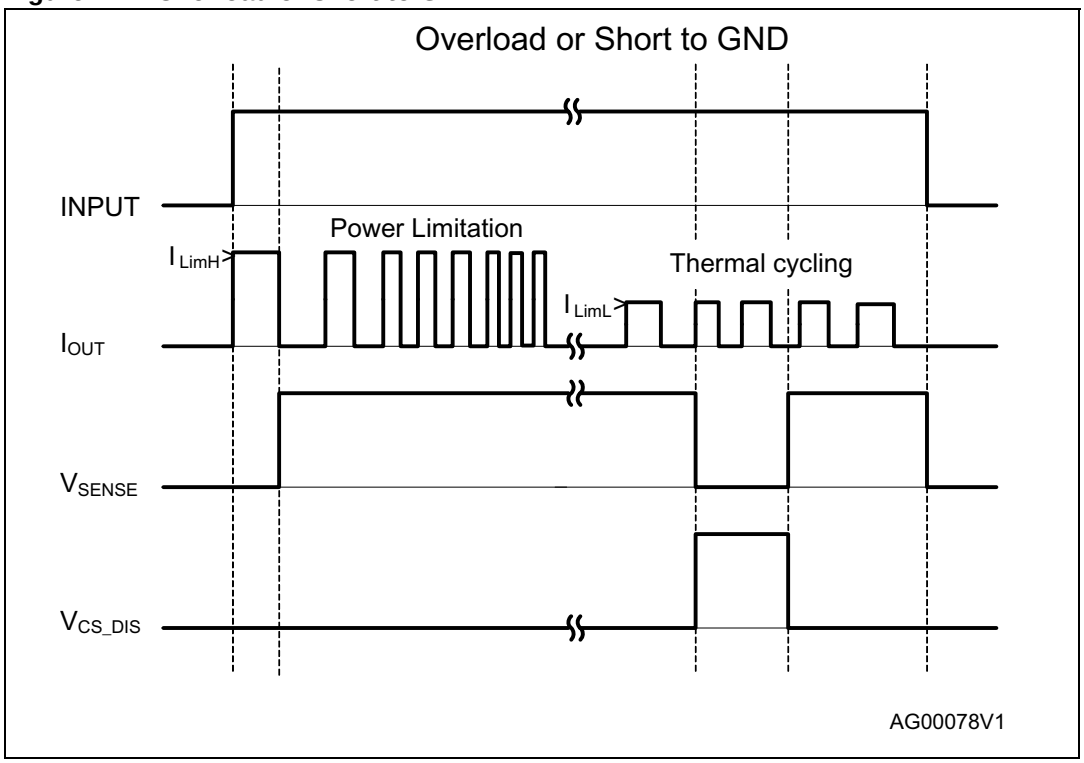

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Figure 13. Intermittent overload

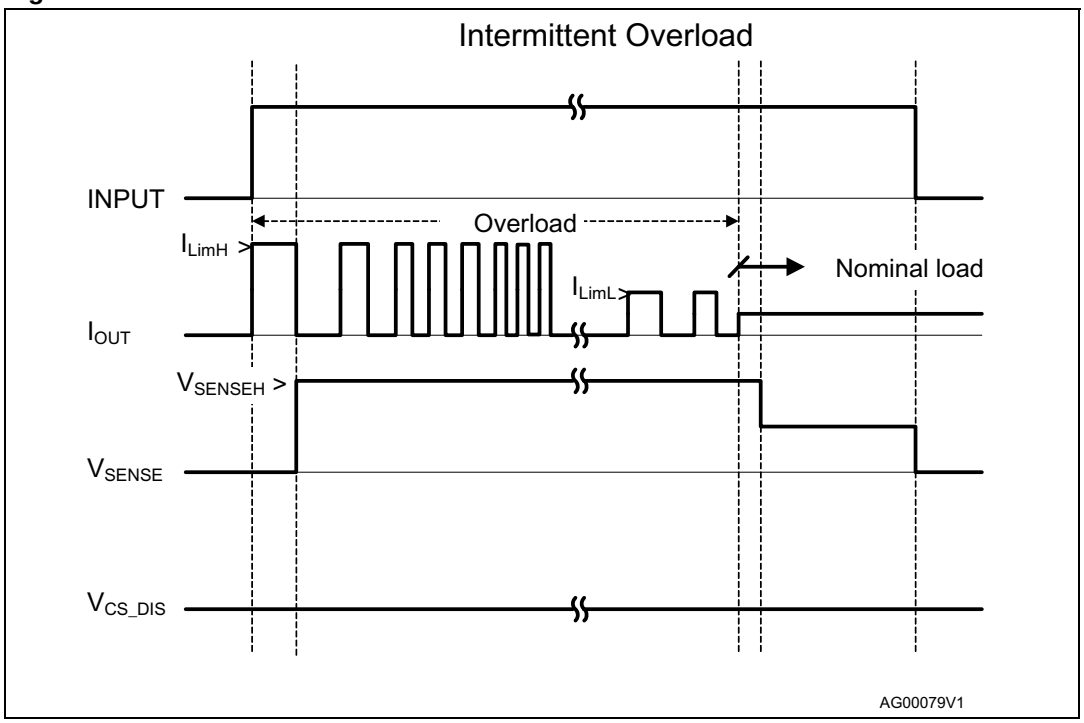

Figure 14. OFF-state open-load with external circuitry

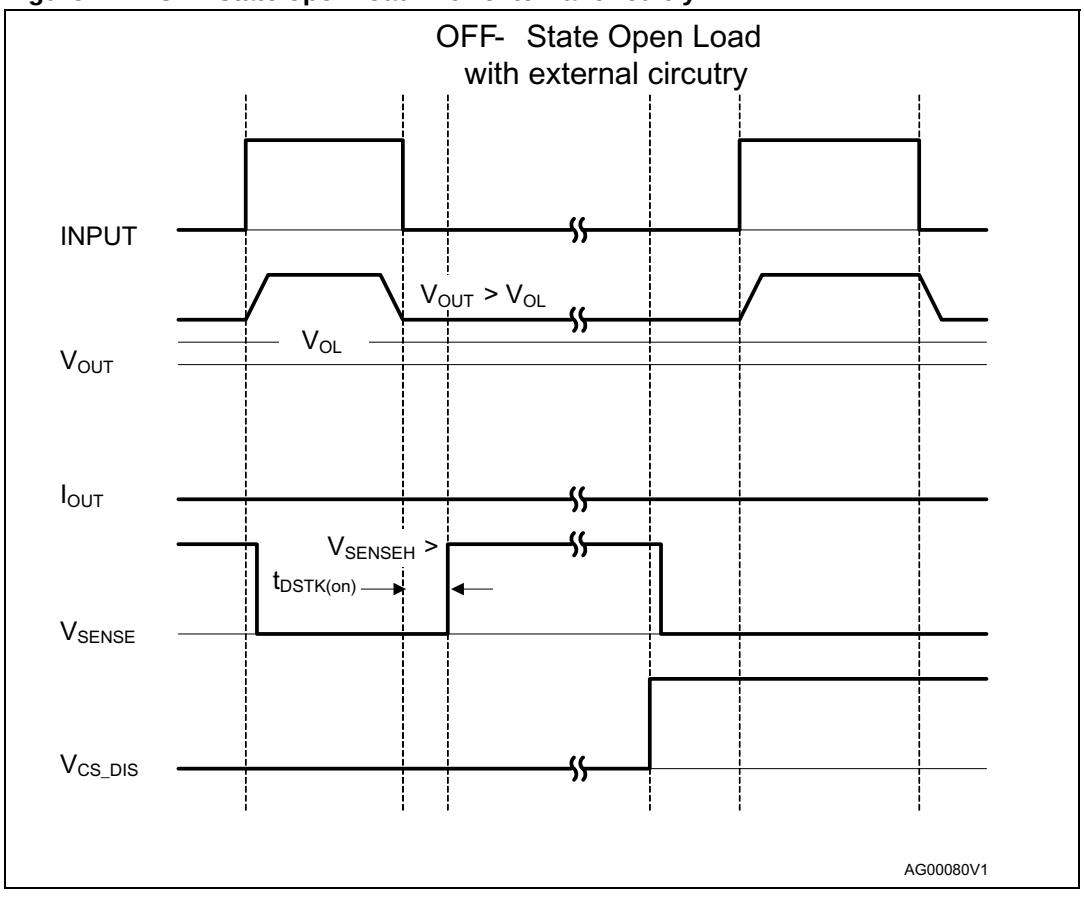

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Figure 15. Short to V_{CC}

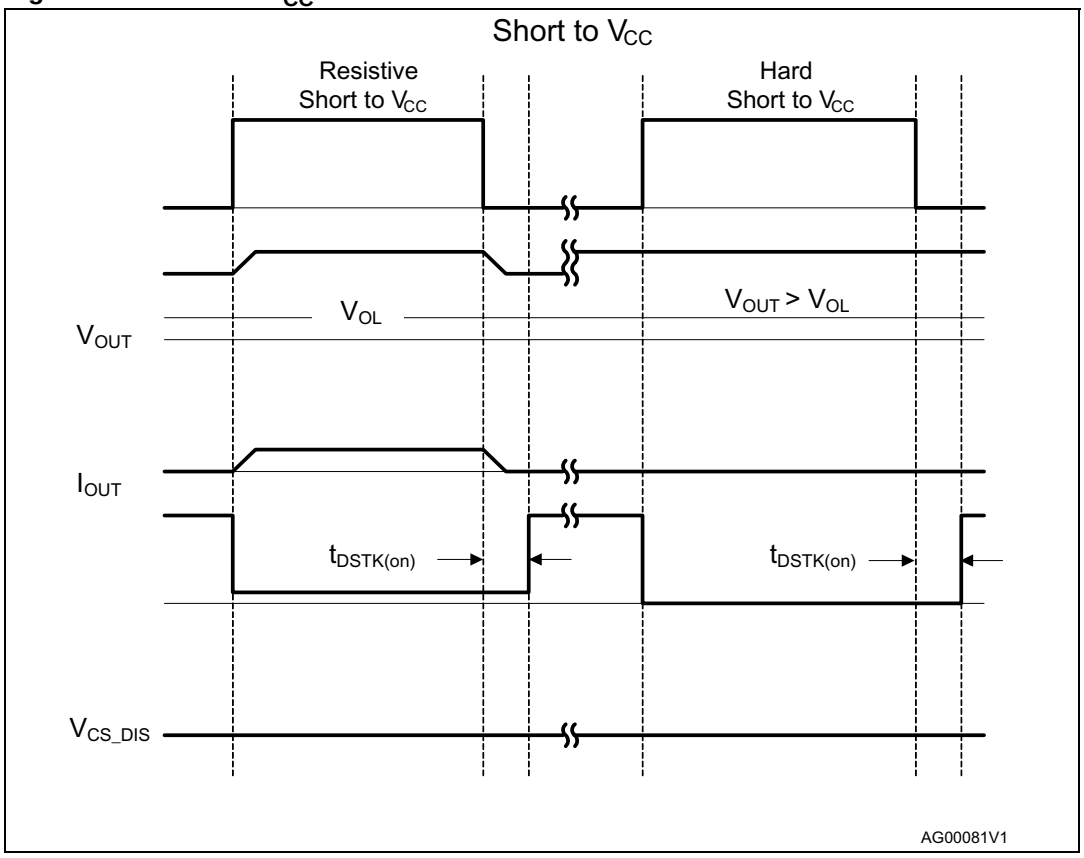
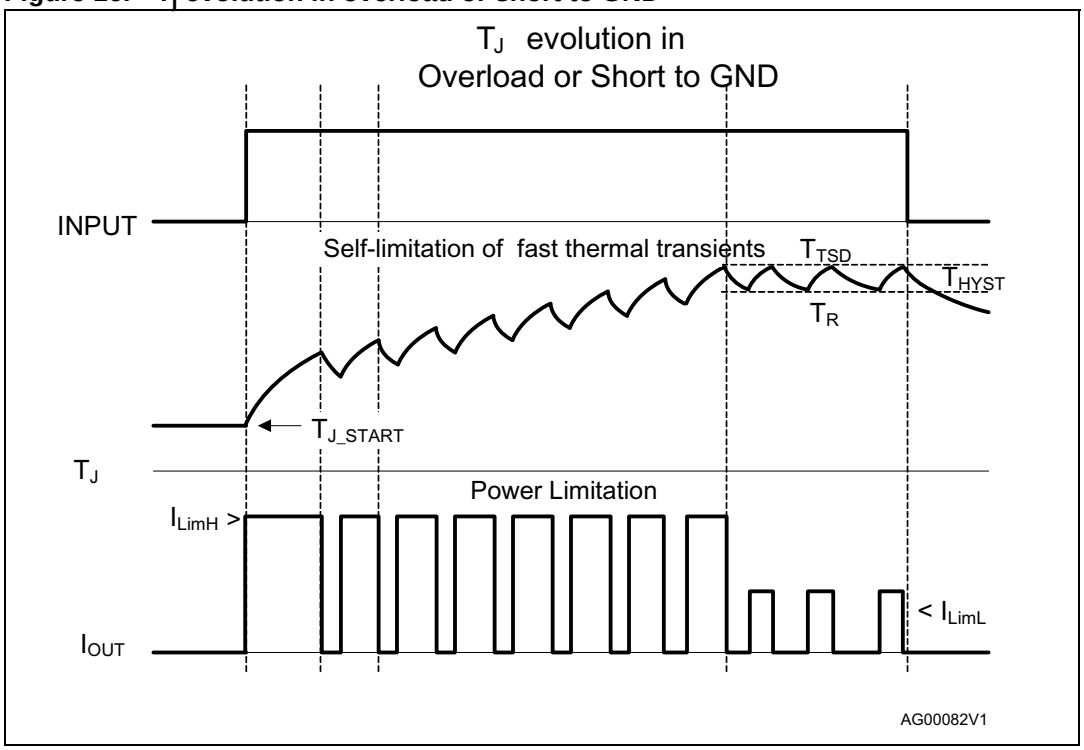


Figure 16. T_j evolution in overload or short to GND



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2.5 Electrical characteristics curves

Figure 17. OFF-state output current

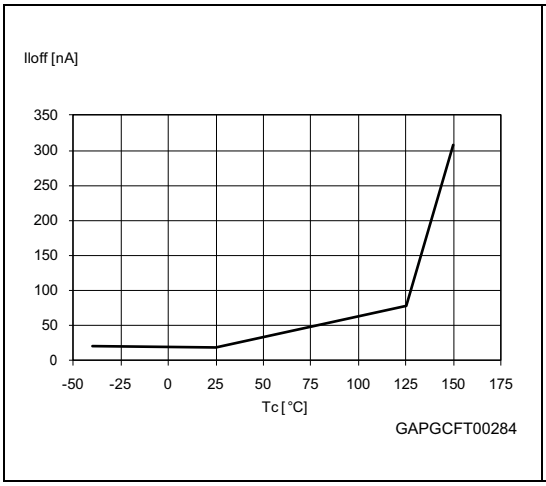

Figure 18. High-level input current

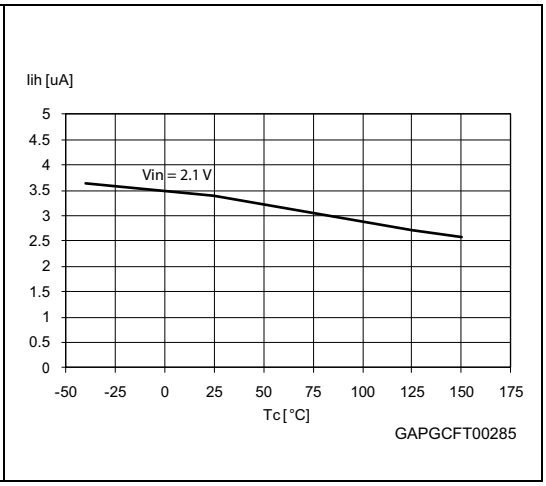

Figure 19. Input voltage clamp

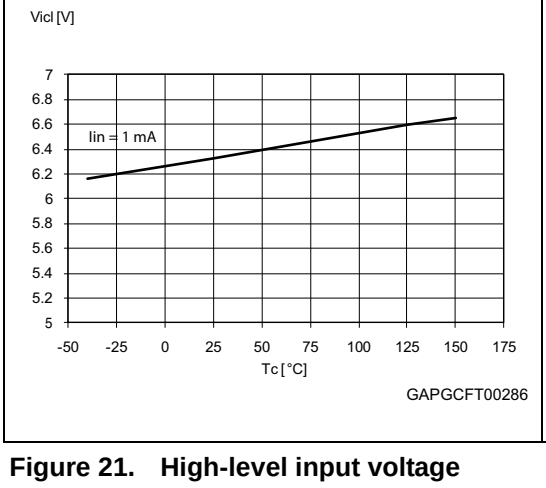

Figure 20. Low-level input voltage

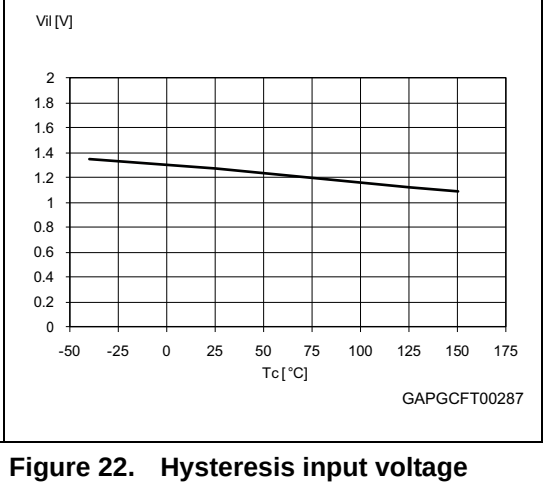

Figure 21. High-level input voltage

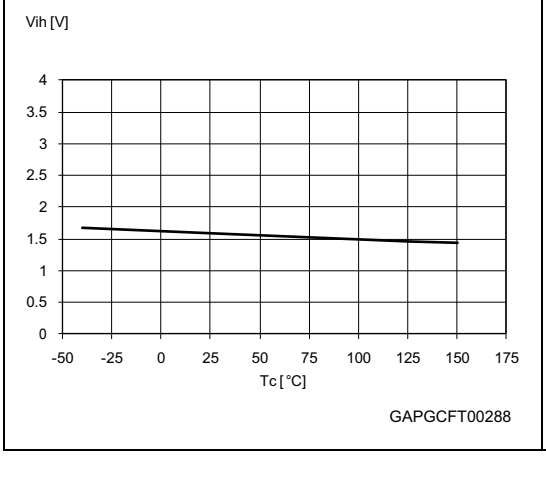

Figure 22. Hysteresis input voltage

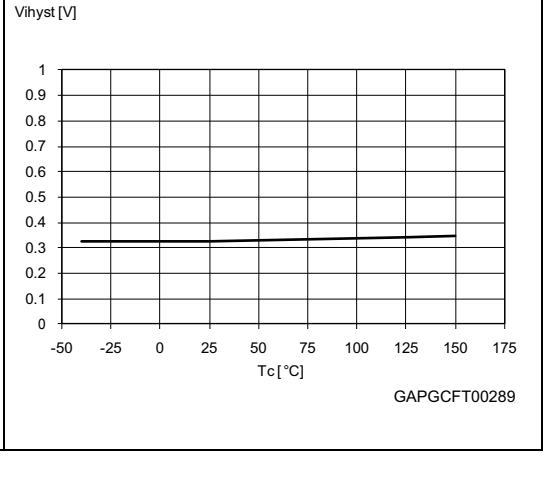

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Figure 23. ON-state resistance vs T_{case}

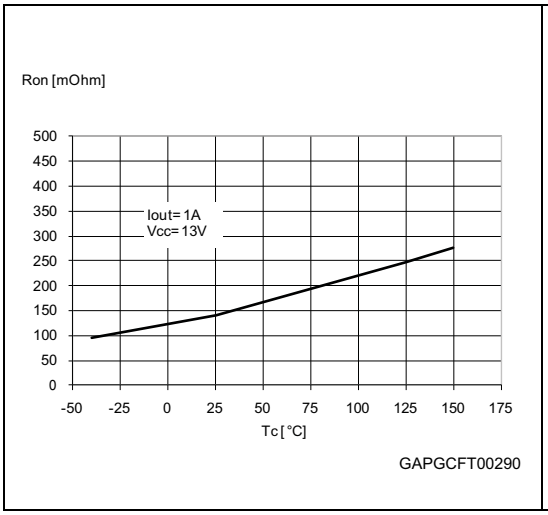

Figure 24. ON-state resistance vs V_{CC}

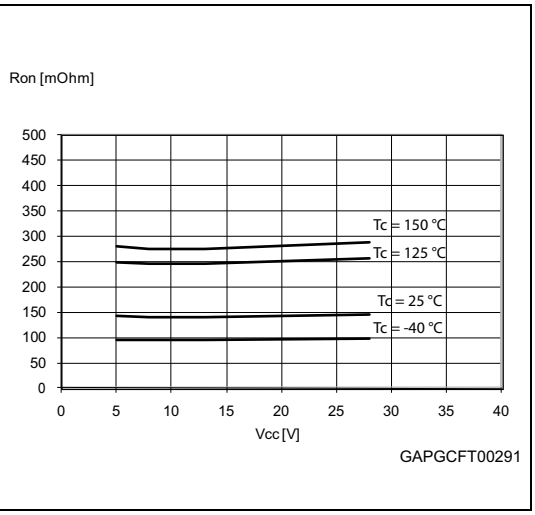

Figure 25. Undervoltage shutdown

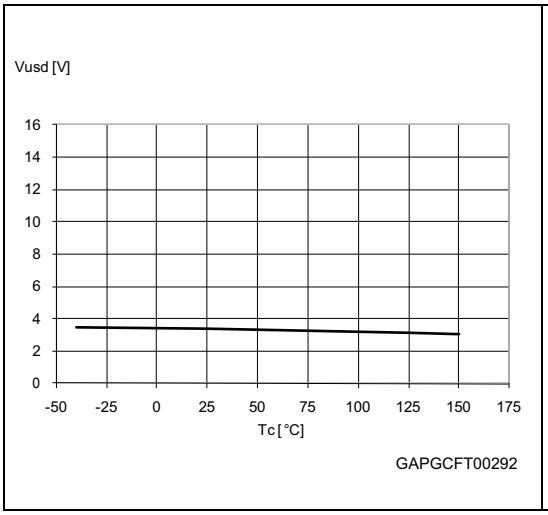

Figure 26. Turn-on voltage slope

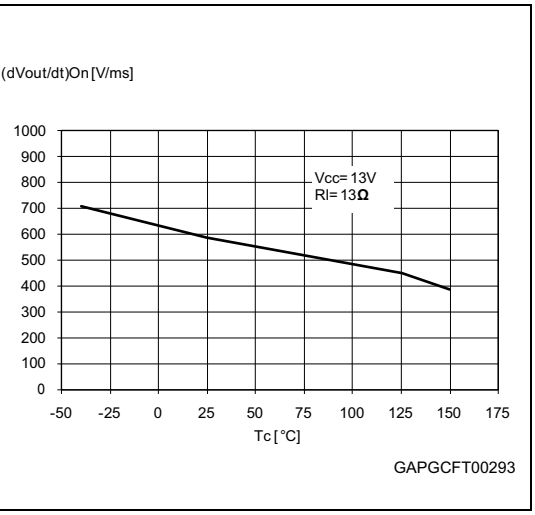

Figure 27. I_{LIMH} vs T_{case}

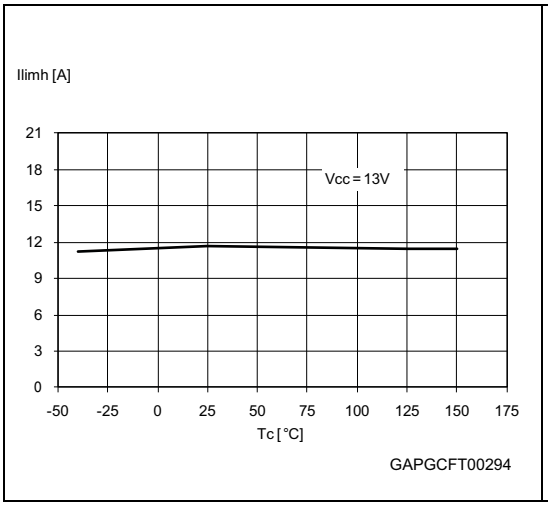

Figure 28. Turn-off voltage slope

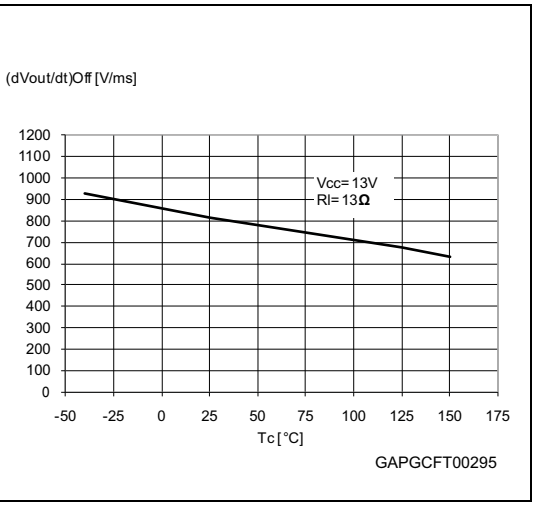

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Figure 29. High-level CS_DIS voltage

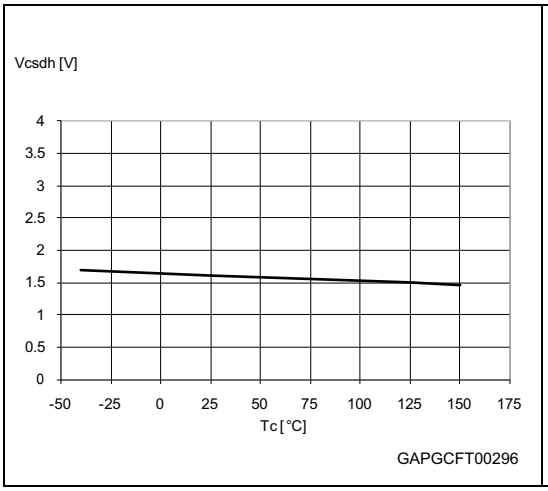


Figure 30. CS_DIS voltage clamp

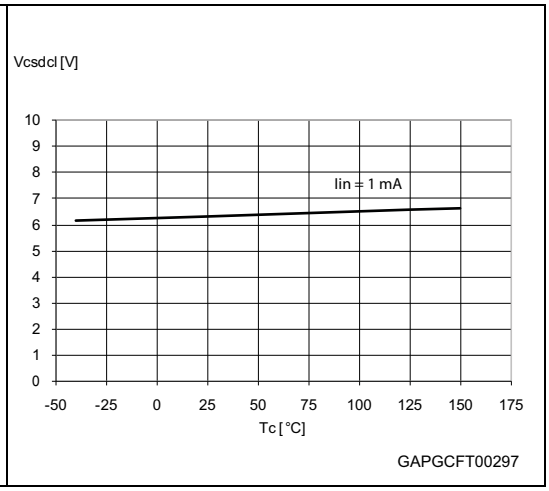
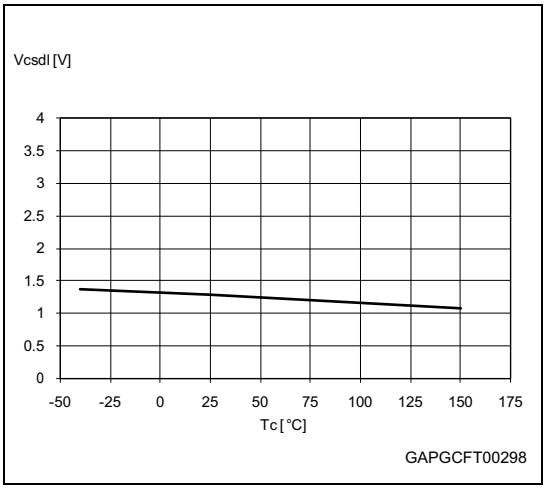


Figure 31. Low-level CS_DIS voltage



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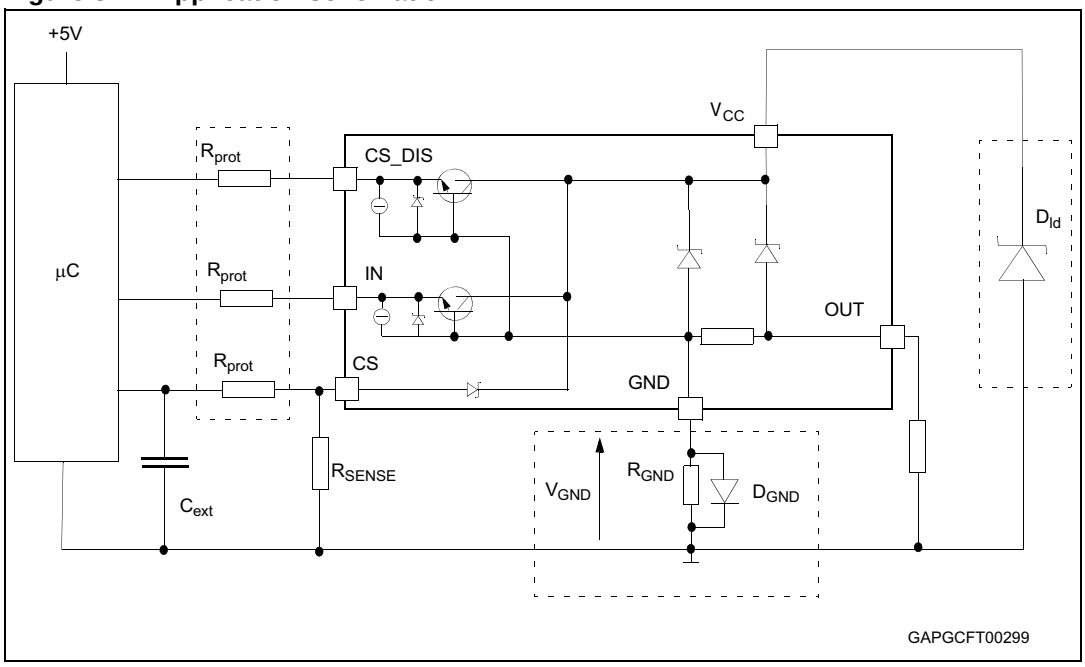
3 Application information

Figure 32. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to resize the R_{GND} resistor.

1. $R_{GND} \leq 600\ mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

Equation 1

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum ON-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output

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values. This shift varies depending on how many devices are ON in case of several high-side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see *Section 3.1.2: Solution 2: a diode (DGND) in the ground line*).

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} maximux DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 2

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = - 100 V, $I_{latchup} \geq$ 20 mA, $V_{OH\mu C} \geq$ 4.5 V

5 kΩ ≤ R_{prot} ≤ 180 kΩ.

Recommended values: R_{prot} =10 kΩ, C_{EXT} = 10 nF.

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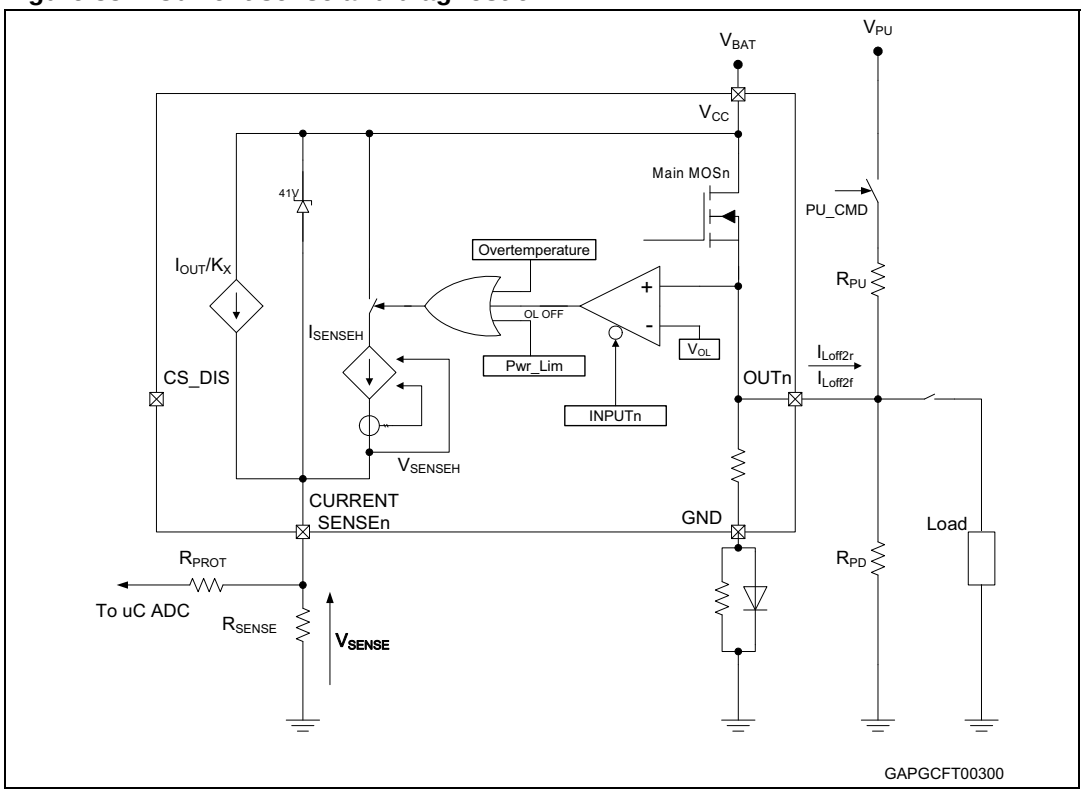
3.4 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 33: Current sense and diagnostic*):

- **Current mirror of the load current in normal operation,** delivering a current proportional to the load current according to a known ratio $\mathbf{K_X}$.
  The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5 V minimum (see parameter V_{SENSE} in *Table 9: Current sense (8 V < V_{CC} < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 9: Current sense (8 V < V_{CC} < 18 V)*).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Table 11: Truth table*):
  - Power limitation activation
  - Overtemperature
  - Short to V_{CC} in OFF-state
  - Open-load in OFF-state with additional external components.

A logic high-level on the CS_DIS pin simultaneously sets all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing the sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostic



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3.4.1 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short-circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device OFF-state. Little or no current is delivered by the current sense during the ON-state depending on the nature of the short-circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off-mode requires an external pull-up resistor (R_{PU}) connecting the output to a positive supply voltage (V_{PU}).

It is preferable that V_{PU} is switched-off during the module standby mode to avoid an increase in overall standby current consumption in normal conditions, that is, when the load is connected.

An external pull-down resistor (R_{PD}) connected between output and GND is mandatory to avoid misdetection in case of floating outputs in OFF-state (see *Figure 33: Current sense and diagnostic*).

R_{PD} must be selected in order to ensure $V_{OUT} < V_{OLmin}$ unless pulled up by the external circuitry:

Equation 3

$$V_{OUT}|_{Pull\text{-}up\_OFF} = R_{PD} \cdot I_{L(off2)f} < V_{OLmin} = 2\ V$$

$R_{PD} \leq 22\ K\Omega$ is recommended.

For proper open load detection in OFF-state, the external pull-up resistor must be selected according to the following formula:

Equation 4

$$V_{OUT}|_{Pull\text{-}up\_ON} = \frac{(R_{PD} \cdot V_{PU}) - (R_{PU} \cdot R_{PD} \cdot I_{L(off2)r})}{(R_{PU} + R_{PD})} > V_{OLmax} = 4\ V$$

For the values of V_{OLmin} ,V_{OLmax}, $I_{L(off2)r}$ and $I_{L(off2)f}$ (see *Table 10: Open-load detection (8 V < V_{CC} < 18 V)*.

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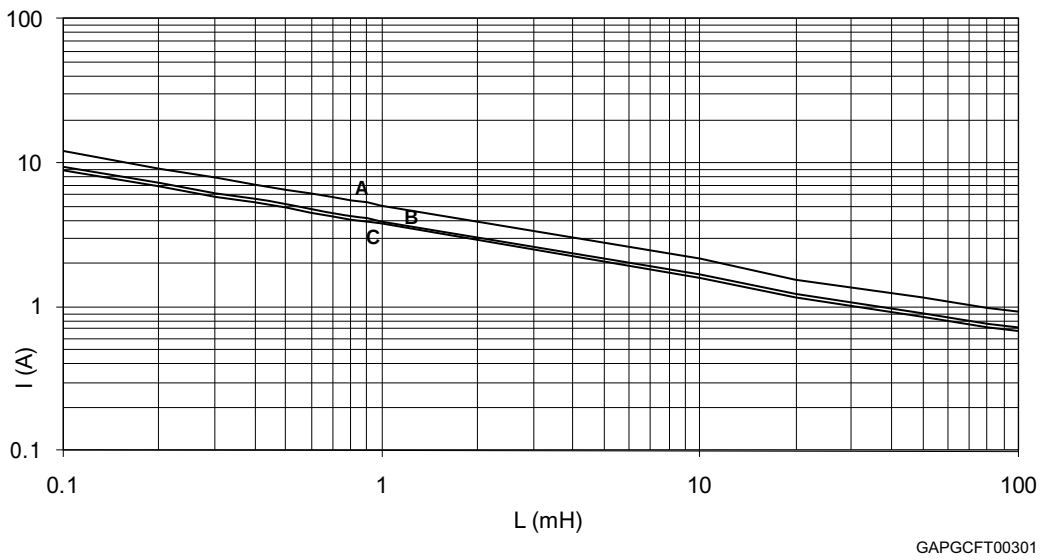
3.5 Maximum demagnetization energy (V_{CC} = 13.5 V)

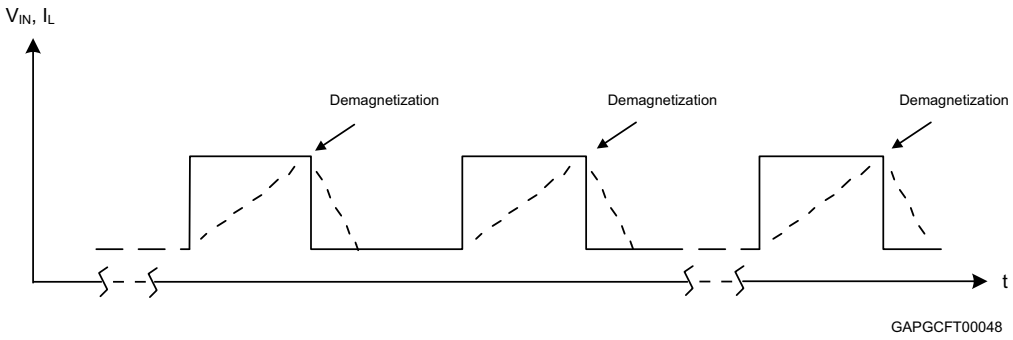
Figure 34. Maximum turn-off current versus inductance (for each channel)(1)



A: T_{jstart} = 150°C single pulse

B: T_{jstart} = 100°C repetitive pulse

C: T_{jstart} = 125°C repetitive pulse



1. Values are generated with R_L = 0 Ω.
In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

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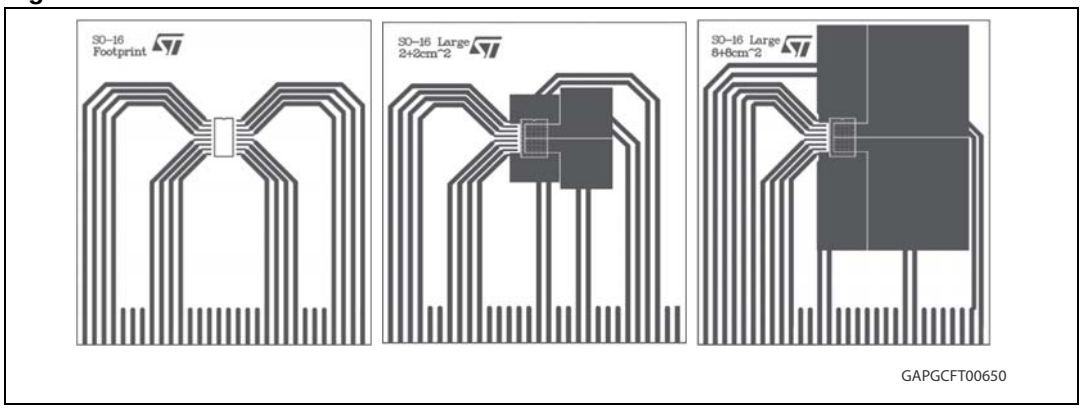
4 Package and PC board thermal data

4.1 SO-16L thermal data

Figure 35. SO-16L PC board



Note: Layout condition of Rth and Zth measurements (PCB: Double Layers, Thermal Vias,FR4 area 77mm x 86 mm, PCB thickness=1.6mm, Cu thickness = 70µm (front and back side), Copper area from minimum pad lay- out to 24 cm2).

Figure 36. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

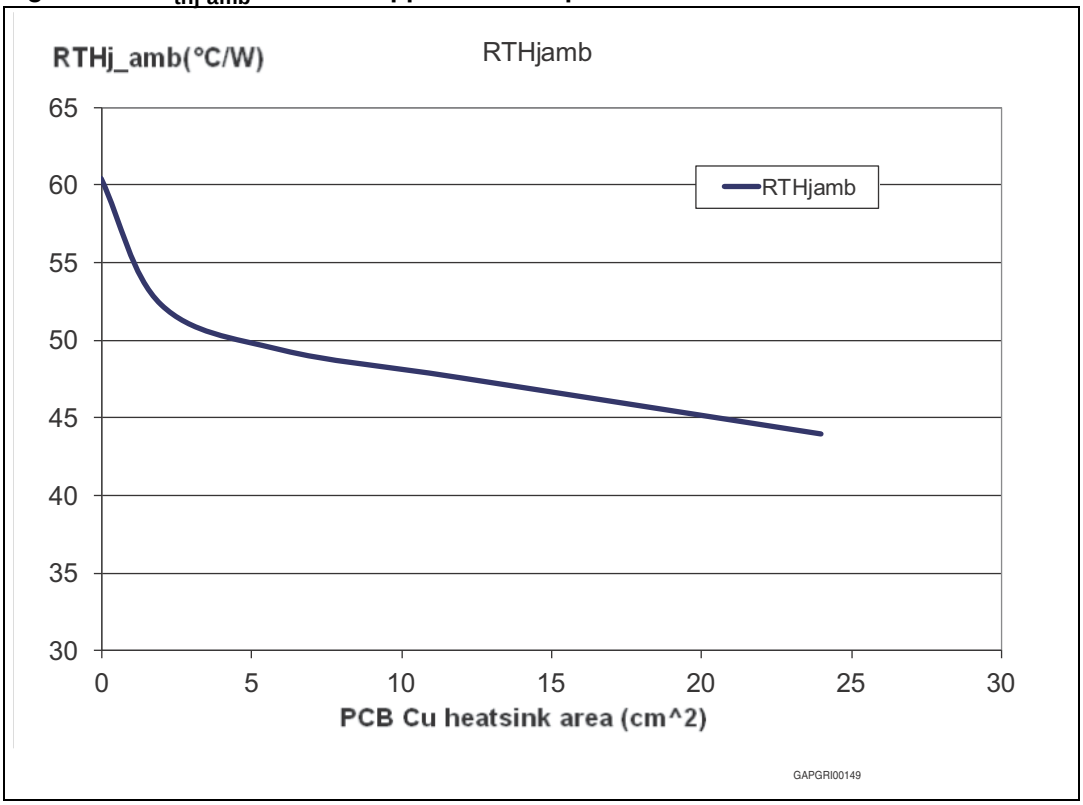


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Figure 37. SO-16L thermal impedance junction ambient single pulse

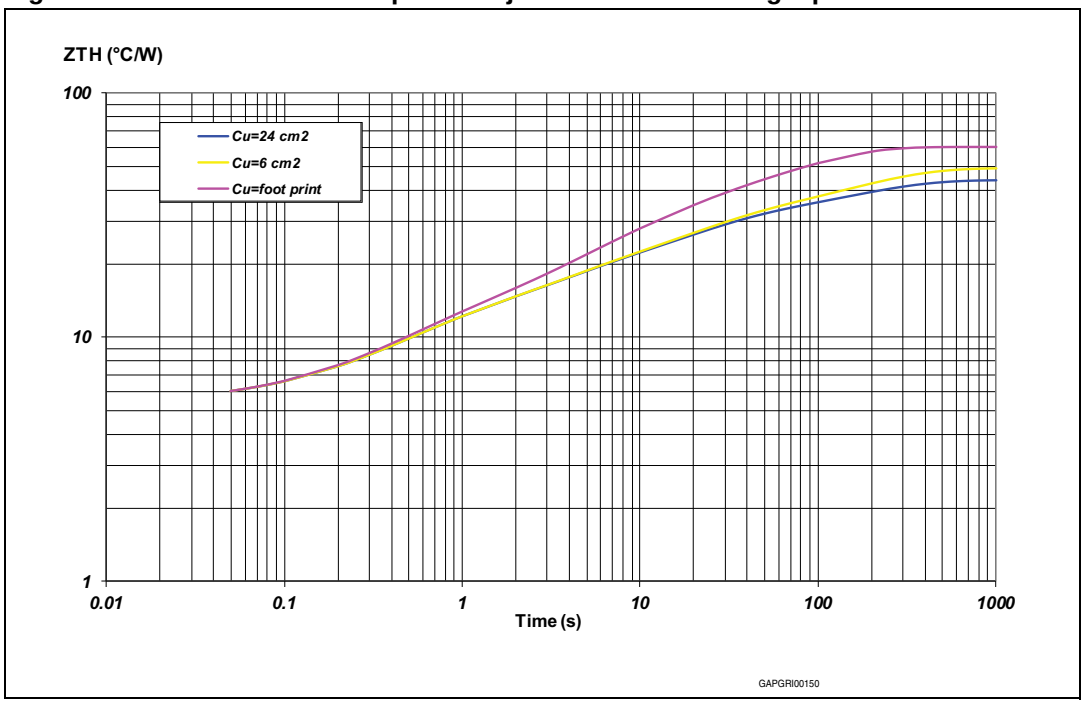
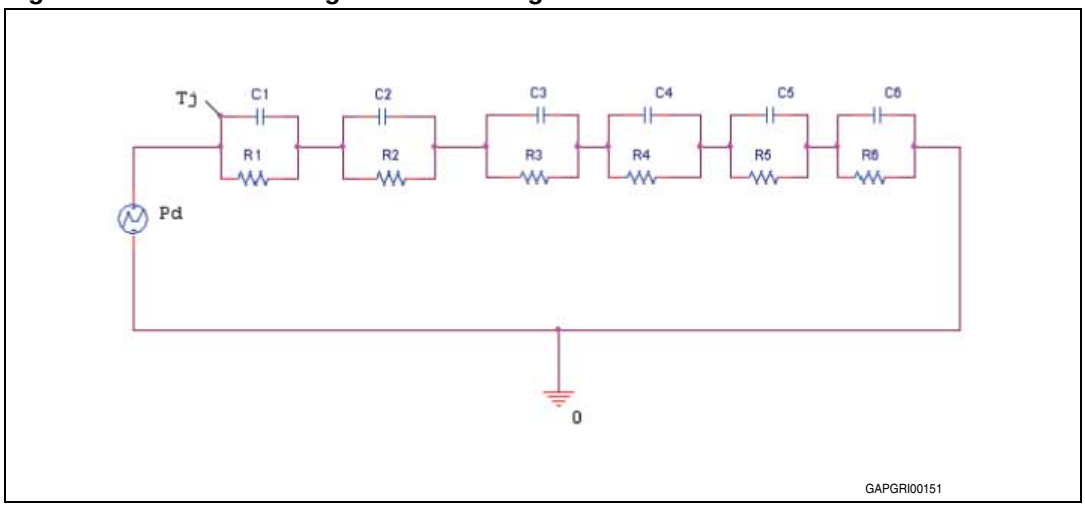


Figure 38. Thermal fitting model of a single channel HSD in SO-16L



Equation 5: pulse calculation formula:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

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Table 15. Thermal parameter

Area/island (cm^2)	Footprint	2	8
R1 (°C/W)	1.2		
R2 (°C/W)	4.2		
R3 (°C/W)	5		
R4 (°C/W)	8	6	6
R5 (°C/W)	14	13	13
R6 (°C/W)	28	20	14.5
C1 (W.s/°C)	0.0008		
C2 (W.s/°C)	0.002		
C3 (W.s/°C)	0.1		
C4 (W.s/°C)	0.5		
C5 (W.s/°C)	1	1.5	1.5
C6 (W.s/°C)	3	9	12

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5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 Package mechanical data

Figure 39. SO-16L package dimensions

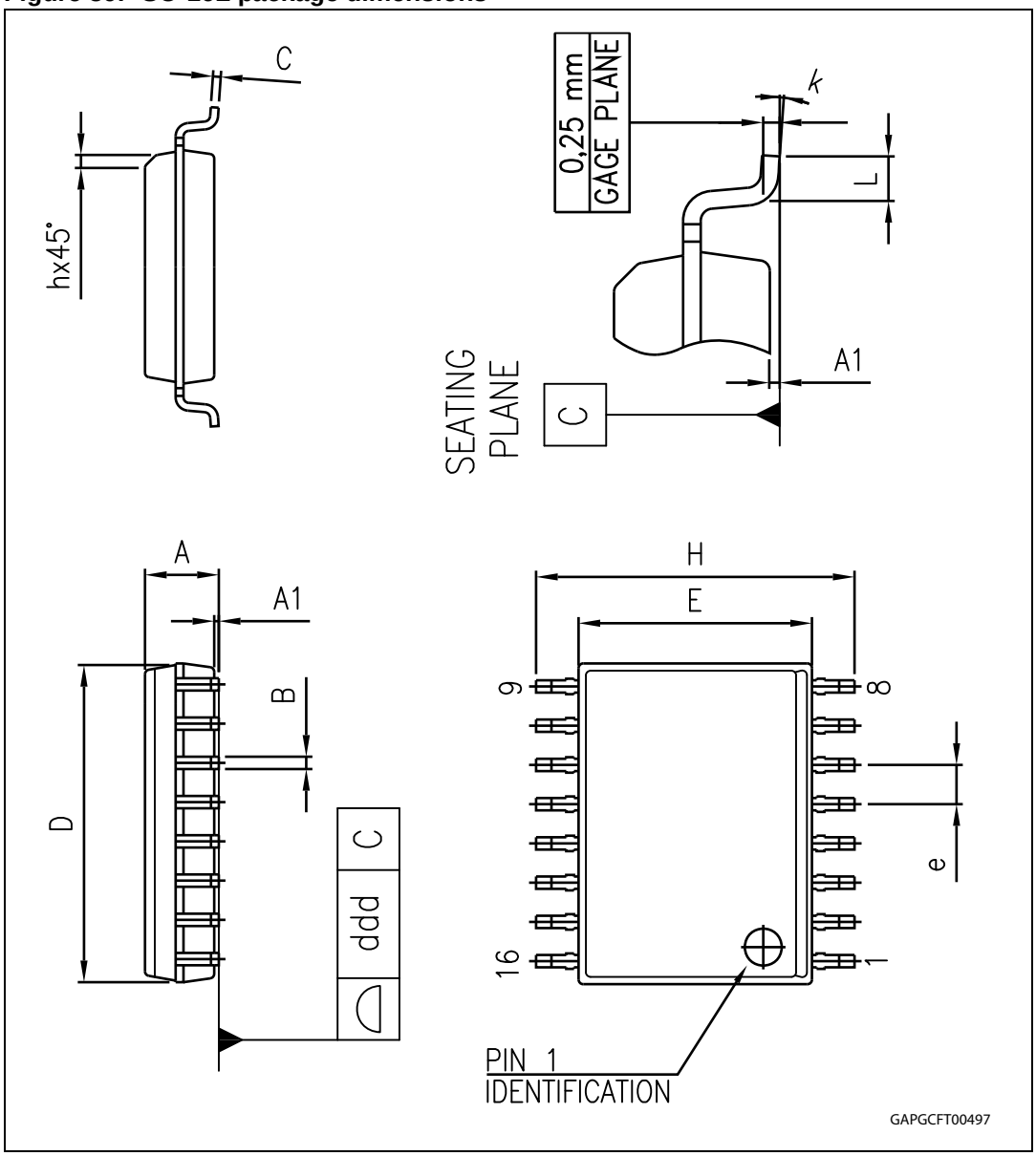

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Table 16. SO-16L mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	10.10		10.50
E	7.40		7.60
e		1.27	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

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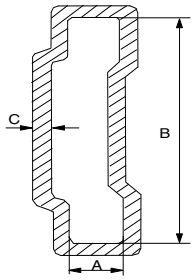
5.3 Packing information

Figure 40. SO-16L tube shipment (no suffix)



Base Q.ty	50
Bul k Q.ty	1000
Tube le ngth (± 0. 5)	532
A	3.5
B	13.8
C (± 0. 1)	0.6

All dimensio ns are in mm.

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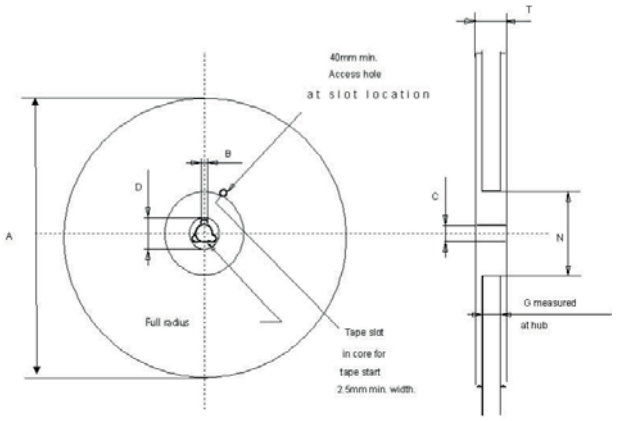
Figure 41. SO-16L tape and reel shipment (suffix "TR")



Reel dimensions

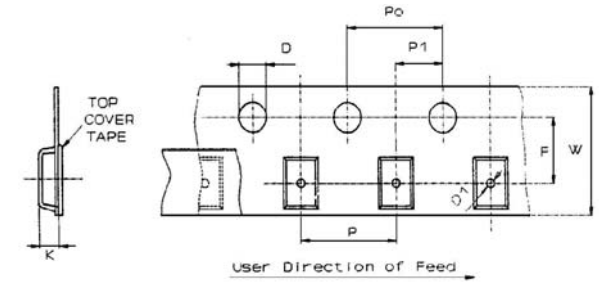
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

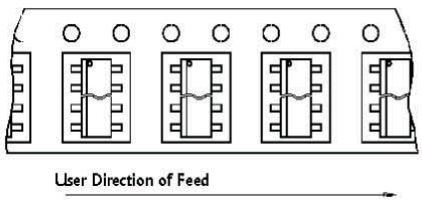
Tape dimensions

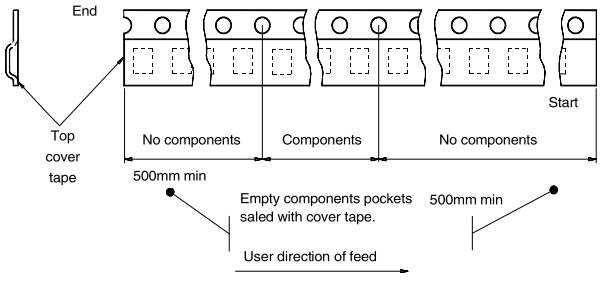
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







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6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-16L	VN5E160ASO-E	VN5E160ASOTR-E

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7 Revision history

Table 18. Document revision history

Date	Revision	Changes
14-Dec-2011	1	Initial release.
03-May-2012	2	Update *Table 5: Power section* Added *Section 4: Package and PC board thermal data*
25-Jun-2012	3	*Table 4: Thermal data*: – $R_{thj\text{-}pins}$: removed row – $R_{thj\text{-}pcb}$: added row
18-Sep-2012	4	Updated *Table 4: Thermal data*
18-Sep-2013	5	Updated disclaimer.

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