# VN10K

#### **Thermal Characteristics**

Package	Ι <sub>D</sub> (continuous) <sup>†</sup>	Ι <sub>D</sub> (pulsed)	Power Dissipation @T <sub>c</sub> = 25°C	l <sub>DR</sub> <sup>†</sup>	I DRM
TO-92	310mA	1.0A	1.0W	310mA	1.0A

Notes:

†  $I_{p}$  (continuous) is limited by max rated  $T_{i}$ . (VN0106N3 can be used if an  $I_{p}$  (continuous) of 500mA is needed.)

#### **Electrical Characteristics** (*T<sub>A</sub>* = 25°C unless otherwise specified)

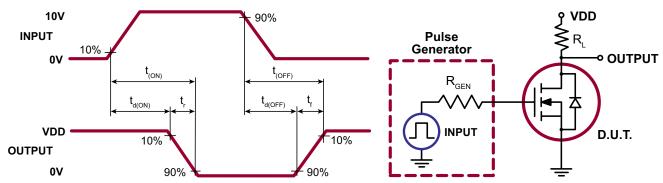
Sym	Parameter	Min	Тур	Max	Units	Conditions	
BV <sub>DSS</sub>	Drain-to-source breakdown voltage	60	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 100µA	
V <sub>GS(th)</sub>	Gate threshold voltage	0.8	-	2.5	V	$V_{GS} = V_{DS}, I_{D} = 1.0 \text{mA}$	
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.8	-	mV/ºC	$V_{GS} = V_{DS}, I_{D} = 1.0 \text{mA}$	
I <sub>GSS</sub>	Gate body leakage	-	-	100	nA	V <sub>GS</sub> = 15V, V <sub>DS</sub> = 0V	
	Zero gate voltage drain current		-	10		$V_{GS} = 0V, V_{DS} = 45V$	
I <sub>DSS</sub>			-	500	μA	$V_{GS} = 0V, V_{DS} = 45V, T_{A} = 125^{\circ}C$	
I <sub>D(ON)</sub>	On-state drain current	0.75	-	-	A	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 10V	
	Statia drain to acurac an atota registeres	-	-	7.5	Ω	V <sub>GS</sub> = 5.0V, I <sub>D</sub> = 200mA	
R <sub>DS(ON)</sub>	Static drain-to-source on-state resistance	-	-	5.0		V <sub>GS</sub> = 10V, I <sub>D</sub> = 500mA	
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.7	-	%/°C	V <sub>GS</sub> = 10V, I <sub>D</sub> = 500mA	
G <sub>FS</sub>	Forward transductance	100	-	-	mmho	$V_{\rm DS}$ = 10V, $I_{\rm D}$ = 500mA	
C <sub>ISS</sub>	Input capacitance	-	48	60		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0MHz	
C <sub>oss</sub>	Common source output capacitance	-	16	25	pF		
C <sub>RSS</sub>	Reverse transfer capacitance	-	2.0	5.0			
t <sub>(ON)</sub>	Turn-on time	-	-	10	ns	$V_{DD} = 15V,$ $I_{D} = 600mA,$	
t <sub>(OFF)</sub>	Turn-off time	-	-	10	113	$R_{gen} = 25\Omega$	
V <sub>SD</sub>	Diode forward voltage drop	-	0.8	-	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 500mA	
t <sub>rr</sub>	Reverse recovery time	-	160	-	ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 500mA	

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

2. All A.C. parameters sample tested.

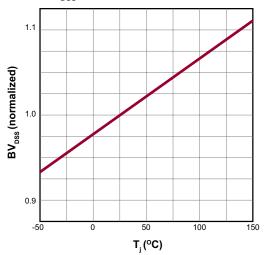
### **Switching Waveforms and Test Circuit**

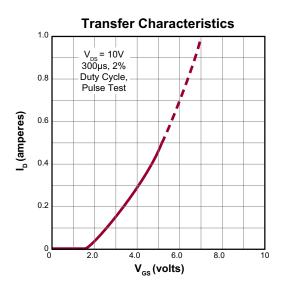


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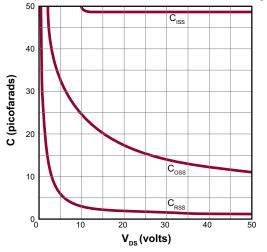
### **Typical Performance Curves**

#### **BV**<sub>DSS</sub> Variation with Temperature

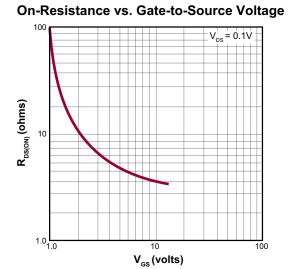




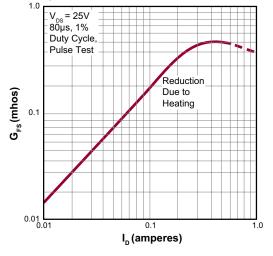
Capacitance vs. Drain-to-Source Voltage



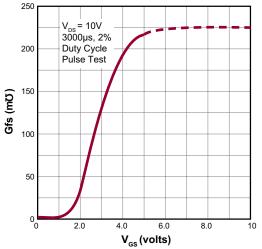
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**Output Conductance vs Drain Current** 

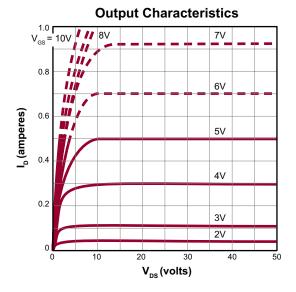




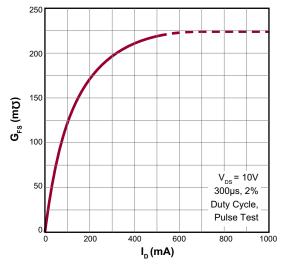


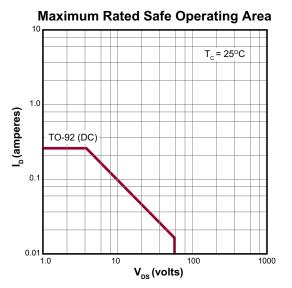
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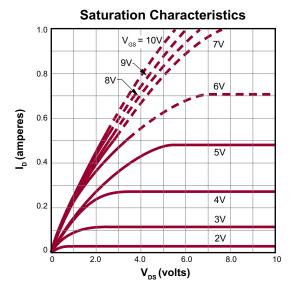
#### Typical Performance Curves (cont.)



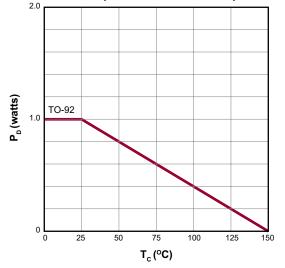
Transconductance vs. Drain Current

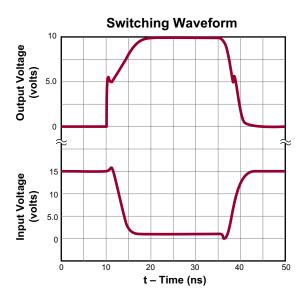






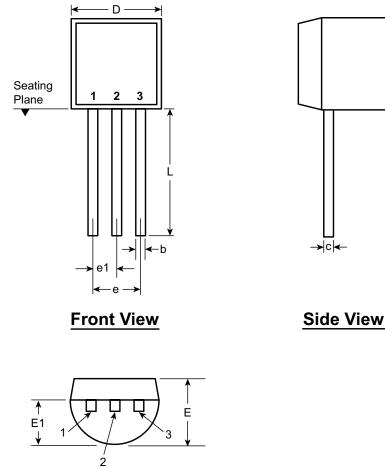
Power Dissipation vs. Case Temperature





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# 3-Lead TO-92 Package Outline (N3)



Bottom View

Symb	ol	Α	b	С	D	E	E1	е	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

*†* This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <u>http://www.supertex.com/packaging.html</u>.)

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