

ORDER NUMBER(S):**USB2640i/USB2641i-HZH-XX for 48-PIN, QFN LEAD-FREE ROHS COMPLIANT PACKAGE**

“XX” in the order number indicates the internal ROM firmware revision level.

Please contact your SMSC representative for more information.



80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Copyright © 2009 SMSC or its subsidiaries. All rights reserved.

Circuit diagrams and other information relating to SMSC products are included as a means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. Although the information has been checked and is believed to be accurate, no responsibility is assumed for inaccuracies. SMSC reserves the right to make changes to specifications and product descriptions at any time without notice. Contact your local SMSC sales office to obtain the latest specifications before placing your product order. The provision of this information does not convey to the purchaser of the described semiconductor devices any licenses under any patent rights or other intellectual property rights of SMSC or others. All sales are expressly conditional on your agreement to the terms and conditions of the most recently dated version of SMSC's standard Terms of Sale Agreement dated before the date of your order (the "Terms of Sale Agreement"). The product may contain design defects or errors known as anomalies which may cause the product's functions to deviate from published specifications. Anomaly sheets are available upon request. SMSC products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of SMSC and further testing and/or modification will be fully at the risk of the customer. Copies of this document or other SMSC literature, as well as the Terms of Sale Agreement, may be obtained by visiting SMSC's website at <http://www.smSC.com>. SMSC is a registered trademark of Standard Microsystems Corporation ("SMSC"). Product names and company names are the trademarks of their respective holders.

SMSC DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT AND THE LIKE, AND ANY AND ALL WARRANTIES ARISING FROM ANY COURSE OF DEALING OR USAGE OF TRADE. IN NO EVENT SHALL SMSC BE LIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES; OR FOR LOST DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND; REGARDLESS OF THE FORM OF ACTION, WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF SMSC OR OTHERS; STRICT LIABILITY; BREACH OF WARRANTY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER OR NOT SMSC HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Overview

The SMSC USB2640i/USB2641i is an integrated USB 2.0 compliant, Hi-Speed hub for USB port expansion with an attached bulk only mass storage class peripheral controller. This multi-format flash media controller and USB Hub Combo features three downstream ports: one port is dedicated to an internally connected ultra fast flash media reader/writer and two exposed downstream ports are available for external peripheral expansion.

The SMSC USB2640i/USB2641i is an ultra fast, OEM-configurable, hub controller IC with three downstream ports for embedded USB solutions. The USB2640i/USB2641i will attach to an upstream port as a Full-Speed Hub or as a Full-/Hi-Speed Hub. The hub supports Low-Speed, Full-Speed, and Hi-Speed (if operating as a Hi-Speed Hub) downstream devices on all of the enabled downstream ports.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors on D+ and D– pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB2640i/USB2641i includes programmable features such as:

PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB2640i/USB2641i hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB2640i/USB2641i automatically reorders the remaining ports to match the USB host controller's port numbering scheme.

PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D–) to connectors avoiding uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost which enables four programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost attempts to restore USB signal integrity that has been compromised by system level variables such as poor PCB layout, long cables, etc.

Device Features

Hardware Features

- Single chip flash media controller
- The SMSC USB2640i/USB2641i supports the industrial temperature range of -40°C to 85°C
- Transaction translator (TT) in the hub supports operation of FS and LS peripherals
- Full power management with individual or ganged power control of each downstream port
- Optional support for external firmware access via SPI interface
 - 30 MHz or 60 MHz operation support
 - Single bit or dual bit mode support
 - Mode 0 or mode 3 SPI support

Compliant with the following flash media card specifications:

- Secure Digital 2.0 / MultiMediaCard 4.2
 - SD 2.0, HS-SD, HC-SD
 - TransFlash[™] and reduced form factor media
 - 1/4/8 bit MMC 4.2
- SDIO and MMC streaming mode support
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
 - Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- xD-Picture Card 1.2 (USB2640i only)
- On board 24 MHz crystal driver circuit
- Optional external 24 MHz clock input
 - Must be used with an external resistor divider to provide a 1.8 V signal
- Up to 9 GPIOs: Configuration and polarity for special function use such as LED indicators, button inputs, and power control to memory devices
 - The number of actual GPIOs depends on the implementation configuration used
 - One GPIO available with up to 200 mA drive and protected “fold-back” short circuit current
- 8051 8-bit microprocessor
 - 60 MHz - single cycle execution
 - 64 KB ROM; 9 KB RAM
- Internal regulator for 1.8 V core operation
- Optimized pinout improves signal flow, easing implementation and allowing for improved signal integrity treatment

Software Features

- Optimized for low latency interrupt handling
- Hub and flash media reader/writer configuration from a single source: External I²C ROM or external SPI ROM
- EEPROM update via USB
- Please see the USB2640i/USB2641i Software Release Notes for additional software features

OEM Selectable Features

Hub

A default configuration is available in USB2640i/USB2641i following a reset. The USB2640i/USB2641i may also be configured by an external I²C EEPROM or via external SPI ROM flash.

The USB2640i/USB2641i supports several OEM selectable features:

- Compound Device support (port is permanently hardwired to a downstream USB peripheral device), on a port-by-port basis.
- Select over-current sensing and port power control on an individual (port-by-port) or ganged (all ports together) basis to match the OEM's choice of circuit board component selection.
- Port power control and over-current detection/delay features
- Configure the delay time for filtering the over-current sense inputs.
- Configure the delay time for turning on downstream port power.
- Bus- or self-powered selection
- Hub port disable or non-removable configurations
- Flexible port mapping and disable sequence. Ports can be disabled/reordered in any sequence to support multiple platforms with a single design. The hub will automatically reorder the remaining ports to match the host controller's numbering scheme.
- Programmable USB differential-pair pin location.
 - Eases PCB layout by aligning USB signal lines directly to connectors
- Programmable USB signal drive strength. Recover USB signal integrity due to compromised system environments using 4 levels of signal drive strength.
- Indicate the maximum current that the 2-port hub consumes from the USB upstream port.
- Indicate the maximum current required for the hub controller.

Flash Media Controller

- Customize vendor ID, product ID, and device ID.
- 12-hex digit (max) serial number string
- Customizable vendor specific data by optional use of external serial EEPROM
- 28-character manufacturer ID and product string for flash media reader/writer
- LED blink interval or duration

The block diagram illustrates the internal architecture of the USB 2.0 to FireWire 400 Bridge IC. The IC is organized into several functional blocks and interfaces:

- External Interfaces (Left):**
 - To Upstream V_{BUS} :** Connected to the Bus-Power Detect/ V_{BUS} Pulse block.
 - Upstream USB Data:** Connected to the Upstream PHY block.
 - 3.3 V Crystal:** Connected to the PLL and 1.8 V Reg blocks.
 - 1.8 V:** Connected to the 1.8 V Reg block.
- Internal Blocks:**
 - Bus-Power Detect/ V_{BUS} Pulse:** Manages power detection and pulse generation.
 - Upstream PHY:** USB 2.0 PHY interface.
 - Repeater:** Signal repeater for USB data.
 - Serial Interface Engine:** Manages serial communication.
 - Controller:** Central control logic.
 - Port Controller:** Manages port operations.
 - Transaction Translator:** Translates between USB and FireWire protocols.
 - Routing & Port Re-Ordering Logic:** Manages data routing and port re-ordering.
 - PHY (Port #3 and Port #2):** FireWire PHY interfaces.
 - OC Sense Switch Driver:** Drivers for OC sense switches.
 - BRIDGE:** Core bridge logic.
 - SIE CTL:** Serial Interface Engine Control Logic.
 - BUS INTFC:** Bus interface blocks.
 - RAM:** Internal memory (3 K total), including EP0 TX, EP0 RX, EP2 RX, and EP2 TX.
 - BUS INTFC + XDATA BRIDGE + BUS ARBITER:** Manages bus arbitration and data transfer.
 - 8051 PROCESSOR:** On-chip microcontroller.
 - SFR RAM:** Special Function Register RAM.
 - ADDR MAP:** Address map for RAM (6 K) and ROM (64 K).
 - PWR_FET0:** Power FET control.
 - GPIOs:** General Purpose I/Os (6 pins).
 - SPI (4 pins) / GPIO (2 pins):** Serial Peripheral Interface and General Purpose I/O.
 - GPIO10 (CRD_PWR):** General Purpose I/O for CRD power.
 - AUTO_CBW PROC:** Auto Command Wrapper Processor.
 - BUS INTFC:** Bus interface for FireWire.
 - FMDU CTL:** FireWire Media Data Unit Control Logic.
 - Flash Media Cards:** Supports SD/MMC, MS, and xD cards (require Combo socket).
- Internal Connections:**
 - The 8051 Processor is connected to SFR RAM, ADDR MAP, and the Controller.
 - The Controller is connected to the Serial Interface Engine, Port Controller, Transaction Translator, and Routing & Port Re-Ordering Logic.
 - The Port Controller is connected to the Transaction Translator and the Routing & Port Re-Ordering Logic.
 - The Transaction Translator is connected to the Routing & Port Re-Ordering Logic and the PHY blocks.
 - The Routing & Port Re-Ordering Logic is connected to the PHY blocks and the BRIDGE.
 - The BRIDGE is connected to the SIE CTL and the BUS INTFC.
 - The BUS INTFC is connected to the RAM and the BUS INTFC + XDATA BRIDGE + BUS ARBITER.
 - The RAM is connected to the BUS INTFC + XDATA BRIDGE + BUS ARBITER.
 - The BUS INTFC + XDATA BRIDGE + BUS ARBITER is connected to the 8051 Processor, the PWR_FET0, the GPIOs, and the Flash Media Cards.
 - The PWR_FET0 is connected to the 8051 Processor and the GPIOs.
 - The GPIOs are connected to the 8051 Processor and the PWR_FET0.
 - The SPI is connected to the 8051 Processor and the PWR_FET0.
 - The GPIO10 (CRD_PWR) is connected to the 8051 Processor and the PWR_FET0.
 - The AUTO_CBW PROC is connected to the BUS INTFC + XDATA BRIDGE + BUS ARBITER.
 - The BUS INTFC is connected to the BUS INTFC + XDATA BRIDGE + BUS ARBITER.
 - The FMDU CTL is connected to the BUS INTFC + XDATA BRIDGE + BUS ARBITER.
 - The Flash Media Cards are connected to the BUS INTFC + XDATA BRIDGE + BUS ARBITER.

Revision 2.1 (06-29-09)

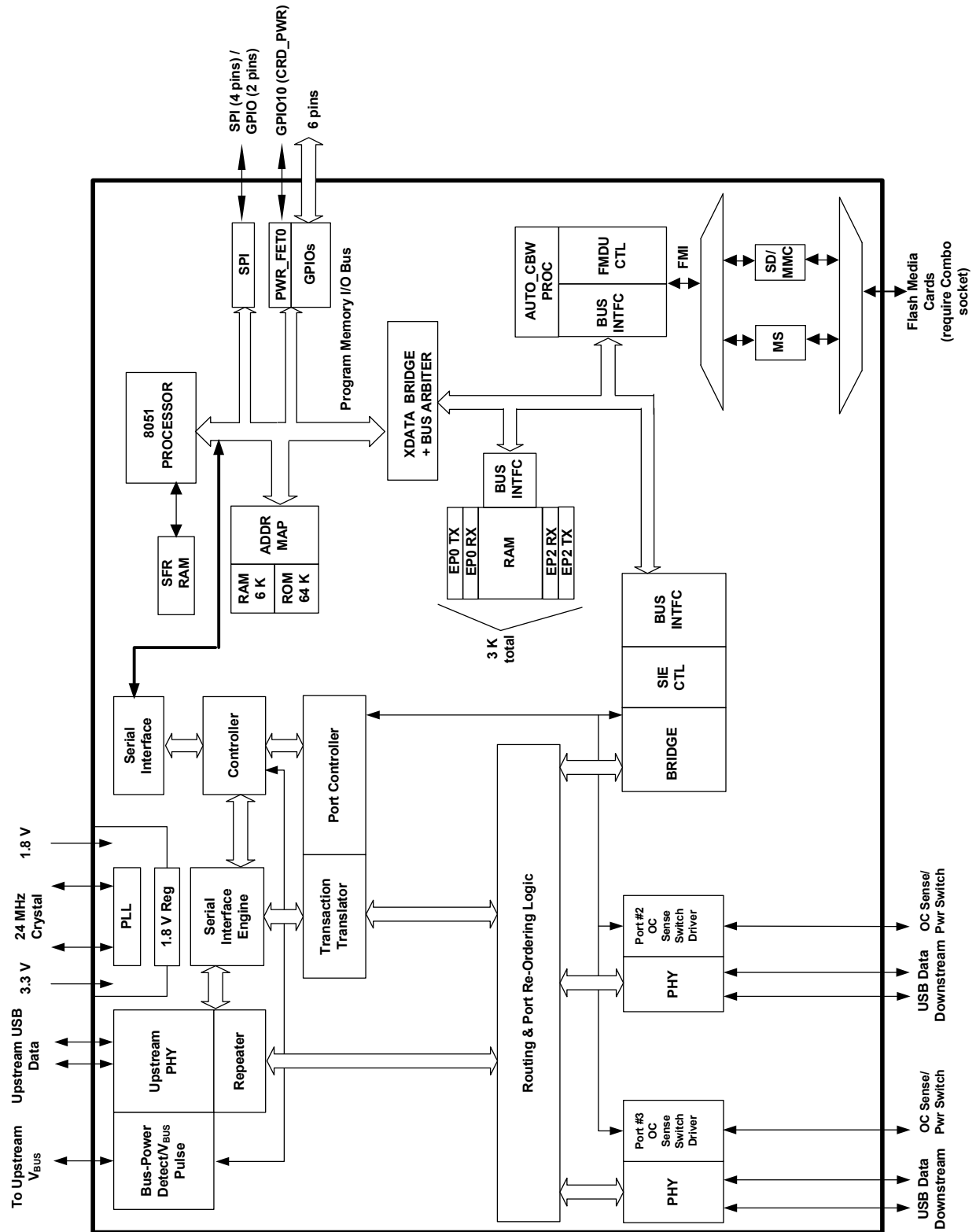


Figure 2 USB2641i Block Diagram

Package Outline

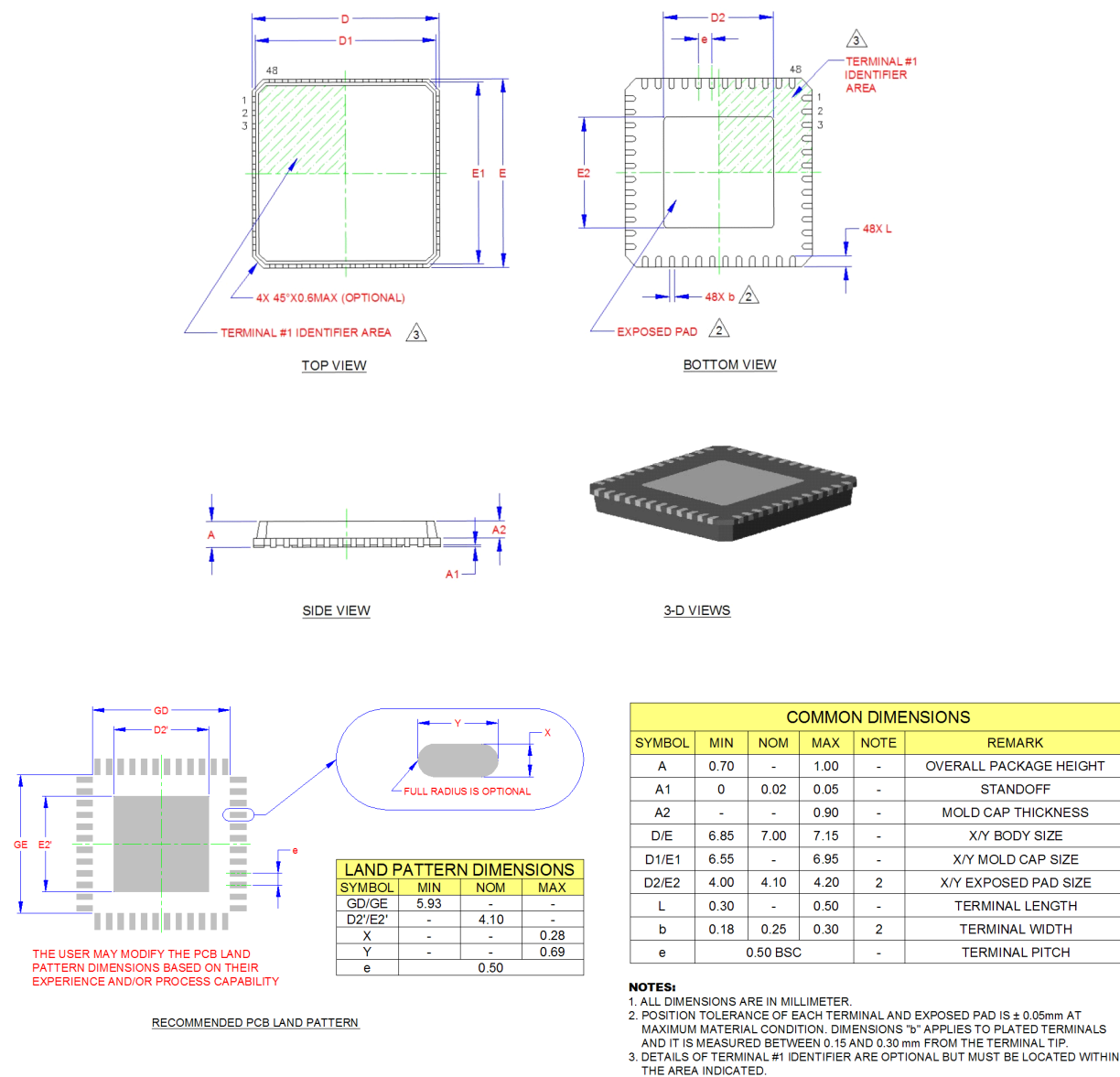


Figure 3 48-Pin QFN Package