Description (continued)

The inputs are compatible with 5 and 12 V logic systems: TTL, Schottky TTL, DTL, PMOS, and CMOS. In all cases, the output is switched ON by an active high input level. Compared to predecessor devices, the UDN2987LW-6 has a significantly faster T_{PHL} (200 ns typical) and a lower driver supply voltage rating (4.75 V), which allows the use of 5 V logic.

The UDN2987LW-6 is supplied in a 20-lead small-outline (SOIC-W) plastic package. All packages are lead (Pb) free, with 100% matte-tin leadframe plating.

Selection Guide

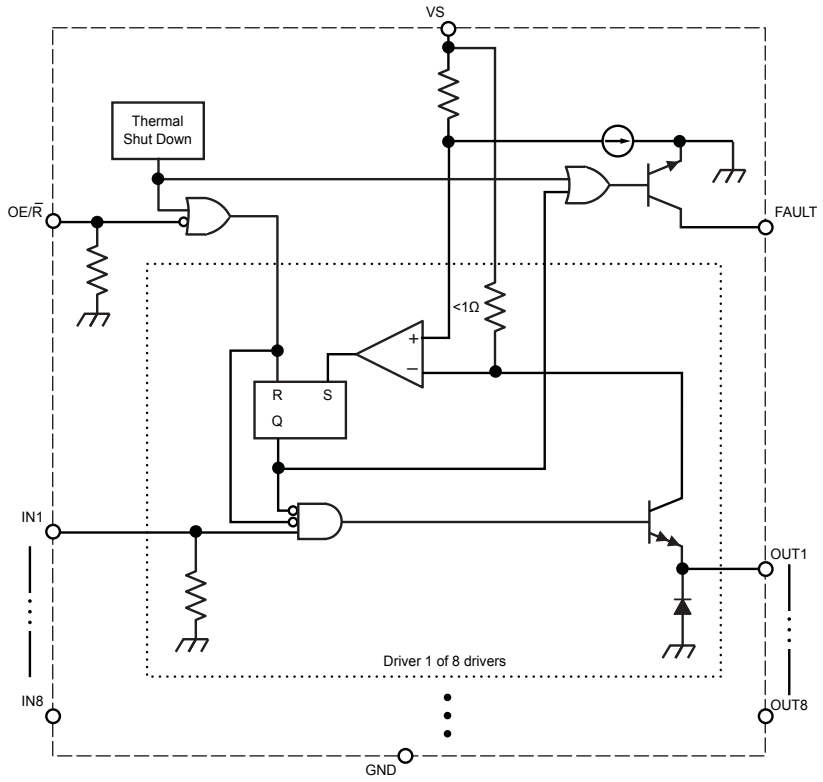
Part Number	Packing	Package
UDN2987LWTR-6-T	1000 pieces/13-in. reel	20-pin SOIC, wide body

Absolute Maximum Ratings

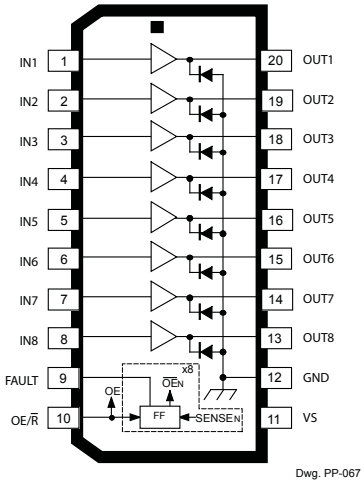
Parameter	Symbol	Notes	Rating	Units
Supply Voltage	V_S		35	V
Continuous Output Current*	I_{OUT}	Outputs are disabled at approximately –500 mA	–500	mA
FAULT Output Voltage	V_{CE}		35	V
FAULT Output Current	I_C		30	mA
Input Voltage	V_{IN}		–0.3 to 14	V
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_S	Range N	–55 to 150	°C
Operating Temperature Range	T_A		–20 to 85	°C

*For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

Functional Block Diagram



Pin-Out Diagram



Dwg. PP-067

Terminal List Table

Number	Name	Description
1	IN1	Logic input 1
2	IN2	Logic input 2
3	IN3	Logic input 3
4	IN4	Logic input 4
5	IN5	Logic input 5
6	IN6	Logic input 6
7	IN7	Logic input 7
8	IN8	Logic input 8
9	FAULT	Fault output
10	OE/R̄	Logic input for Output Enable and Reset
11	VS	Supply voltage
12	GND	Supply ground
13	OUT8	Output 8 to load
14	OUT7	Output 7 to load
15	OUT6	Output 6 to load
16	OUT5	Output 5 to load
17	OUT4	Output 4 to load
18	OUT3	Output 3 to load
19	OUT2	Output 2 to load
20	OUT1	Output 1 to load

ELECTRICAL CHARACTERISTICS, valid at T_A = 25°C, V_{OER} = 2.4 V, V_S = 35 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
Supply Voltage Functional Range	V_S		4.75	—	35	V
Output Leakage Current[2]	I_{OUTCEX}	V_{IN} = 0.4 V, all inputs simultaneously	– 200	<–5.0	–	µA
Output Sustaining Voltage	$V_{OUT(sus)}$	I_{OUT} = –350 mA, L = 2.0 mH	35	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{IN} = 2.4 V, I_{OUT} = –100 mA	—	1.6	1.8	V
		V_{IN} = 2.4 V, I_{OUT} = –225 mA	—	1.7	1.9	V
		V_{IN} = 2.4 V, I_{OUT} = –350 mA	—	1.8	2.0	V
Channel Shut Down Threshold[2]	I_M	V_{IN} = 2.4 V, V_s = 30 V	–	–500	– 370	mA
FAULT Leakage Current	I_{CEX}	V_{CC} = 35 V	—	<1.0	100	µA
FAULT Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 mA	—	0.3	0.8	V
Input Voltage	$V_{IN(ON)}$		2.4	—	—	V
	$V_{IN(OFF)}$		—	—	0.4	V
Input Current: INx, OE/$\overline{R}$ pins	$I_{IN(ON)}$	V_{IN} = 2.4 V	—	—	100	µA
		V_{IN} = 5.0 V	—	—	600	µA
		V_{IN} = 12 V	—	—	1000	µA
	$I_{IN(OFF)}$	V_{IN} = 0.4 V	—	—	15	µA
Clamp Diode Leakage Current	I_R	V_R = 35 V, T_A = 70°C	—	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.5	1.8	V
Supply Current	$I_{S(ON)}$	V_{IN} = 2.4 V, all inputs simultaneously; outputs open	—	7.0	18	mA
	$I_{S(OFF)}$	V_{IN} = 0.4 V, all inputs simultaneously	—	6.0	12	mA
Thermal Shut Down	T_{JTSD}		—	165	—	°C
Thermal Hysteresis	$T_{JTSDhys}$		—	15	—	°C
Reset Pulse Duration	t_{RPD}		1.0	—	—	µs
Propagation Delay Time	t_{PLH}	V_S = 35 V, R_L = 100 Ω, C_{LOAD} = 30 pF	—	100	600	ns
	t_{PHL}	V_S = 35 V, R_L = 100 Ω, C_{LOAD} = 30 pF	—	200	1000	ns
Blank Time	t_{BLANK}		—	1.0	—	µs

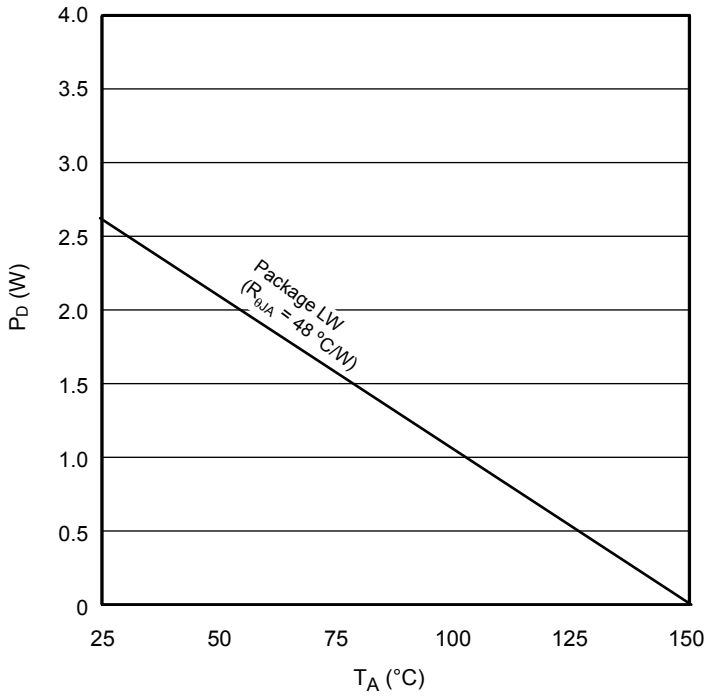
[1]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.
[2]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

THERMAL CHARACTERISTICS

Characteristics	Symbol	Test Conditions	Rating	Unit
Package Thermal Resistance*	$R_{\theta JA}$	Package LW, on 4-layer board based on JEDEC standard	48	°C/W

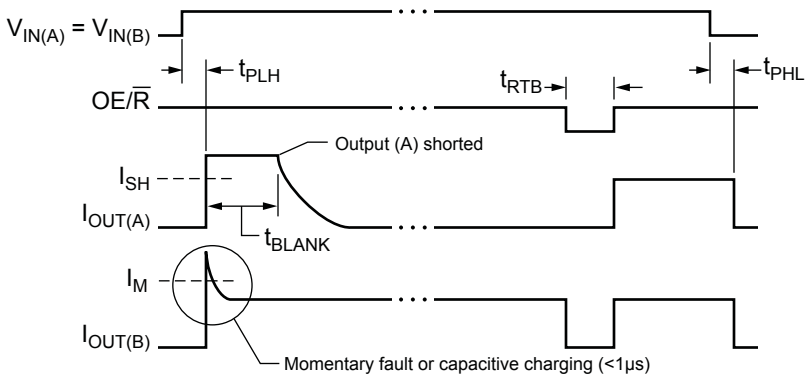
*Additional thermal information is available on the Allegro Web site.

Power Dissipation versus Ambient Temperature



Characteristic Performance

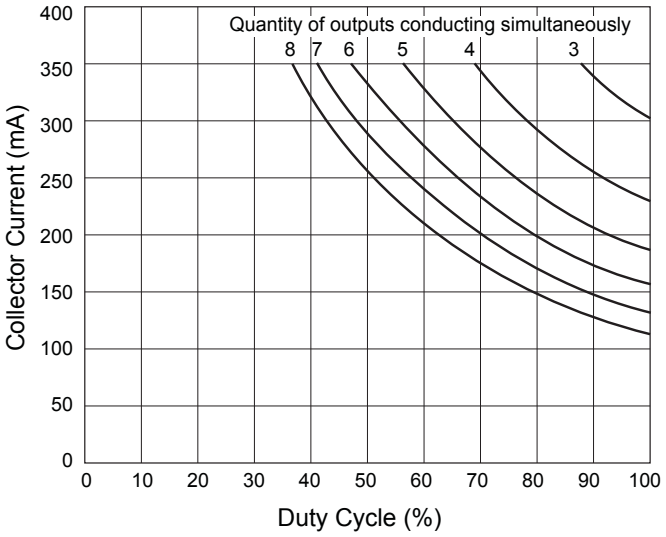
Output Current Waveshapes



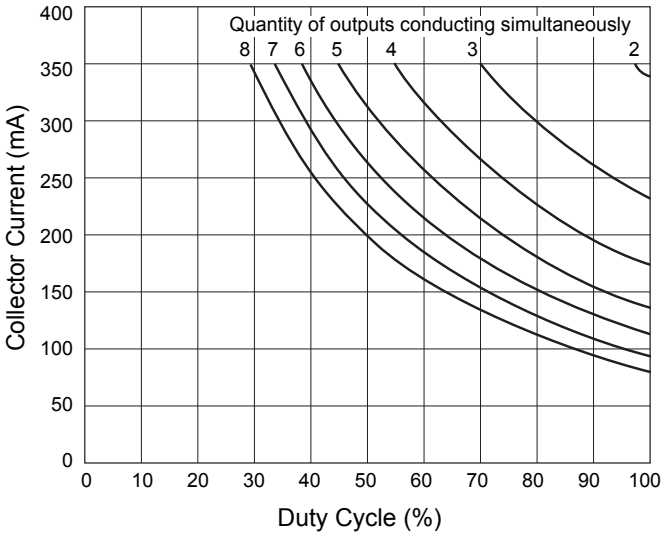
Allowable Output Current as a Function of Duty Cycle

(Multiply by 78% for UDN2987LW-6)

T_A= 25°C, V_S = 35 V



T_A= 50°C, V_S = 35 V



Applications Information and Circuit Description

As with all power integrated circuits, the UDN2987LW-6 has a maximum allowable output current rating. The 500 mA rating does not imply that operation at that value is permitted or even obtainable. The channel output current trip point is specified as –370 mA, minimum; therefore, attempted operation at current levels greater than –370 mA may cause a fault indication and channel shutdown. The device is tested at a maximum of –350 mA and that is the recommended maximum output current per driver. It provides protection for current overloads or shorted loads up to 30 V.

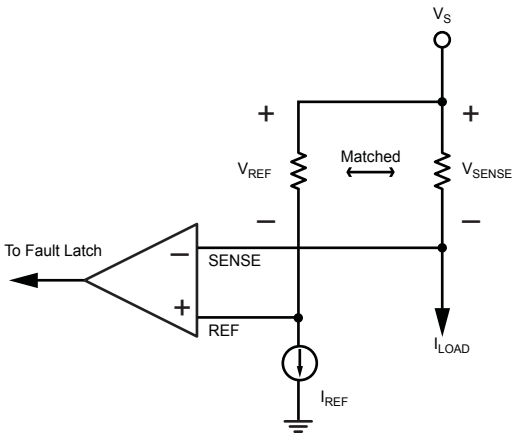
All outputs are enabled by pulling the OE/$\overline{R}$ input high. When OE/$\overline{R}$ is low or allowed to float (internal pull-down), all outputs are inhibited and the latches are reset. Note that the reset pulse duration (OE/$\overline{R}$ low) should be at least 1 µs. This will ensure safe operation under attempted reset conditions with a shorted load. The latches are also reset during power-up, regardless of the state of the OE/$\overline{R}$ input.

The load current causes a small voltage drop across the internal low-value sense resistor. This voltage is compared to the voltage drop across a reference resistor with a constant current. The two resistors are matched to eliminate errors due to manufacturing tolerances or temperature effects. Each channel includes a comparator and its own latch. An overcurrent fault ($V_{SENSE} > V_{REF}$) will set the affected latch and shut down only that channel. All other channels will continue to operate normally. The latch includes a 1 µs blanking delay, t_{BLANK}, to prevent unwanted triggering due to crossover currents generated when switching inductive loads. For an abrupt short circuit, the blanking and output switching times will allow a brief, permissible current in excess of the trip current before the output driver is turned off.

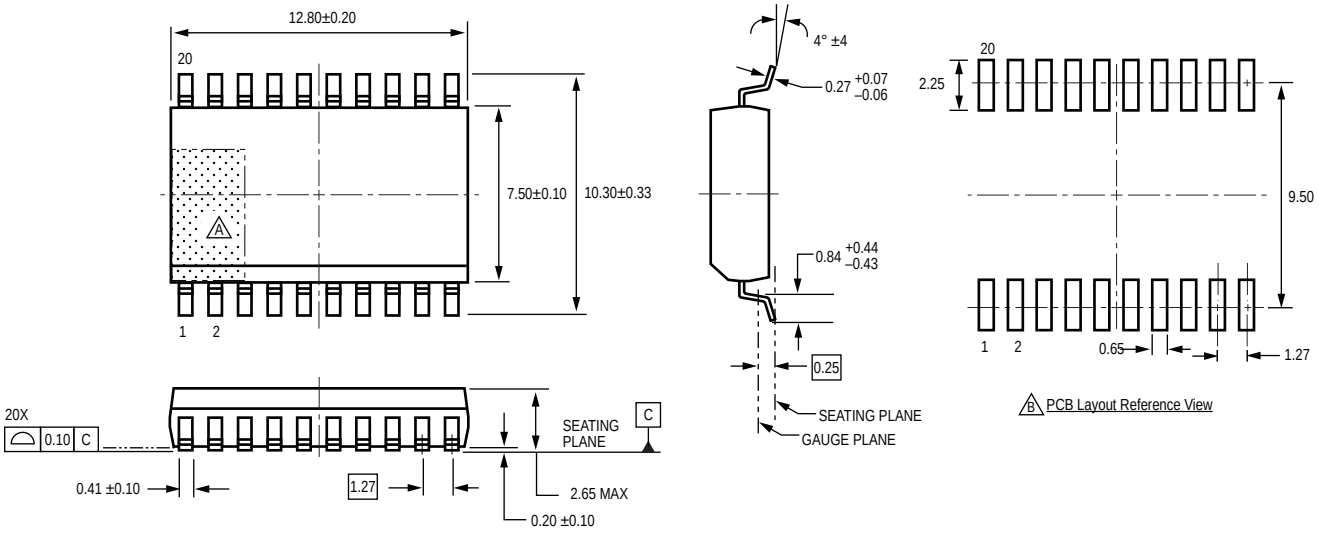
A common thermal shutdown disables all outputs if the chip temperature exceeds 165°C. At thermal shutdown, all latches are reset. The outputs are disabled until the chip cools down to approximately 150°C (thermal hysteresis).

In the event of an overcurrent condition on any channel, or chip thermal shutdown, the FAULT open-collector output is pulled low (turned on).

Overcurrent Fault Sense Circuit



Package LW, 20-pin SOIC-W



For Reference Only
Dimensions in millimeters
(Reference JEDEC MS-013 AC)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-20M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Revision History

Revision	Revision Date	Description of Revision
Rev. 6	April 30, 2012	Update product availability

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