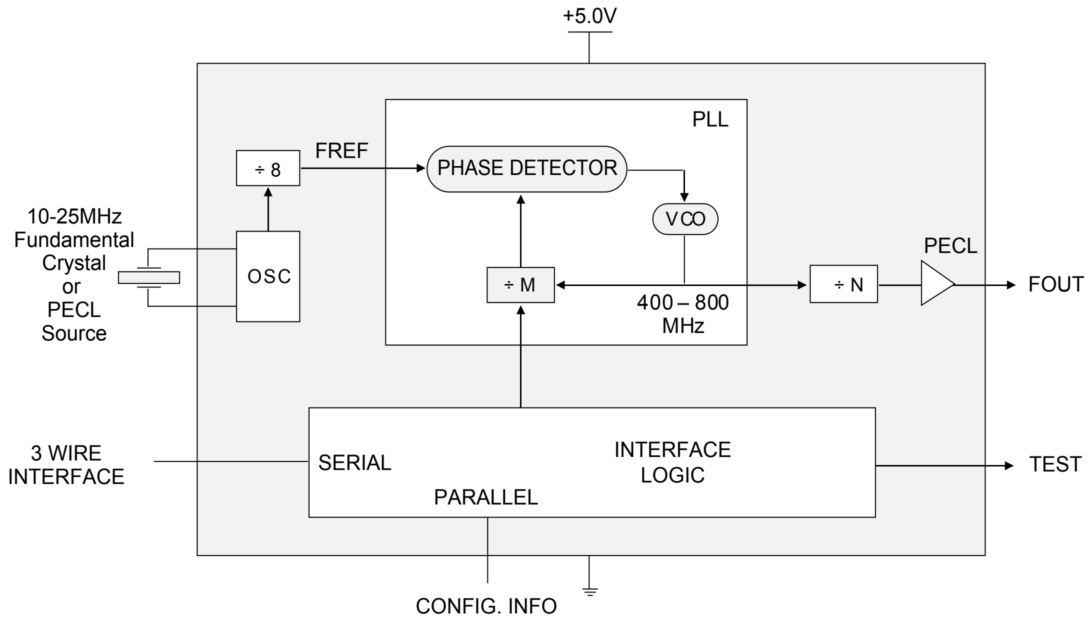
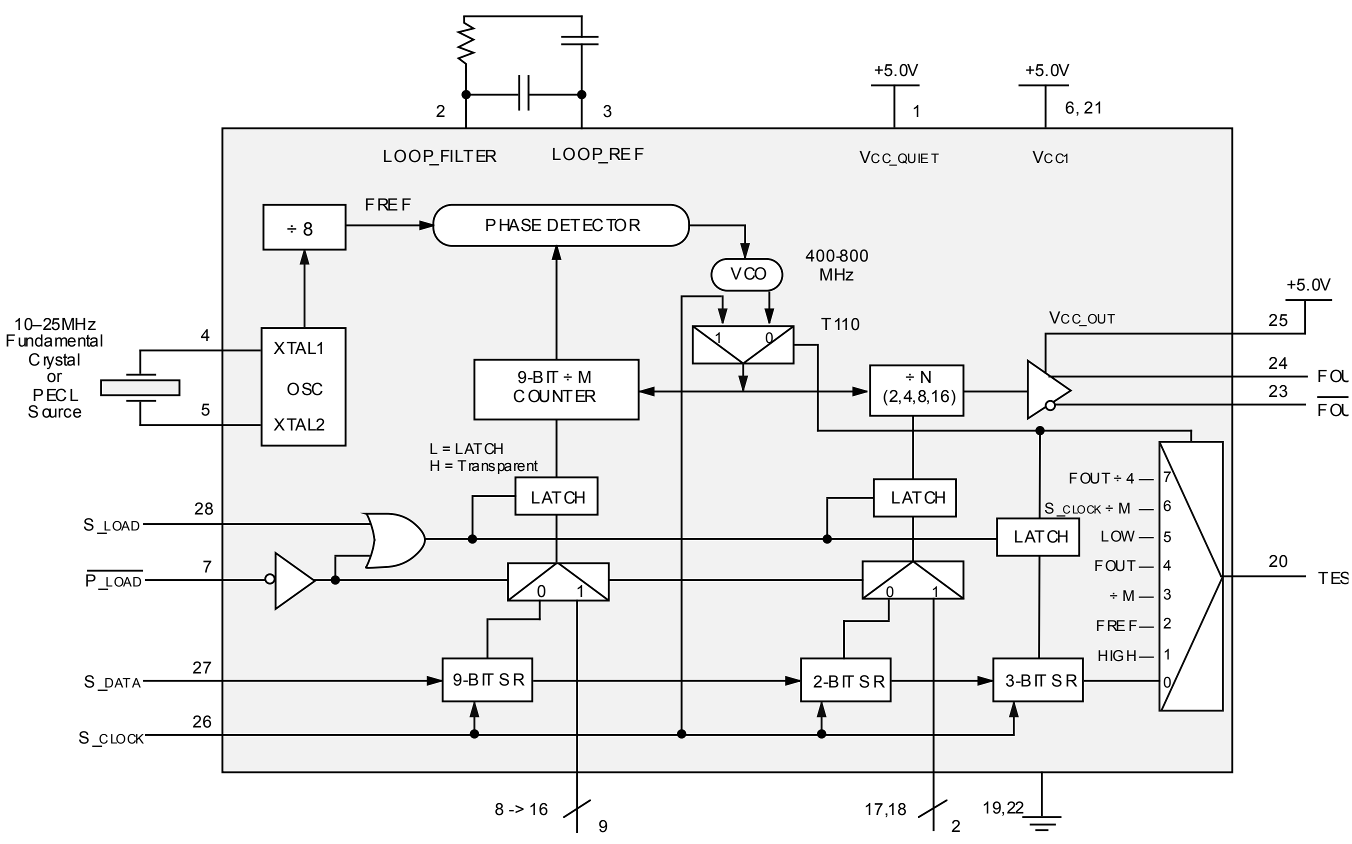
BLOCK DIAGRAM



DETAILED BLOCK DIAGRAM



NOTE:

Pin numbers reference PLCC pinout.

PIN DESCRIPTIONS

INPUTS

XTAL1, XTAL2

These pins form an oscillator when connected to an external crystal. The crystal is series resonant. Alternatively, these pins can be driven with 100K PECL level by an external source.

S_LOAD

This TTL pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH; thus, the register data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.

S_DATA

This TTL pin is the input to the serial configuration shift registers.

S_CLOCK

This TTL pin clocks the serial configuration shift registers. On the rising edge of this signal, data from S_DATA is sampled.

P_LOAD

This TTL pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW; thus, the parallel data must be stable on the LOW-to-HIGH transition of P_LOAD for proper operation.

M[8:0]

These TTL pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of P_LOAD. M[8] is the MSB, M[0] is the LSB. The binary count on the M pins equates to the divide-by value for the PLL.

N[1:0]

These TTL pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of P_LOAD.

N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	16

OUTPUTS

FOUT, $\overline{\text{FOUT}}$

These differential positive-referenced ECL signals (PECL) are the output of the synthesizer.

TEST

The function of this TTL output is determined by the serial configuration bits T[2:0].

POWER

VCC1

This is the positive supply for the chip and is normally connected to +5.0V.

VCC_OUT

This is the positive reference for the PECL outputs, FOUT and $\overline{\text{FOUT}}$. It is constrained to be less than or equal to VCC1.

VCC_QUIET

This is the positive supply for the PLL and should be as noise-free as possible for low-jitter operation.

GND

These pins are the negative supply for the chip and are normally all connected to ground.

OTHER

LOOP_FILTER

This is an analog I/O pin that provides the loop filter for the PLL.

LOOP_REF

This is an analog I/O pin that provides a reference voltage for the PLL.

WITH 16MHZ INPUT

VCO Frequency (MHz)	M Count	256 M8	128 M7	64 M6	32 M5	16 M4	8 M3	4 M2	2 M1	1 M0
400	200	0	1	1	0	0	1	0	0	0
402	201	0	1	1	0	0	1	0	0	1
404	202	0	1	1	0	0	1	0	1	0
406	203	0	1	1	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
794	397	1	1	0	0	0	1	1	0	1
796	398	1	1	0	0	0	1	1	1	0
798	399	1	1	0	0	0	1	1	1	1
800	400	1	1	0	0	1	0	0	0	0

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter		Value	Unit
V_{CC}	Power Supply Voltage		–0.5 to +7.0	V
V_I	Input Voltage		–0.5 to +7.0	V
I_{OUT}	Output Source	Continuous Surge	50 100	mA
T_{store}	Storage Temperature		–65 to +150	°C
T_A	Operating Temperature		–0 to +75	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by eight before being sent to the phase detector. With a 16MHz crystal, this provides a reference frequency of 2MHz.

The VCO within the PLL operates over a range of 400–800MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock. External loop filter components are utilized to allow for optimal phase jitter performance.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. The output divider is configured through either the serial or the parallel interfaces and can provide one of four divider ratios (2, 4, 8 or 16). This divider extends the performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated in 50ý. The positive reference for the output driver is provided by a dedicated power pin (V_{CC_OUT}) to reduce noise and provide application flexibility.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally upon system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. With S_LOAD held LOW, on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pull-up resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count.

The serial interface logic is implemented with a 14-bit shift register scheme. The register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet set-up and hold timing as specified in the AC parameters section of this data sheet. With $\overline{\text{P\_LOAD}}$ held HIGH, the configuration latches will capture the value in the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

PROGRAMMING INTERFACE

Programming the device is accomplished by properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can be represented by this formula:

$$FOUT = \left(\frac{FXTAL}{8}\right) X \frac{M}{N}$$

Where FXTAL is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be 200 M 400 for a 16MHz input reference.

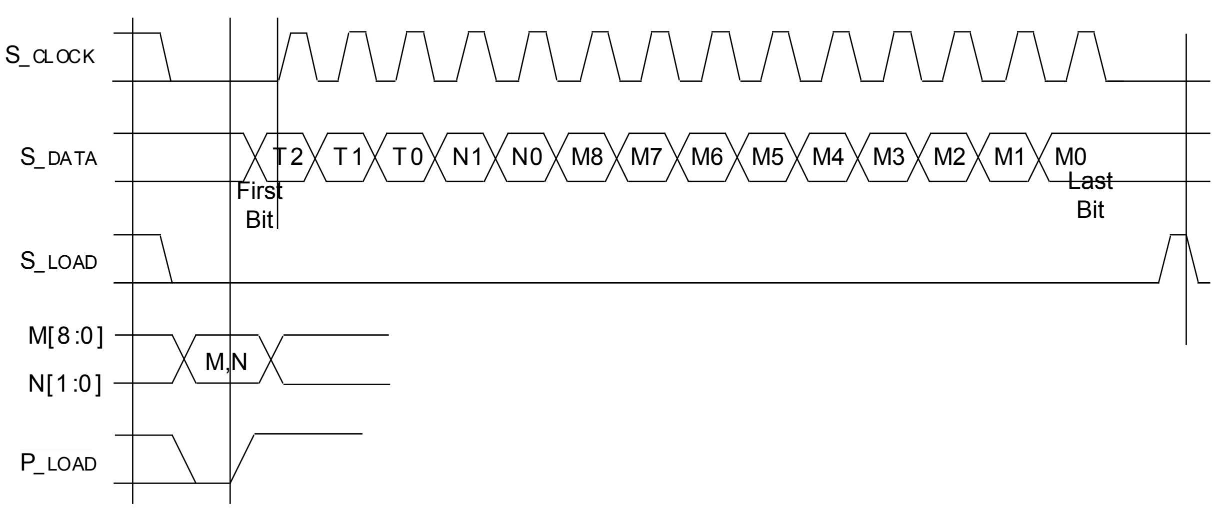
M[8:0] and N[1:0] are normally specified once at power-on, through the parallel interface, and then possibly again through the serial interface. This approach allows the designer to bring up the application at one frequency and then change or fine-tune the clock, as the ability to control the serial interface becomes available. To minimize transients in the frequency domain, the output should be varied in the smallest step size possible.

T2	T1	T0	TEST	FOUT / $\overline{\text{FOUT}}$
0	0	0	Data Out – Last Bit SR	FVCO ÷ N
0	0	1	HIGH	FVCO ÷ N
0	1	0	FREF	FVCO ÷ N
0	1	1	M Counter Output	FVCO ÷ N
1	0	0	FOUT	FVCO ÷ N
1	0	1	LOW	FVCO ÷ N
1	1	0	S_CLOCK ÷ M	S_CLOCK ÷ N
1	1	1	FOUT ÷ 4	FVCO ÷ N

The TEST output provides visibility for one of several internal nodes (as determined by the T[1:0] bits in the serial configuration stream). It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the TTL output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1, T0 configuration latches are preset to 000 when $\overline{\text{P\_LOAD}}$ is low, so that the FOUT outputs are as jitter-free as possible. The serial configuration port can be used to select one of the alternate functions for this pin.

The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8).

When T[2:0] is set to 100 the SY89429A is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree (See detailed Block Diagram). Because the S_CLOCK is a TTL level the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 125MHz as the minimum divide ratio of the N counter is 2. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.



Input S_DATA to M0 then M1, then M2, etc., as indicated above.

100H ECL DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC\_QUIET} = V_{CC\_TTL}$ = +5.0V ±5%; V_{CC_OUT} = +3.3V to +5.0V ±5%; T_A = 0°C to +75°C

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	V_{CC_OUT} –1.075	V_{CC_OUT} –0.830	V	50ý to V_{CC_OUT} –2V
V_{OL}	Output LOW Voltage	V_{CC_OUT} –1.860	V_{CC_OUT} –1.570	V	50ý to V_{CC_OUT} –2V

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC\_QUIET} = V_{CC\_TTL}$ = +5.0V ±5%; V_{CC_OUT} = +3.3V to +5.0V ±5%; T_A = 0°C to +75°C

		T_A = 0°C		T_A = +25°C		T_A = +75°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0	—	2.0	—	2.0	—	V	—
V_{IL}	Input LOW Voltage	—	0.8	—	0.8	—	0.8	V	—
I_{IH}	Input HIGH Current	—	50	—	50	—	50	µA	V_{IN} = 2.7V
I_{IL}	Input LOW Current	—	–0.6	—	–0.6	—	–0.6	mA	V_{IN} = 0.5V
V_{IK}	Input Clamp Voltage	—	–1.2	—	–1.2	—	–1.2	V	I_{IN} = –12mA
V_{OH}	Output HIGH Voltage	—	2.5	—	2.5	—	2.5	V	I_{OH} = –2.0mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 8mA
I_{OS}	Output Short Circuit Current	–80 (Typ.)		–80 (Typ.)		–80 (Typ.)		mA	V_{OUT} = 0V
I_{CC1}	Supply Current	—	225	—	225	—	225	mA	—
	Typical % of I_{CC1} V_{CC1}	91%		91%		91%			
	V_{CC_OUT}	4.5%		4.5%		4.5%			
	V_{CC_QUIET}	2.25%		2.25%		2.25%			
	V_{CC_TTL}	2.25%		2.25%		2.25%			

AC ELECTRICAL CHARACTERISTICS

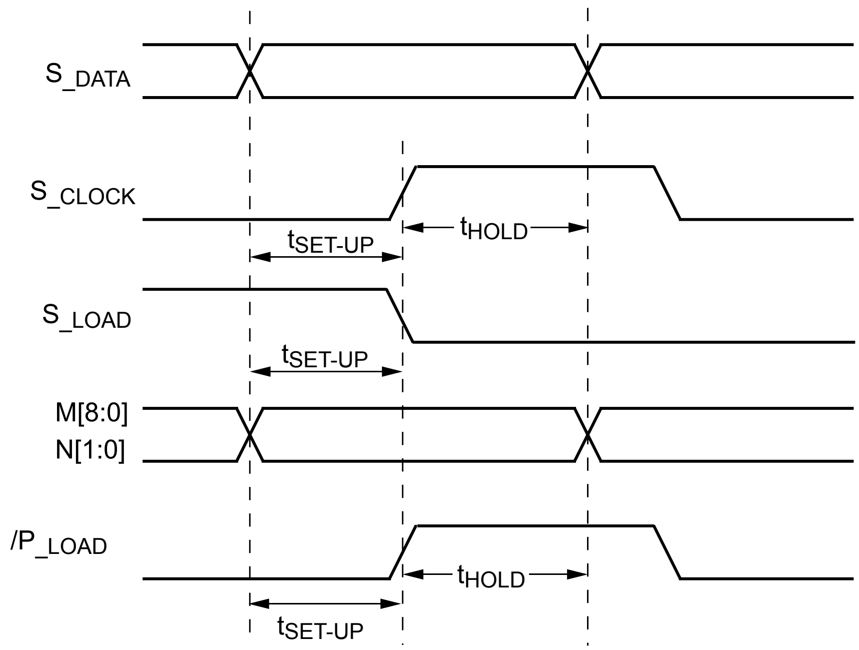
$V_{CC1} = V_{CC\_QUIET} = V_{CC\_TTL}$ = +5.0V ±5%; V_{CC_OUT} = +3.3V to +5.0V ±5%; T_A = 0°C to +75°C

		T_A = 0°C		T_A = +25°C		T_A = +75°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
f_{MAXI}	Maximum Input Frequency(1) S_CLOCK	—	10	—	10	—	10	MHz	Fundamental
	Xtal Oscillator	10	25	10	25	10	25		Cyrstal
f_{MAXO}	Maximum Output Frequency VCO (Internal)	400	800	400	800	400	800	MHz	
	FOUT	25	400	25	400	25	400		
t_{LOCK}	Maximum PLL Lock Time	—	10	—	10	—	10	ms	
t_{jitter}	Cycle-to-Cycle Jitter (Peak-toPeak)	—	±25	—	±25	—	±25	ps	Test output static
t_S	Setup Time S_DATA to S_CLOCK	20	—	20	—	20	—	ns	
	S_CLOCK to S_LOAD	20	—	20	—	20	—		
	M, N to P_LOAD	20	—	20	—	20	—		
t_H	Hold Time S_DATA to S_CLOCK	20	—	20	—	20	—	ns	
	S_CLOCK to S_LOAD	20	—	20	—	20	—		
	M, N to P_LOAD	20	—	20	—	20	—		
$t_{pw(MIN)}$	Minimum Pulse Width S_LOAD	50	—	50	—	50	—	ns	
	P_LOAD	50	—	50	—	50	—		
t_{DC}	FOUT Duty Cycle	45	55	45	55	45	55	%	
t_r t_f	Output Rise/Fall FOUT 20% to 80%	300	800	300	800	300	800	ps	

NOTE:

1. 10MHz is the maximum frequency to load the feedback divide registers. S_CLOCK can be switched at high frequencies when used as a test clock in TEST_MODE 6.

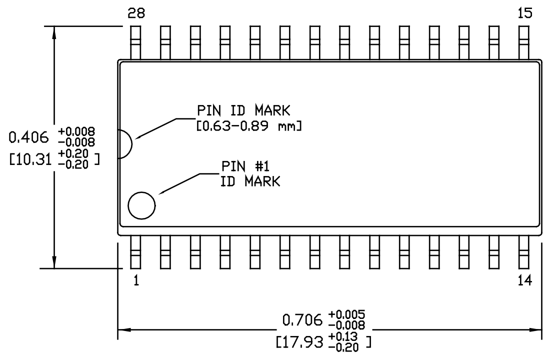
TIMING DIAGRAM



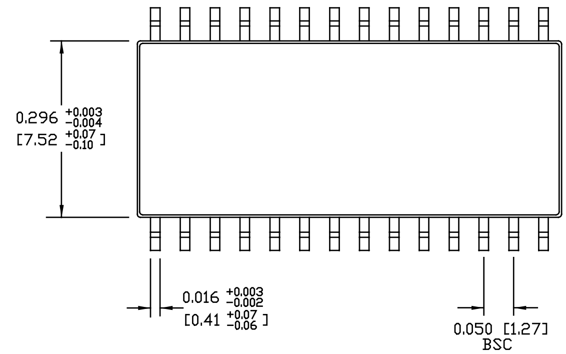
PRODUCT ORDERING CODE

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89429AJC	J28-1	Commercial	SY89429A	Sn-Pb
SY89429AJCTR	J28-1	Commercial	SY89429A	Sn-Pb
SY89429AJZ	J28-1	Industrial	SY89429A with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89429AJZTR	J28-1	Industrial	SY89429A with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89429AZC	Z28-1	Commercial	SY89429A	Sn-Pb
SY89429AZCTR	Z28-1	Commercial	SY89429A	Sn-Pb
SY89429AZH	Z28-1	Industrial	SY89429A with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89429AZHTR	Z28-1	Industrial	SY89429A with Pb-Free bar-line indicator	Pb-Free NiPdAu

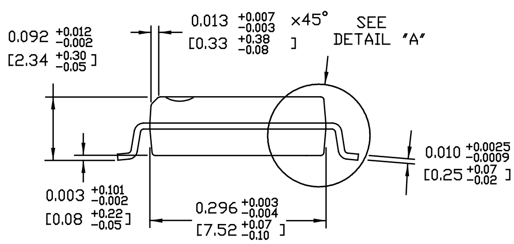
28 LEAD SOIC .300" WIDE (Z28-1)



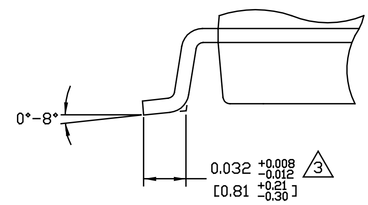
TOP VIEW



BOTTOM VIEW



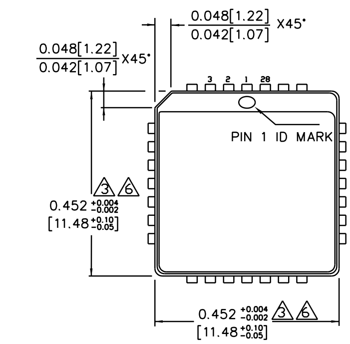
END VIEW



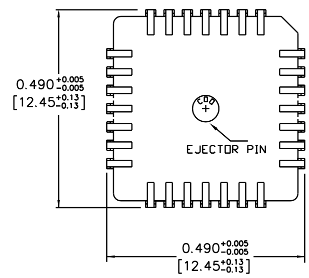
DETAIL "A"

NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

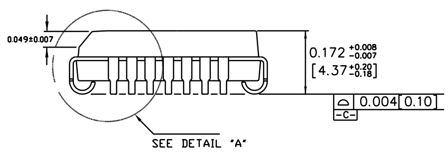
28 LEAD PLCC (J28-1)



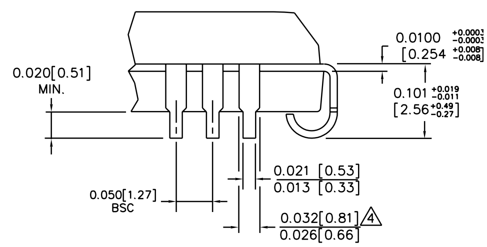
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:
1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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