

MPS6521 (NPN) MPS6523 (PNP)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage (I _C = 0.5 mAdc, I _B = 0)	V _{(BR)CEO}	25	–	Vdc
Emitter – Base Breakdown Voltage (I _E = 10 μAdc, I _C = 0)	V _{(BR)EBO}	4.0	–	Vdc
Collector Cutoff Current (V _{CB} = 30 Vdc, I _E = 0) (V _{CB} = 20 Vdc, I _E = 0)	I _{CBO}	– –	0.05 0.05	μAdc
ON CHARACTERISTICS				
DC Current Gain (I _C = 100 μAdc, V _{CE} = 10 Vdc)	h _{FE}	150	–	–
(I _C = 2.0 mAdc, V _{CE} = 10 Vdc)		300	600	
(I _C = 100 μAdc, V _{CE} = 10 Vdc)		150	–	
(I _C = 2.0 mAdc, V _{CE} = 10 Vdc)		300	600	
Collector – Emitter Saturation Voltage (I _C = 50 mAdc, I _B = 5.0 mAdc)	V _{CE(sat)}	–	0.5	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz)	C _{obo}	–	3.5	pF
Noise Figure (I _C = 10 μAdc, V _{CE} = 5.0 Vdc, R _S = 10 k Ω, Power Bandwidth = 15.7 kHz, 3.0 dB points @ 10 Hz and 10 kHz)	NF	–	3.0	dB

NPN MPS6521 EQUIVALENT SWITCHING TIME TEST CIRCUITS

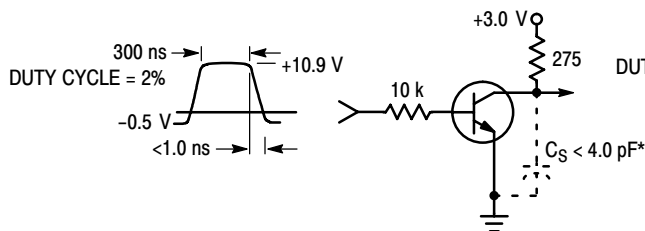


Figure 1. Turn-On Time

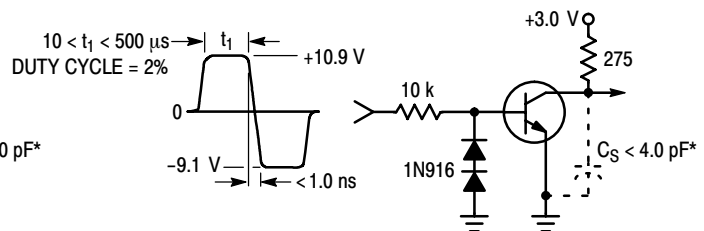


Figure 2. Turn-Off Time

*Total shunt capacitance of test jig and connectors

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TYPICAL NOISE CHARACTERISTICS

($V_{CE} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$)

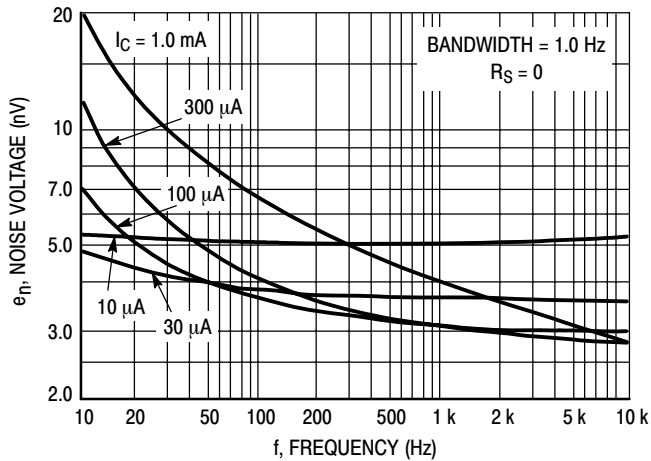


Figure 3. Noise Voltage

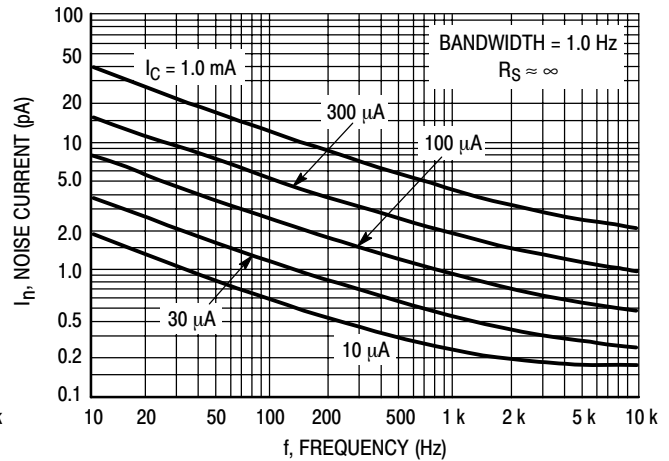


Figure 4. Noise Current

NPN

MPS6521

NOISE FIGURE CONTOURS

($V_{CE} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$)

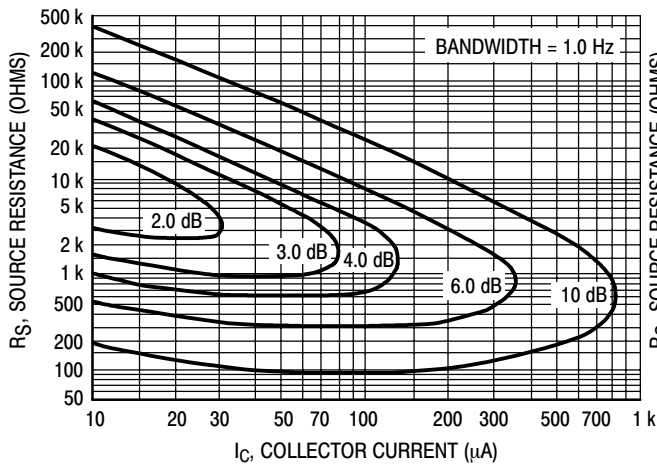


Figure 5. Narrow Band, 100 Hz

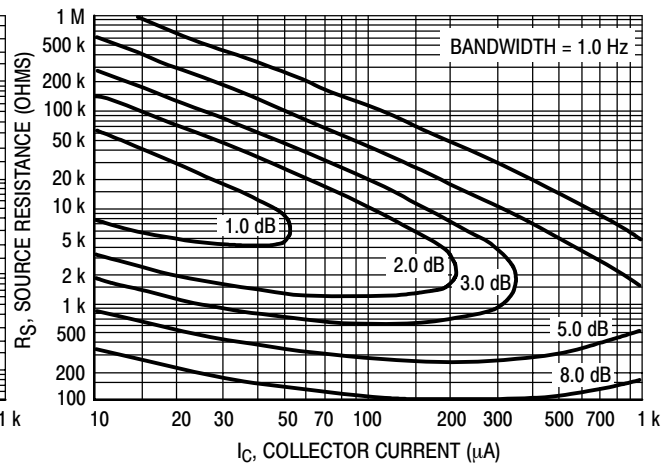


Figure 6. Narrow Band, 1.0 kHz

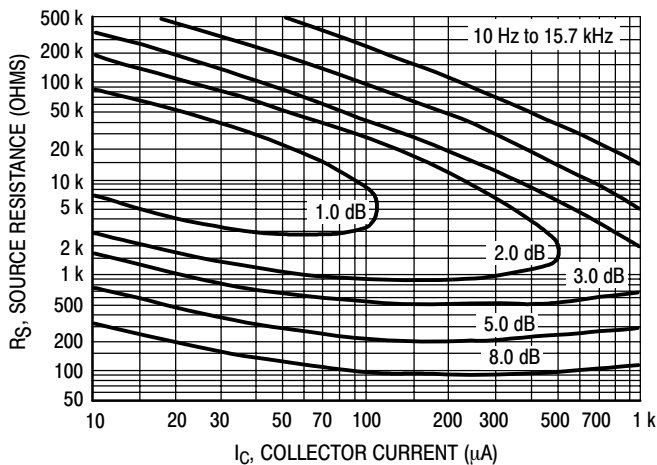


Figure 7. Wideband

Noise Figure is defined as:

$$NF = 20 \log_{10} \left(\frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S} \right)^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)

I_n = Noise Current of the Transistor referred to the input. (Figure 4)

K = Boltzman's Constant ($1.38 \times 10^{-23} \text{ J/}^\circ\text{K}$)

T = Temperature of the Source Resistance ($^\circ\text{K}$)

R_S = Source Resistance (Ohms)

MPS6521 (NPN) MPS6523 (PNP)

NPN MPS6521 TYPICAL STATIC CHARACTERISTICS

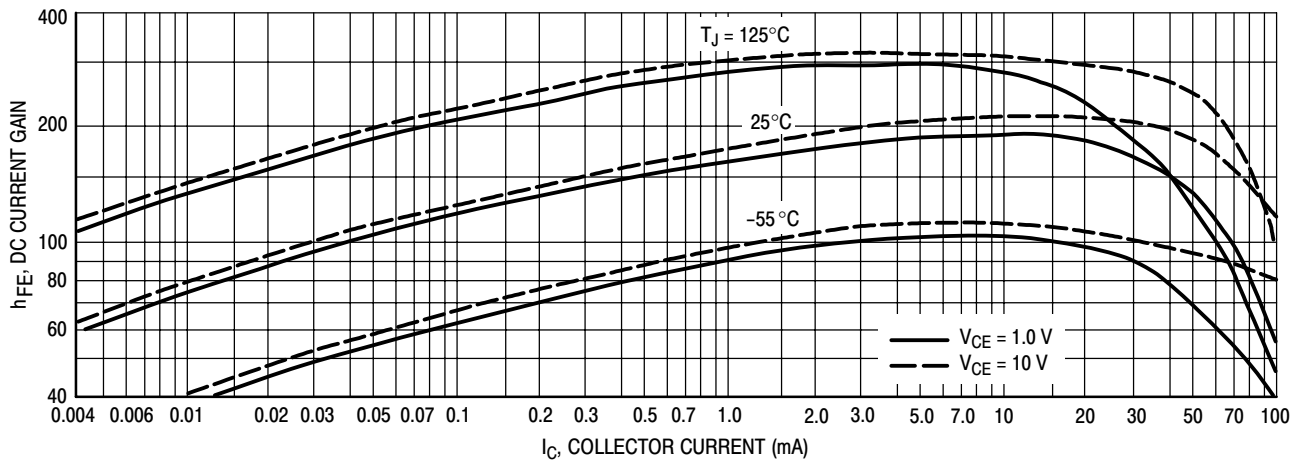


Figure 8. DC Current Gain

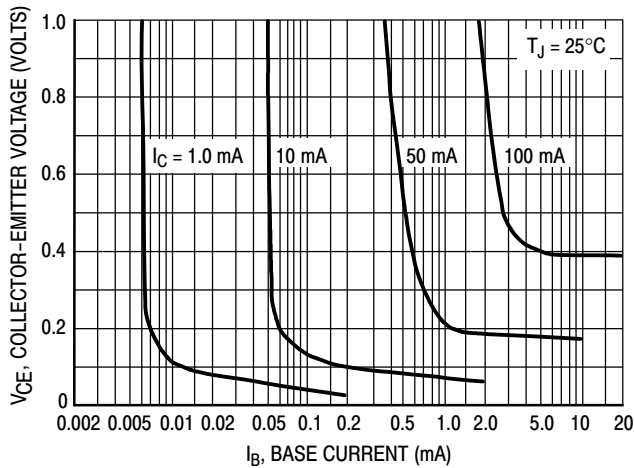


Figure 9. Collector Saturation Region

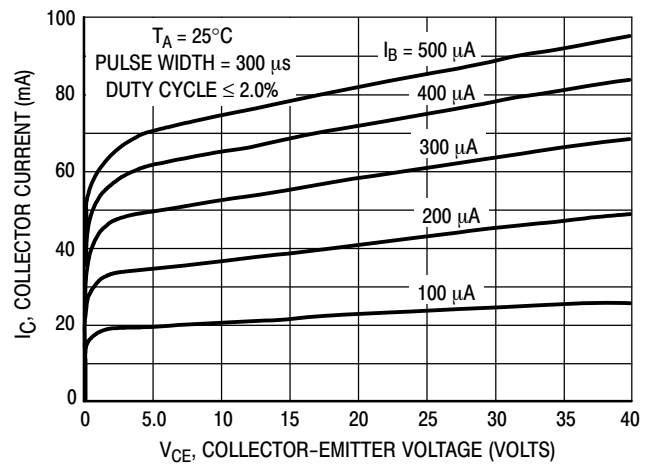


Figure 10. Collector Characteristics

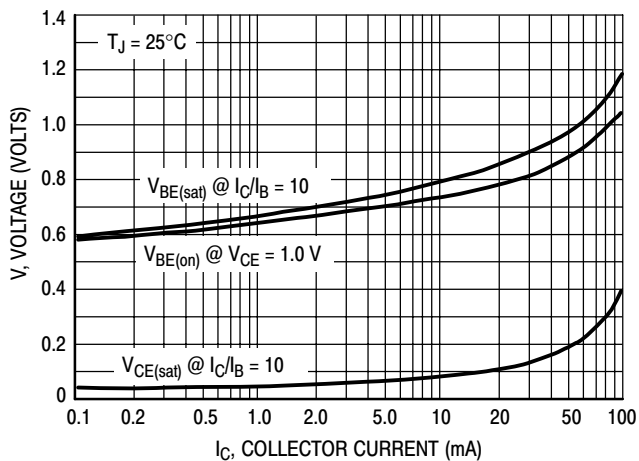


Figure 11. "On" Voltages

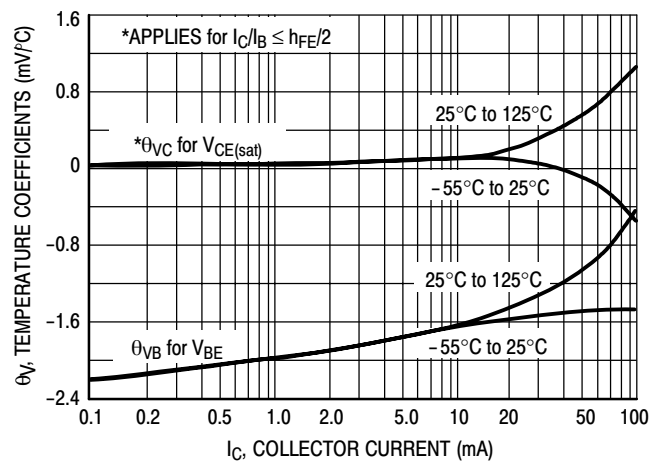


Figure 12. Temperature Coefficients

NPN
MPS6521
TYPICAL DYNAMIC CHARACTERISTICS

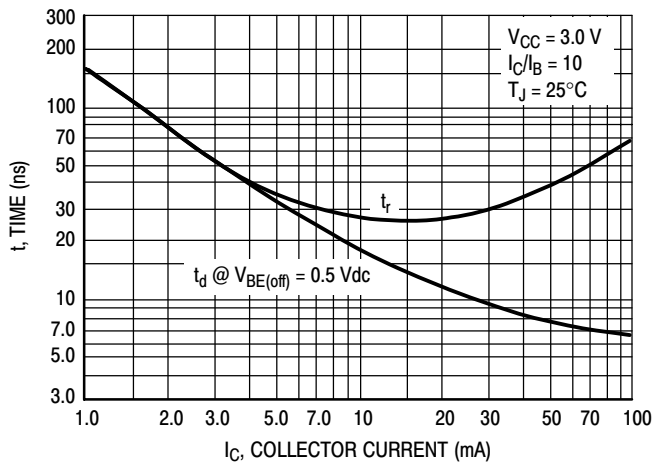


Figure 13. Turn-On Time

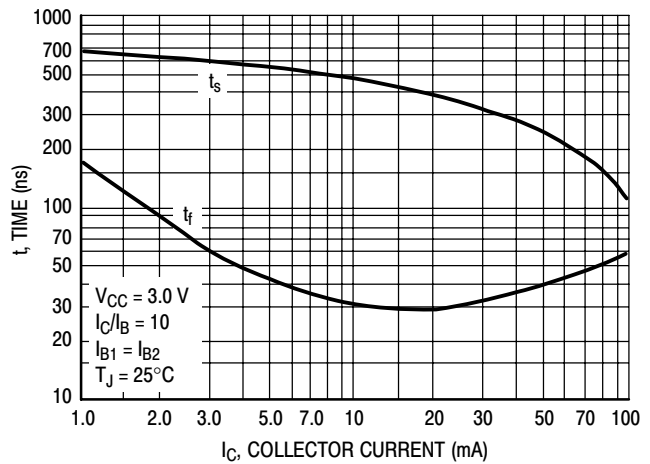


Figure 14. Turn-Off Time

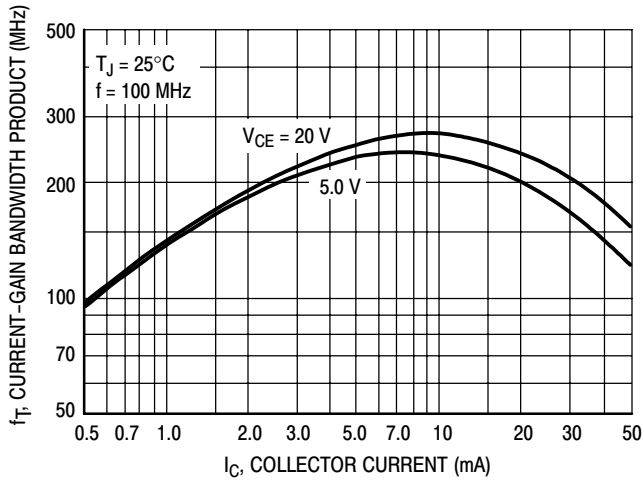


Figure 15. Current-Gain — Bandwidth Product

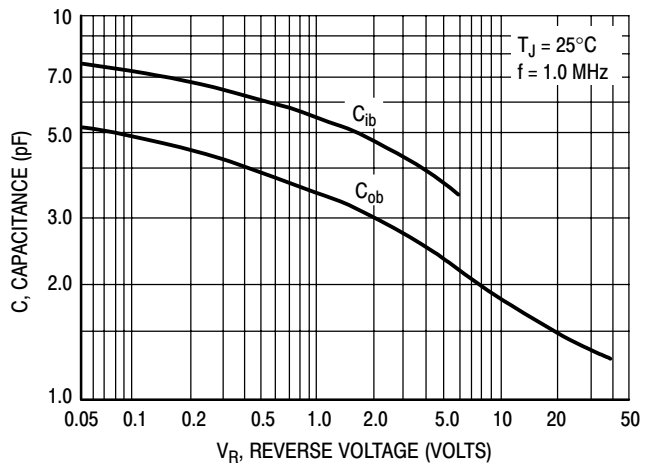


Figure 16. Capacitance

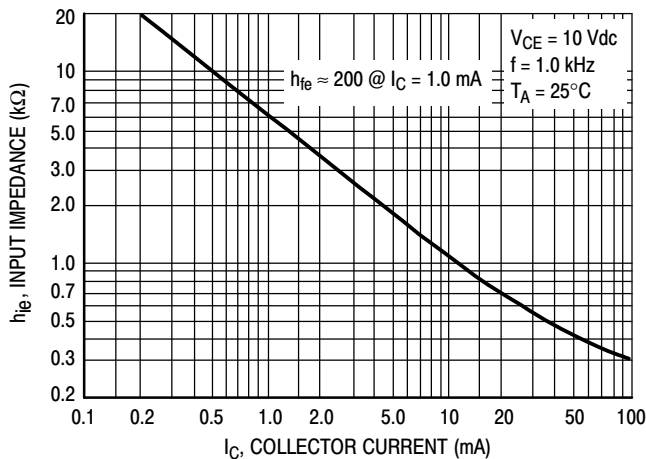


Figure 17. Input Impedance

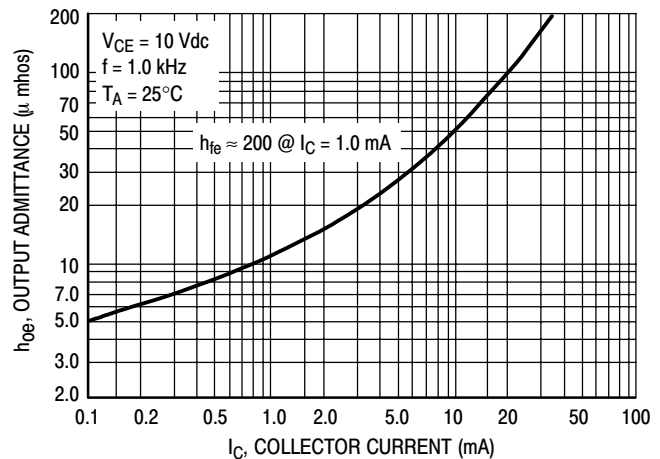


Figure 18. Output Admittance

NPN
MPS6521

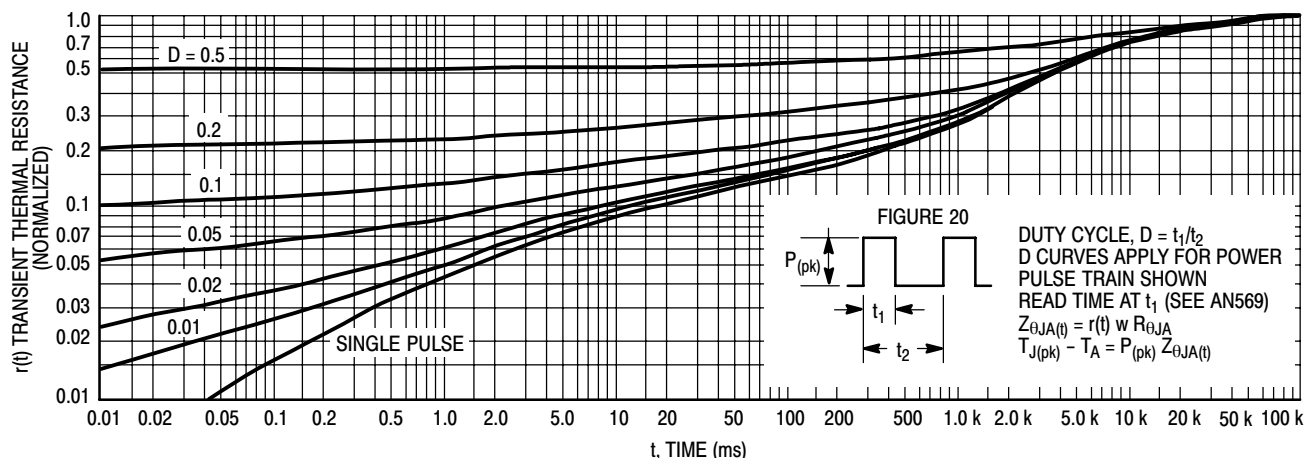


Figure 19. Thermal Response

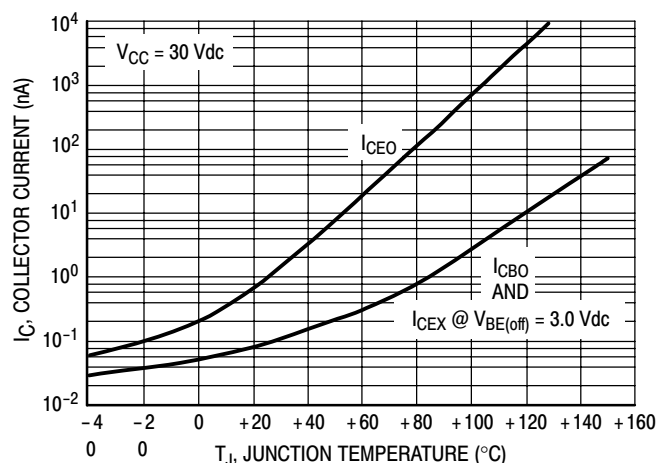


Figure 21.

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 20. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 19 was calculated for various duty cycles.

To find $Z_{\theta JA}(t)$, multiply the value obtained from Figure 19 by the steady state value $R_{\theta JA}$.

Example:

The MPS6521 is dissipating 2.0 watts peak under the following conditions:

$t_1 = 1.0$ ms, $t_2 = 5.0$ ms. ($D = 0.2$)

Using Figure 19 at a pulse width of 1.0 ms and $D = 0.2$, the reading of $r(t)$ is 0.22.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88^\circ\text{C}.$$

For more information, see ON Semiconductor Application Note AN569/D, available from the Literature Distribution Center or on our website at www.onsemi.com.

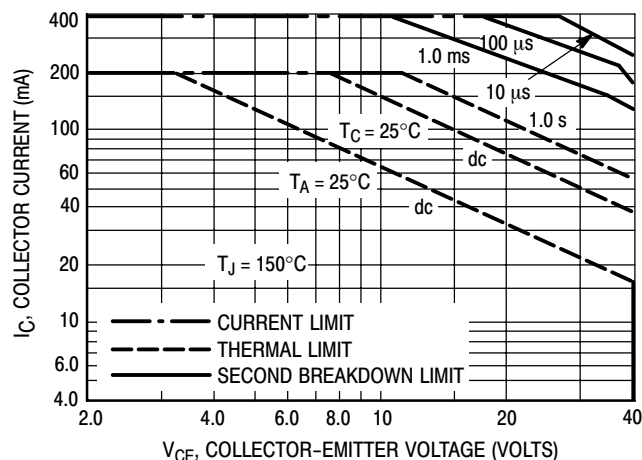


Figure 22.

The safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 22 is based upon $T_{J(pk)} = 150^\circ\text{C}$; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 19. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PNP
MPS6523

TYPICAL NOISE CHARACTERISTICS

($V_{CE} = -5.0$ Vdc, $T_A = 25^\circ\text{C}$)

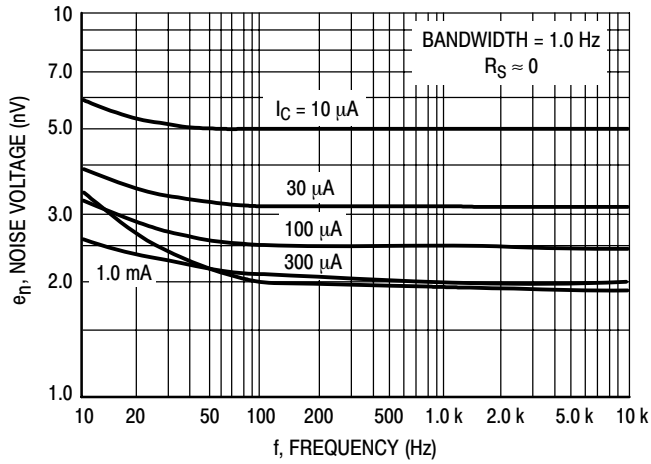


Figure 23. Noise Voltage

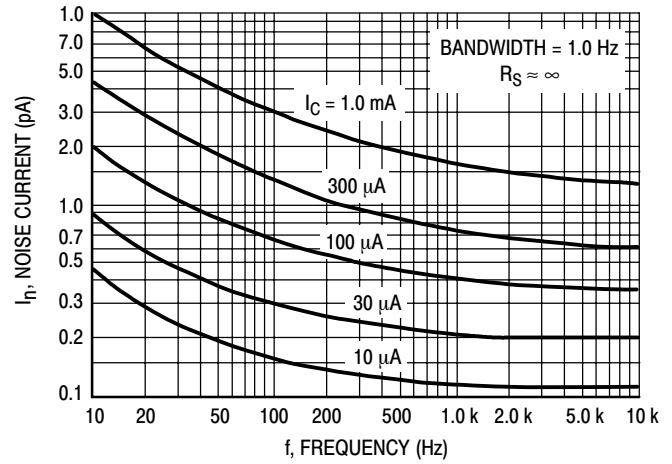


Figure 24. Noise Current

NOISE FIGURE CONTOURS

($V_{CE} = -5.0$ Vdc, $T_A = 25^\circ\text{C}$)

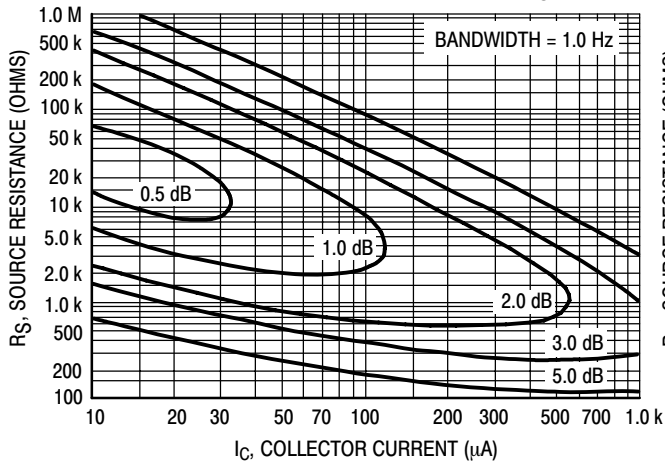


Figure 25. Narrow Band, 100 Hz

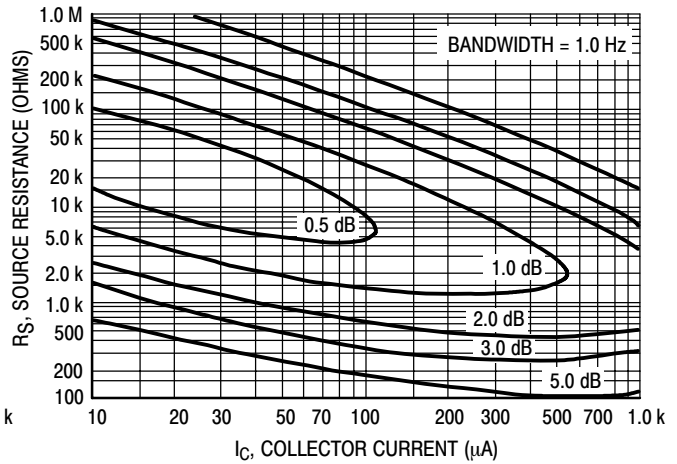


Figure 26. Narrow Band, 1.0 kHz

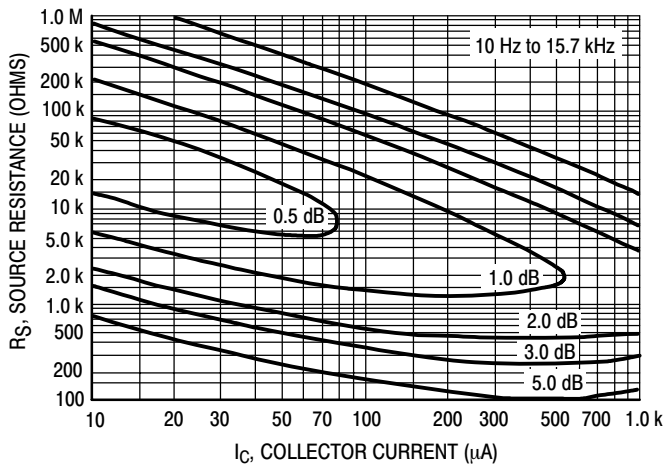


Figure 27. Wideband

Noise Figure is Defined as:

$$NF = 20 \log_{10} \left[\frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S} \right]^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)

I_n = Noise Current of the Transistor referred to the input. (Figure 4)

K = Boltzman's Constant (1.38×10^{-23} J/°K)

T = Temperature of the Source Resistance (°K)

R_S = Source Resistance (Ohms)

PNP
MPS6523
TYPICAL STATIC CHARACTERISTICS

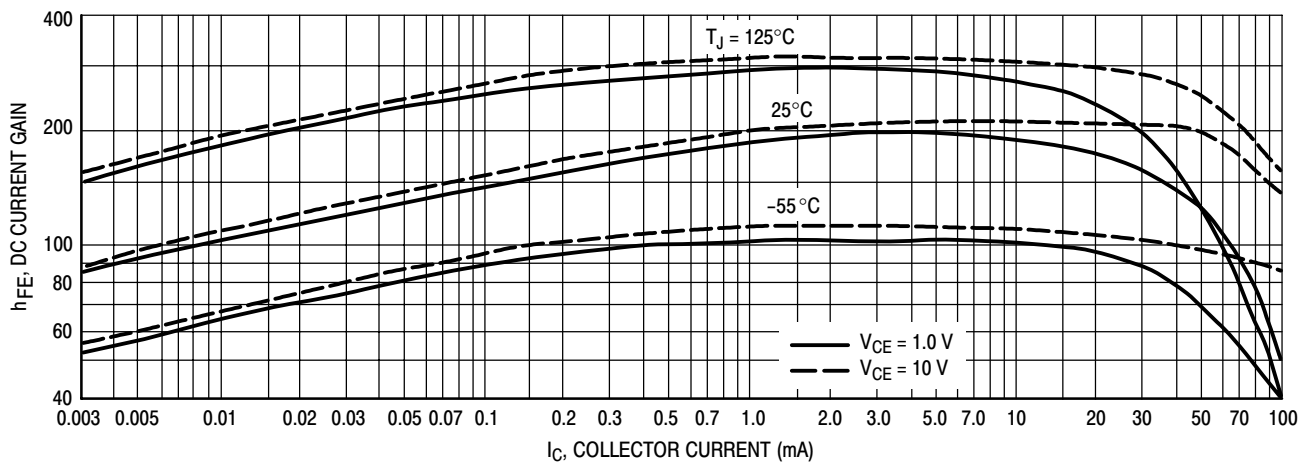


Figure 28. DC Current Gain

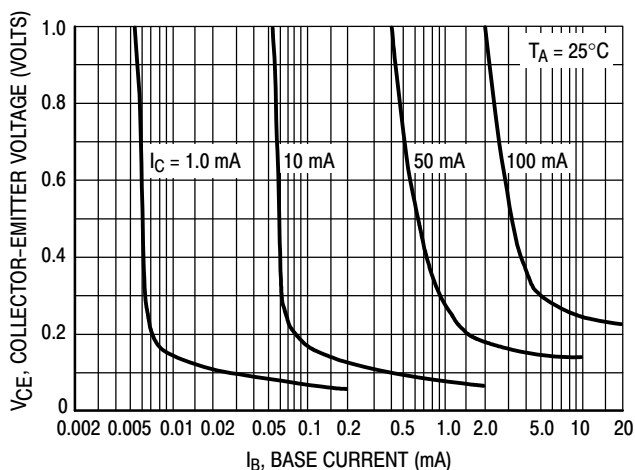


Figure 29. Collector Saturation Region

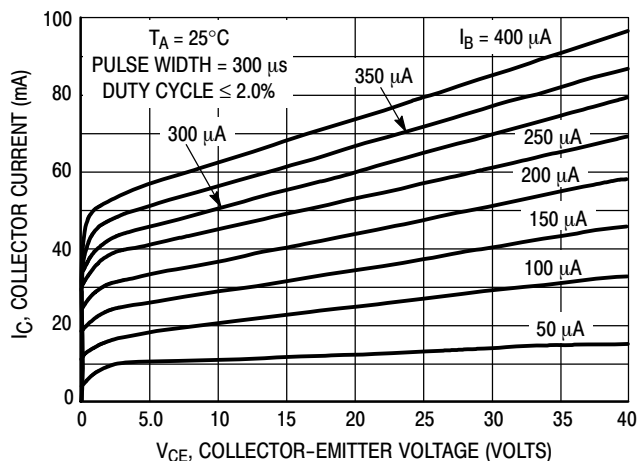


Figure 30. Collector Characteristics

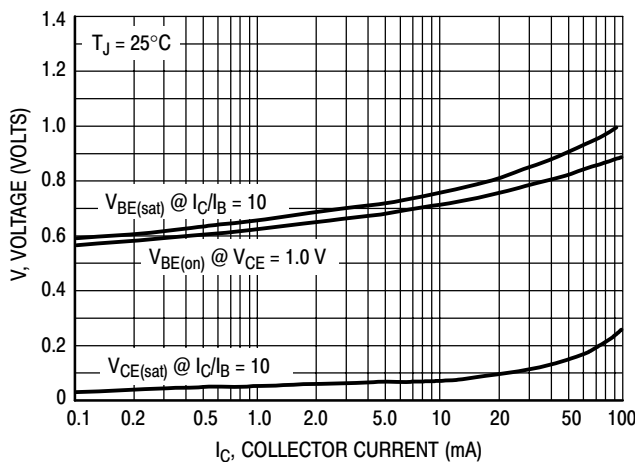


Figure 31. "On" Voltages

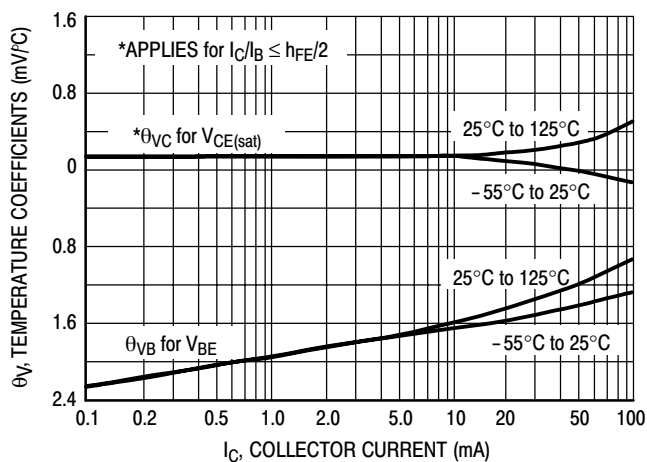


Figure 32. Temperature Coefficients

MPS6521 (NPN) MPS6523 (PNP)

PNP MPS6523 TYPICAL DYNAMIC CHARACTERISTICS

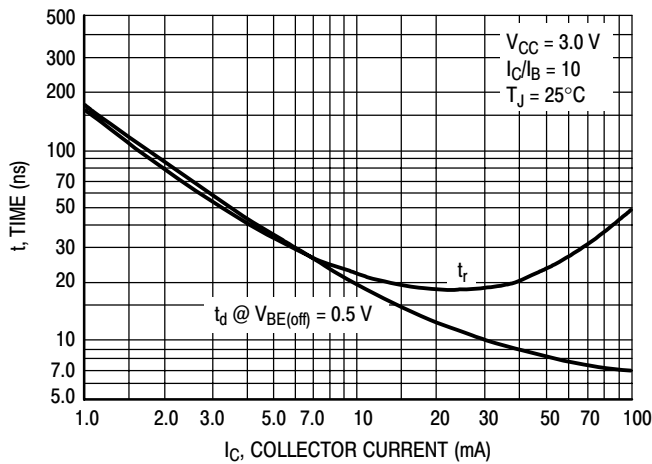


Figure 33. Turn-On Time

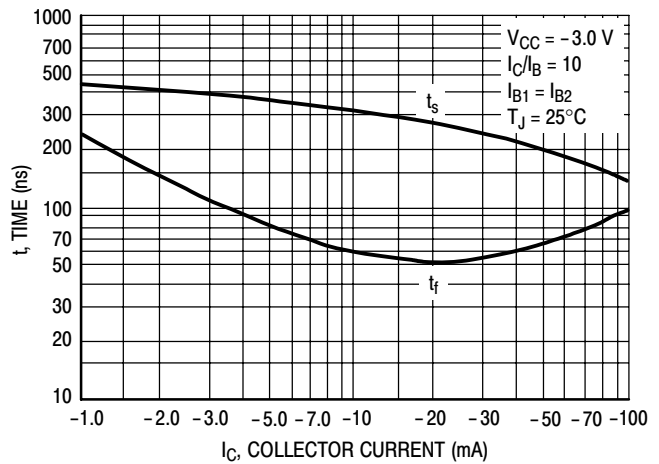


Figure 34. Turn-Off Time

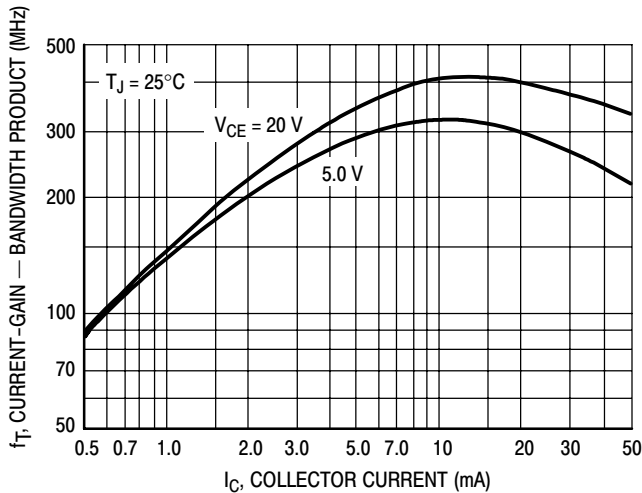


Figure 35. Current-Gain — Bandwidth Product

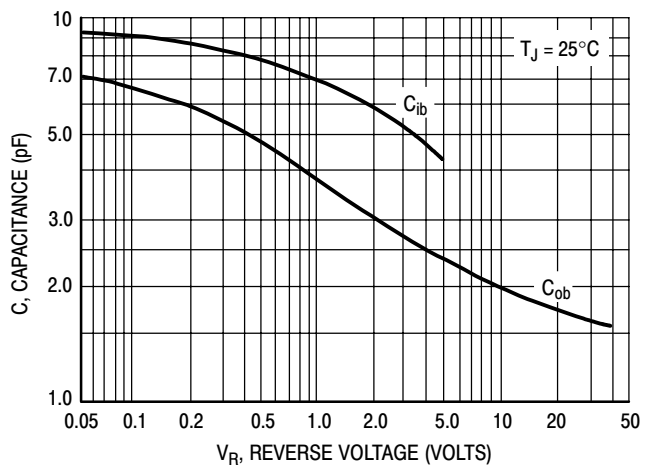


Figure 36. Capacitance

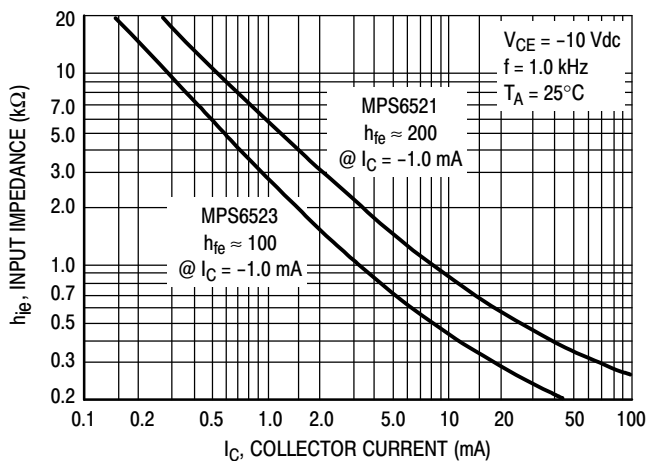


Figure 37. Input Impedance

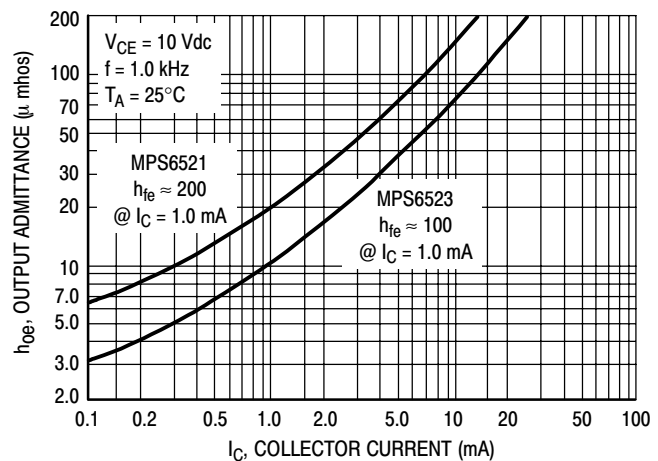


Figure 38. Output Admittance

PNP
MPS6523

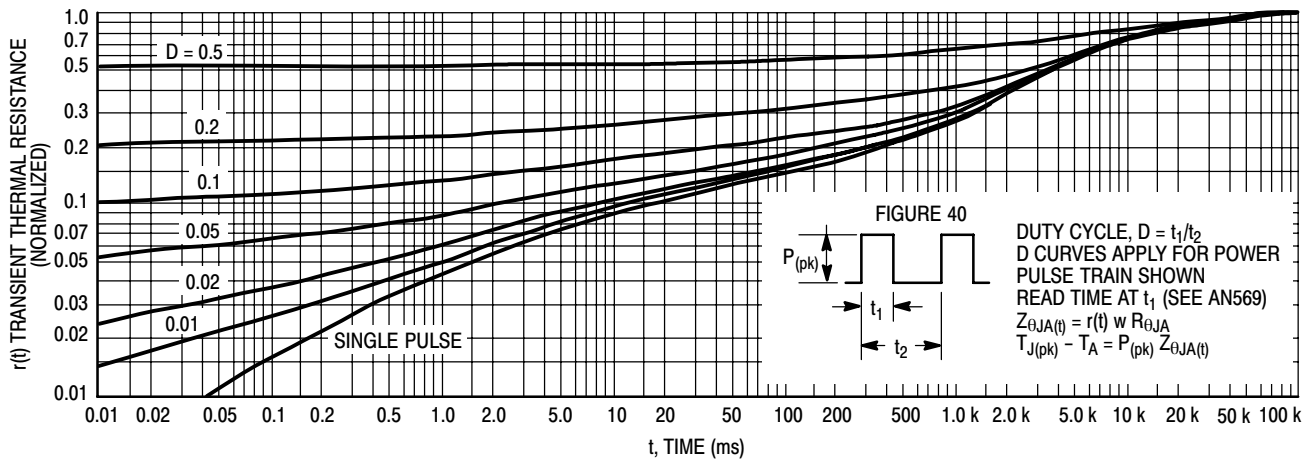


Figure 39. Thermal Response

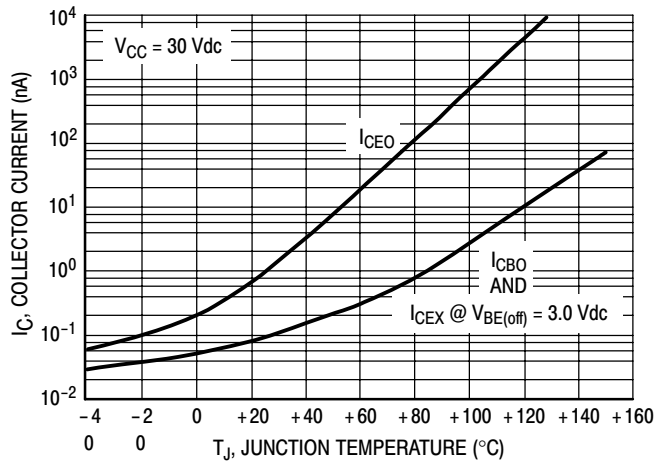


Figure 41.

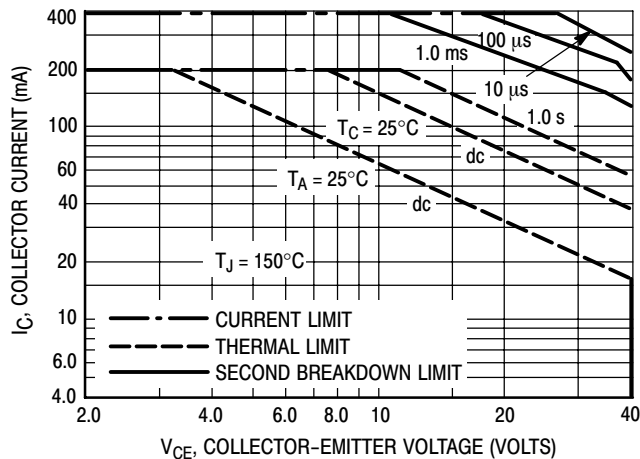


Figure 42.

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 40. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 39 was calculated for various duty cycles.

To find $Z_{\theta JA}(t)$, multiply the value obtained from Figure 39 by the steady state value $R_{\theta JA}$.

Example:

The MPS6523 is dissipating 2.0 watts peak under the following conditions:

$t_1 = 1.0 \text{ ms}$, $t_2 = 5.0 \text{ ms}$. ($D = 0.2$)

Using Figure 39 at a pulse width of 1.0 ms and $D = 0.2$, the reading of $r(t)$ is 0.22.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88^\circ\text{C}.$$

For more information, see ON Semiconductor Application Note AN569/D, available from the Literature Distribution Center or on our website at www.onsemi.com.

The safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 42 is based upon $T_{J(pk)} = 150^\circ\text{C}$; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 39. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

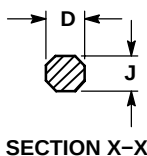
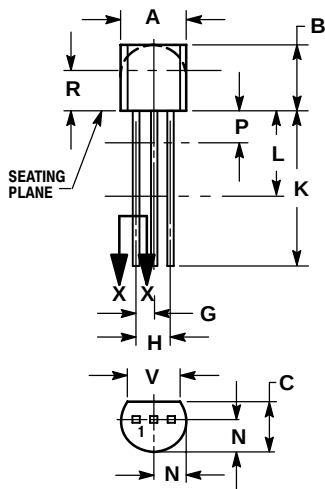
MPS6521 (NPN) MPS6523 (PNP)

PACKAGE DIMENSIONS

TO-92 (TO-226)

CASE 29-11

ISSUE AL



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 1:

1. PIN 1. EMITTER
2. BASE
3. COLLECTOR

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