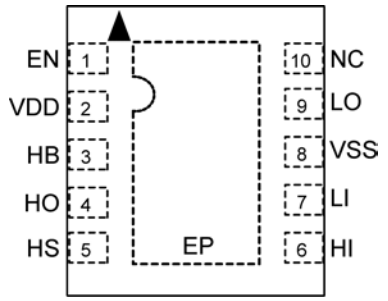
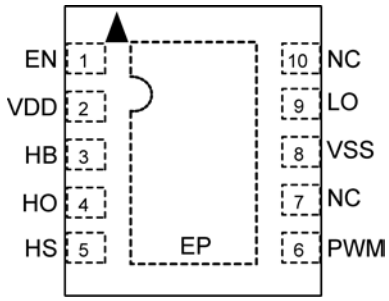
Ordering Information

Part Number	Part Marking	Input	Junction Temperature Range	Package
MIC4605-1YMT	165	Dual TTL Inputs	–40°C to +125°C	10-pin 2.5mm × 2.5mm TDFN
MIC4605-2YMT	265	Single PWM TTL Input	–40°C to +125°C	10-pin 2.5mm × 2.5mm TDFN
MIC4605-1YM	4605-1YM	Dual TTL Inputs	–40°C to +125°C	8-pin SOIC-8
MIC4605-2YM	4605-2YM	Single PWM TTL Input	–40°C to +125°C	8-pin SOIC-8

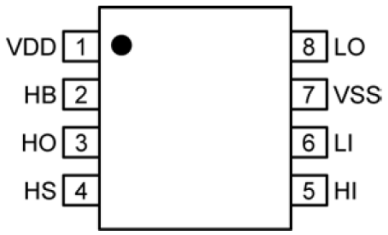
Pin Configurations



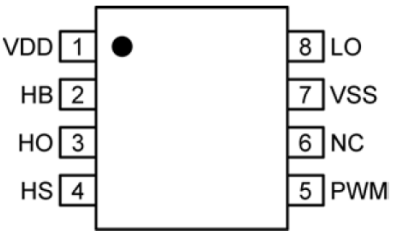
MIC4605-1YMT
10-Pin 2.5mm × 2.5mm TDFN (MT)
(Top View)



MIC4605-2YMT
10-Pin 2.5mm × 2.5mm TDFN (MT)
(Top View)



MIC4605-1YM
8-Pin SOIC (M)
(Top View)



MIC4605-2YM
8-Pin SOIC (M)
(Top View)

Pin Description

MIC4605-1 TDFN Pin Number	MIC4605-2 TDFN Pin Number	MIC4605-1 SOIC-8 Pin Number	MIC4605-2 SOIC-8 Pin Number	Pin Name	Pin Function
1	1	—	—	EN	Enable Input. Logic high on the enable pin results in normal operation, conversely, the device enters shutdown mode with a logic low applied to enable.
2	2	1	1	VDD	Input Supply for Gate Drivers. Decouple this pin to VSS with a >0.1µF capacitor.
3	3	2	2	HB	High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and HS. An on-board bootstrap diode is connected from VDD to HB.
4	4	3	3	HO	High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
5	5	4	4	HS	High-Side Drive Reference Connection. Connect to source of the external high-side power MOSFET. Connect the bottom of bootstrap capacitor to this pin.
6	—	5	—	HI	High-Side Drive Input
—	6	—	5	PWM	Single PWM Input. Drives both the high- and low-side outputs out of phase
7	—	6	—	LI	Low-Side Drive Input.
—	7	—	6	NC	No Connect. This pin is not connected internally.
8	8	7	7	VSS	Driver Reference Supply Input. Generally connected to the power ground of external circuitry.
9	9	8	8	LO	Low-Side Drive Output. Connect to the gate of the external low-side power MOSFET.
10	10	—	—	NC	No Connect. This pin is not connected internally.
EP	EP	—	—	ePad	Exposed Pad. Connect to VSS.

Absolute Maximum Ratings[1]

Supply Voltage (VDD, $V_{HB} – V_{HS}$) ..... –0.3V to 18V
Input Voltages (V_{LI}, V_{HI}, V_{EN}) ..... –0.3V to VDD + 0.3V
Voltage on LO (V_{LO}) ..... –0.3V to VDD + 0.3V
Voltage on HO (V_{HO}) ..... V_{HS} – 0.3V to V_{HB} + 0.3V
Voltage on HS (continuous) ..... –1V to 90V
Voltage on HB 108V
Average Current in VDD to HB Diode 100mA
Storage Temperature (T_S) ..... –60°C to +150°C
ESD Rating[3]
HBM 1kV
MM 200V

Operating Ratings[2]

Supply Voltage (VDD) [decreasing VDD] ..... 5.25V to 16V
Supply Voltage (VDD) [increasing VDD] ..... 5.5V to 16V
Voltage on HS ..... –1V to 85V
Voltage on HS (repetitive transient) ..... –5V to 90V
HS Slew Rate 50V/ns
Voltage on HB ..... V_{HS} + VDD
and/or ..... VDD – 1V to VDD + 85V
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
2.5mm × 2.5mm TDFN-10L (θ_{JA}) ..... 71.4°C/W
SOIC-8L (θ_{JA}) ..... 99°C/W

Electrical Characteristics[4]

VDD = V_{HB} = 12V; VSS = V_{HS} = 0V; No load on LO or HO; T_A = +25°C; unless otherwise noted.
Bold values indicate –40°C ≤ T_J ≤ +125°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply Current						
I_{DD}	VDD Quiescent Current	LI = HI = 0V		100	**250**	µA
I_{DDSH}	VDD Shutdown Current	EN = 0V with HS = floating		2.2	**10**	µA
		EN = 0V		25	**50**	
I_{DDO}	VDD Operating Current	f = 20kHz		170	**500**	µA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V or LI = 0V and HI =5V		35	**75**	µA
I_{HBO}	Total HB Operating Current	f = 20kHz		50	**400**	µA
I_{HBS}	HB to VSS Current, Quiescent	V_{HS} = V_{HB} = 90V		0.05	5	µA
I_{HBSO}	HB to VSS Current, Operating	f = 20kHz		30	**300**	µA
Input (TTL: LI, HI, EN)[5]						
V_{IL}	Low-Level Input Voltage				**0.8**	V
V_{IH}	High-Level Input Voltage		**2.2**			V
V_{HYS}	Input Voltage Hysteresis			0.1		V
R_I	Input Pull-Down Resistance	LI and HI	**100**	300	**500**	kΩ
		PWM	**50**	130	**250**	
Undervoltage Protection						
V_{DDR}	VDD Falling Threshold		**4.0**	4.4	**4.9**	V
V_{DDH}	VDD Threshold Hysteresis			0.25		V
V_{HBR}	HB Falling Threshold		**4.0**	4.4	**4.9**	V
V_{HBH}	HB Threshold Hysteresis			0.25		V

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Devices are ESD sensitive. Handling precautions are recommended.
4. Specification for packaged product only.
5. $V_{IL\ (MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low. $V_{IH\ (MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

Electrical Characteristics[4] (Continued)

VDD = V_{HB} = 12V; VSS = V_{HS} = 0V; No load on LO or HO; T_A = +25°C; unless otherwise noted.
Bold values indicate –40°C ≤ T_J ≤ +125°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Bootstrap Diode						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100µA		0.4	**0.70**	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 50mA		0.7	**1.0**	V
R_D	Dynamic Resistance	I_{VDD-HB} = 50mA		2.0	**5.0**	Ω
LO Gate Driver						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 50mA		0.3	**0.6**	V
V_{OHL}	High-Level Output Voltage	I_{LO} = –50mA, V_{OHL} = VDD – V_{LO}		0.5	**1.0**	V
I_{OHL}	Peak Sink Current	V_{LO} = 0V		1		A
I_{OLL}	Peak Source Current	V_{LO} = 12V		1		A
HO Gate Driver						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 50mA		0.3	**0.6**	V
V_{OHH}	High-Level Output Voltage	I_{HO} = –50mA, V_{OHH} = V_{HB} – V_{HO}		0.5	**1.0**	V
I_{OHH}	Peak Sink Current	V_{HO} = 0V		1		A
I_{OLH}	Peak Source Current	V_{HO} = 12V		1		A
Switching Specifications (LI/HI mode with inputs non-overlapping, assumes HS low before LI goes high and LO low before HI goes high)						
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			35	**75**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			35	**75**	ns
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)			35	**75**	ns
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)			35	**75**	ns
$t_{RC/FC}$	Output Rise/Fall Time	C_L = 1000pF		20		ns
$t_{R/F}$	Output Rise/Fall Time (3V to 9V)	C_L = 0.1µF		0.8		µs
t_{PW}	Minimum Input Pulse Width that Changes the Output[5]			50		ns
Switching Specifications PWM Mode (MIC4605-2) or LI/HI Mode (MIC4605-1) with Overlapping LI/HI Inputs						
t_{LOOFF}	Delay from PWM Going High / LI Low, to LO Going Low			35	**75**	ns
V_{LOOFF}	LO Output Voltage Threshold for LO FET to be Considered Off			1.9		V
t_{HOON}	Delay from LO off to HO Going High			35	**75**	ns
t_{HOOFF}	Delay from PWM Going Low / HI Low, to HO Going Low			35	**75**	ns
V_{SWTH}	Switch Node Voltage Threshold Signaling HO is Off		1	2.2	4	V

Electrical Characteristics[4] (Continued)

VDD = V_{HB} = 12V; VSS = V_{HS} = 0V; No load on LO or HO; T_A = +25°C; unless otherwise noted.
Bold values indicate –40°C ≤ T_J ≤ +125°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Switching Specifications PWM Mode (MIC4605-2) or LI/HI Mode (MIC4605-1) with Overlapping LI/HI Inputs						
t_{LOON}	Delay Between HO FET Being Considered Off to LO Turning On			35	**75**	ns
t_{LOONHI}	For HS Low/LI High, Delay from PWM/HI Low to LO going HI			80	**150**	ns
t_{SWTO}	Force LO On if V_{SWTH} is Not Detected		**100**	250	**500**	ns

Timing Diagrams

In LI/HI input mode, external LI/HI inputs are delayed to the point that HS is low before LI is pulled high and similarly LO is low before HI goes high

HO goes high with a high signal on HI after a typical delay of 35ns (t_{HPLH}). HI going low drives HO low also with typical delay of 35ns (t_{HPHL}).

Likewise, LI going high forces LO high after typical delay of 35ns (t_{LPLH}) and LO follows low transition of LI after typical delay of 35ns (t_{LPHL}).

HO and LO output rise and fall times (t_R/t_F) are typically 20ns driving 1000pF capacitive loads.

Note: All propagation delays are measured from the 50% voltage level.

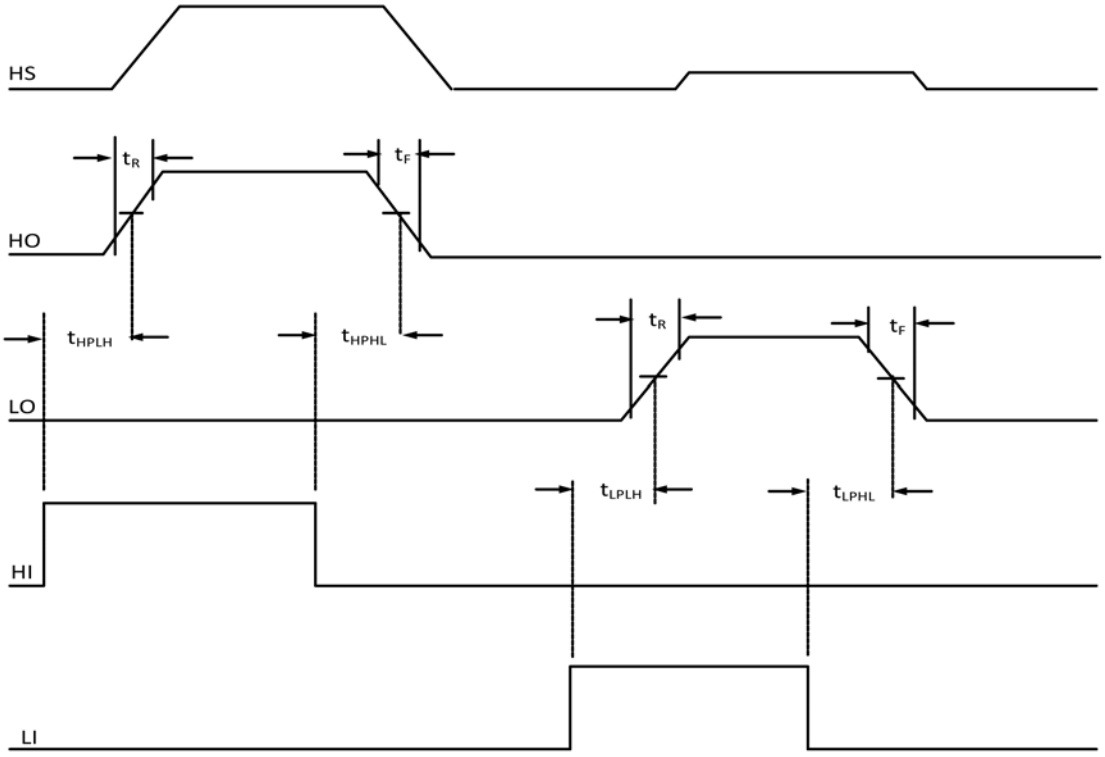


Figure 1. Separate Non-Overlapping LI/HI Input Mode (MIC4605-1)

Timing Diagrams (Continued)

When LI/HI input on conditions overlap, LO/HO output states are dominated by the first output to be turned on. That is, if LI goes high (on), while HO is high, HO stays high until HI goes low at which point, after a delay of t_{HOOFF} and when HS < 2.2V, LO goes high with a delay of t_{LOON}. Should HS never trip the aforementioned internal comparator reference (2.2V), a falling HI edge delayed by 250ns will set “HS latch” allowing LO to go high.

If HS falls very fast, LO will be held low by a 35ns delay gated by HI going low. Conversely, HI going high (on) when LO is high has no effect on outputs until LI is pulled low (off) and LO falls to < 1.9V. Delay from LI going low to LO falling is t_{LOOFF} and delay from LO < 1.9V to HO being on is t_{HOON}.

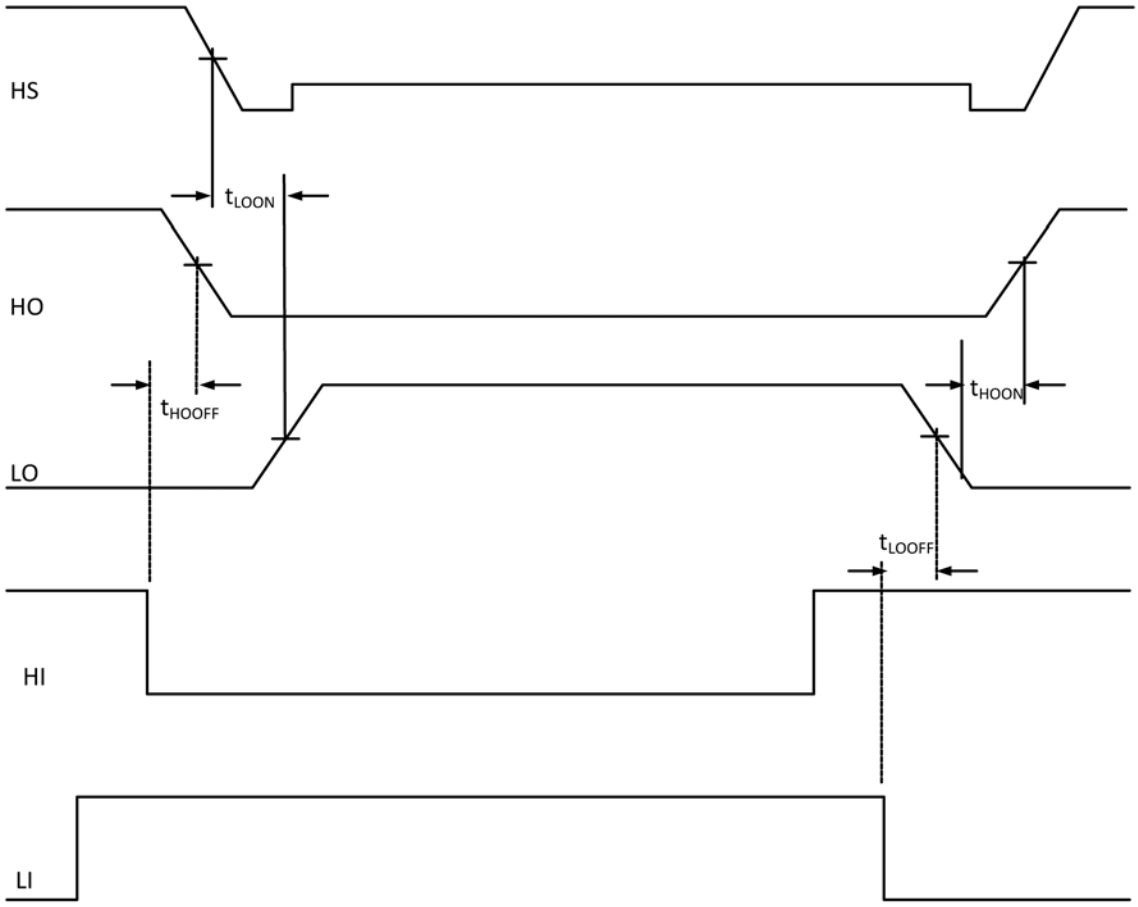


Figure 2. Separate Overlapping LI/HI Input Mode (MIC4605-1)

Timing Diagrams (Continued)

PWM signal applied to the MIC4605-2 going low causes HO to go low typically 35ns (t_{HOOFF}) after the PWM input goes low, at which point the switch node HS falls (1 – 2).

When HS reaches 2.2V (V_{SWTH}), the external high-side MOSFET is deemed off and LO goes high, typically within 35ns (t_{LOON}). HS falling below 1.9V sets a latch that can only be reset by PWM going high. This design prevents ringing on HS from causing an indeterminate LO state. Should HS never trip the aforementioned internal comparator reference (2.2V), a falling PWM edge delayed by 250ns will set "HS latch" allowing LO to go high. An 80ns delay gated by PWM going low may determine the time to LO going high for fast falling HS designs (3 – 4).

PWM goes high forcing LO low in typically 35ns (t_{LOOFF}) (5 – 6).

When LO reaches 1.9V (V_{LOOFF}), the low-side MOSFET is deemed off and HO is allowed to go high. The delay between these two points is typically 35ns (t_{LOON}). HO goes high with a high signal on HI after a typical delay of 35ns (t_{HPLH}). HI going low drives HO low also with a typical delay of 35ns (t_{HPHL}) (7 – 8).

HO and LO output rise and fall times (t_R/t_F) are typically 20ns driving 1000pF capacitive loads.

Note: All propagation delays are measured from the 50% voltage level.

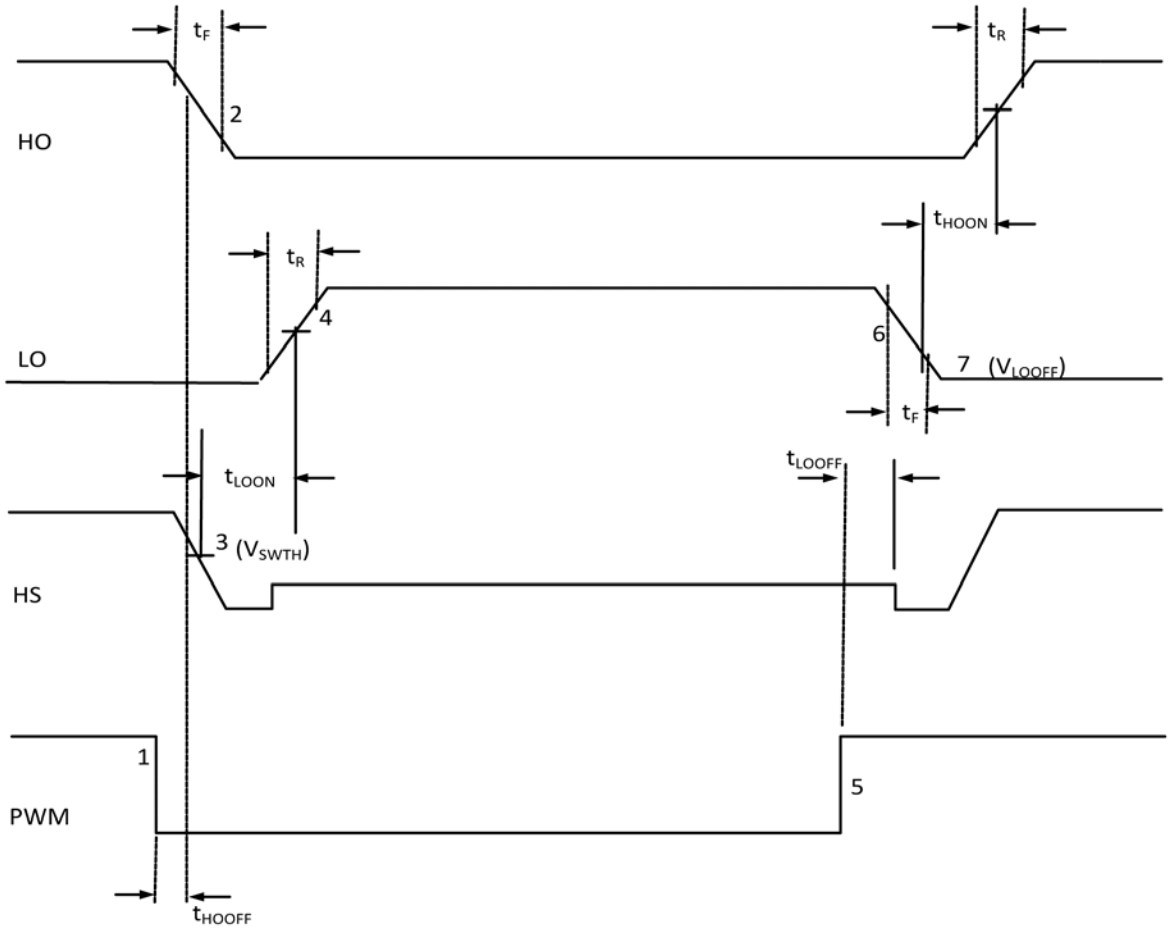


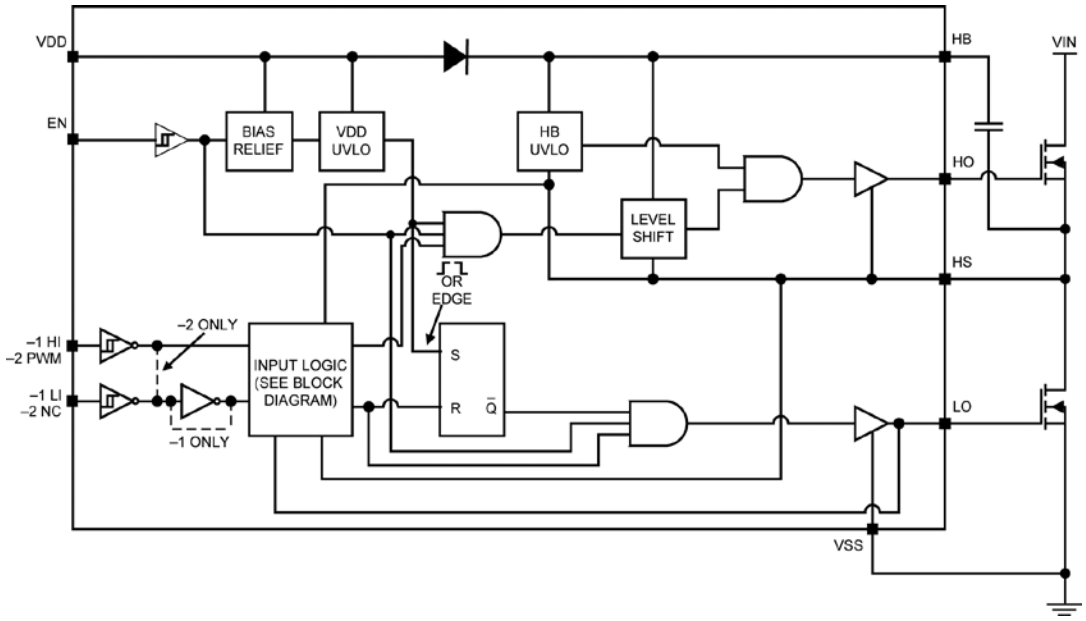
Figure 3. PWM Mode (MIC4605-2)

Block Diagram

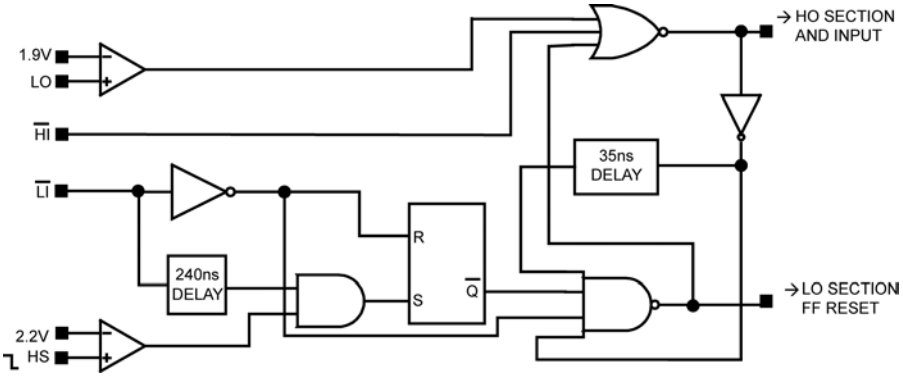
For HO to be high, HI must be high and LO must be low. HO going high is delayed by LO falling below 1.9V. The HI and LI inputs must not rise at the same time to prevent a glitch from occurring on the output. A minimum 50ns delay between both inputs is recommended.

LO is turned off very quickly on the LI falling edge. LO going high is delayed by the longer of 35ns delay of HO control signal going “off” or the RS latch being set.

The latch is set by the quicker of either the falling edge of HS or LI gated delay of 240ns. The latch is present to lockout LO bounce due to ringing on HS. If HS never adequately falls due to the absence of or the presence of a very weak external pull-down on HS, the gated delay of 240ns at LI will set the latch allowing LO to transition high. This in turn allows the LI startup pulse to charge the bootstrap capacitor if the load inductor current is very low and HS is uncontrolled. The latch is reset by the LI falling edge.



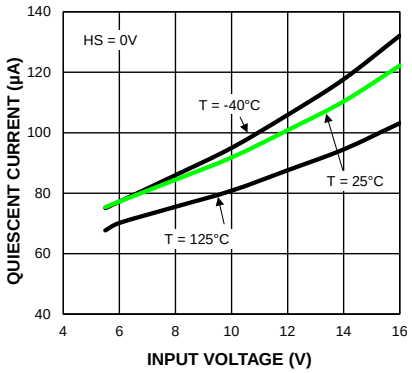
MIC4605 Top Level Block Diagram



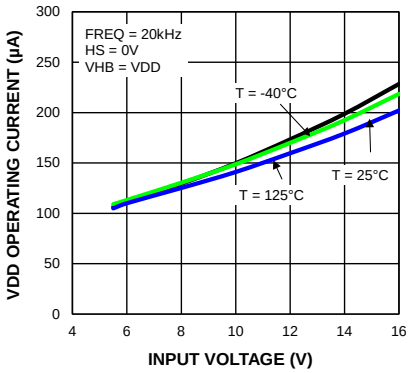
MIC4605-1 Cross-Conduction Lockout/PWM Input Logic Block Diagram

Typical Characteristics

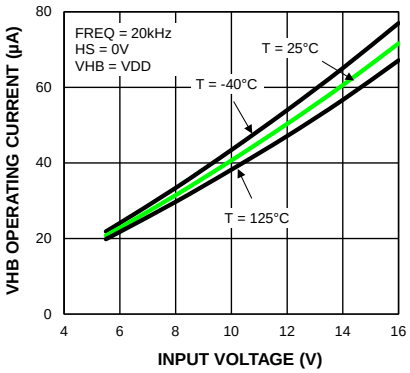
Quiescent Current vs. Input Voltage



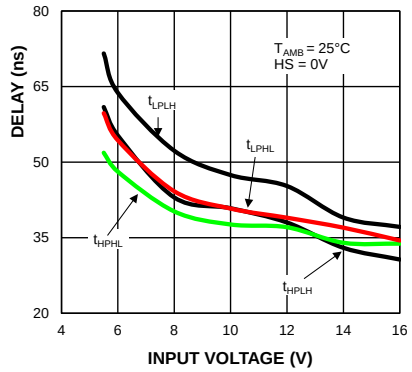
VDD Operating Current vs. Input Voltage



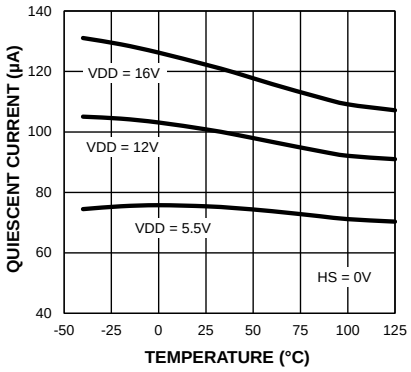
VHB Operating Current vs. Input Voltage



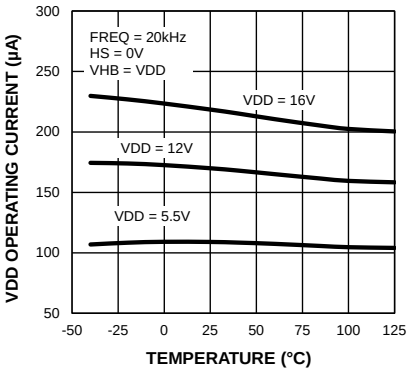
Propagation Delay vs. Input Voltage



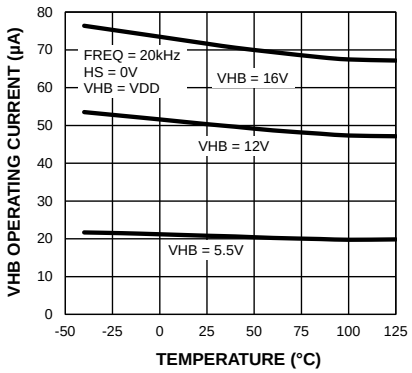
Quiescent Current vs. Temperature



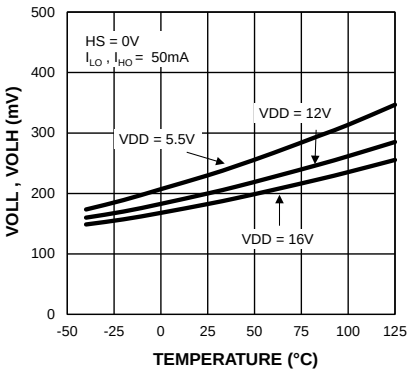
VDD Operating Current vs. Temperature



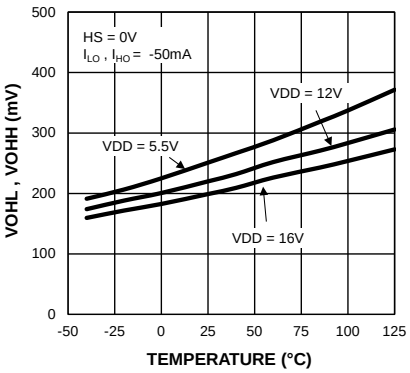
VHB Operating Current vs. Temperature



Low-Level Output Voltage vs. Temperature

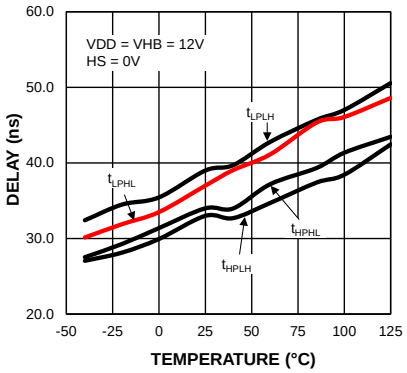


High-Level Output Voltage vs. Temperature

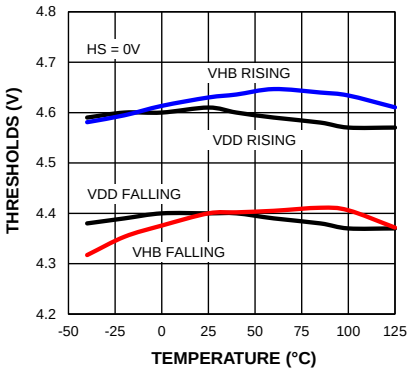


Typical Characteristics (Continued)

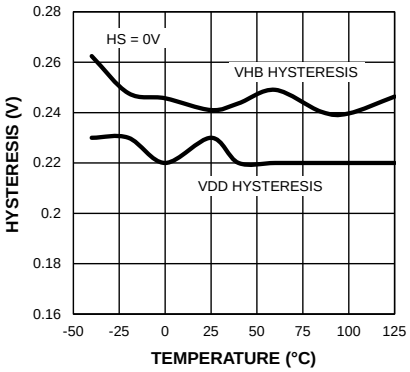
Propagation Delay vs. Temperature



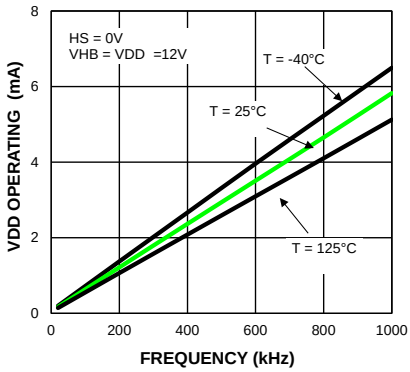
UVLO Thresholds vs. Temperature



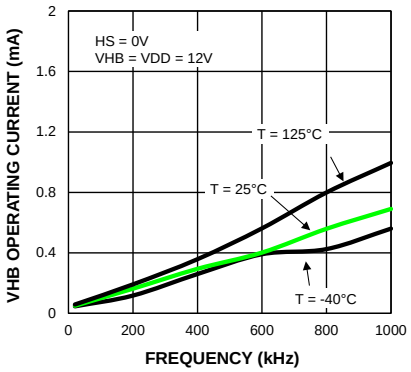
UVLO Hysteresis vs. Temperature



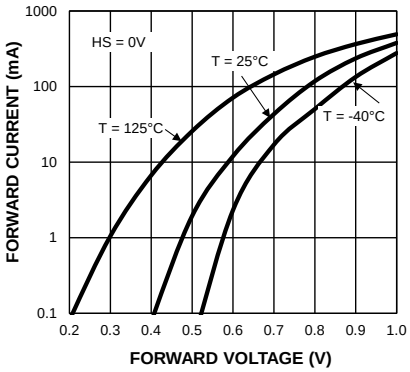
VDD Operating Current vs. Frequency



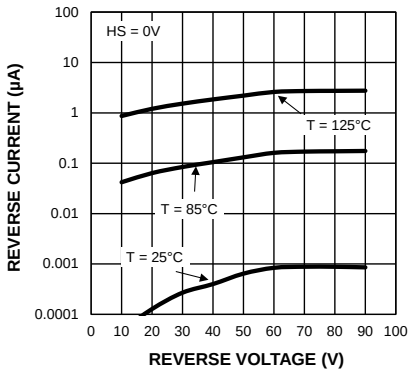
VHB Operating Current vs. Frequency



Bootstrap Diode I-V Characteristics



Bootstrap Diode Reverse Current



Functional Description

The MIC4605 is a non-inverting, 85V half-bridge MOSFET driver designed to independently drive both high-side and low-side N-Channel MOSFETs. The MIC4605 offers a wide 5.5V to 16V operating supply range with either dual TTL inputs (MIC4605-1) or a single PWM input (MIC4605-2). Refer to the MIC4605 Top Level Block Diagram.

Both drivers contain an input buffer with hysteresis, a UVLO circuit, and an output buffer. The high-side output buffer includes a high-speed level-shifting circuit that is referenced to the HS pin. An internal diode is used as part of a bootstrap circuit to provide the drive voltage for the high-side output.

Startup and UVLO

The UVLO circuit forces the driver output low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the VDD and VSS pins. The high-side UVLO circuit monitors the voltage between the HB and HS pins. Hysteresis in the UVLO circuit prevents noise and finite circuit impedance from causing chatter during turn-on.

Enable Input

The 10-pin 2.5mm × 2.5mm TDFN package features an enable pin for on/off control of the device. Logic high on the enable pin (EN) allows for startup and normal operation to occur. Conversely, when a logic low is applied on the enable pin, the device enters shutdown mode.

Input Stage

Both the HI/LI pins of the MIC4605-1 and the single PWM input of the MIC4605-2 are referenced to the VSS pin. The voltage state of the input signal(s) does not change the quiescent current draw of the driver.

The MIC4605 has a TTL-compatible input range and can be used with input signals with amplitude less than the supply voltage. The threshold level is independent of the VDD supply voltage and there is no dependence between I_{VDD} and the input signal amplitude with the MIC4605. This feature makes the MIC4605 an excellent level translator that will drive high-threshold MOSFETs from a low-voltage PWM IC.

Low-Side Driver

A block diagram of the low-side driver is shown in Figure 4. The low-side driver is designed to drive a ground (VSS pin) referenced N-channel MOSFET.

Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low R_{DSON} from the external MOSFET.

A high level applied to LI pin causes the upper driver MOSFET to turn on and VDD voltage is applied to the gate of the external MOSFET. A low level on the LI pin turns off the upper driver and turns on the low side driver to ground the gate of the external MOSFET.

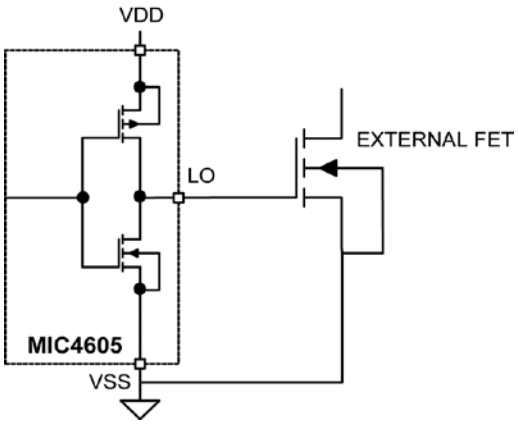


Figure 4. Low-Side Driver Block Diagram

High-Side Driver and Bootstrap Circuit

A block diagram of the high-side driver and bootstrap circuit is shown in Figure 5. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.

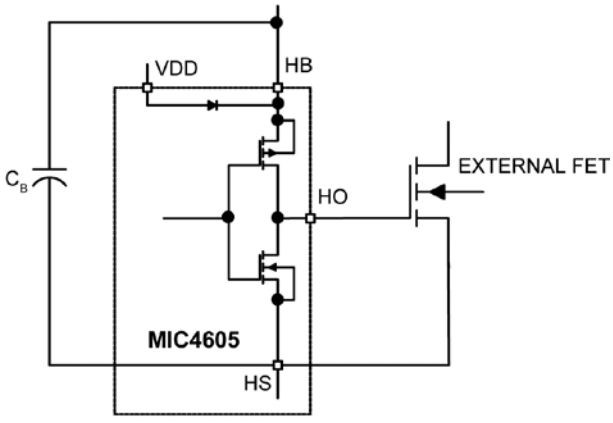


Figure 5. High-Side Driver and Bootstrap Circuit Block Diagram

A low-power, high-speed, level-shifting circuit isolates the low side (VSS pin) referenced circuitry from the high-side (HS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap circuit while the voltage level of the HS pin is shifted high.

The bootstrap circuit consists of an internal diode and external capacitor, C_B. In a typical application, such as the synchronous buck converter shown in Figure 6, the HS pin is at ground potential while the low-side MOSFET is on. The internal diode allows capacitor C_B to charge up to VDD-VF during this time (where VF is the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the HO pin turns on, the voltage across capacitor C_B is applied to the gate of the upper external MOSFET. As the upper MOSFET turns on, voltage on the HS pin rises with the source of the high-side MOSFET until it reaches VIN. As the HS and HB pin rise, the internal diode is reverse biased preventing capacitor C_B from discharging.

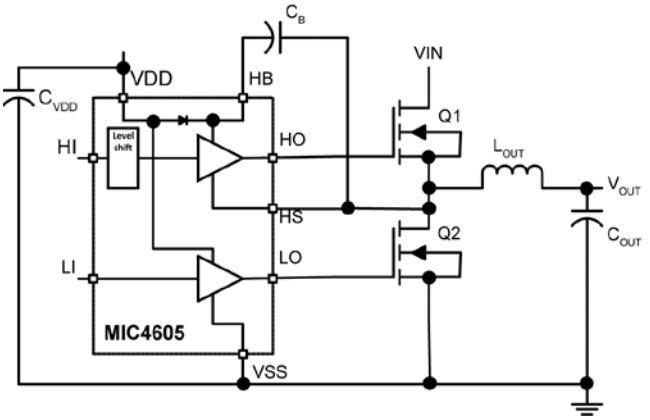


Figure 6. MIC4605 Driving a Synchronous Buck Converter

Programmable Gate Drive

The MIC4605 offers programmable gate drive, which means the MOSFET gate drive (gate to source voltage) equals the VDD voltage. This feature offers designers flexibility in driving the MOSFETs. Different MOSFETs require different VGS characteristics for optimum R_{DSON} performance. Typically, the higher the gate voltage (up to 16V), the lower the R_{DSON} achieved. For example, a NTMSF4899NF MOSFET can be driven to the ON state at 4.5V gate voltage but R_{DSON} is 7.5mΩ. If driven to 10V gate voltage, R_{DSON} is 4.5mΩ. In low-current applications, the losses due to R_{DSON} are minimal, but in high-current applications such as power hand tools, the difference in R_{DSON} can cut into the efficiency budget.

In portable hand tools and other battery-powered applications, the MIC4605 offers the ability to drive motors at a lower voltage compared to the traditional MOSFET drivers because of the wide VDD range (5.5V to 16V). Traditional MOSFET drivers typically require a VDD greater than 9V. The MIC4605 drives a motor using only two Li-ion batteries (total 7.2V) compared to traditional MOSFET drivers which will require at least three cells (total of 10.8V) to exceed the minimal VDD range. As an additional benefit, the low 5.5V gate drive capability allows a longer run time. This is because the Li-ion battery can run down to 5.5V, which is just above its 4.8V minimum recommended discharge voltage. This is also a benefit in higher current power tools that use five or six cells. The driver can be operated up to 16V to minimize the R_{DSON} of the MOSFETs and use as much of the discharge battery pack as possible for a longer run time. For example, an 18V battery pack can be used to the lowest operating discharge voltage of 13.5V.

Application Information

Adaptive Dead Time

The MIC4605 Door Lock/Unlock Module diagram illustrates how the MIC4605 drives the power stage of a DC motor. It is important that only one of the two MOSFETs is on at any given time. If both MOSFETs on the same side of the half bridge are simultaneously on, VIN will short to ground. The high current from the shorted VIN supply will then "shoot through" the MOSFETs into ground. Excessive shoot-through causes higher power dissipation in the MOSFETs, voltage spikes and ringing in the circuit. The high current and voltage ringing generate conducted and radiated EMI. Table 1 illustrates truth tables for both the MIC4605-1 (dual TTL inputs) and MIC4605-2 (single PWM input) that details the "first on" priority as well as the failsafe delay.

Table 1. MIC4605-1 and MIC4605-2 Truth Tables

LI	HI	LO	HO	Comments
0	0	0	0	Both outputs off.
0	1	0	1	HO will not go high until LO falls below 1.9V.
1	0	1	0	LO will be delayed an extra 240ns if HS never falls below 2.2V.
1	1	X	X	First ON stays on until input of same goes low.
	PWM	**LO**	**HO**	**Comments**
	0	1	0	LO will be delayed an extra 240ns if HS never falls below 2.2V.
	1	0	1	HO will not go high until LO falls below 1.9V.

Minimizing shoot-through can be done passively, actively or through a combination of both. Passive shoot-through protection can be achieved by implementing delays between the high and low gate drivers to prevent both MOSFETs from being on at the same time. These delays can be adjusted for different applications. Although simple, the disadvantage of this approach is requires long delays to account for process and temperature variations in the MOSFET and MOSFET driver.

Adaptive dead time monitors voltages on the gate drive outputs and switch node to determine when to switch the MOSFETs on and off. This active approach adjusts the delays to account for some of the variations, but it too has its disadvantages. High currents and fast switching voltages in the gate drive and return paths can cause parasitic ringing to turn the MOSFETs back on even while the gate driver output is low. Another disadvantage is that the driver cannot monitor the gate voltage inside the MOSFET. Figure 7 shows an equivalent circuit of the gate driver section, including parasitics.

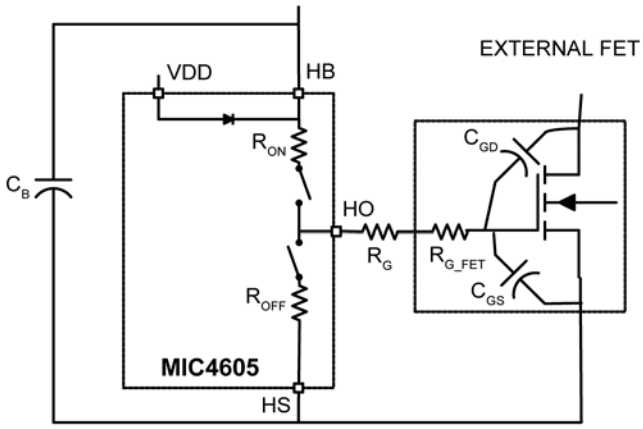


Figure 7. MIC4605 Driving an External MOSFET

The internal gate resistance (R_{G_FET}) and any external damping resistor (R_G) isolate the MOSFET's gate from the driver output. There is a delay between when the driver output goes low and the MOSFET turns off. This turn-off delay is usually specified in the MOSFET data sheet. This delay increases when an external damping resistor is used.

The MIC4605 uses a combination of active sensing and passive delay to ensure that both MOSFETs are not on at the same time, minimizing shoot-through current. Figure 8 illustrates how the adaptive dead time circuitry works.

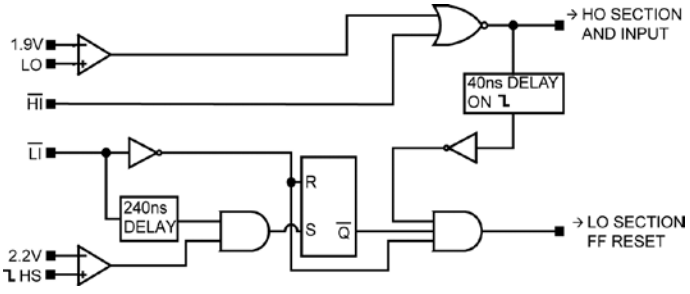


Figure 8. Adaptive Dead Time Logic Diagram (PWM)

Figure 9 shows the dead time (<20ns) between the gate drive output transitions as the low-side driver transitions from on-to-off while the high-side driver transitions from off-to-on.

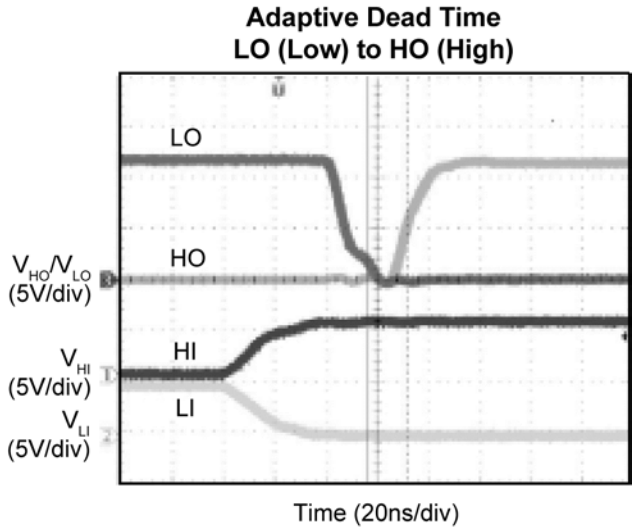


Figure 9. Adaptive Dead Time LO (Low) to HO (High)

A high level on the PWM pin causes the LO pin to go low. The MIC4605 monitors the LO pin voltage and prevents the HO pin from turning on until the voltage on the LO pin reaches the V_{LOOFF} threshold. After a short delay, the MIC4605 drives the HO pin high. Monitoring the LO voltage eliminates any excessive delay due to the MOSFET drivers turn-off time and the short delay accounts for the MOSFET turn-off delay as well as letting the LO pin voltage settle out. An external resistor between the LO output and the MOSFET may affect the performance of the LO pin monitoring circuit and is not recommended.

A low on the PWM pin causes the HO pin to go low after a short delay (T_{HOOFF}). Before the LO pin can go high, the voltage on the switching node (HS pin) must have dropped to 2.2V. Monitoring the switch voltage instead of the HO pin voltage eliminates timing variations and excessive delays due to the high side MOSFET turn-off. The LO driver turns on after a short delay (T_{LOON}). Once the LO driver is turned on, it is latched on until the PWM signal goes high. This prevents any ringing or oscillations on the switch node or HS pin from turning off the LO driver. If the PWM pin goes low and the voltage on the HS pin does not cross the V_{SWTH} threshold, the LO pin will be forced high after a short delay (T_{SWTO}), insuring proper operation.

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Care must be taken to ensure that the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is determined by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned back on.

Although the adaptive dead time circuit in the MIC4605 prevents the driver from turning both MOSFETs on at the same time, other factors outside of the anti-shoot-through circuit's control can cause shoot-through. Other factors include ringing on the gate drive node and capacitive coupling of the switching node voltage on the gate of the low-side MOSFET.

Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation

Quiescent current dissipation used to supply the internal logic and control functions.

Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the C_B capacitor multiplied by the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by Equation 1:

$$I_{F(AVE)} = Q_{GATE} \times f_S \qquad \text{Eq. 1}$$

Where:
Q_{GATE} = Total gate charge at $V_{HB} – V_{HS}$

f_S = gate drive switching frequency

The average power dissipated by the forward voltage drop of the diode equals, as illustrated in Equation 2:

$$P_{DIODE_{FWD}} = I_{F(AVE)} \times V_F \quad \text{Eq. 2}$$

Where:

V_F = Diode forward voltage drop

The value of V_F should be taken at the peak current through the diode; however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used, which will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 3µA at a reverse voltage of 85V at 125°C. Power dissipation due to reverse leakage is typically much less than 1mW and can be ignored.

Reverse recovery time is the time required for the injected minority carriers to be swept away from the depletion region during turn-off of the diode. Power dissipation due to reverse recovery can be calculated by computing the average reverse current due to reverse recovery charge times the reverse voltage across the diode. The average reverse current and power dissipation due to reverse recovery can be estimated by Equation 3:

$$I_{RR(AVE)} = 0.5 \times I_{RRM} \times t_{RR} \times f_S$$
$$P_{DIODE_{RR}} = I_{RR(AVE)} \times V_{REV} \quad \text{Eq. 3}$$

Where:
I_{RRM} = Peak reverse recovery current

t_{RR} = Reverse recovery time

The total diode power dissipation is noted in Equation 4:

$$P_{DIODE_{TOTAL}} = P_{DIODE_{FWD}} + P_{DIODE_{RR}} \quad \text{Eq. 4}$$

Figure 10 illustrates an optional external bootstrap diode may be used instead of the internal diode.

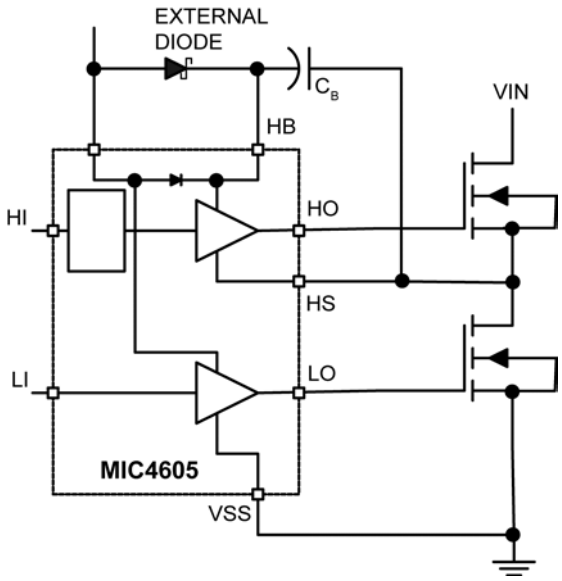


Figure 10. Optional Bootstrap Diode

An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the VDD supply voltage. The above equations can be used to calculate power dissipation in the external diode; however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated as in Equation 5:

$$P_{DIODE_{REV}} = I_R \times V_{REV} \times (1 - D) \quad \text{Eq. 5}$$

Where:
I_R = Reverse current flow at V_{REV} and T_J

V_{REV} = Diode reverse voltage

D = Duty cycle = $t_{ON} \times f_S$

The on-time is the time the high-side switch is conducting. In most topologies, the diode is reverse biased during the switching cycle off-time.

Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 11 shows a simplified equivalent circuit of the MIC4605 driving an external high-side MOSFET.

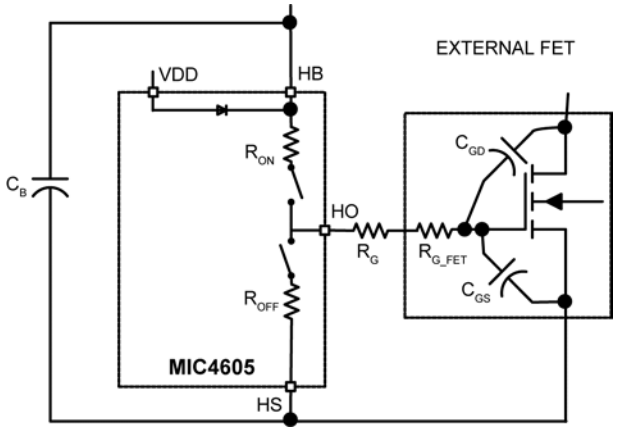


Figure 11. MIC4605 Driving an External MOSFET

Dissipation during the External MOSFET Turn-On

Energy from capacitor C_B is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{ON}, R_G and R_{G_FET}. R_{ON} is the on resistance of the upper driver MOSFET in the MIC4605. R_G is the series resistor (if any) between the driver IC and the MOSFET. R_{G_FET} is the gate resistance of the MOSFET. R_{G_FET} is usually listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{ON} and R_{G_FET}.

The effective capacitances of C_{GD} and C_{GS} are difficult to calculate because they vary non-linearly with Id, V_{GS}, and V_{DS}. Fortunately, most power MOSFET specifications include a typical graph of total gate charge vs. V_{GS}. Figure 12 shows a typical gate charge curve for an arbitrary power MOSFET. This chart shows that for a gate voltage of 10V, the MOSFET requires about 23.5nC of charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as noted in Equation 6:

$$E = \frac{1}{2} \times C_{ISS} \times V_{GS}^{2},$$

but

$$Q = C \times V, \qquad \text{Eq. 6}$$

so

$$E = \frac{1}{2} \times Q_G \times V_{GS}$$

Where:

C_{ISS} = Total gate capacitance of the MOSFET

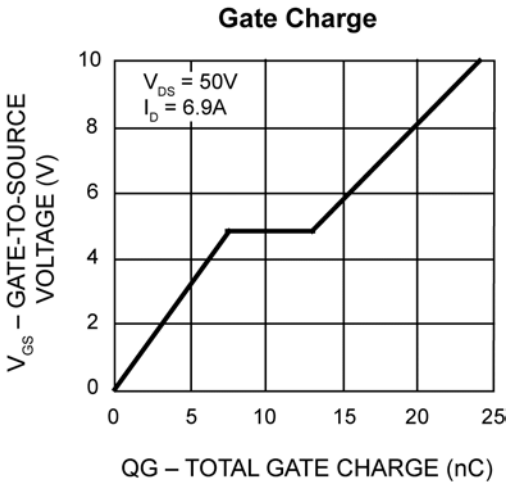


Figure 12. Typical Gate Charge vs. V_{GS}

The same energy is dissipated by R_{OFF}, R_G, and R_{G_FET} when the driver IC turns the MOSFET off. Assuming Ron is approximately equal to R_{OFF}, the total energy and power dissipated by the resistive drive elements is illustrated in Equation 7:

$$E_{DRIVER} = Q_G \times V_{GS}$$

and

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S \qquad \text{Eq. 7}$$

Where:

E_{DRIVER} = Energy dissipated per switching cycle

P_{DRIVER} = Power dissipated per switching cycle

Q_G = Total gate charge at V_{GS}

V_{GS} = Gate to source voltage on the MOSFET

f_S = Switching frequency of the gate drive circuit

The power dissipated inside the MIC4605 is equal to the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_FET}. Letting R_{ON} = R_{OFF}, the power dissipated in the MIC4605 due to driving the external MOSFET is illustrated in Equation 8:

$$P_{DISSDRIVER} = P_{DRIVER} \frac{R_{ON}}{R_{ON} + R_G + R_{G\_FET}} \quad \text{Eq. 8}$$

Supply Current Power Dissipation

Power is dissipated in the MIC4605 even if nothing is being driven. The supply current is drawn by the bias for the internal circuitry, the level shifting circuitry, and shoot-through current in the output drivers. The supply current is proportional to operating frequency and the VDD and VHB voltages. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4605 due to supply current is illustrated in Equation 9:

$$P_{DISSSUPPLY} = VDD \times IDD + VHB \times IHB \quad \text{Eq. 9}$$

Total Power Dissipation and Thermal Considerations

Total power dissipation in the MIC4605 is equal to the power dissipation caused by driving the external MOSFETs, the supply current and the internal bootstrap diode, as in Equation 10:

$$P_{DISSTOTAL} = P_{DISSSUPPLY} + P_{DISSDRIVE} + P_{DIODETOTAL} \quad \text{Eq. 10}$$

The die temperature can be calculated after the total power dissipation is known, as in Equation 11:

$$T_J = T_A + P_{DISSTOTAL} \times \theta_{JA} \quad \text{Eq. 11}$$

Where:

T_A = Maximum ambient temperature

T_J = Junction temperature (°C)

$P_{DISSTOTAL}$ = Power dissipation of the MIC4605

θ_{JA} = Thermal resistance from junction to ambient air

Other Timing Considerations

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned on.

Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low side (VDD) and high side (HB) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs and also minimize the voltage ripple on these pins. The capacitor from HB to HS has two functions: it provides decoupling for the high-side circuitry and also provides current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended because of the large change in capacitance over temperature and voltage. A minimum value of 0.1µF is required for each of the capacitors, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are used because even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for VDD should be placed as close as possible between the VDD and VSS pins. The bypass capacitor (C_B) for the HB supply pin must be located as close as possible between the HB and HS pins. The etch connections must be short, wide, and direct. The use of a ground plane to minimize connection impedance is recommended (refer to the Grounding, Component Placement, and Circuit Layout section for more information).

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge versus V_{GS} voltage. Based on this information and a recommended ΔV_{HB} of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

$$C_B \geq \frac{Q_{GATE}}{\Delta V_{HB}} \qquad \text{Eq. 12}$$

Where:

Q_{GATE} = Total gate charge at V_{HB}

ΔV_{HB} = Voltage drop at the HB pin

The decoupling capacitor for the VDD input may be calculated in with the same formula; however, the two capacitors are usually equal in value.

DC Motor Applications

MIC4605 MOSFET drivers are widely used in DC motor applications. They address brushed motors in both half-bridge and full-bridge motor topologies as well as three-phase brushless motors. As shown in Figure 13, Figure 14, and Figure 15, the drivers switch the MOSFETs at variable duty cycles that modulate the voltage to control motor speed. In the half-bridge topology, the motor turns in one direction only. The full-bridge topology allows for bidirectional control. Three-phase motors are more efficient compared to the brushed motors but require three half-bridge switches and additional circuitry to sense the position of the rotor.

The MIC4605 85V operating voltage offers the engineer margin to protect against back electromotive force (EMF) which is a voltage spike caused by the rotation of the rotor. The back EMF voltage amplitude depends on the speed of the rotation. It is good practice to have at least twice the HV voltage of the motor supply. 85V is plenty of margin for 12V, 24V, and 40V motors.

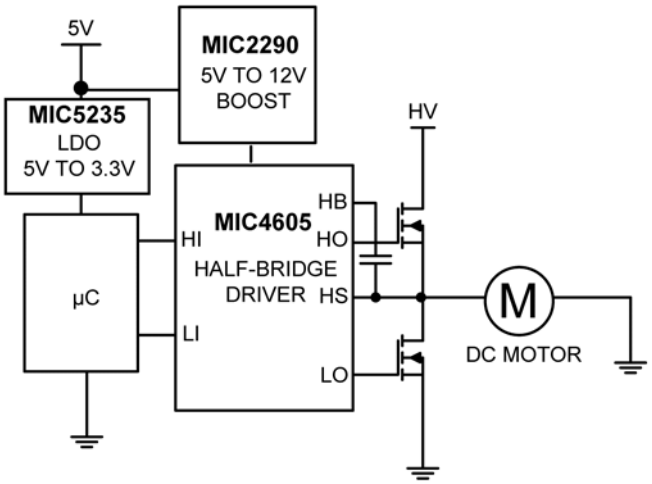


Figure 13. Half-Bridge DC Motor

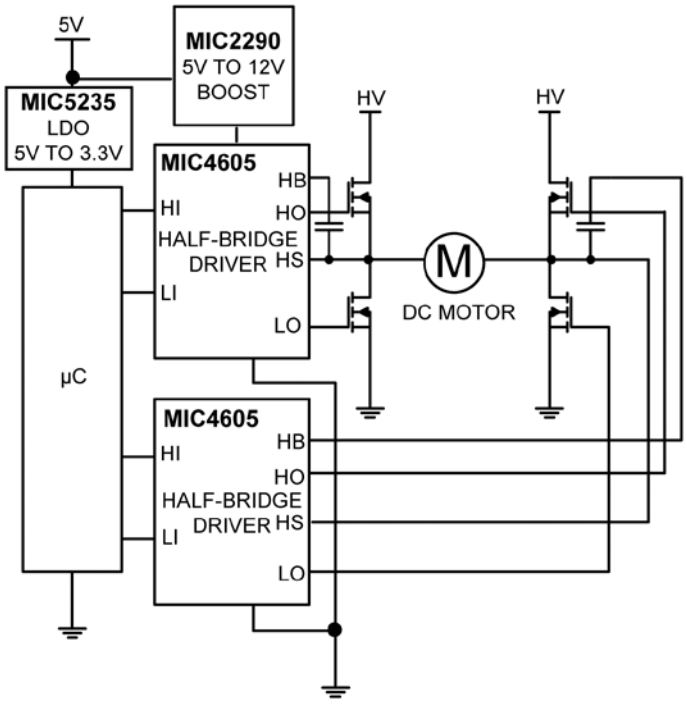


Figure 14. Full-Bridge DC Motor

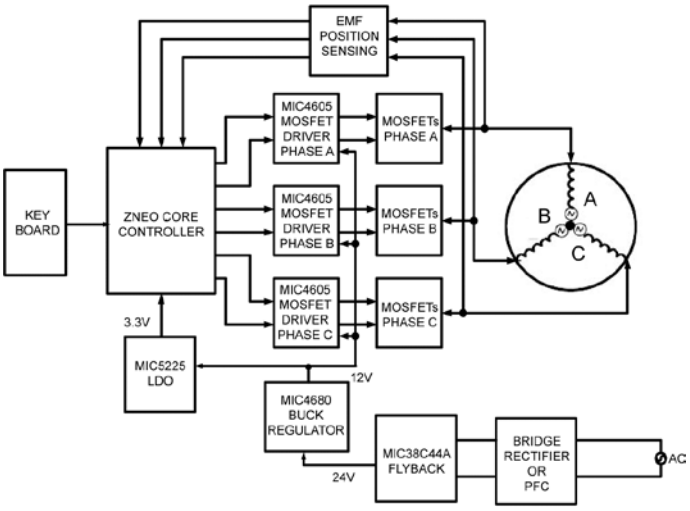


Figure 15. Three-Phase Brushless DC Motor Driver – 24V Block Diagram

The MIC4605 is offered in a small 2.5mm × 2.5mm TDFN package for applications that are space constrained and an SOIC-8 package for ease of manufacturing. The motor trend is to put the motor control circuit inside the motor casing, which requires small packaging because of the size of the motor.

The MIC4605 offers low UVLO threshold and programmable gate drive, which allows for longer operation time in battery operated motors such as power hand tools.

Cross conduction across the half bridge can cause catastrophic failure in a motor application. Engineers typically add dead time between states that switch between high input and low input to ensure that the low-side MOSFET completely turns off before the high-side MOSFET turns on and vice versa. The dead time depends on the MOSFET used in the application, but 200ns is typical for most motor applications.

Power Inverter

Power inverters are used to supply AC loads from a DC operated battery system, mainly during power failure. The battery voltage can be 12VDC, 24VDC, or up to 36VDC, depending on the power requirements. There two popular conversion methods, Type I and Type II, that convert the battery energy to AC line voltage (110VAC or 230VAC).

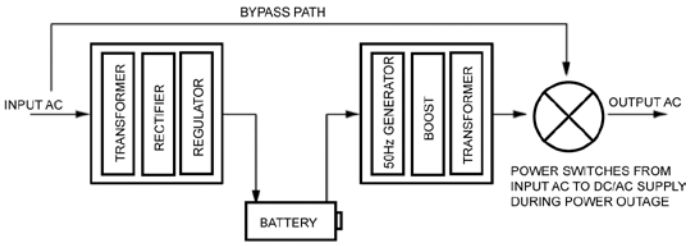


Figure 16. Type I Inverter Topology

As shown in Figure 16, Type I is a dual-stage topology where line voltage is converted to DC through a transformer to charge the storage batteries. When a power failure is detected, the stored DC energy is converted to AC through another transformer to drive the AC loads connected to the inverter output. This method is simplest to design but tends to be bulky and expensive because it uses two transformers.

Type II is a single-stage topology that uses only one transformer to charge the bank of batteries to store the energy. During a power outage, the same transformer is used to power the line voltage. The Type II switches at a higher frequency compared to the Type I topology to maintain a small transformer size.

Both types require a half bridge or full bridge topology to boost the DC to AC. This application can use two MIC4605s. The 85V operating voltage offers enough margin to address all of the available banks of batteries commonly used in inverter applications. The 85V operating voltage allows designers to increase the bank of batteries up to 72V, if desired. The MIC4605 can sink as much as 1A, which is enough current to overcome the MOSFET's input capacitance and switch the MOSFET up to 50kHz. This makes the MIC4605 an ideal solution for inverter applications.

As with all half bridge and full bridge topologies, cross conduction is a concern to inverter manufactures because it can cause catastrophic failure. This can be remedied by adding the appropriate dead time between transitioning from the high-side MOSFET to the low-side MOSFET and vice versa.

Grounding, Component Placement, and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MIC4605 drivers require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing, or circuit latch-up.

Figure 17 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD} and C_B. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate, and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the HB pin and out the HO pin, into the gate of the high side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor C_B. The high-side circuit return path usually does not have a low-impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the MOSFET.

It is important to note that capacitor CB must be placed close to the HB and HS pins. This capacitor not only provides all the energy for turn-on but it must also keep HB pin noise and ripple low for proper operation of the high-side drive circuitry.

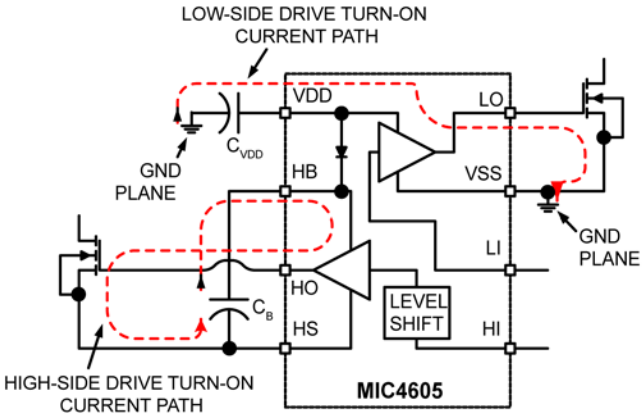


Figure 17. Turn-On Current Paths

Figure 18 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, C_B.

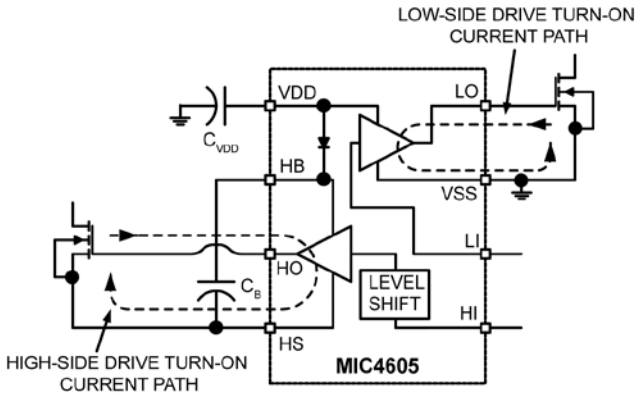
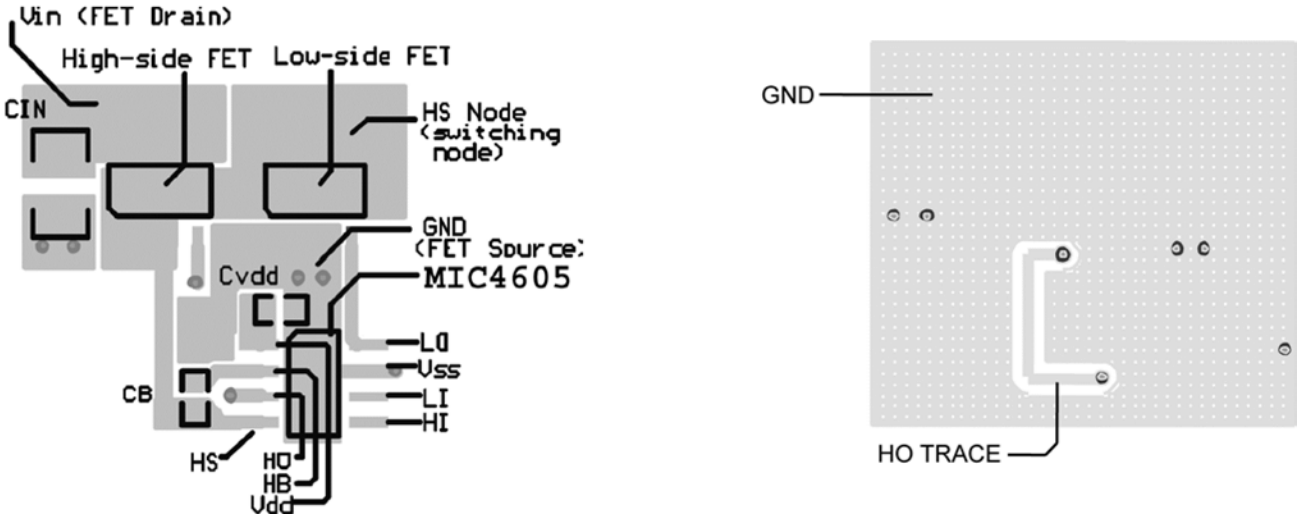


Figure 18. Turn-Off Current Paths

Use the following layout guidelines for optimum circuit performance:

- Use a ground plane to minimize parasitic inductance and impedance of the return paths. The MIC4605 is capable of greater than 1A peak currents and any impedance between the MIC4605, the decoupling capacitors, and the external MOSFET will degrade the performance of the driver.
- A typical layout of a synchronous buck converter power stage is shown in Figure 19.

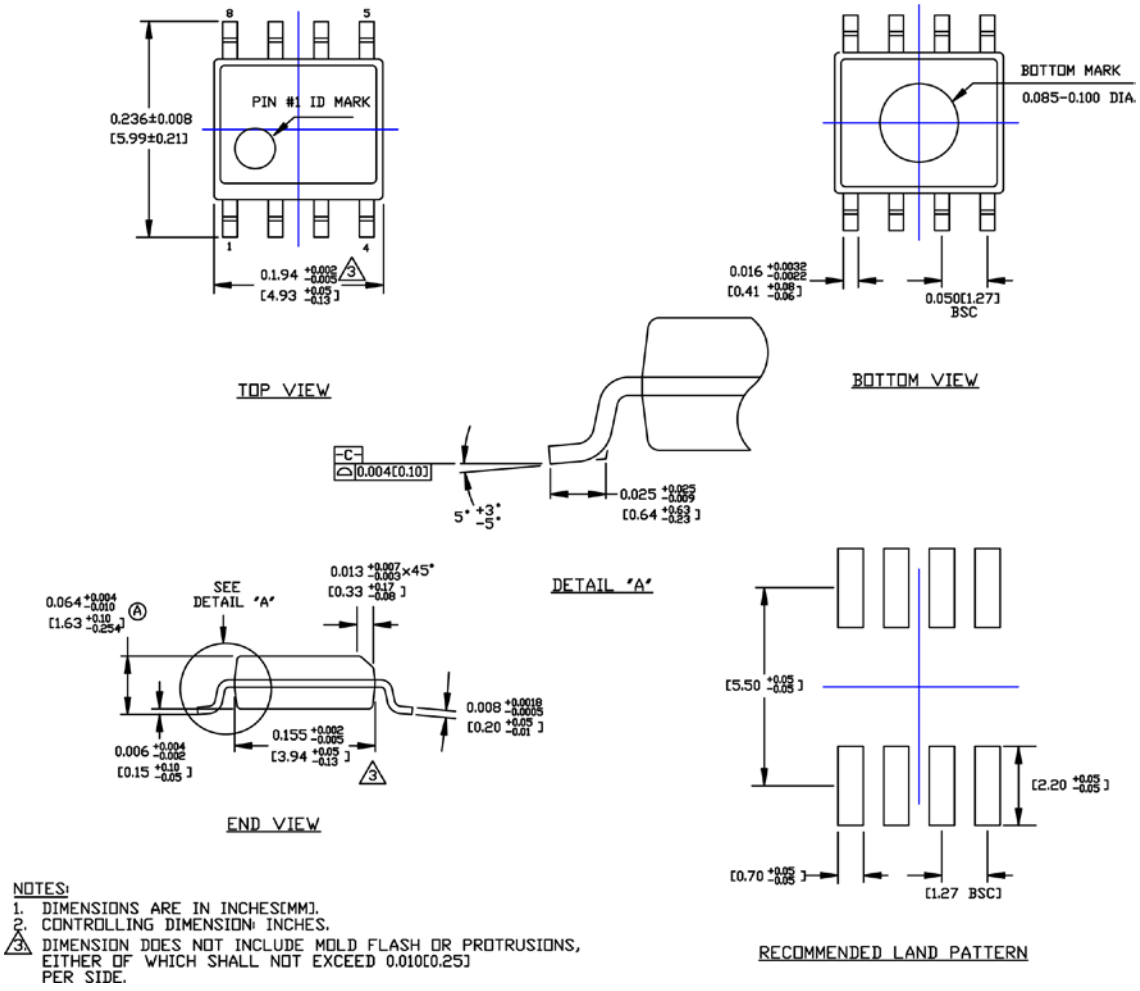
The high-side MOSFET drain connects to the input supply voltage (drain) and the source connects to the switching node. The low-side MOSFET drain connects to the switching node and its source is connected to ground. The buck converter output inductor (not shown) connects to the switching node. The high-side drive trace, HO, is routed on top of its return trace, HS, to minimize loop area and parasitic inductance. The low-side drive trace LO is routed over the ground plane to minimize the impedance of that current path. The decoupling capacitors, C_B and C_{VDD}, are placed to minimize etch length between the capacitors and their respective pins. This close placement is necessary to efficiently charge capacitor C_B when the HS node is low. All traces are 0.025in wide or greater to reduce impedance. C_{IN} is used to decouple the high current path through the MOSFETs.



Top Side **Bottom Side**

Figure 19. Typical Layout of a Synchronous Buck Converter Power Stage

Package Information[6] and Recommended Layout Pattern

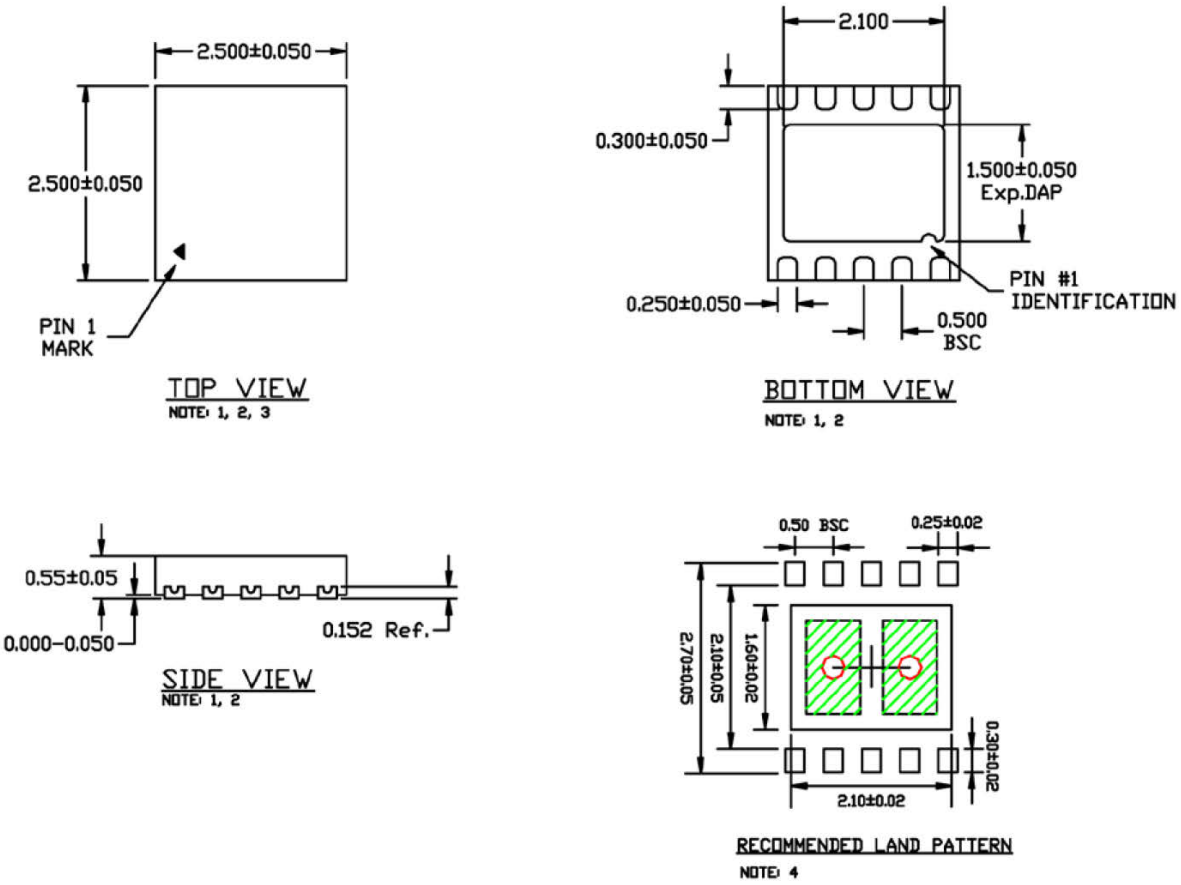


8-Pin SOIC (M)

Note:

6. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information[6] and Recommended Layout Pattern (Continued)



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. GREEN RECTANGLES (SHADED AREA) INDICATE STENCIL OPENING ON EXPOSED AREA. SIZE IS 0.6X0.9MM, SPACING IS 0.3MM.
5. RED CIRCLES REPRESENT THERMAL VIAS & SHOULD BE CONNECTED TO GND FOR MAX PERFORMANCE. 0.30 – 0.35 MM RECOMMENDED DIAMETER, 1.00 MM PITCH

2.5mm × 2.5mm 10-Pin TDFN (MT)

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