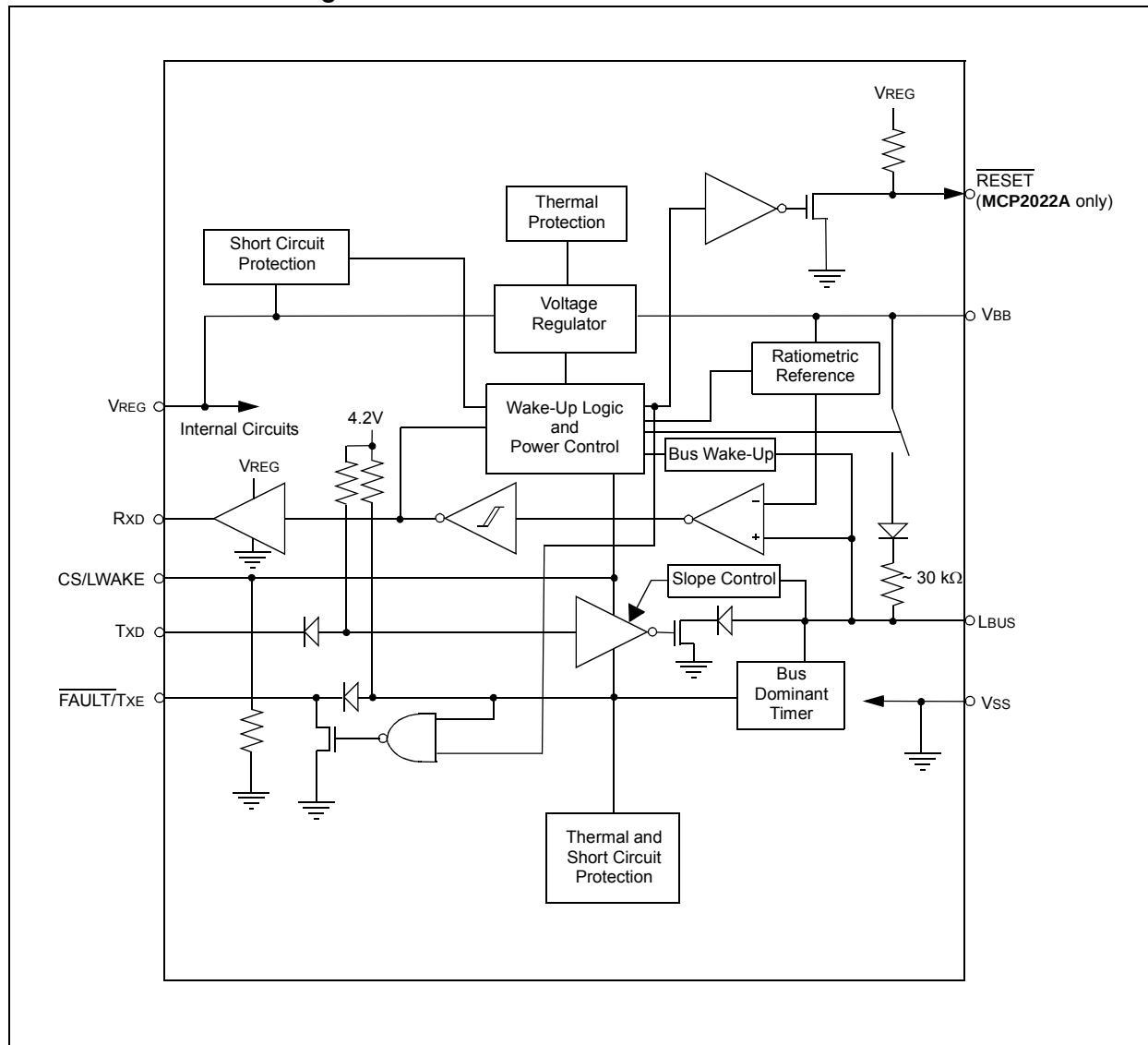


MCP2021A/2A

MCP2021A/2A Block Diagram



1.0 DEVICE OVERVIEW

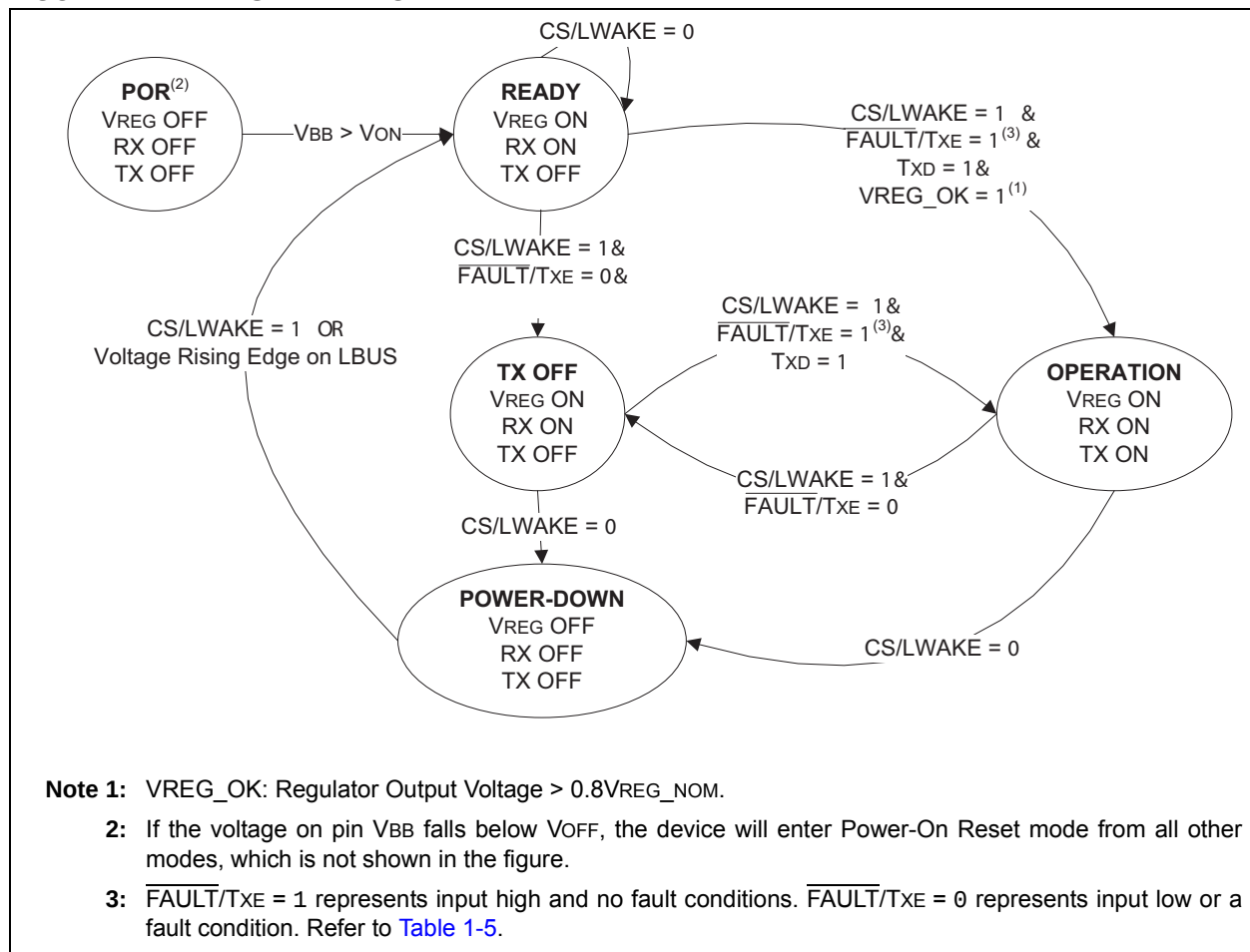
The MCP2021A/2A devices provide a physical interface between a microcontroller and a LIN half-duplex bus. They are intended for automotive and industrial applications with serial bus baud rates up to 20 kBaud. These devices will translate the CMOS/TTL logic levels to LIN logic levels and vice versa.

The MCP2021A/2A offer optimum EMI and ESD performance and can withstand high voltage on the LIN bus. The devices support two low-power modes to meet automotive industry power consumption requirements. The MCP2021A/2A also provide a +5V or 3.3V regulated power output at 70 mA.

1.1 Modes of Operation

The MCP2021A/2A work in five modes: Power-On Reset, Power-Down, Ready, Operation and Transmitter Off. For an overview of all operational modes, please refer to [Table 1-1](#). For the operational mode transition, please refer to [Figure 1-1](#).

FIGURE 1-1: STATE DIAGRAM



1.1.1 POWER-ON RESET MODE

Upon application of VBB or whenever the voltage on VBB is below the threshold of regulator turn-off voltage VOFF (typically 4.50V), the device enters Power-On Reset (POR) mode. During this mode, the device maintains the digital section in a Reset mode and waits until the voltage on the VBB pin rises above the threshold of regulator turn-on voltage VON (typically 5.75V) to enter Ready mode. In Power-On Reset mode, the LIN physical layer and voltage regulator are disabled and the RESET output (**MCP2022A** only) is forced to low.

1.1.2 READY MODE

The device enters Ready mode from POR mode after the voltage on VBB rises above the threshold of regulator turn-on voltage VON or from Power-Down mode when a remote or local wake-up event happens.

Upon entering Ready mode, the voltage regulator and the receiver section of the transceiver are powered up. The transmitter remains in an off state. The device is ready to receive data but not to transmit. In order to minimize the power consumption, the regulator operates in a reduced-power mode. It has a lower GBW product and it is thus slower. However, the 70 mA drive capability is unchanged.

The device stays in Ready mode until the output of the voltage regulator has stabilized and the CS/LWAKE pin is high ('1').

1.1.3 OPERATION MODE

If VREG is OK ($V_{REG} > 0.8 V_{REG_NORM}$) and the CS/LWAKE, FAULT/TXE and TXD pins are high, the part enters Operation mode from either Ready or Transmitter Off mode.

In this mode, all internal modules are operational. The internal pull-up resistor between LBUS and VBB is connected only in this mode.

The device goes into Power-Down mode at the falling edge on CS/LWAKE or into Transmitter Off mode at the falling edge on FAULT/TXE while CS/LWAKE stays high.

1.1.4 TRANSMITTER OFF MODE

In Transmitter Off mode, the receiver is enabled but the LBUS transmitter is off. It is a lower power mode.

In order to minimize power consumption, the regulator operates in a reduced-power mode. It has a lower GBW product and it is thus slower. However, the 70 mA drive capability is unchanged.

The transmitter may be re-enabled whenever the FAULT/TXE signal returns high, by removing the internal fault condition and by driving FAULT/TXE high. The transmitter will not be enabled even if the FAULT/TXE pin is brought high externally, when the internal fault is still present. However, externally forcing the FAULT/TXE high while the internal fault is still present should be avoided, since this will induce high current and power dissipation in the FAULT/TXE pin.

The transmitter is also turned off whenever the voltage regulator is unstable or recovering from a fault. This prevents unwanted disruption of the bus during times of uncertain operation.

1.1.5 POWER-DOWN MODE

In Power-Down mode, the transceiver and the voltage regulator are both off. Only the bus wake-up section and the CS/LWAKE pin wake-up circuits are in operation. This is the lowest power mode.

If any bus activity (e.g., a Break character) occurs during Power-Down mode, the device will immediately enter Ready mode and enable the voltage regulator. Then, once the regulator output has stabilized (approximately 0.3 ms to 1.2 ms), it goes into Operation mode. Refer to [Section 1.1.6 "Remote Wake-Up"](#).

The part will also enter Ready mode from Power-Down mode, followed by the Operation mode, if the CS/LWAKE pin becomes active high ('1').

1.1.6 REMOTE WAKE-UP

The Remote Wake-Up sub-module observes the LBUS in order to detect bus activity. In Power-Down mode, normal LIN recessive/dominant threshold is disabled and the LIN bus wake-up voltage threshold VWK(LBUS) is used to detect bus activities. Bus activity is detected when the voltage on the LBUS falls below the LIN bus wake-up voltage threshold VWK(LBUS) (approximately 3.5V) for at least tBDB (a typical duration of 80 μ s) followed by a rising edge. Such a condition causes the device to leave Power-Down mode.

TABLE 1-1: OVERVIEW OF OPERATIONAL MODES

State	Transmitter	Receiver	Internal Wake Module	Voltage Regulator	Operation	Comments
POR	OFF	OFF	OFF	OFF	Proceed to Ready mode after $V_{BB} > V_{ON}$	
Ready	OFF	ON	OFF	ON	If CS/LWAKE is high, then proceed to Operation or Transmitter Off mode.	Bus Off state
Operation	ON	ON	OFF	ON	If CS/LWAKE is low, then proceed to Power-Down mode. If $\overline{\text{FAULT/TXE}}$ is low, then proceed to Transmitter Off mode.	Normal Operation mode
Power-Down	OFF	OFF	ON Activity Detect	OFF	On LIN bus rising edge or CS/LWAKE high level, go to Ready mode.	Lowest power mode
Transmitter Off	OFF	ON	OFF	ON	If CS/LWAKE is low, then proceed to Power-Down mode. If $\overline{\text{FAULT/TXE}}$ is high, then proceed to Operation mode.	Bus Off state, lower power mode

MCP2021A/2A

1.2 Pin Descriptions

The descriptions of the pins are listed in [Table 1-2](#).

TABLE 1-2: PIN FUNCTION TABLE

Pin Name	Pin Number			Pin Type	Description
	8-lead PDIP, SOIC	4x4 DFN	14-lead PDIP, SOIC, TSSOP		
RxD	1	1	1	Output	Receive Data Output
CS/LWAKE	2	2	2	TTL Input, HV-tolerant	Chip Select and Local Wake-up Input
VREG	3	3	3	Output	Voltage Regulator Output
TxD	4	4	4	Input, HV-tolerant	Transmit Data Input
RESET	—	—	5	Output	Reset Output
NC	—	—	6–10	—	No Connection
VSS	5	5	11	Power	Ground
LBUS	6	6	12	I/O, HV	LIN Bus
VBB	7	7	13	Power	Battery
FAULT/TxE	8	8	14	I/O, HV-tolerant	Fault Detect Output/Transmitter Enable Input
EP	—	9	—	—	Exposed Thermal Pad

1.2.1 RECEIVE DATA OUTPUT (RxD)

Receive Data Output pin. The RxD pin is a standard CMOS output pin and it follows the state of the LBUS pin.

1.2.2 CHIP SELECT AND LOCAL WAKE-UP INPUT (CS/LWAKE)

Chip Select and Local Wake-up Input pin (TTL level, high-voltage tolerant). This pin controls the device state transition. Refer to [Figure 1-1](#).

If CS/LWAKE = 1, the device can work in Operation mode (FAULT/TxE = 1) or in Transmitter Off mode (FAULT/TxE = 0). If CS/LWAKE = 0, the device can work in Power-Down mode or in Ready mode.

An internal pull-down resistor will keep the CS/LWAKE pin low to ensure that no disruptive data will be present on the bus while the microcontroller is executing a Power-On Reset and I/O initialization sequence. When CS/LWAKE is '1', a weak pull-down (~600 kΩ) is used to reduce current. When CS/LWAKE is '0', a stronger pull-down (~300 kΩ) is used to maintain the logic level.

This pin may also be used as a local wake-up input (see [Figure 1-1](#)). The microcontroller will set the I/O pin to control the CS/LWAKE. An external switch or another source can then wake up both the transceiver and the microcontroller.

Note: CS/LWAKE should NOT be tied directly to the VREG pin as this could force the MCP2021A/2A into Operation mode before the microcontroller is initialized.

1.2.3 POWER OUTPUT (VREG)

Positive Supply Voltage Regulator Output pin. An on-chip LDO gives +5.0 or +3.3V at 70 mA regulated voltage on this pin.

1.2.4 TRANSMIT DATA INPUT (TxD)

Transmit Data Input pin (TTL level, HV-compliant, adaptive pull-up). The transmitter reads the data stream on the TxD pin and sends it to the LIN bus. The LBUS pin is low (dominant) when TxD is low and high (recessive) when TxD is high.

TxD is internally pulled up to approximately 4.2V. When TxD is '0', a weak pull-up (~900 kΩ) is used to reduce current. When TxD is '1', a stronger pull-up (~300 kΩ) is used to maintain the logic level. A series reverse-blocking diode allows applying TxD input voltages greater than the internally generated 4.2V and renders the TxD pin HV-compliant up to 30V (see [MCP2021A/2A Block Diagram](#)).

1.2.5 RESET (MCP2022A ONLY)

RESET output pin. This pin is open-drain with ~90 kΩ pull-up to VREG. It indicates the internal voltage has reached a valid, stable level. As long as the internal voltage is valid (above 0.8 VREG), this pin will remain high ('1'); otherwise, the RESET pin switches to low ('0').

1.2.6 NO CONNECTION (NC)

No internal connection.

1.2.7 GROUND (Vss)

Ground pin.

1.2.8 LIN BUS (LBUS)

LIN Bus pin. LBUS is a bidirectional LIN bus interface pin and is controlled by the signal TxD. It has an open collector output with a current limitation. To reduce electromagnetic emission, the slopes during signal changes are controlled and the LBUS pin has corner-rounding control for both falling and rising edges.

The internal LIN receiver observes the activities on the LIN bus and generates the output signal RxD that follows the state of the LBUS. A 1st degree 160 kHz low-pass input filter optimizes electromagnetic immunity.

1.2.9 BATTERY POSITIVE SUPPLY VOLTAGE (VBB)

Battery Positive Supply Voltage pin. An external diode is connected in series to prevent the device from being reversely powered (refer to [Figure 1-7](#)).

1.2.10 FAULT DETECT OUTPUT/TRANSMITTER ENABLE INPUT (FAULT/TxE)

Fault Detect Output/Transmitter Enable Input pin. The output section is HV-tolerant open-drain (up to 30V). The input section is identical to the TxD section (TTL level, HV-compliant, adaptive pull-up). The internal pull-up resistor may be too weak for some applications. We recommend adding a 10 kΩ external pull-up resistor to ensure a logic high level. Its state is defined as shown in [Table 1-5](#). The device is placed in Transmitter Off mode whenever this pin is low ('0'), either from an internal fault condition or by external drive.

If CS/LWAKE is high ('1'), the $\overline{\text{FAULT/TxE}}$ signals a mismatch between the TxD input and the LBUS level. This can be used to detect a bus contention. Since the bus exhibits a propagation delay, the sampling of the internal compare is debounced to eliminate false faults.

After the device wakes up, the $\overline{\text{FAULT/TxE}}$ indicates what wakes the device if CS/LWAKE remains low ('0') (refer to [Table 1-5](#)).

The $\overline{\text{FAULT/TxE}}$ pin sampled at a rate faster than every 10 μs.

TABLE 1-3: $\overline{\text{FAULT/TxE}}$ TRUTH TABLE

TxD In	RxD Out	LINBUS I/O	Thermal Override	FAULT/TxE		Definition
				External Input	Driven Output	
CS = 1						
L	H	VBB	OFF	H	L	FAULT , TxD driven low, LBUS shorted to VBB (Note 1) or LBUS/TxD permanent dominant detected and Transmit time-out shutdown.
H	H	VBB	OFF	H	H	OK
L	L	GND	OFF	H	H	OK
H	L	GND	OFF	H	H	OK , data is being received from LBUS
x	x	VBB	ON	H	L	FAULT , Transceiver in thermal shutdown
x	x	VBB	x	L	x	NO FAULT , the CPU is commanding the transceiver to turn off the transmitter driver
CS = 0						
x	x	x	x	x	L	Wake-up from LIN bus activity
x	x	x	x	x	H	Wake-up from POR

Legend: x = Don't care

Note 1: The $\overline{\text{FAULT/TxE}}$ is valid after approximately 25 μs after the TxD falling edge. This is to eliminate false fault reporting during bus propagation delays.

1.3 Fail-Safe Features

1.3.1 GENERAL FAIL-SAFE FEATURES

- An internal pull-down resistor on CS/LWAKE pin disables the transmitter if the pin is floating.
- An internal pull-up resistor on the TXD pin places TXD in high and the LBUS in recessive if the TXD pin is floating.
- High-impedance and low-leakage current on LBUS during loss of power or ground.
- The current limit on LBUS protects the transceiver from being damaged if the pin is shorted to VBB.

1.3.2 THERMAL PROTECTION

The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter and voltage regulator.

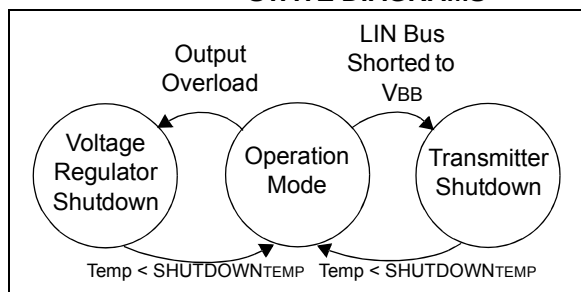
There are three causes for a thermal overload. A thermal shutdown can be triggered by any one, or a combination of, the following thermal overload conditions:

- Voltage regulator overload
- LIN bus output overload
- Increase in die temperature due to increase in environment temperature

The recovery time from the thermal shutdown is equal to adequate cooling time.

Driving the TXD and checking the RXD pin make it possible to determine whether there is a bus contention (TXD = high, RXD = low) or a thermal overload condition (TXD = low, RXD = high).

FIGURE 1-2: THERMAL SHUTDOWN STATE DIAGRAMS



1.3.3 TXD/LBUS TIME-OUT TIMER

The LIN bus can be driven to a dominant level either from the TXD pin or externally. An internal timer deactivates the LBUS transmitter if a dominant status (low) on the LIN bus lasts longer than Bus Dominant Time-out Time, $t_{TO(LIN)}$ (approximately 20 milliseconds). At the same time, the RXD output is put in recessive (high), FAULT/TXE is also driven to low and the internal LIN pull-up resistor is disconnected. The timer is reset on any recessive LBUS status or POR mode. The recessive status on LBUS can be caused either by the bus being externally pulled up or by the TXD pin being returned high.

1.4 Internal Voltage Regulator

The MCP2021A/2A have a positive regulator capable of supplying +5.00 or +3.30 VDC $\pm 3\%$ at up to 70 mA of load current over the entire operating temperature range of -40°C to $+125^{\circ}\text{C}$. The regulator uses a LDO design, is short-circuit-protected and will turn the regulator output off if its output falls below the shutdown voltage threshold, VSD.

With a load current of 70 mA, the minimum input to output voltage differential required for the output to remain in regulation is typically +0.5V (+1V maximum over the full operating temperature range). Quiescent current is less than 100 μA with a full 70 mA load current when the input to output voltage differential is greater than +3.00V.

Regarding the correlation between VBB, VREG and IDD, please refer to Figures 1-4 and 1-5. When the input voltage (VBB) drops below the differential needed to provide stable regulation, the voltage regulator output, VREG, will track the input down to approximately VOFF, at which point the regulator will turn off the output. This will allow PIC[®] microcontrollers with internal POR circuits to generate a clean arming of the POR trip point. The MCP2021A/2A will then monitor VBB and turn on the regulator when VBB is above the threshold of regulator turn-on voltage, VON.

In Power-Down mode, the VBB monitor is turned off.

Under specific ambient temperature and battery voltage range, the voltage regulator can output as high as 150 mA current. For current load capability of the voltage regulator, refer to Figures 2-8 and 2-9.

Note: The regulator has an overload current limit of approximately 250 mA. The regulator output voltage, VREG, is monitored. If output voltage VREG is lower than VSD, the voltage regulator will turn off. After a recovery time of about 3 ms, the VREG will be checked again. If there is no short circuit ($V_{REG} > V_{SD}$), then the voltage regulator remains on.

The regulator requires an external output bypass capacitor for stability. See [Figure 2-1](#) for correct capacity and ESR for stable operation.

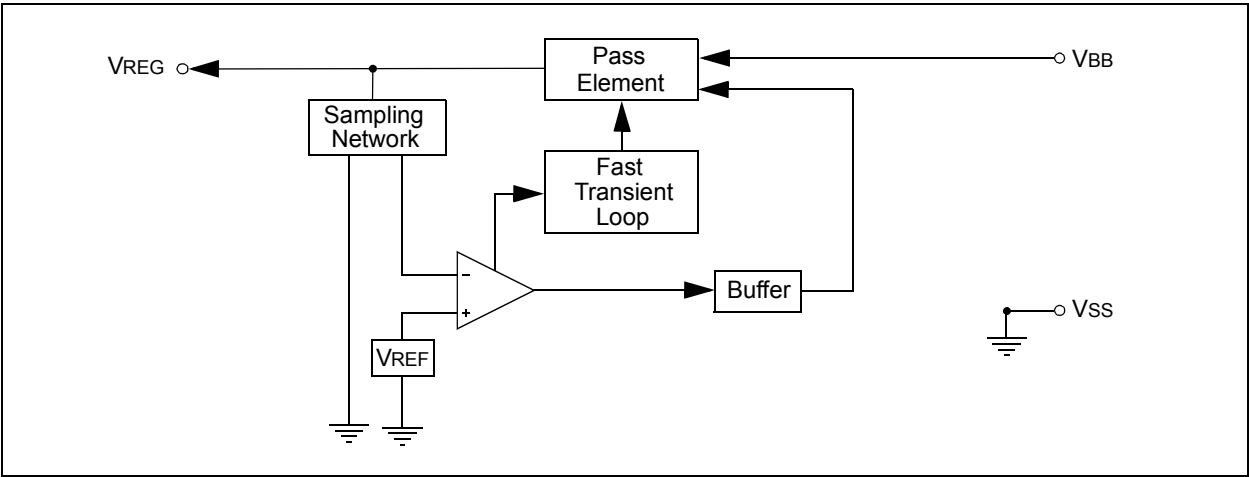
Note: A ceramic capacitor of at least 10 μF or a tantalum capacitor of at least 2.2 μF is recommended for stability.

In worst-case scenarios, the ceramic capacitor may derate by 50%, based on tolerance, voltage and temperature. Therefore, in order to ensure stability, ceramic capacitors smaller than 10 μF may require a small series resistance to meet the ESR requirements, as shown in [Table 1-4](#).

TABLE 1-4: RECOMMENDED SERIES RESISTANCE FOR CERAMIC CAPACITORS

Resistance	Capacitor
1 Ω	1 μF
0.47 Ω	2.2 μF
0.22 Ω	4.7 μF
0.1 Ω	6.8 μF

FIGURE 1-3: VOLTAGE REGULATOR BLOCK DIAGRAM



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FIGURE 1-4: VOLTAGE REGULATOR OUTPUT ON POWER-ON RESET

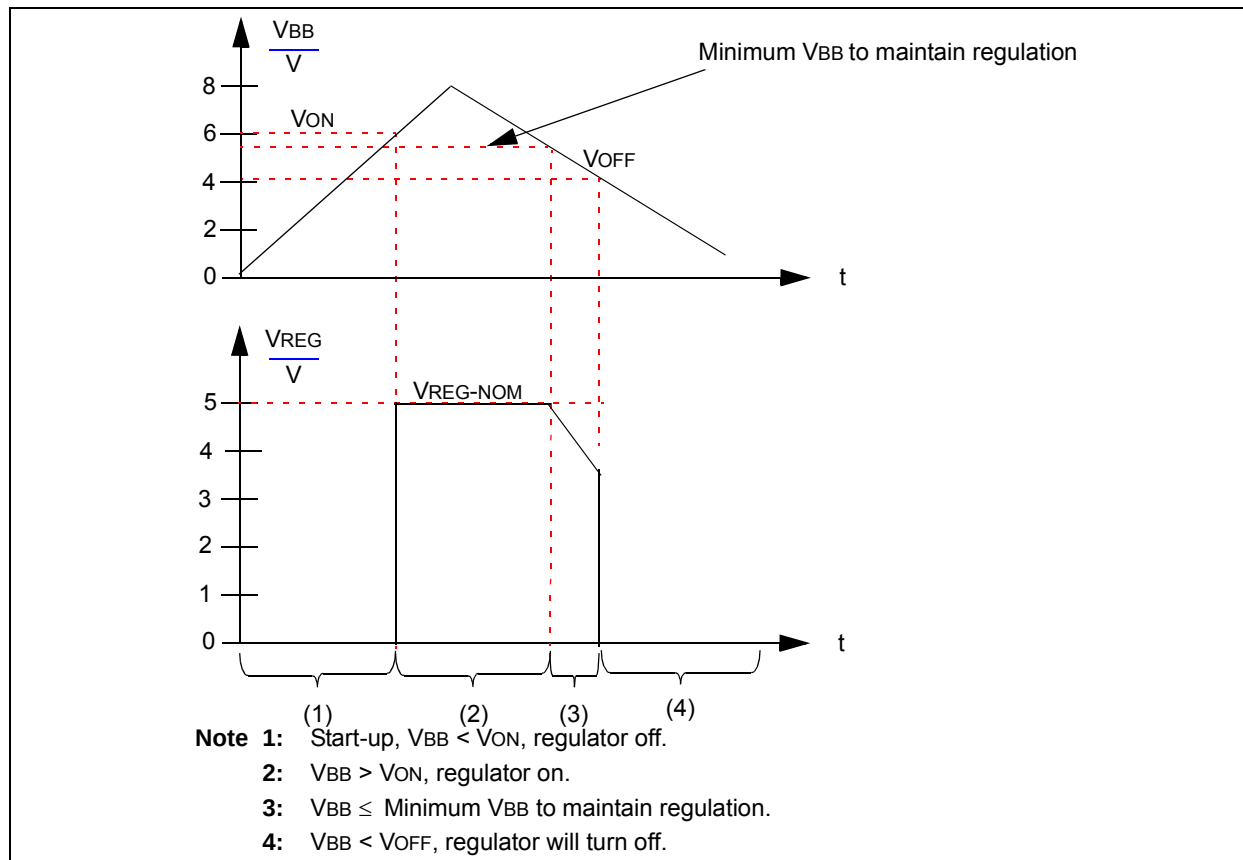
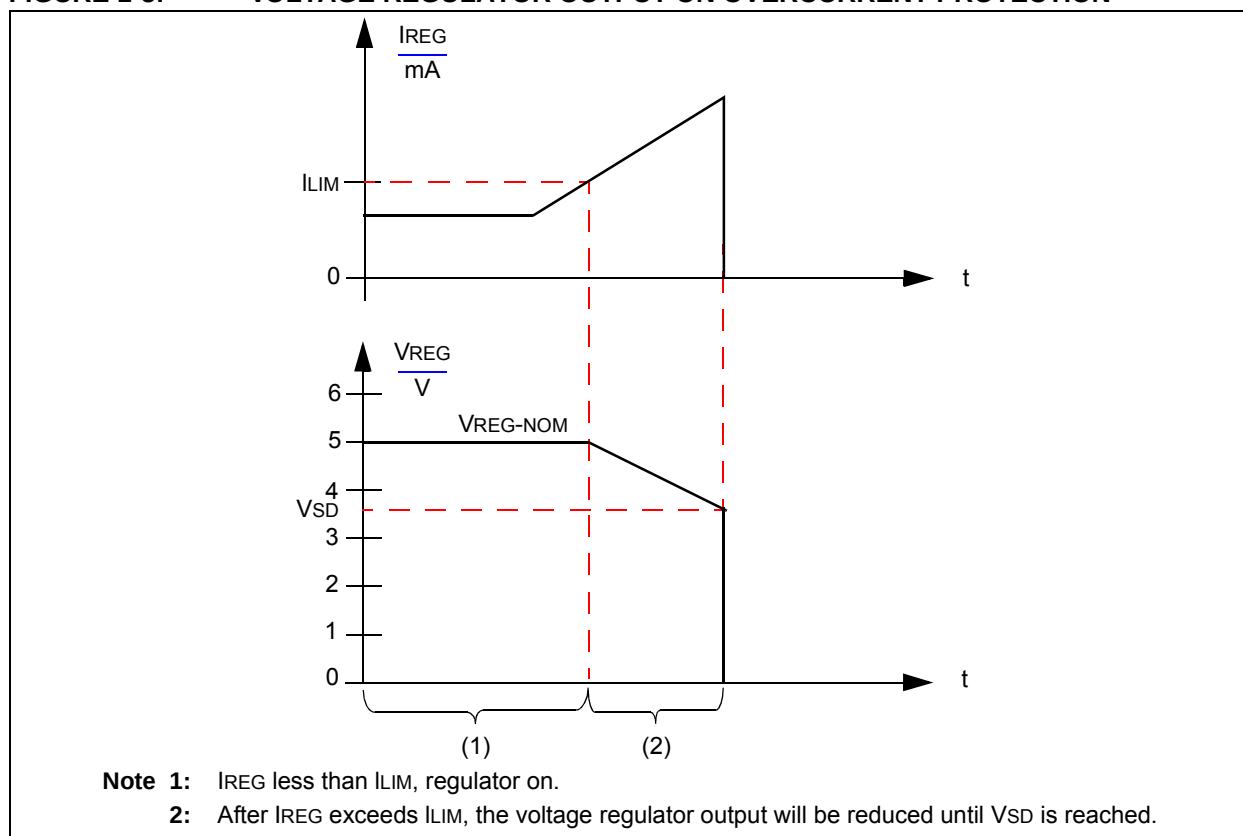


FIGURE 1-5: VOLTAGE REGULATOR OUTPUT ON OVERCURRENT PROTECTION



1.5 Optional External Protection

1.5.1 REVERSE BATTERY PROTECTION

An external reverse-battery-blocking diode should be used to provide polarity protection (see [Figure 1-7](#)).

1.5.2 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 43V transient suppressor (TVS) diode, between V_{BB} and ground, with a transient protection resistor (R_{TP}) in series with the battery supply and the V_{BB} pin, protects the device from power transients and ESD events greater than 43V (see [Figure 1-7](#)). The maximum value for the RTP protection resistor depends upon two parameters: the minimum voltage the part will start at and the impacts of this RTP resistor on the V_{BB} value, thus on the bus recessive level and slopes.

This leads to a set of three equations to fulfill.

[Equation 1-1](#) provides a maximum RTP value according to the minimum battery voltage the user wants.

[Equation 1-2](#) provides a maximum RTP value according to the maximum error on the recessive level, thus V_{BB}, since the part uses V_{BB} as the reference value for the recessive level.

[Equation 1-3](#) provides a maximum RTP value according to the maximum relative variation the user can accept on the slope when I_{REG} varies.

Since both [Equations 1-1](#) and [1-2](#) must be fulfilled, the maximum allowed value for RTP is thus the smaller of the two values found when solving [Equations 1-1](#) and [1-2](#).

Usually [Equation 1-1](#) gives the higher constraint (smaller value) for RTP, as shown in the following example where V_{BATmin} is 8V.

However, the user needs to check that the value found with [Equation 1-1](#) fulfills [Equations 1-2](#) and [1-3](#).

While this protection is optional, it should be considered as good engineering practice.

EQUATION 1-1:

$$R_{TP} \leq \frac{V_{BATmin} - 5.5V}{250 \text{ mA}}$$

$$5.5V = V_{OFF} + 1.0V$$

Where:

250 mA = Peak current at power-on when V_{BB} = 5.5V

Assume V_{BATmin} = 8V. [Equation 1-1](#) shows 10Ω.

EQUATION 1-2:

$$R_{TP} \leq \frac{\Delta V_{RECESSIVE}}{I_{REGMAX}}$$

Where:

ΔV_{RECESSIVE} = Maximum variation tolerated on the recessive level

Assume ΔV_{RECESSIVE} = 1V and I_{REGMAX} = 50 mA. [Equation 1-2](#) shows 20Ω.

EQUATION 1-3:

$$R_{TP} \leq \frac{\Delta \text{Slope} \times (V_{BATmin} - 1V)}{I_{REGMAX}}$$

Where:

ΔSlope = Maximum variation tolerated on the slope level

I_{REGMAX} = Maximum current the current will provide to the load

V_{BATmin} > V_{OFF} + 1.0V

Assume ΔSlope = 15%, V_{BATmin} = 8V and I_{REGMAX} = 50 mA. [Equation 1-2](#) shows 20Ω.

1.5.3 CBAT CAPACITOR

Selecting C_{BAT} = 10 x C_{REG} is recommended. However, this leads to a high value capacitor. Lower values for C_{BAT} capacitor can be used with respect to some rules. In any case, the voltage at the V_{BB} pin should remain above V_{OFF} when the device is turned on.

The current peak at start-up (due to the fast charge of the C_{REG} and C_{BAT} capacitors) may induce a significant drop on the V_{BB} pin. This drop is proportional to the impedance of the V_{BAT} connection (see [Figure 1-7](#)).

The V_{BAT} connection is mainly inductive and resistive. Therefore, it can be modeled as a resistor (R_{TOT}) in series with an inductor (L). R_{TOT} and L can be measured.

The following formula gives an indication of the minimum value of C_{BAT} using R_{TOT} and L:

EQUATION 1-4:

$$\frac{C_{BAT}}{C_{REG}} = \sqrt{\frac{100L^2 + R_{TOT}^2}{1 + L^2 + \frac{R_{TOT}^2}{100}}}$$

Where:

L = Inductor (measured in mH)

R_{TOT} = R_{LINE} + R_{TP} (measured in Ω)

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Equation 1-4 allows lower C_{BAT}/C_{REG} values than the 10x ratio we recommend.

Assume that we have a good quality VBAT connection with $R_{TOT} = 0.1\Omega$ and $L = 0.1\text{ mH}$.

Solving the equation gives $C_{BAT}/C_{REG} = 1$.

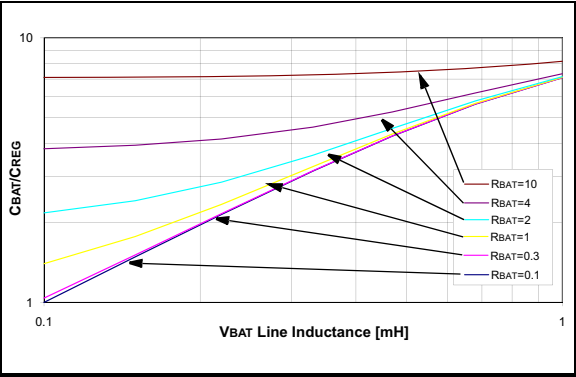
If we increase R_{TOT} up to 1Ω , the result becomes $C_{BAT}/C_{REG} = 1.4$. However, if the connection is highly resistive or highly inductive (poor connection), the C_{BAT}/C_{REG} ratio greatly increases.

TABLE 1-5: **C_{BAT}/C_{REG} RATIO BY VBAT CONNECTION TYPE**

Connection Type	R_{TOT}	L	C_{BAT}/C_{REG} Ratio
Good	0.1Ω	0.1 mH	1
Typical	1Ω	0.1 mH	1.4
Highly inductive	0.1Ω	1 mH	7
Highly resistive	10Ω	0.1 mH	7

Figure 1-6 shows the minimum recommended C_{BAT}/C_{REG} ratio as a function of the impedance of the VBAT connection.

FIGURE 1-6: **MINIMUM RECOMMENDED C_{BAT}/C_{REG} RATIO**



1.6 Typical Applications

FIGURE 1-7: TYPICAL APPLICATION CIRCUIT

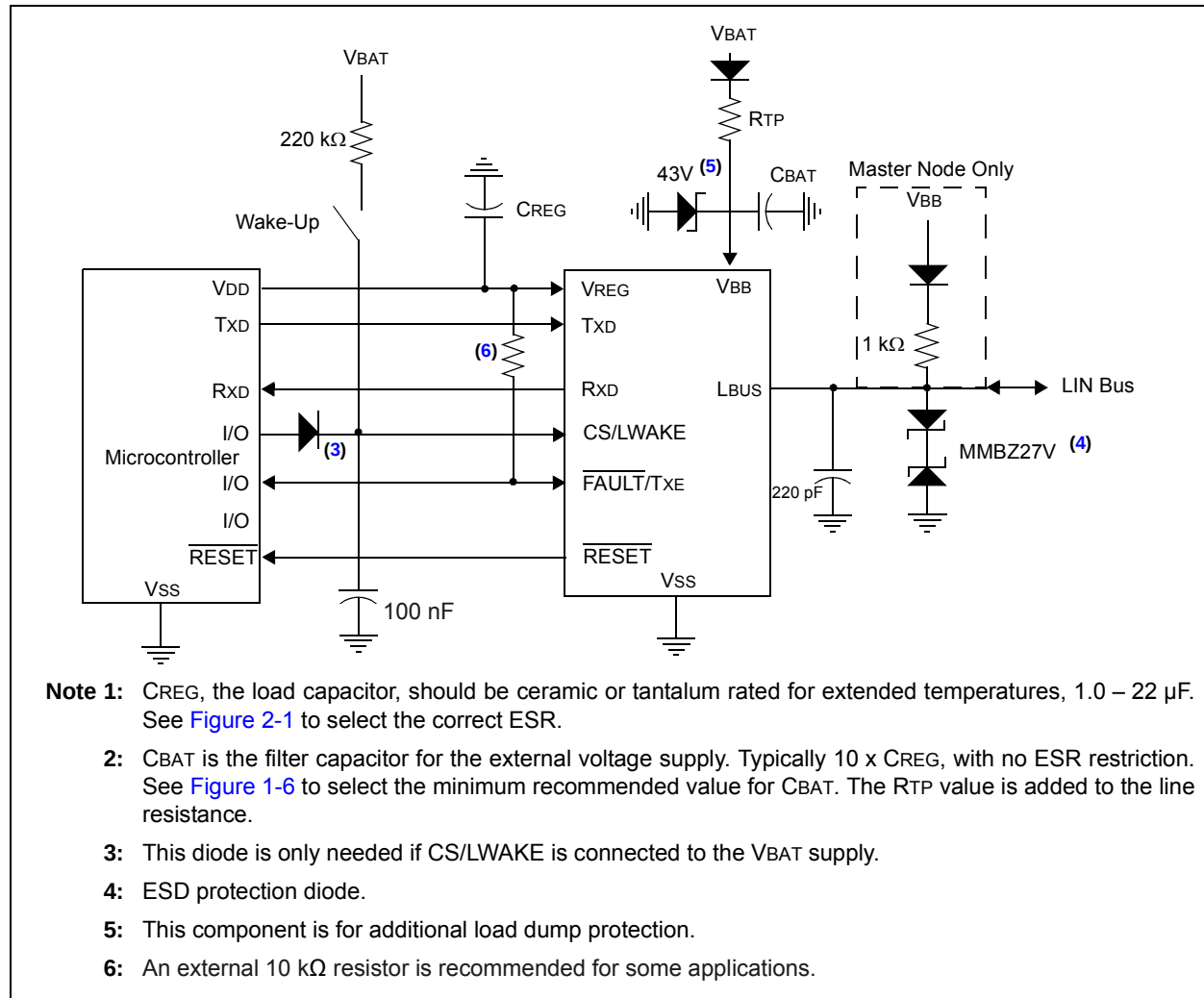
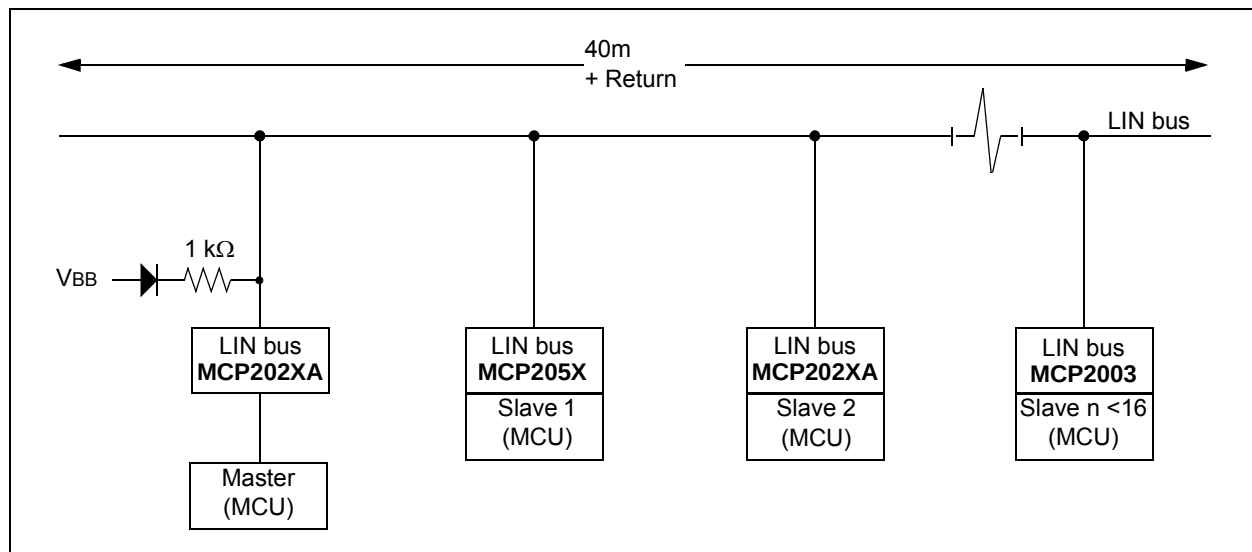


FIGURE 1-8: TYPICAL LIN NETWORK CONFIGURATION



MCP2021A/2A

1.7 ICSP™ Considerations

The following should be considered when the MCP2021A/2A are connected to pins supporting in-circuit programming:

- Power used for programming the microcontroller can be supplied from the programmer or from the MCP2021A/2A.
- The voltage on the VREG pin should not exceed the maximum value of VREG in [DC Specifications](#).

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

V _{IN} DC Voltage on RXD and $\overline{\text{RESET}}$	-0.3V to V _{REG} + 0.3
V _{IN} DC Voltage on TXD, CS/LWAKE, $\overline{\text{FAULT}}$ /TXE	-0.3 to +40V
V _{BB} Battery Voltage, continuous, non-operating (Note 1)	-0.3 to +40V
V _{BB} Battery Voltage, non-operating (LIN bus recessive, no regulator load, t < 60s) (Note 2)	-0.3 to +43V
V _{BB} Battery Voltage, transient ISO 7637 Test 1	-100V
V _{BB} Battery Voltage, transient ISO 7637 Test 2a	+75V
V _{BB} Battery Voltage, transient ISO 7637 Test 3a	-150V
V _{BB} Battery Voltage, transient ISO 7637 Test 3b	+100V
V _{LBUS} Bus Voltage, continuous	-18 to +30V
V _{LBUS} Bus Voltage, transient (Note 3)	-27 to +43V
I _{LBUS} Bus Short Circuit Current Limit	200 mA
ESD protection on LIN, V _{BB} (IEC 61000-4-2) (Note 4)	±15 kV
ESD protection on LIN, V _{BB} (Human Body Model) (Note 5)	±8 kV
ESD protection on all other pins (Human Body Model) (Note 5)	±4 kV
ESD protection on all pins (Charge Device Model) (Note 6)	±1500V
ESD protection on all pins (Machine Model) (Note 7)	±200V
Maximum Junction Temperature	150°C
Storage Temperature	-65 to +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: LIN 2.x compliant specification.

2: SAE J2602-2 compliant specification.

3: ISO 7637/1 load dump compliant (t < 500 ms).

4: According to IEC 61000-4-2, 330Ω, 150 pF and Transceiver EMC Test Specifications [2] to [4].

5: According to AEC-Q100-002/JESD22-A114.

6: According to AEC-Q100-011B.

7: According to AEC-Q100-003/JESD22-A115.

2.2 Nomenclature Used in This Document

Some terms and names used in this data sheet deviate from those referred to in the LIN specifications. Equivalent values are shown below.

LIN 2.1 Name	Term used in the following tables	Definition
V _{BAT}	<i>not used</i>	ECU operating voltage
V _{SUP}	V _{BB}	Supply voltage at device pin
V _{BUS_LIM}	ISC	Current limit of driver
V _{BUSREC}	V _{IH} (LBUS)	Recessive state
V _{BUSDOM}	V _{IL} (LBUS)	Dominant state

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2.3 DC Specifications

DC Specifications		Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $18.0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, $C_{REG} = 10 \mu F$.				
Parameter	Sym	Min	Typ	Max	Units	Conditions
Power						
VBB Quiescent Operating Current	IBBQ	—	—	200	μA	$I_{OUT} = 0 \text{ mA}$ LBUS recessive $V_{REG} = 5.0V$
		—	—	200	μA	$I_{OUT} = 0 \text{ mA}$ LBUS recessive $V_{REG} = 3.3V$
VBB Ready Current	IBBRD	—	—	100	μA	$I_{OUT} = 0 \text{ mA}$ LBUS recessive $V_{REG} = 5.0V$
		—	—	100	μA	$I_{OUT} = 0 \text{ mA}$ LBUS recessive $V_{REG} = 3.3V$
VBB Transmitter-Off Current	IBBTO	—	—	100	μA	With voltage regulator on, transmitter off, receiver on, $FAULT/TXE = V_{IL}$, $CS = V_{IH}$, $V_{REG} = 5.0V$
		—	—	100	μA	With voltage regulator on, transmitter off, receiver on, $FAULT/TXE = V_{IL}$, $CS = V_{IH}$, $V_{REG} = 3.3V$
VBB Power-Down Current	IBBPD	—	4.5	8	μA	With voltage regulator off, receiver on and transmitter off, $FAULT/TXE = V_{IH}$, $TxD = V_{IH}$, $CS = V_{IL}$
VBB Current with VSS Floating	IBBNOGND	-1	—	1	mA	$V_{BB} = 12V$, GND to V_{BB} , $V_{LIN} = 0 - 18V$
Microcontroller Interface						
High-Level Input Voltage (TxD , $FAULT/TxE$)	V_{IH}	2.0	—	$V_{REG} + 0.3$	V	
Low-Level Input Voltage (TxD , $FAULT/TxE$)	V_{IL}	-0.3	—	0.8	V	
High-Level Input Current (TxD , $FAULT/TxE$)	I_{IH}	-2.5	—	0.4	μA	Input voltage = 4.0V ~800 k Ω internal adaptive pull-up
Low-Level Input Current (TxD , $FAULT/TxE$)	I_{IL}	-10	—	—	μA	Input voltage = 0.5V ~800 k Ω internal adaptive pull-up
High-Level Input Voltage ($CS/LWAKE$)	V_{IH}	2.0	—	V_{BB}	V	Through a current-limiting resistor
Low-Level Input Voltage ($CS/LWAKE$)	V_{IL}	-0.3	—	0.8	V	

- Note 1:** Internal current limited. 2.0 ms maximum recovery time ($R_{LBS} = 0W$, $T_X = 0$, $V_{LBS} = V_{BB}$).
- 2:** Characterized, not 100% tested.
- 3:** In Power-Down mode, normal LIN recessive/dominant threshold is disabled. $V_{WK}(LBS)$ is used to detect bus activities.

2.3 DC Specifications (Continued)

DC Specifications	Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $18.0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, $C_{REG} = 10 \mu F$.					
Parameter	Sym	Min	Typ	Max	Units	Conditions
High-Level Input Current (CS/LWAKE)	I _{IH}	—	—	8.0	μA	Input voltage = $0.8V_{REG}$ ~1.3 M Ω internal pull-down to V _{SS}
Low-Level Input Current (CS/LWAKE)	I _{IL}	—	—	5.0	μA	Input voltage = $0.2V_{REG}$ ~1.3 M Ω internal pull-down to V _{SS}
Low-Level Output Voltage (R _{XD})	V _{OLRXD}	—	—	$0.2V_{REG}$	V	I _{OL} = 2 mA
High-Level Output Voltage (R _{XD})	V _{OH_{RXD}}	$0.8V_{REG}$	—	—	V	I _{OH} = 2 mA
Low-Level Output Voltage (FAULT/T _{XE})	V _{OL_{OD}}	—	—	1.0	V	I _{OL} = 4 mA
Low-Level Output Voltage (RESET)	V _{OL_{RST}}	—	—	1.0	V	I _{OL} = 4 mA
Bus Interface						
High-Level Input Voltage	V _{IH} (L _{BUS})	$0.6 V_{BB}$	—	—	V	Recessive state
Low-Level Input Voltage	V _{IL} (L _{BUS})	-8	—	$0.4 V_{BB}$	V	Dominant state
Input Hysteresis	V _{HYS}	—	—	$0.175 V_{BB}$	V	V _{IH} (L _{BUS}) – V _{IL} (L _{BUS})
Low-Level Output Current	I _{OL} (L _{BUS})	40	—	200	mA	Output voltage = $0.1 V_{BB}$, V _{BB} = 12V
Pull-Up Current on Input	I _{PU} (L _{BUS})	-180	—	-72	μA	~30 k Ω internal pull-up @ V _{IH} (L _{BUS}) = $0.7 V_{BB}$, V _{BB} = 12V
Short Circuit Current Limit	I _{SC}	50	—	200	mA	Note 1
High-Level Output Voltage	V _{OH} (L _{BUS})	$0.8 V_{BB}$	—	V _{BB}	V	
Driver Dominant Voltage	V _{LOSUP}	—	—	1.1	V	V _{BB} = 7.3V R _{LOAD} = 1000 Ω
	V _{HISUP}	—	—	1.2	V	V _{BB} = 18V R _{LOAD} = 1000 Ω
Input Leakage Current (at the receiver during dominant bus level)	I _{BUS_PAS_DOM}	-1	—	—	mA	Driver off V _{BUS} = 0V V _{BB} = 12V
Input Leakage Current (at the receiver during recessive bus level)	I _{BUS_PAS_REC}	-20	—	20	μA	Driver off $8V < V_{BB} < 18V$ $8V < V_{BUS} < 18V$ V _{BUS} $\geq$ V _{BB}
Leakage Current (disconnected from ground)	I _{BUS_NO_GND}	-10	—	+10	μA	GND _{DEVICE} = V _{BB} $0V < V_{BUS} < 18V$ V _{BB} = 12V
Leakage Current (disconnected from V _{BB})	I _{BUS_NO_PWR}	-10	—	+10	μA	V _{BB} = GND $0 < V_{BUS} < 18V$
Receiver Center Voltage	V _{BUS_CNT}	$0.475 V_{BB}$	$0.5 V_{BB}$	$0.525 V_{BB}$	V	V _{BUS_CNT} = (V _{IL} (L _{BUS}) + V _{IH} (L _{BUS}))/2
Slave Termination	R _{SLAVE}	20	30	47	k Ω	Note 2

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{L_{BUS}} = 0W, TX = 0, V_{L_{BUS}} = V_{BB}).

2: Characterized, not 100% tested.

3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled. V_{WK}(L_{BUS}) is used to detect bus activities.

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2.3 DC Specifications (Continued)

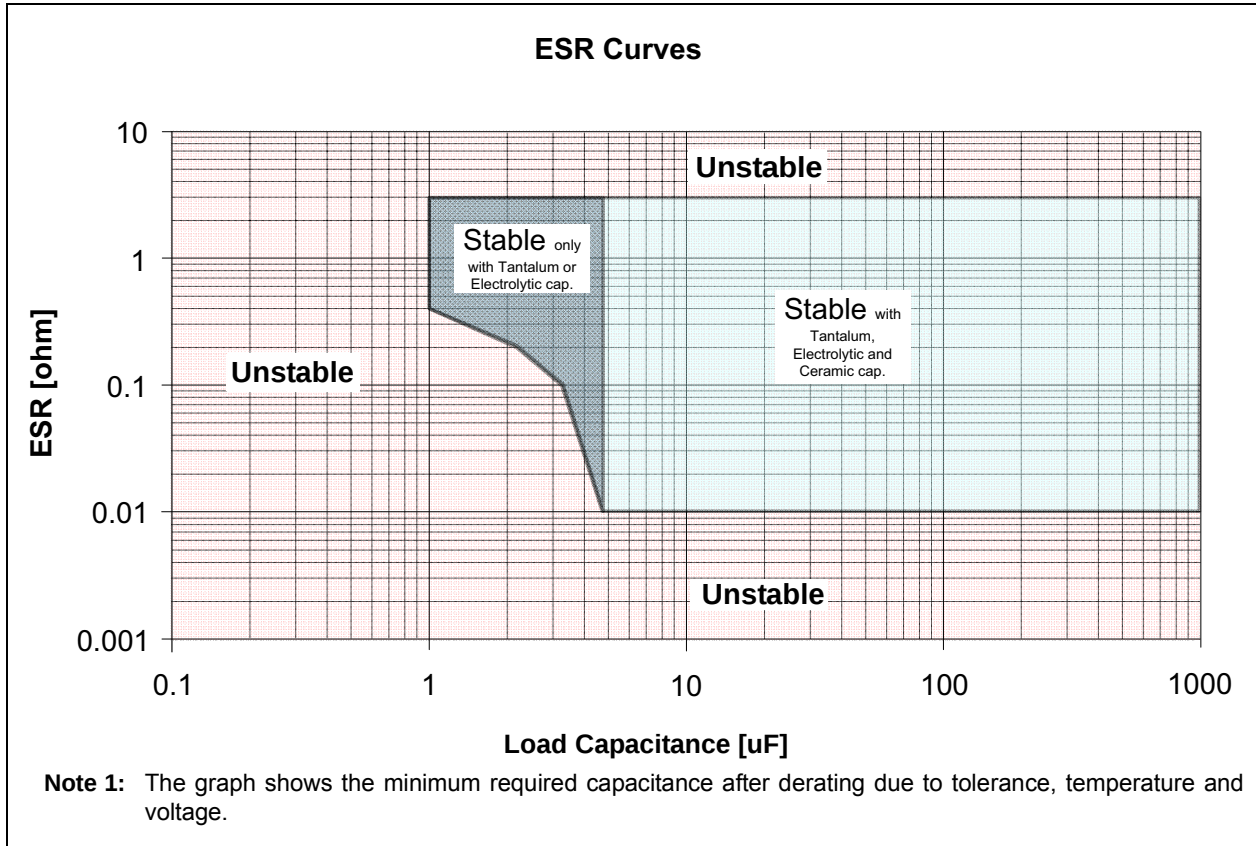
DC Specifications		Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $18.0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, $C_{REG} = 10 \mu F$.				
Parameter	Sym	Min	Typ	Max	Units	Conditions
Capacitance of Slave Node	CSLAVE	—	—	50	pF	Note 2
Wake-Up Voltage Threshold on LIN Bus	VWK(LBUS)	—	—	3.4	V	Wake-up from Power-Down mode (Note 3)
Voltage Regulator – 5.0V						
Output Voltage Range	VREG	4.85	5.00	5.15	V	$0 \text{ mA} < I_{OUT} < 70 \text{ mA}$
Line Regulation	ΔV_{OUT1}	—	10	50	mV	$I_{OUT} = 1 \text{ mA}$ $6.0V < V_{BB} < 18V$
Load Regulation	ΔV_{OUT2}	—	10	50	mV	$5 \text{ mA} < I_{OUT} < 70 \text{ mA}$ $6.0V < V_{BB} < 12V$
Power Supply Ripple Reject	PSRR	—	—	50	dB	$1 V_{PP} @ 10 - 20 \text{ kHz}$ $I_{LOAD} = 20 \text{ mA}$
Output Noise Voltage	eN	—	—	100	μV_{RMS}	10 Hz – 40 MHz $C_{FILTER} = 10 \mu f$ $C_{BP} = 0.1 \mu f$ $I_{LOAD} = 20 \text{ mA}$
Shutdown Voltage Threshold	VSD	3.5	—	4.0	V	See Figure 1-5 (Note 2)
Input Voltage to Turn-Off Output	V _{OFF}	3.9	—	4.5	V	
Input Voltage to Turn-On Output	V _{ON}	5.25	—	6.0	V	
Voltage Regulator – 3.3V						
Output Voltage	VREG	3.20	3.30	3.40	V	$0 \text{ mA} < I_{OUT} < 70 \text{ mA}$
Line Regulation	ΔV_{OUT1}	—	10	50	mV	$I_{OUT} = 1 \text{ mA}$ $6.0V < V_{BB} < 18V$
Load Regulation	ΔV_{OUT2}	—	10	50	mV	$5 \text{ mA} < I_{OUT} < 70 \text{ mA}$ $6.0V < V_{BB} < 12V$
Power Supply Ripple Reject	PSRR	—	—	50	dB	$1 V_{PP} @ 10 - 20 \text{ kHz}$ $I_{LOAD} = 20 \text{ mA}$
Output Noise Voltage	eN	—	—	100	$\mu V_{RMS}/\sqrt{Hz}$	10 Hz – 40 MHz $C_{FILTER} = 10 \mu f$ $C_{BP} = 0.1 \mu f$ $I_{LOAD} = 20 \text{ mA}$
Shutdown Voltage Threshold	VSD	2.5	—	2.7	V	See Figure 1-5 (Note 2)
Input Voltage to Turn-Off Output	V _{OFF}	3.9	—	4.5	V	
Input Voltage to Turn-On Output	V _{ON}	5.25	—	6	V	

Note 1: Internal current limited. 2.0 ms maximum recovery time ($R_{LBUS} = 0W$, $T_X = 0$, $V_{LBUS} = V_{BB}$).

2: Characterized, not 100% tested.

3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled. VWK(LBUS) is used to detect bus activities.

FIGURE 2-1: ESR CURVES FOR LOAD CAPACITOR SELECTION



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2.4 AC Specifications

AC Characteristics		Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $18.0V$; $T_A = -40^{\circ}C$ to $+125^{\circ}C$.				
Parameter	Sym	Min	Typ	Max	Units	Conditions
Bus Interface – Constant Slope Time Parameters						
Slope Rising and Falling Edges	t_{SLOPE}	3.5	—	22.5	μs	$7.3V \leq V_{BB} \leq 18V$
Propagation Delay of Transmitter	$t_{TRANSPD}$	—	—	5.0	μs	$t_{TRANSPD} = \max.$ ($t_{TRANSPDR}$ or $t_{TRANSPDF}$)
Propagation Delay of Receiver	t_{RECPD}	—	—	6.0	μs	$t_{RECPD} = \max.$ (t_{RECPDR} or t_{RECPDF})
Symmetry of Propagation Delay of Receiver Rising Edge w.r.t. Falling Edge	t_{RECSYM}	-2.0	—	2.0	μs	$t_{RECSYM} = \max.$ ($t_{RECPDF} - t_{RECPDR}$) $R_{RXD} = 2.4 k\Omega$ to V_{CC} $C_{RXD} = 20 pF$
Symmetry of Propagation Delay of Transmitter Rising Edge w.r.t. Falling Edge	$t_{TRANSSYM}$	-2.0	—	2.0	μs	$t_{TRANSSYM} = \max.$ ($t_{TRANSPDF} - t_{TRANSPDR}$)
Bus Dominant Time-Out Time	$t_{TO(LIN)}$	—	25	—	ms	
Time to Sample $FAULT/TXE$ for Bus Conflict Reporting	t_{FAULT}	—	—	32.5	μs	$t_{FAULT} = \max.$ ($t_{TRANSPD} + t_{SLOPE} + t_{RECPD}$)
Duty Cycle 1 @ 20.0 kbps		0.396	—	—	%tBIT	CBUS; RBUS conditions: 1 nF; 1 k Ω 6.8 nF; 660 Ω 10 nF; 500 Ω $TH_{REC(MAX)} = 0.744 \times V_{BB}$, $TH_{DOM(MAX)} = 0.581 \times V_{BB}$, $V_{BB} = 7.0V - 18V$; $t_{BIT} = 50 \mu s$. $D1 = t_{BUS_REC(MIN)}/2 \times t_{BIT}$
Duty Cycle 2 @ 20.0 kbps		—	—	0.581	%tBIT	CBUS; RBUS conditions: 1 nF; 1 k Ω 6.8 nF; 660 Ω 10 nF; 500 Ω $TH_{REC(MAX)} = 0.284 \times V_{BB}$, $TH_{DOM(MAX)} = 0.422 \times V_{BB}$, $V_{BB} = 7.6V - 18V$; $t_{BIT} = 50 \mu s$. $D2 = t_{BUS_REC(MAX)}/2 \times t_{BIT}$
Duty Cycle 3 @ 10.4 kbps		0.417	—	—	%tBIT	CBUS; RBUS conditions: 1 nF; 1 k Ω 6.8 nF; 660 Ω 10 nF; 500 Ω $TH_{REC(MAX)} = 0.778 \times V_{BB}$, $TH_{DOM(MAX)} = 0.616 \times V_{BB}$, $V_{BB} = 7.0V - 18V$; $t_{BIT} = 96 \mu s$. $D3 = t_{BUS_REC(MIN)}/2 \times t_{BIT}$

- Note 1:** Time depends on external capacitance and load. Test condition: $C_{REG} = 4.7 \mu F$, no resistor load.
Note 2: Characterized, not 100% tested.

2.4 AC Specifications (Continued)

AC Characteristics		Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 6.0V$ to $18.0V$; $T_A = -40^{\circ}C$ to $+125^{\circ}C$.				
Parameter	Sym	Min	Typ	Max	Units	Conditions
Duty Cycle 4 @ 10.4 kbps		—	—	0.590	%tBIT	CBUS; RBUS conditions: 1 nF; 1 k Ω 6.8 nF; 660 Ω 10 nF; 500 Ω THREC(MAX) = $0.251 \times V_{BB}$, THDOM(MAX) = $0.389 \times V_{BB}$, $V_{BB} = 7.6V - 18V$; tBIT = 96 μs . D4 = tBUS_REC(MAX)/2 x tBIT
Voltage Regulator						
Bus Activity Debounce time	tBDB	30	80	250	μs	
Bus Activity to Voltage Regulator Enabled	tBACTIVE	35	—	200	μs	
Voltage Regulator Enabled to Ready	tVEVR	300	—	1200	μs	Note 1
Chip Select to Ready Mode	tCSR	—	—	230	μs	
Chip Select to Power-Down	tCSPD	—	—	330	μs	Note 2
Short Circuit to Shutdown	tSHUTDOWN	20	—	100	μs	
RESET Timing						
VREG OK Detect to RESET Inactive	tRPU	—	—	60	μs	
VREG Not OK Detect to RESET Active	tRPD	—	—	60	μs	

Note 1: Time depends on external capacitance and load. Test condition: $C_{REG} = 4.7 \mu F$, no resistor load.

2: Characterized, not 100% tested.

2.5 Thermal Specifications

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Specified Temperature Range	T_A	-40	—	+125	$^{\circ}C$	
Maximum Junction Temperature	T_J	—	—	+150	$^{\circ}C$	
Storage Temperature Range	T_A	-65	—	+150	$^{\circ}C$	
Recovery Temperature	$\theta_{RECOVERY}$	—	+140	—	$^{\circ}C$	
Shutdown Temperature	$\theta_{SHUTDOWN}$	—	+150	—	$^{\circ}C$	
Short Circuit Recovery Time	tTHERM	—	1.5	5.0	ms	
Thermal Package Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	$^{\circ}C/W$	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	$^{\circ}C/W$	
Thermal Resistance, 8L-DFN	θ_{JA}	—	48	—	$^{\circ}C/W$	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	$^{\circ}C/W$	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	90.8	—	$^{\circ}C/W$	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	$^{\circ}C/W$	

Note 1: The maximum power dissipation is a function of T_{JMAX} , θ_{JA} , and ambient temperature, T_A . The maximum allowable power dissipation at an ambient temperature is $P_D = (T_{JMAX} - T_A) \theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above $150^{\circ}C$ and the MCP2021A/2A will go into thermal shutdown.

2.6 Typical Performance Curves

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{BB} = 6.0V$ to $18.0V$; $T_A = -40^{\circ}C$ to $+125^{\circ}C$.

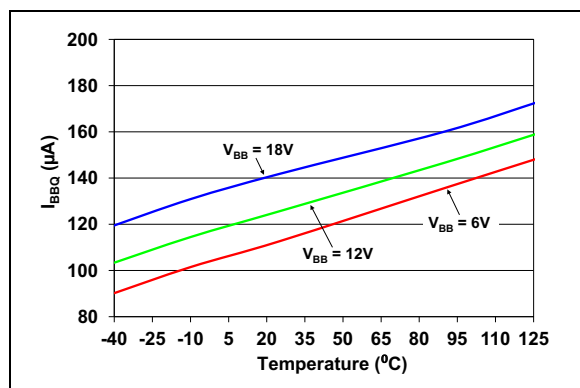


FIGURE 2-2: Typical I_{BBQ} vs. Temperature – 5.0V.

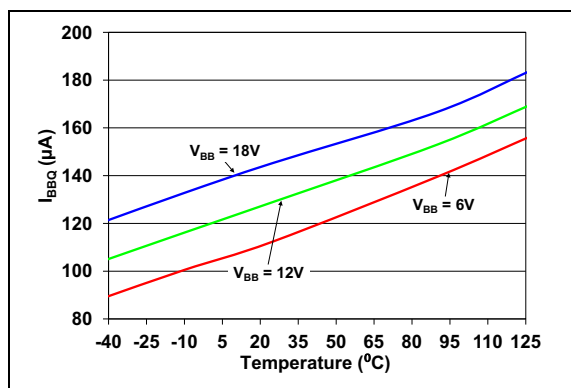


FIGURE 2-5: Typical I_{BBQ} vs. Temperature – 3.3V.

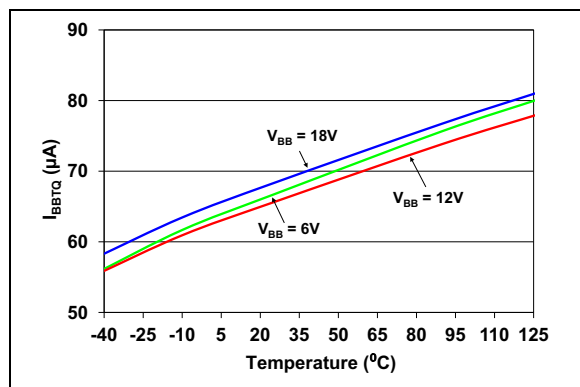


FIGURE 2-3: Typical I_{BBTQ} vs. Temperature – 5.0V.

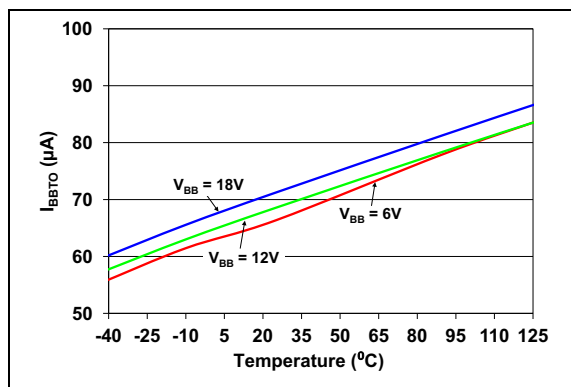


FIGURE 2-6: Typical I_{BBTQ} vs. Temperature – 3.3V.

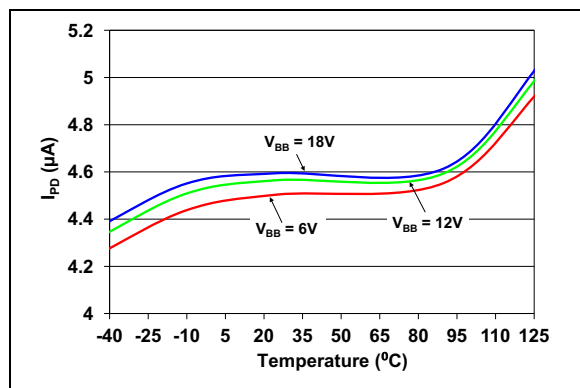


FIGURE 2-4: Typical I_{PD} vs. Temperature – 5.0V.

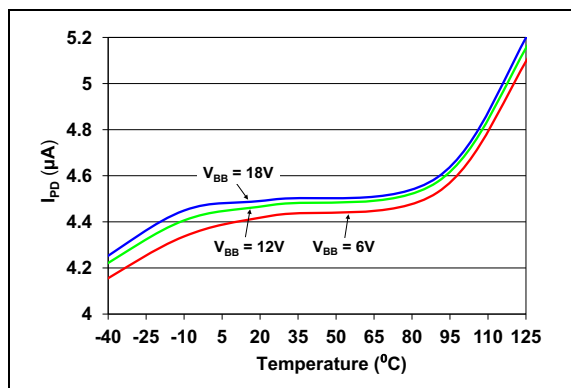


FIGURE 2-7: Typical I_{PD} vs. Temperature – 3.3V.

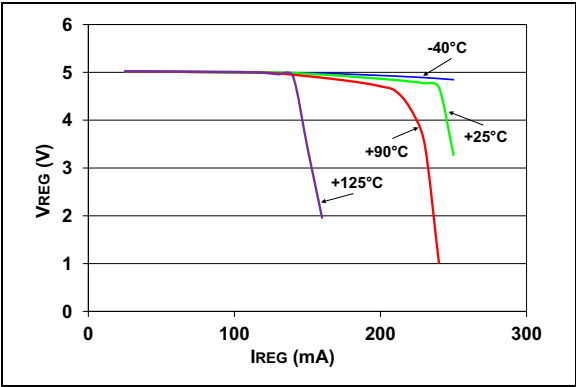


FIGURE 2-8: 5.0V V_{REG} vs. I_{REG} at $V_{BB} = 12V$.

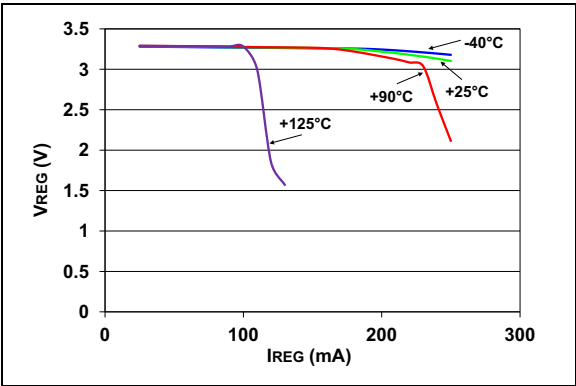


FIGURE 2-9: 3.3V V_{REG} vs. I_{REG} at $V_{BB} = 12V$.

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2.7 Timing Diagrams and Specifications

FIGURE 2-10: BUS TIMING DIAGRAM

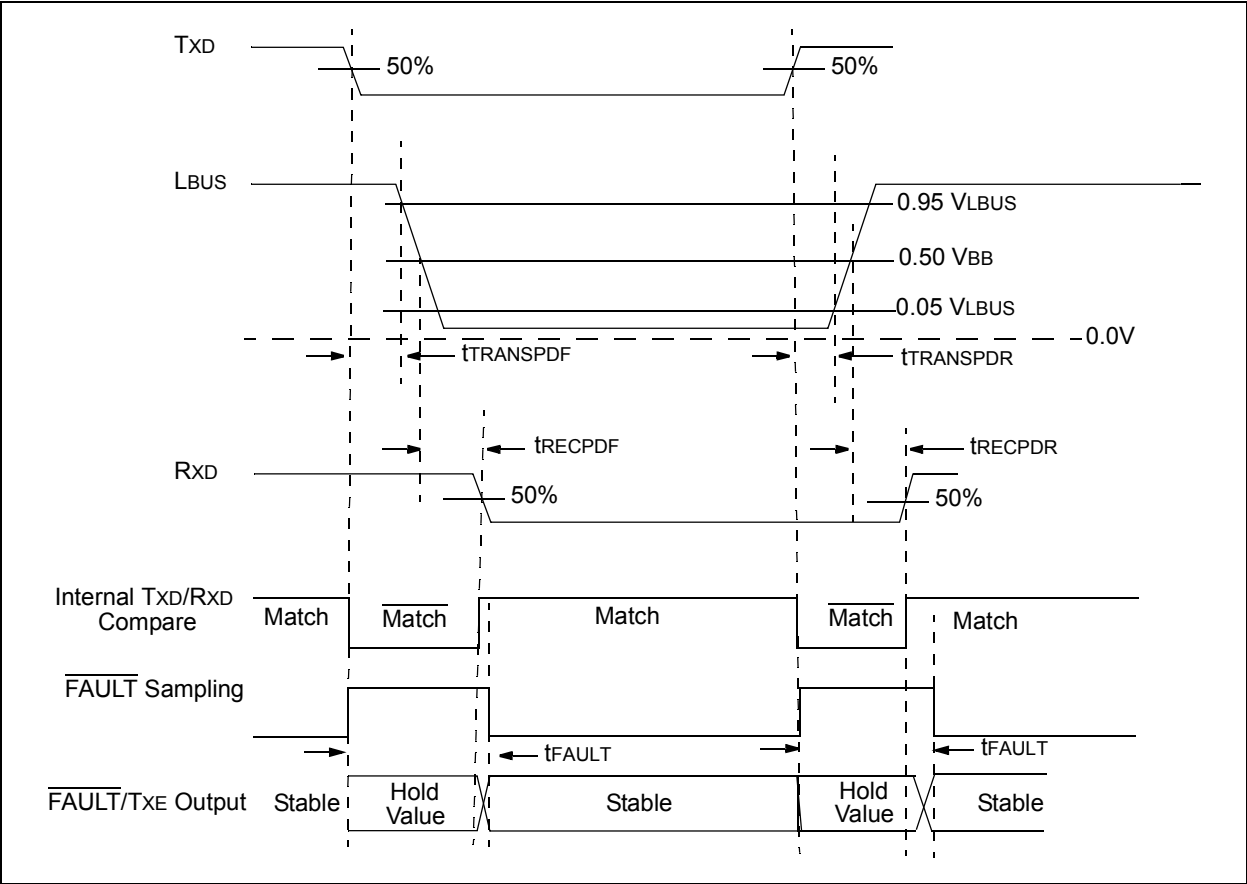


FIGURE 2-11: REGULATOR CS/LWAKE TIMING DIAGRAM

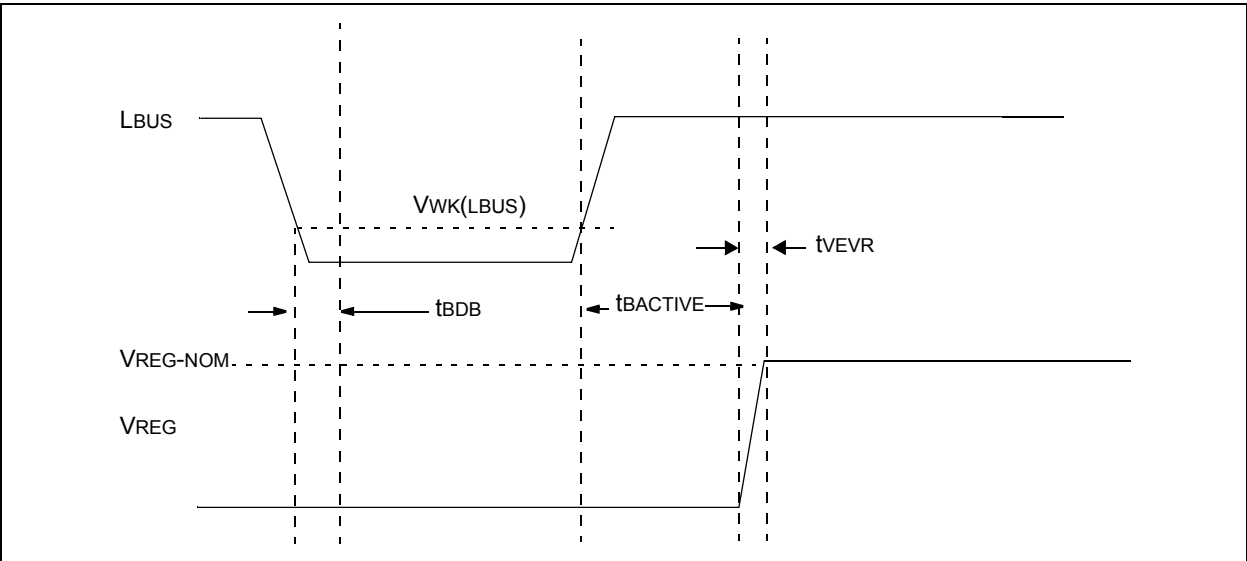
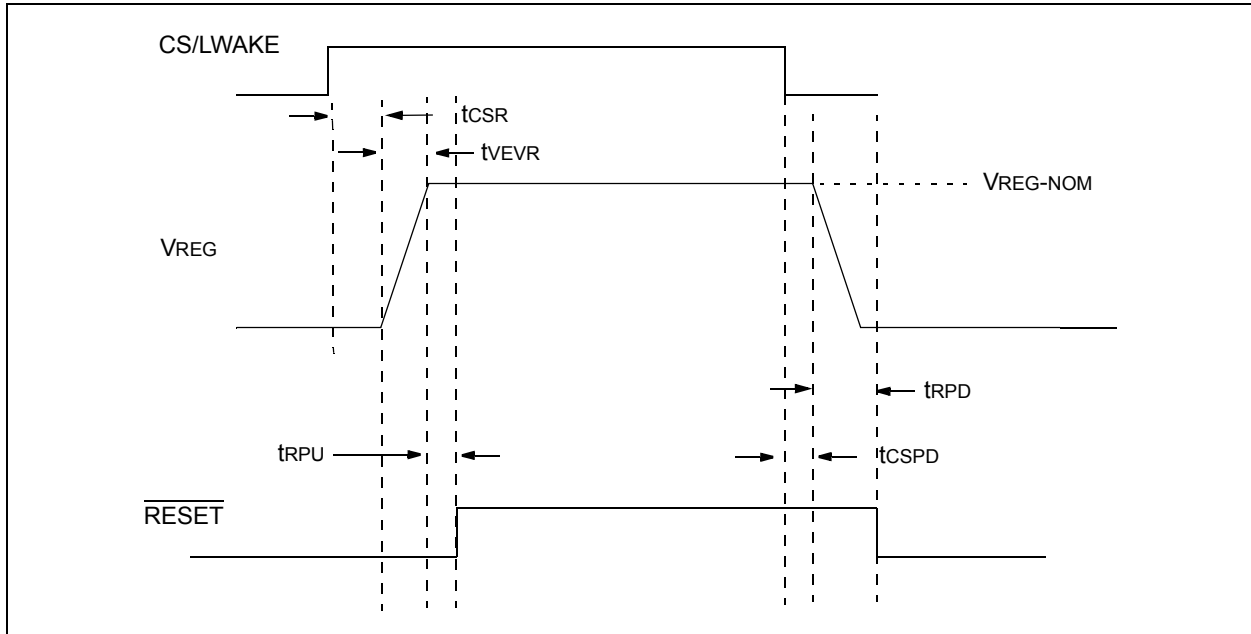


FIGURE 2-12: CS/LWAKE, REGULATOR AND RESET TIMING DIAGRAM

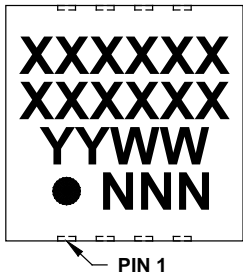


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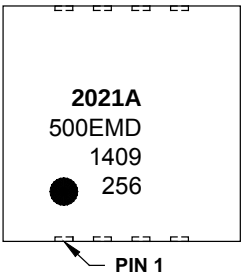
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

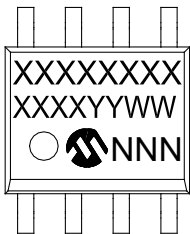
8-Lead DFN (4x4x0.9 mm) (MCP2021A)



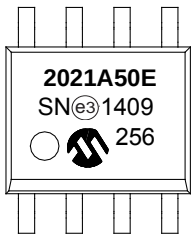
Example



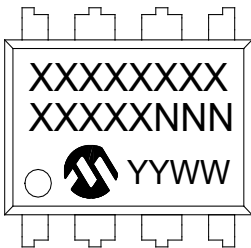
8-Lead SOIC (150 mil) (MCP2021A)



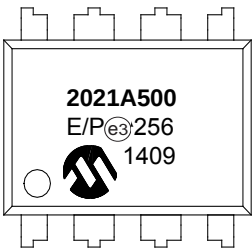
Example



8-Lead PDIP (300 mil) (MCP2021A)



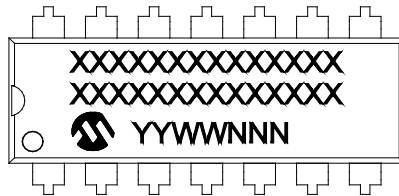
Example



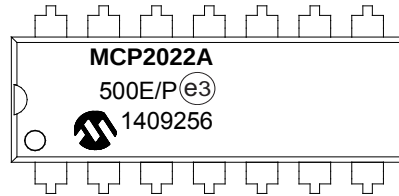
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	ⓔ3	Pb-free JEDEC [®] designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

Package Marking Information (Continued)

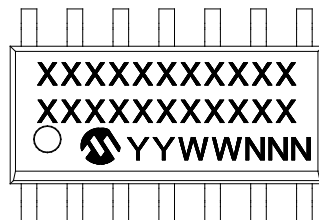
14-Lead PDIP (300 mil) (MCP2022A)



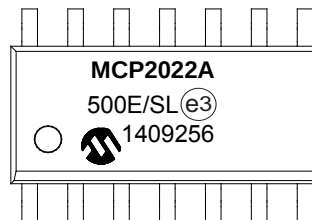
Example



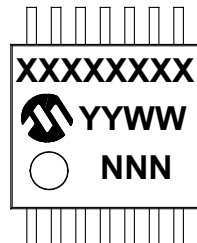
14-Lead SOIC (.150") (MC2022A)



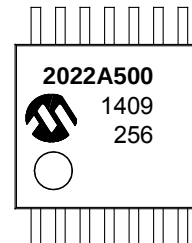
Example



14-Lead TSSOP (MCP2022A)



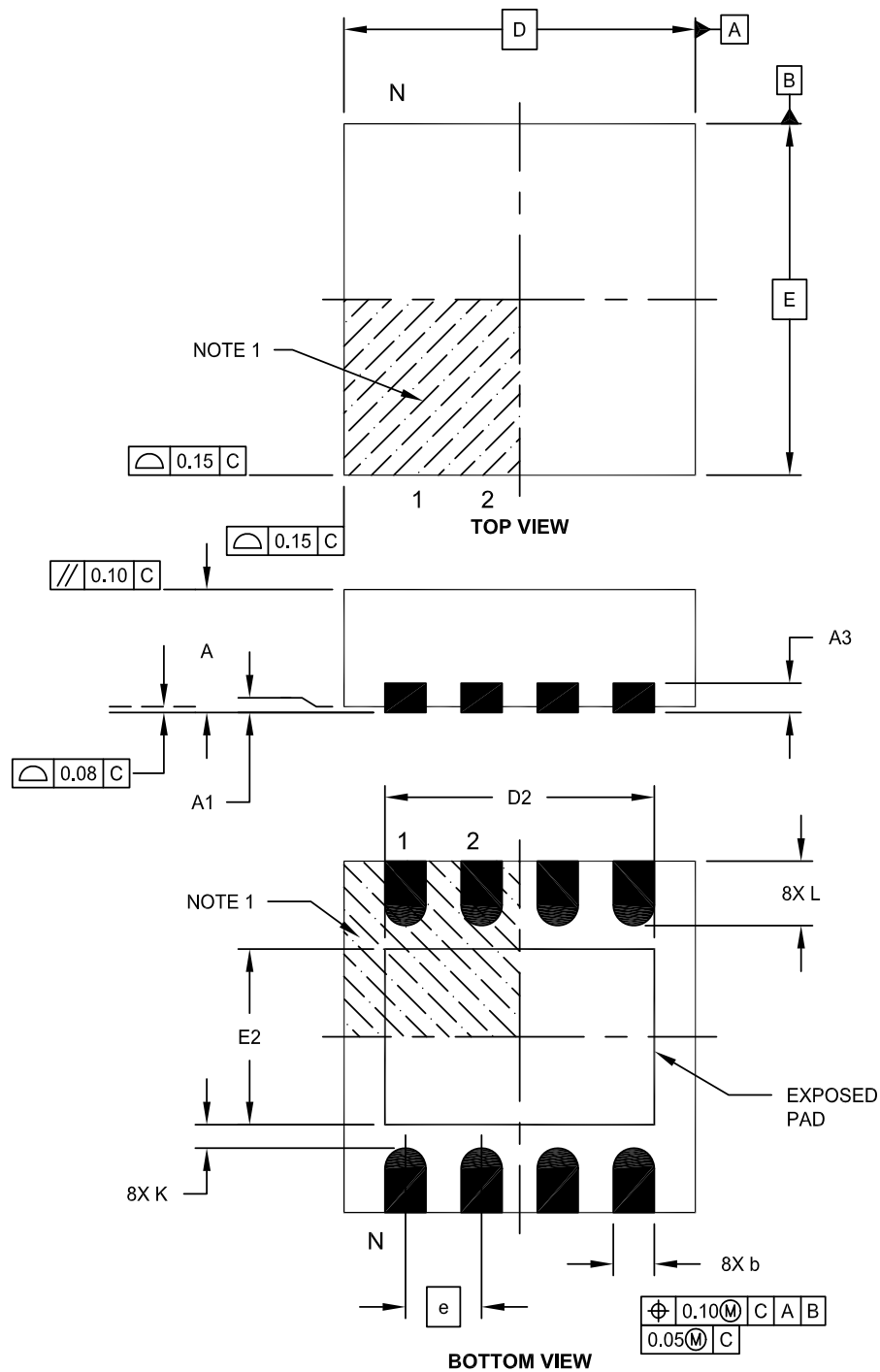
Example



MCP2021A/2A

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

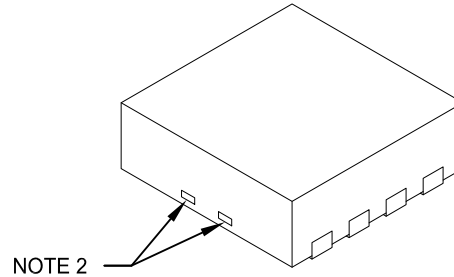
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-131E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.80 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	4.00 BSC		
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Width	E	4.00 BSC		
Exposed Pad Length	D2	3.40	3.50	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

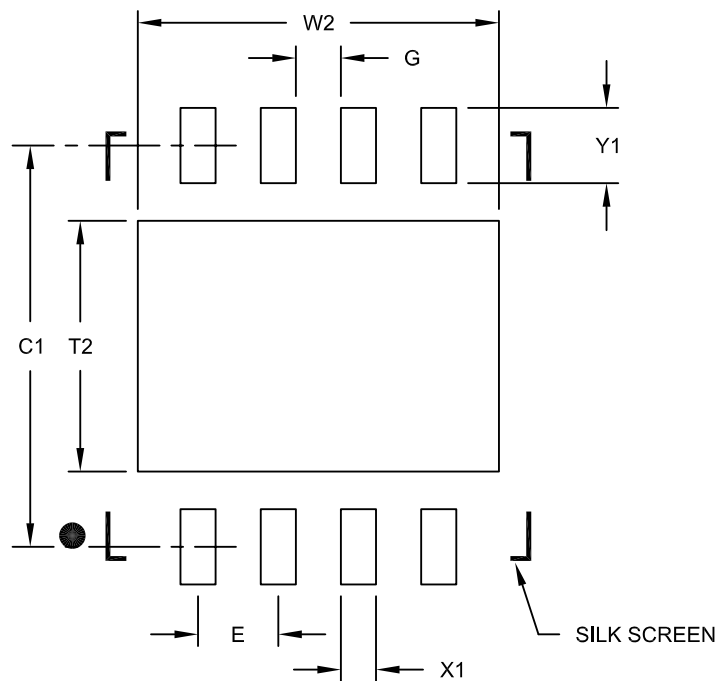
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131E Sheet 2 of 2

MCP2021A/2A

8-Lead Plastic Dual Flat, No Lead Package (MD) - 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Contact Pitch	E		0.80 BSC		
Optional Center Pad Width	W2				3.60
Optional Center Pad Length	T2				2.50
Contact Pad Spacing	C1			4.00	
Contact Pad Width (X8)	X1				0.35
Contact Pad Length (X8)	Y1				0.75
Distance Between Pads	G		0.45		

Notes:

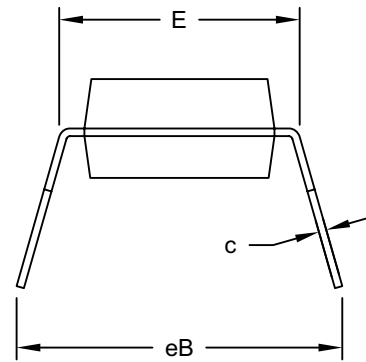
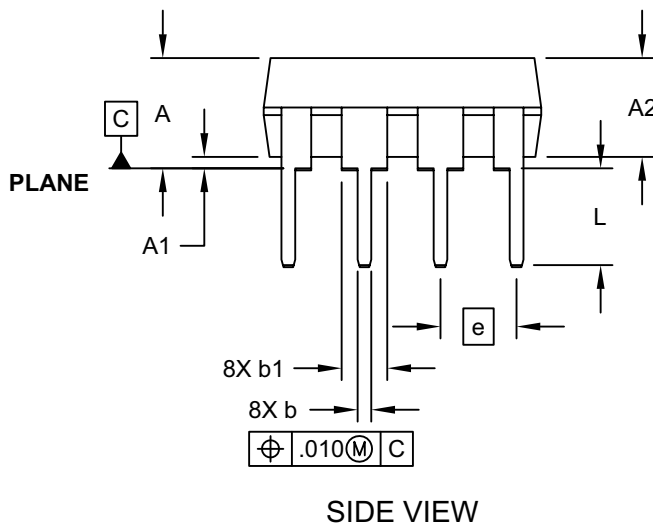
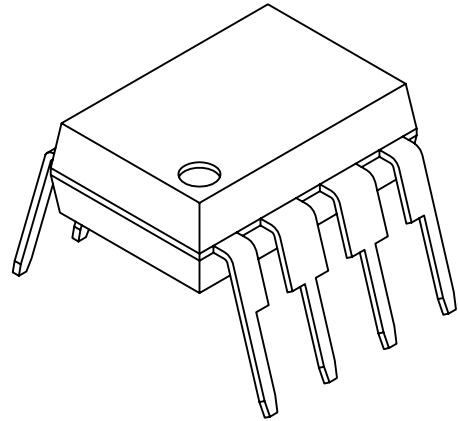
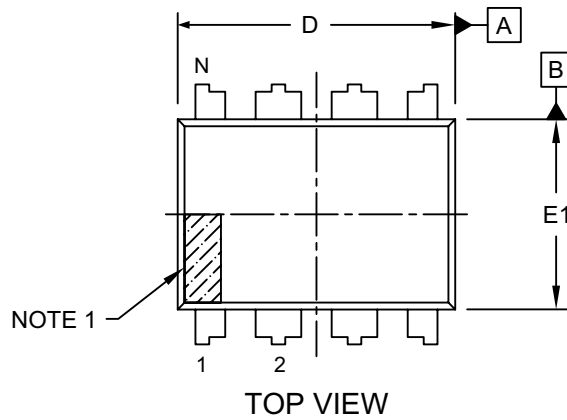
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131C

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



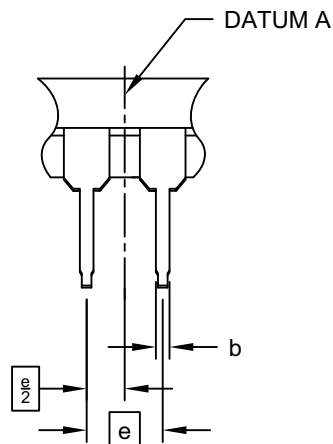
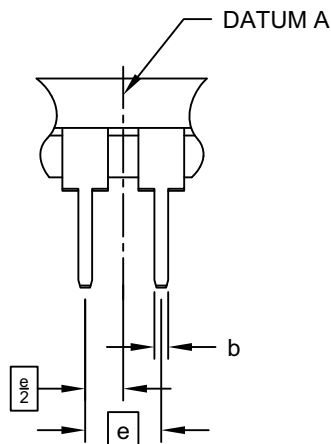
Microchip Technology Drawing No. C04-018D Sheet 1 of 2

MCP2021A/2A

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

ALTERNATE LEAD DESIGN (VENDOR DEPENDENT)



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing	§	eB	-	.430

Notes:

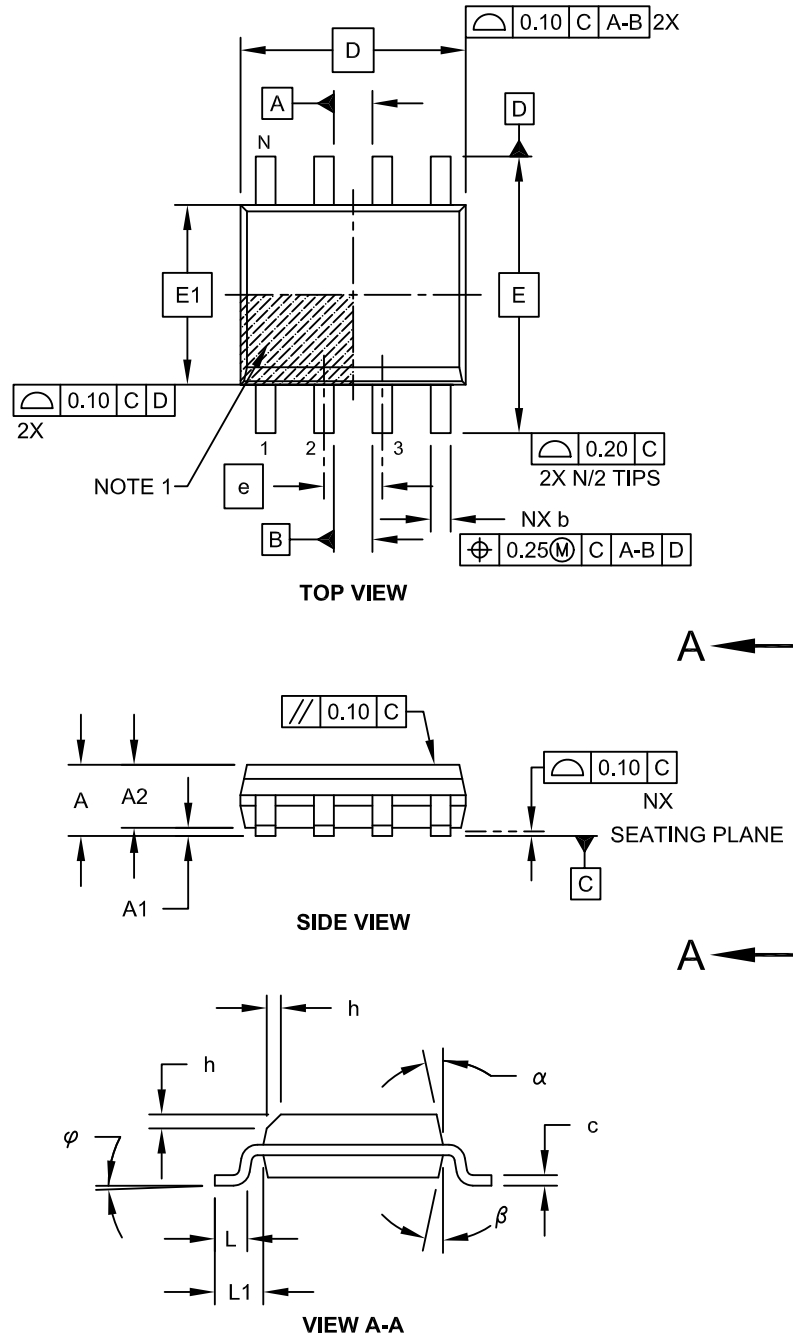
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-018D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

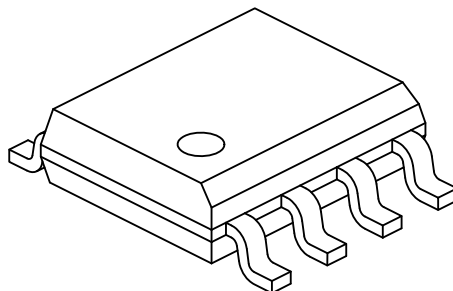


Microchip Technology Drawing No. C04-057C Sheet 1 of 2

MCP2021A/2A

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		1.27 BSC		
Overall Height	A		-	-	1.75
Molded Package Thickness	A2		1.25	-	-
Standoff §	A1		0.10	-	0.25
Overall Width	E		6.00 BSC		
Molded Package Width	E1		3.90 BSC		
Overall Length	D		4.90 BSC		
Chamfer (Optional)	h		0.25	-	0.50
Foot Length	L		0.40	-	1.27
Footprint	L1		1.04 REF		
Foot Angle	φ		0°	-	8°
Lead Thickness	c		0.17	-	0.25
Lead Width	b		0.31	-	0.51
Mold Draft Angle Top	α		5°	-	15°
Mold Draft Angle Bottom	β		5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

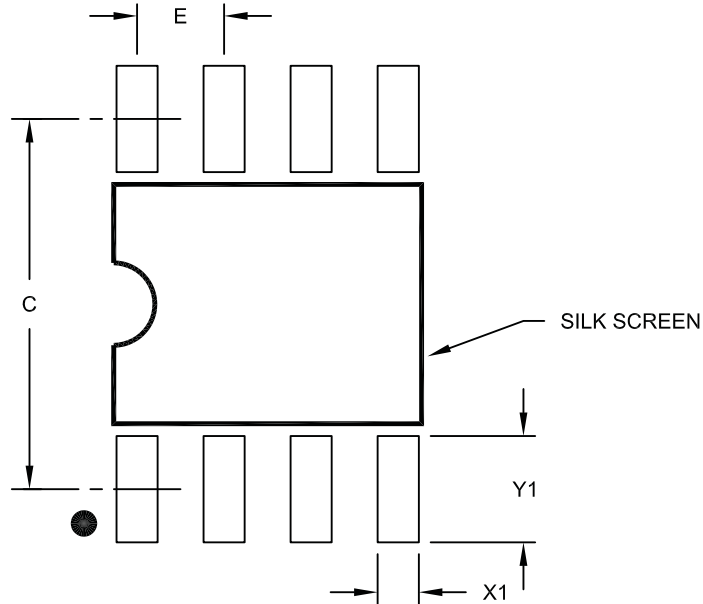
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

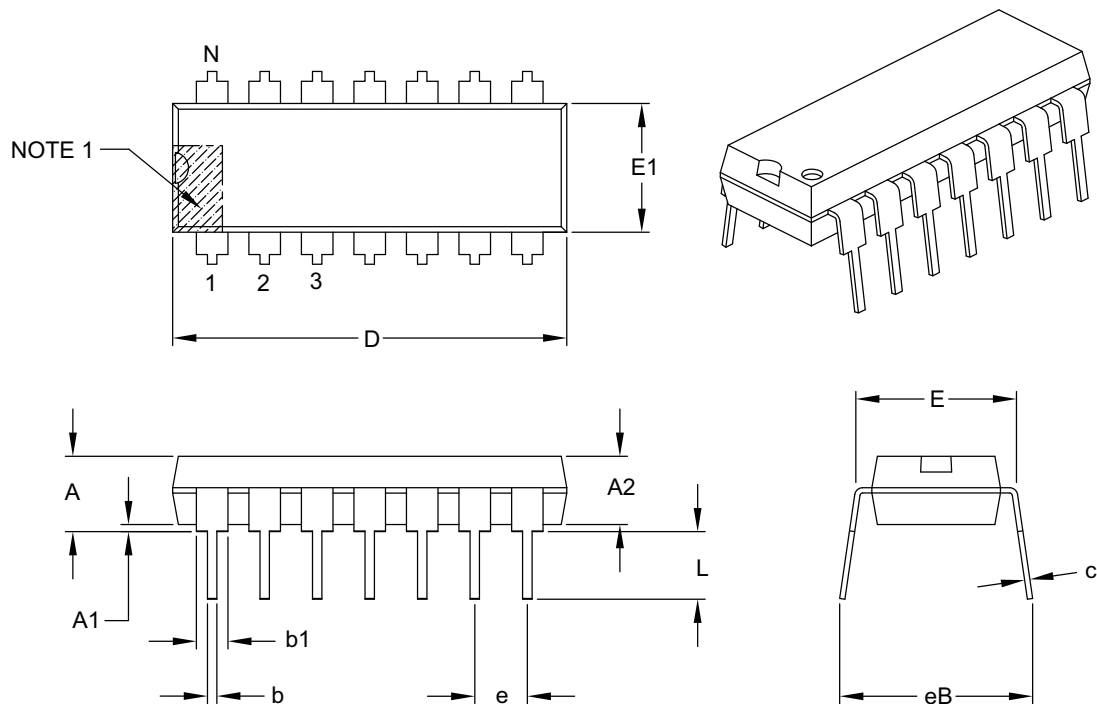
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

MCP2021A/2A

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

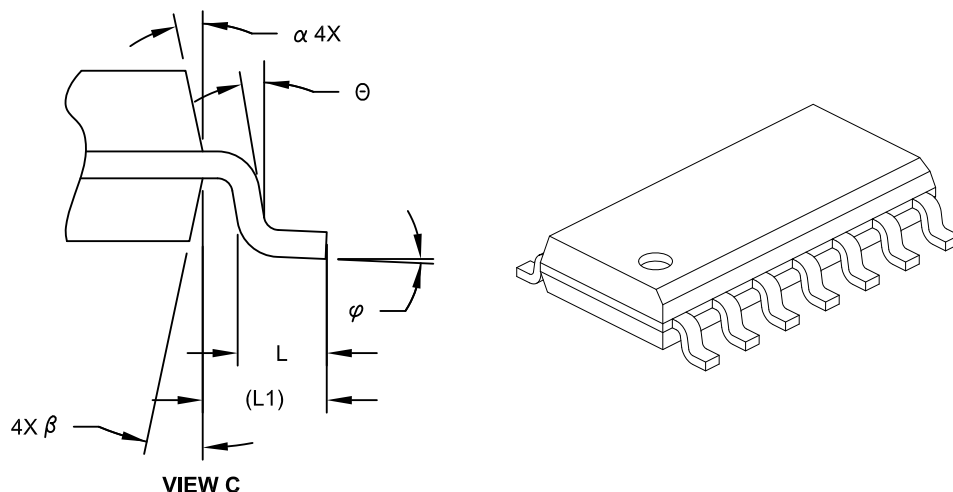
- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

MCP2021A/2A

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

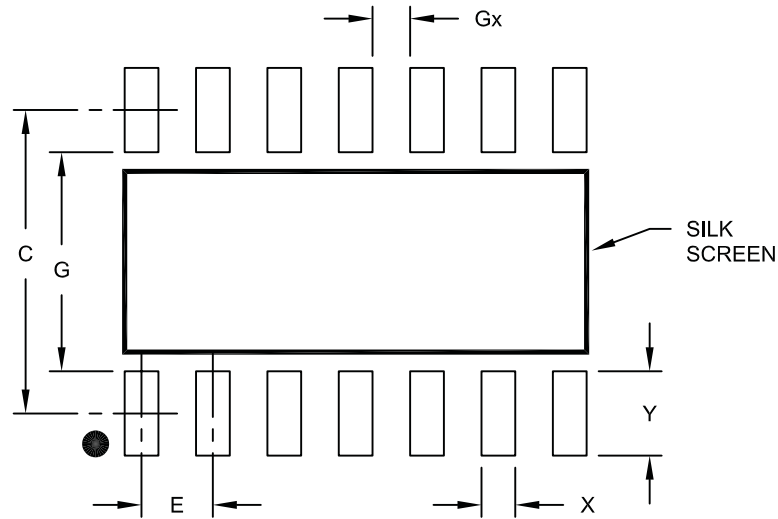
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

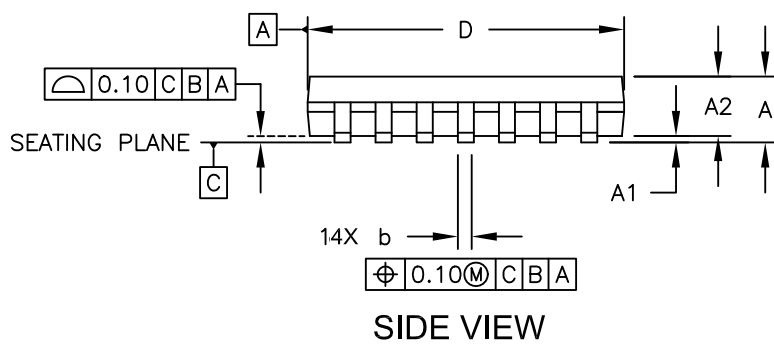
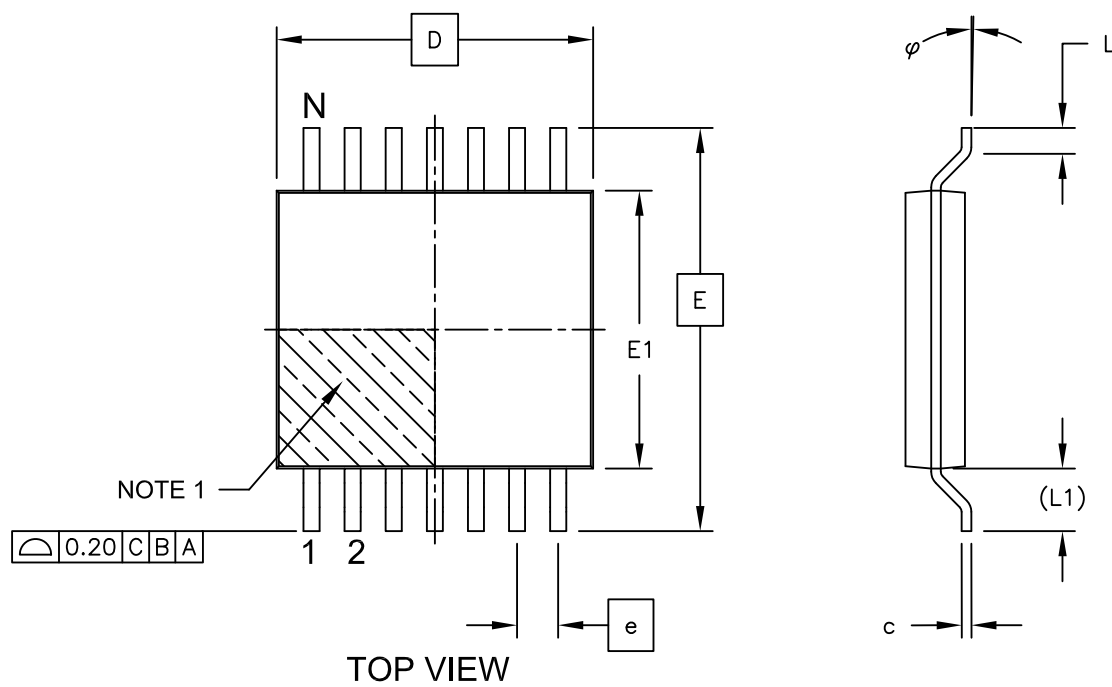
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

MCP2021A/2A

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

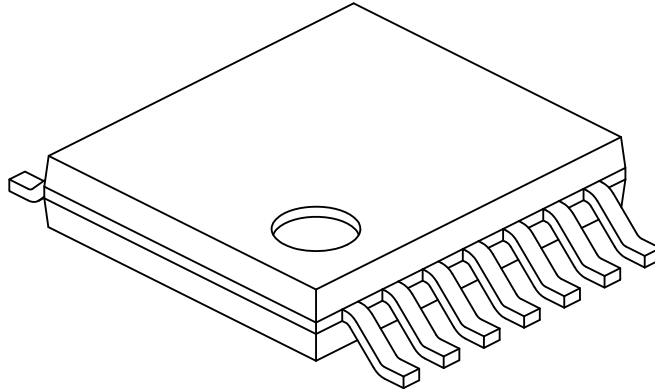
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-087C Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)	1.00 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M

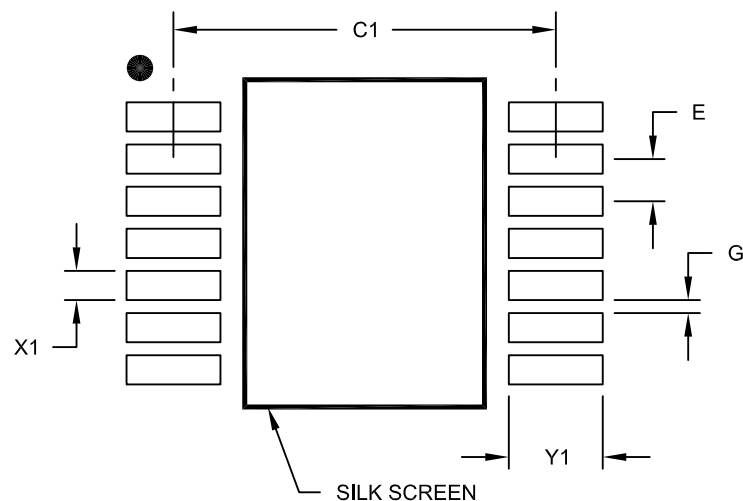
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

MCP2021A/2A

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

APPENDIX A: REVISION HISTORY

Revision C (July 2014)

The following is the list of modifications:

1. Updated **Section 1.6 “Typical Applications”** with values used during ESD tests.
2. Minor typographical corrections.
3. Updated 8-Lead PDIP Package.

Revision B (December 2013)

The following is the list of modifications:

1. Removed two notes in [AC Specifications](#).
2. Updated [Figure 1-3](#).
3. Added pull-up to $\overline{\text{FAULT}}/\text{TxE}$ pin in the pin description and typical applications.
4. Revised product identification examples for SOIC package.

Revision A (March 2012)

- Original Release of this Document.

MCP2021A/2A

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>-X</u>	<u>-X</u>	<u>/XX</u>
Device	Voltage	Temperature Range	Package
Device: MCP2021A: LIN Transceiver with Voltage Regulator MCP2021AT: LIN Transceiver with Voltage Regulator (Tape and Reel) MCP2022A: LIN Transceiver with Voltage Regulator MCP2022AT: LIN Transceiver with Voltage Regulator (Tape and Reel)			
Voltage: 330 = 3.3V 500 = 5.0V			
Temperature Range: E = -40°C to +125°C			
Package: MD = 8LD Plastic Dual Flat, No Lead – 4x4x0.8 mm Body P = 8LD/14LD Plastic Dual In-Line – 300 mil Body SN = 8LD Plastic Small Outline – Narrow, 3.90 mm Body SL = 14LD Plastic Small Outline – Narrow, 3.90 mm Body ST = 14LD Plastic Thin Shrink Small Outline – 4.4 mm Body			

Examples:
a) MCP2021A-330E/MD: 3.3V, 8-lead DFN package
b) MCP2021A-500E/MD: 5.0V, 8-lead DFN package
c) MCP2021AT-330E/MD: 3.3V, 8-lead DFN package, Tape and Reel
d) MCP2021AT-500E/MD: 5.0V, 8-lead DFN package, Tape and Reel
e) MCP2021A-330E/P: 3.3V, 8-lead PDIP package
f) MCP2021A-500E/P: 5.0V, 8-lead PDIP package
g) MCP2021A-330E/SN: 3.3V, 8-lead SOIC package
h) MCP2021AT-330E/SN: 3.3V, 8-lead SOIC package, Tape and Reel
i) MCP2021A-500E/SN: 5.0V, 8-lead SOIC package
j) MCP2021AT-500E/SN: 5.0V, 8-lead SOIC package, Tape and Reel

a) MCP2022A-330E/P: 3.3V, 14-lead PDIP package
b) MCP2022A-500E/P: 5.0V, 14-lead PDIP package
c) MCP2022A-330E/SL: 3.3V, 14-lead SOIC package
d) MCP2022AT-330E/SL: 3.3V, 14-lead SOIC package, Tape and Reel
e) MCP2022A-500E/SL: 5.0V, 14-lead SOIC package
f) MCP2022AT-500E/SL: 5.0V, 14-lead SOIC package, Tape and Reel
g) MCP2022A-330E/ST: 3.3V, 14-lead TSSOP package
h) MCP2022AT-330E/ST: 3.3V, 14-lead TSSOP package, Tape and Reel
i) MCP2022A-500E/ST: 5.0V, 14-lead TSSOP package
j) MCP2022AT-500E/ST: 5.0V, 14-lead TSSOP package, Tape and Reel

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