10-Bit, Nonvolatile, Linear-Taper Digital Potentiometers

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6.0V
V_{SS} to GND.....-3.5V to +0.3V
V_{DD} to V_{SS} .....-0.3V to +6.0V
H, L, W to V_{SS} .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
$\overline{CS}$, SCLK($\overline{INC}$), DIN(U/$\overline{D}$), SPI/$\overline{UD}$ to GND ..-0.3V to (V_{DD} + 0.3V)
Maximum Continuous Current into H, L, and W
  MAX5481/MAX5483.....±5mA
  MAX5482/MAX5484.....±1.0mA
Maximum Current into Any Other Pin .....±50mA

Continuous Power Dissipation (T_A = +70°C)
  16-Pin TQFN (derate 17.5mW/°C above +70°C) 1398.6mW
  14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, V_{SS} = V_{GND} = 0V, V_H = V_{DD}, V_L = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE (MAX5481/MAX5482 programmable voltage-divider)							
Resolution	N			10			Bits
Integral Nonlinearity (Note 2)	INL	V_{DD} = +2.7V				±2	LSB
		V_{DD} = +5V				±2	
Differential Nonlinearity (Note 2)	DNL	V_{DD} = +2.7V				±1	LSB
		V_{DD} = +5V				±1	
End-to-End Resistance Temperature Coefficient	TC_R				35		ppm/°C
Ratiometric Resistance Temperature Coefficient					5		ppm/°C
Full-Scale Error	FSE	MAX5481		-4	-2.5	0	LSB
		MAX5482		-4	-0.75	0	
Zero-Scale Error	ZSE	MAX5481		0	+3.3	+5	LSB
		MAX5482		0	+1.45	+5	
End-to-End Resistance	R_{H-L}	MAX5481		7.5	10	12.5	kΩ
		MAX5482		37.5	50	62.5	
Wiper Capacitance	C_W				60		pF
Resistance from W to L and H		W at code = 15, H and L shorted to V_{SS}, measure resistance from W to H, Figures 1 and 2	MAX5481		6.3		kΩ
			MAX5482		25		
DC PERFORMANCE (MAX5483/MAX5484 variable resistor)							
Resolution	N			10			Bits
Integral Nonlinearity (Note 3)	INL_R	V_{DD} = +2.7V			-1.6		LSB
		V_{DD} = +3V		-4	-1.4	+4	
		V_{DD} = +5V		-4	-1.3	+4	
Differential Nonlinearity (Note 3)	DNL_R	V_{DD} = +2.7V			+0.45		LSB
		V_{DD} = +3V		-1	+0.4	+1	
		V_{DD} = +5V		-1	+0.35	+1	
Variable-Resistor Temperature Coefficient	TC_{VR}	V_{DD} = +3V to +5.25V; code = 128 to 1024			35		ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, V_{SS} = V_{GND} = 0V, V_H = V_{DD}, V_L = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Full-Scale Wiper-to-End Resistance	R_{W-L}	MAX5483		7.5	10	12.5	kΩ
		MAX5484		37.5	50	62.5	kΩ
Zero-Scale Resistor Error	R_Z	Code = 0	MAX5483		70		Ω
			MAX5484		110		
Wiper Resistance	R_W	V_{DD} ≥ +3V (Note 4)			50		Ω
Wiper Capacitance	C_W				60		pF
DIGITAL INPUTS ($\overline{CS}$, SCLK($\overline{INC}$), DIN(U/$\overline{D}$), SPI/$\overline{UD}$) (Note 5)							
Input-High Voltage	V_{IH}	Single-supply operation	V_{DD} = +3.6V to +5.25V	2.4			V
			V_{DD} = +2.7V to +3.6V	0.7 x V_{DD}			
		Dual-supply operation	V_{DD} = +2.5V, V_{SS} = -2.5V	2.0			
Input-Low Voltage	V_{IL}	Single-supply operation	V_{DD} = +2.7V to +5.25V			0.8	V
		Dual-supply operation	V_{DD} = +2.5V, V_{SS} = -2.5V			0.6	
Input Leakage Current	I_{IN}					±1	µA
Input Capacitance	C_{IN}				5		pF
DYNAMIC CHARACTERISTICS							
Wiper -3dB Bandwidth		Wiper at code = 01111 01111, C_{LW} = 10pF	MAX5481		250		kHz
			MAX5482		50		
Total Harmonic Distortion	THD	V_{DD} = +3V, wiper at code = 01111 01111, $1V_{RMS}$ at 10kHz is applied at H, 10pF load on W	MAX5481		0.026		%
			MAX5482		0.03		
NONVOLATILE MEMORY RELIABILITY							
Data Retention		T_A = +85°C			50		Years
Endurance		T_A = +25°C			200,000		Stores
		T_A = +85°C			50,000		
POWER SUPPLY							
Single-Supply Voltage	V_{DD}	V_{SS} = V_{GND} = 0V		2.70		5.25	V
Dual-Supply Voltage	V_{DD}	V_{GND} = 0V		2.50		5.25	V
	V_{SS}	V_{DD} - V_{SS} ≤ +5.25V		-2.5		-0.2	
Average Programming Current	I_{PG}	During nonvolatile write; digital inputs = V_{DD} or GND			220	400	µA
Peak Programming Current		During nonvolatile write only; digital inputs = V_{DD} or GND			4		mA
Standby Current	I_{DD}	Digital inputs = V_{DD} or GND, T_A = +25°C			0.6	1	µA

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, V_{SS} = V_{GND} = 0V, V_H = V_{DD}, V_L = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG SECTION						
Wiper Settling Time (Note 6)	t_S	MAX5481		5		µs
		MAX5482		22		
SPI-COMPATIBLE SERIAL INTERFACE (Figure 3)						
SCLK Frequency	f_{SCLK}				7	MHz
SCLK Clock Period	t_{CP}		140			ns
SCLK Pulse-Width High	t_{CH}		60			ns
SCLK Pulse-Width Low	t_{CL}		60			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		60			ns
SCLK Rise to $\overline{CS}$ Rise Hold	t_{CSH}		0			ns
DIN to SCLK Setup	t_{DS}		40			ns
DIN Hold after SCLK	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		15			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}		60			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		150			ns
Write NV Register Busy Time	t_{BUSY}				12	ms
UP/DOWN DIGITAL INTERFACE (Figure 8)						
$\overline{CS}$ to $\overline{INC}$ Setup	t_{CI}		25			ns
$\overline{INC}$ High to U/$\overline{D}$ Change	t_{ID}		20			ns
U/$\overline{D}$ to $\overline{INC}$ Setup	t_{DI}		25			ns
$\overline{INC}$ Low Period	t_{IL}		25			ns
$\overline{INC}$ High Period	t_{IH}		25			ns
$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	t_{IC}		50			ns
$\overline{CS}$ Deselect Time (Store)	t_{CPH}		50			ns
$\overline{INC}$ Cycle Time	t_{CYC}		50			ns
$\overline{INC}$ Active to $\overline{CS}$ Inactive	t_{IK}		50			ns
Wiper Store Cycle	t_{WSC}				12	ms

Note 1: 100% production tested at T_A = +25°C and T_A = +85°C. Guaranteed by design to T_A = -40°C.

Note 2: The DNL and INL are measured with the device configured as a voltage-divider with H = V_{DD} and L = V_{SS}. The wiper terminal (W) is unloaded and measured with a high-input-impedance voltmeter.

Note 3: The DNL_R and INL_R are measured with D.N.C. unconnected and L = V_{SS} = 0V. For V_{DD} = +5V, the wiper terminal is driven with a source current of I_W = 80µA for the 50kΩ device and 400µA for the 10kΩ device. For V_{DD} = +3V, the wiper terminal is driven with a source current of 40µA for the 50kΩ device and 200µA for the 10kΩ device.

Note 4: The wiper resistance is measured using the source currents given in Note 3.

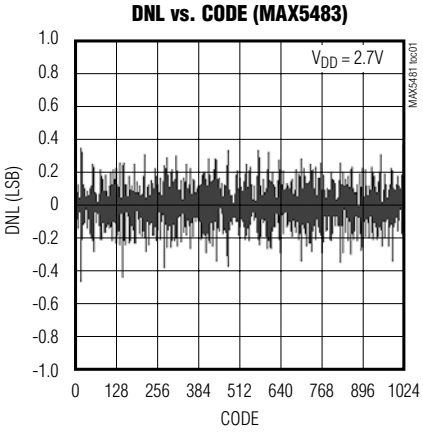
Note 5: The device draws higher supply current when the digital inputs are driven with voltages between (V_{DD} - 0.5V) and (V_{GND} + 0.5V). See Supply Current vs. Digital Input Voltage in the *Typical Operating Characteristics*.

Note 6: Wiper settling test condition uses the voltage-divider configuration with a 10pF load on W. Transition code from 00000 00000 to 01111 01111 and measure the time from $\overline{CS}$ going high to the wiper voltage settling to within 0.5% of its final value.

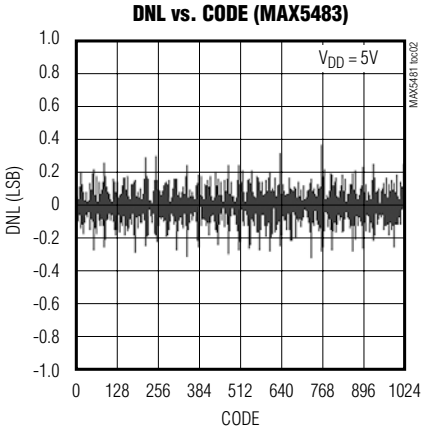
Typical Operating Characteristics

(V_{DD} = 5.0V, V_{SS} = 0V, T_A = +25°C, unless otherwise noted.)

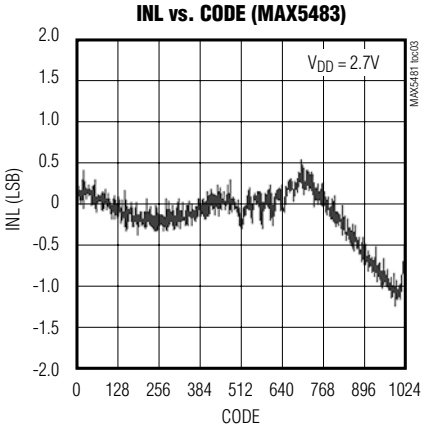
DNL vs. CODE (MAX5483)



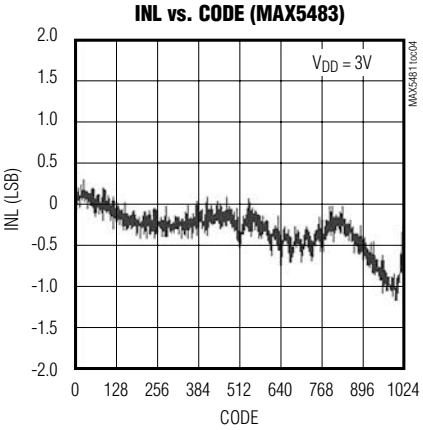
DNL vs. CODE (MAX5483)



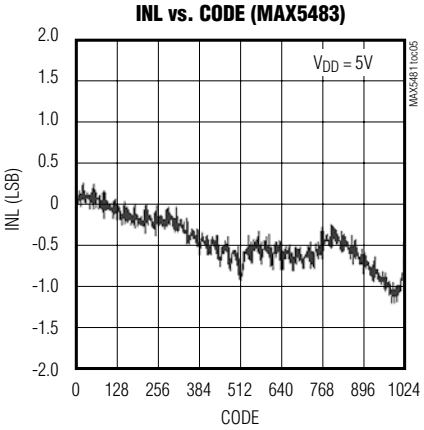
INL vs. CODE (MAX5483)



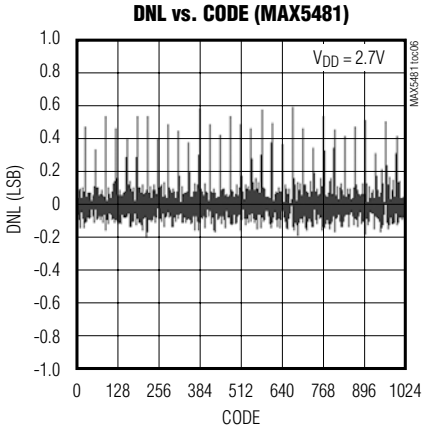
INL vs. CODE (MAX5483)



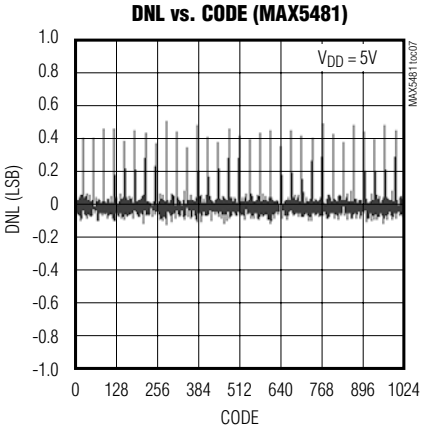
INL vs. CODE (MAX5483)



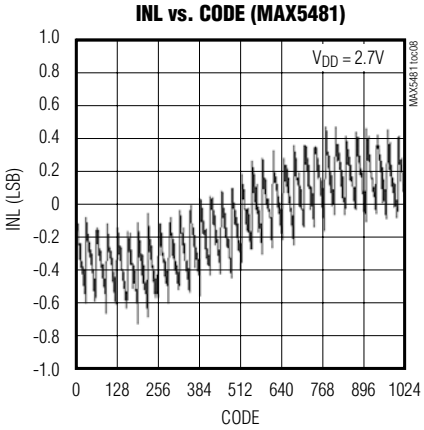
DNL vs. CODE (MAX5481)



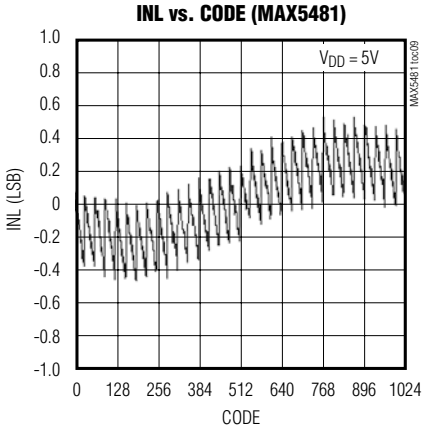
DNL vs. CODE (MAX5481)



INL vs. CODE (MAX5481)



INL vs. CODE (MAX5481)

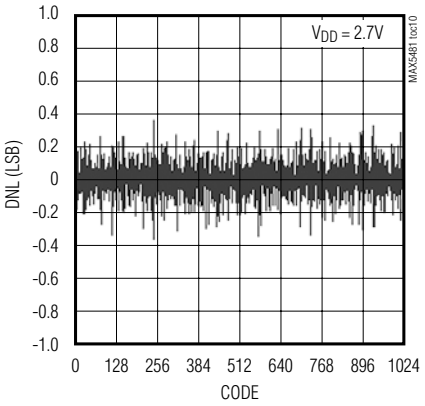


10-Bit, Nonvolatile, Linear-Taper Digital Potentiometers

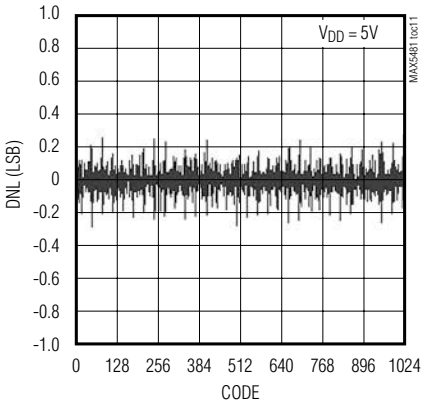
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{SS} = 0V, T_A = +25°C, unless otherwise noted.)

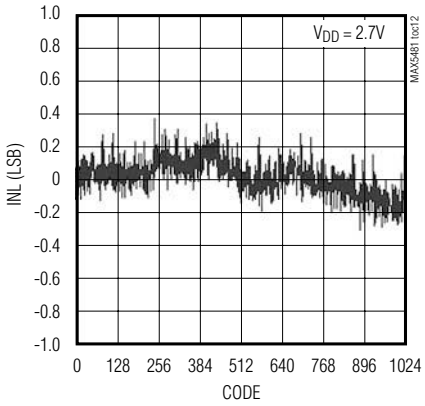
DNL vs. CODE (MAX5484)



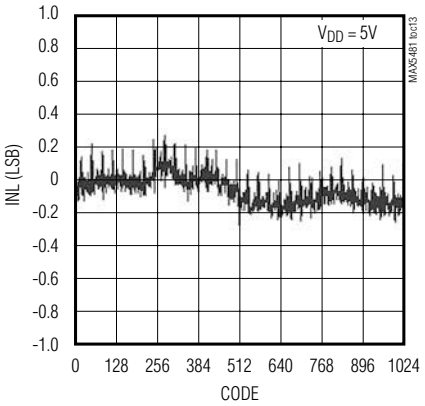
DNL vs. CODE (MAX5484)



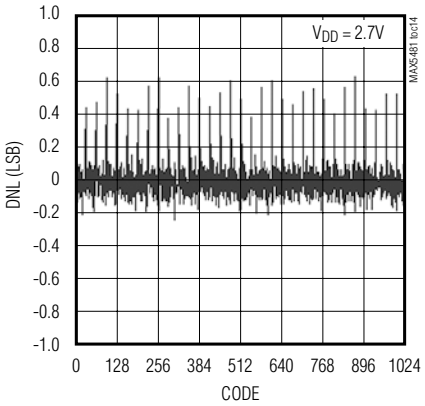
INL vs. CODE (MAX5484)



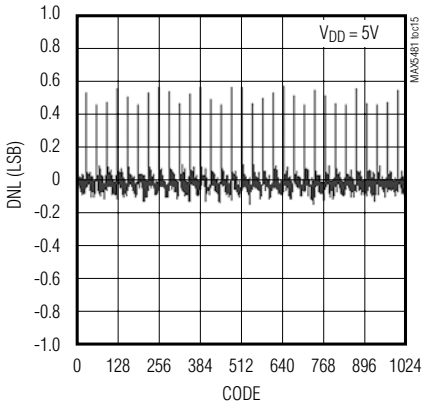
INL vs. CODE (MAX5484)



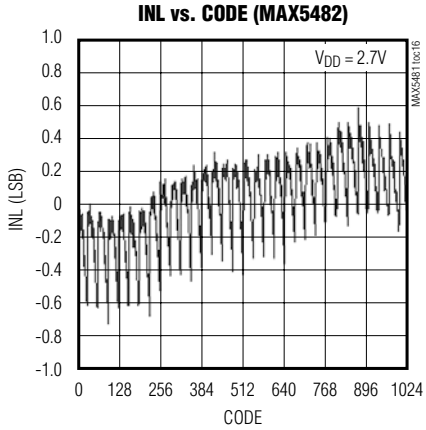
DNL vs. CODE (MAX5482)



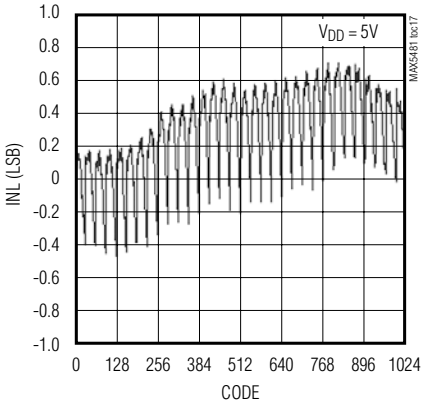
DNL vs. CODE (MAX5482)



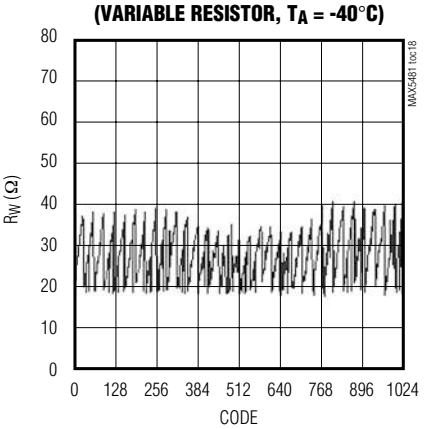
INL vs. CODE (MAX5482)



INL vs. CODE (MAX5482)



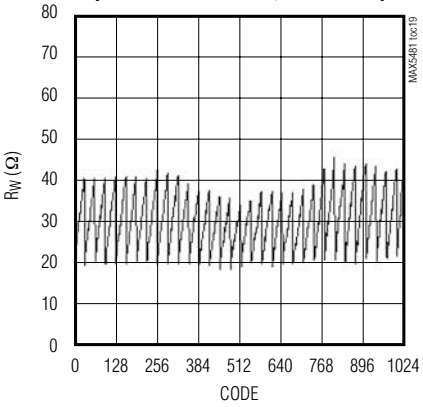
WIPER RESISTANCE vs. CODE (VARIABLE RESISTOR, T_A = -40°C)



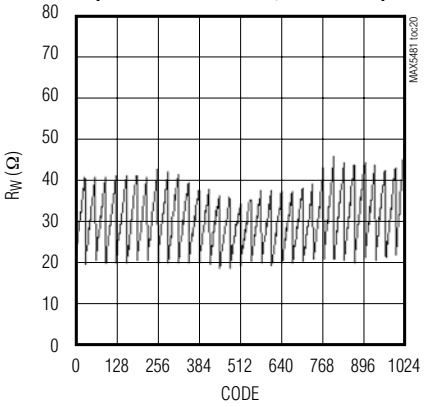
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{SS} = 0V, T_A = +25°C, unless otherwise noted.)

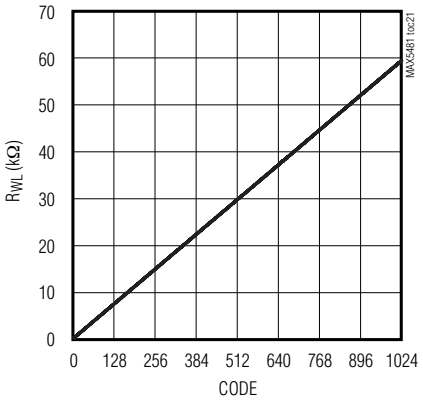
WIPER RESISTANCE vs. CODE (VARIABLE RESISTOR, T_A = +25°C)



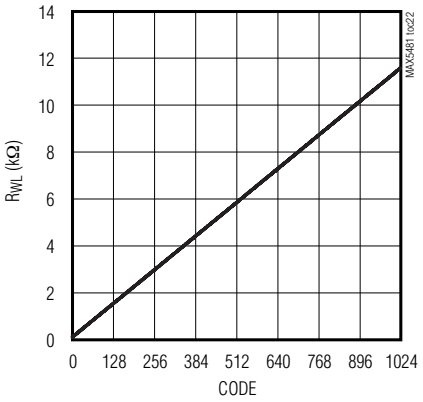
WIPER RESISTANCE vs. CODE (VARIABLE RESISTOR, T_A = +85°C)



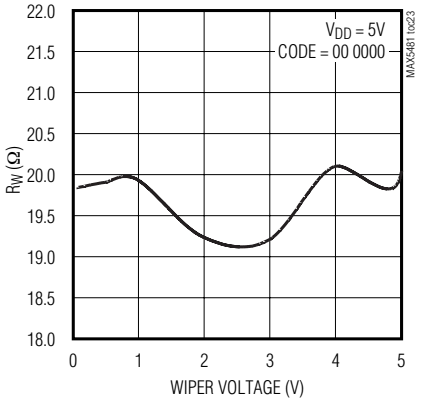
W-TO-L RESISTANCE vs. CODE (MAX5484)



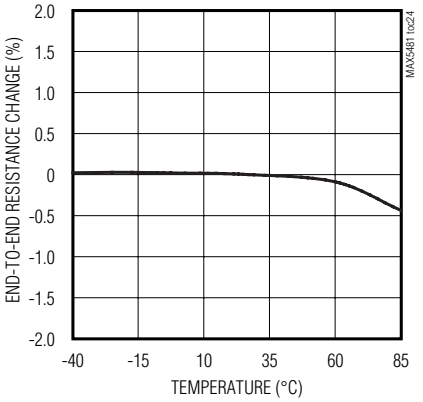
W-TO-L RESISTANCE vs. CODE (MAX5483)



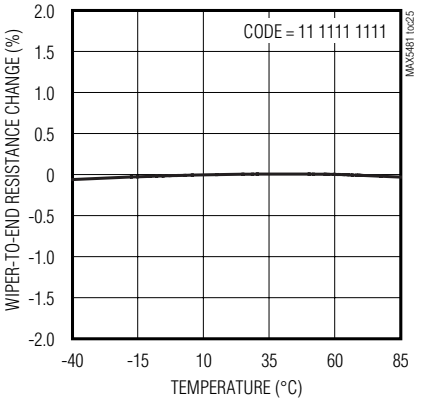
WIPER RESISTANCE vs. WIPER VOLTAGE (VARIABLE RESISTOR)



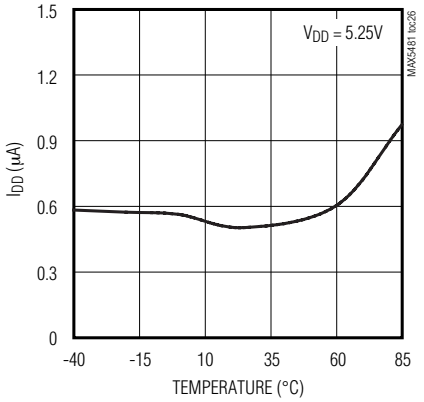
END-TO-END (R_{HL}) % CHANGE vs. TEMPERATURE (VOLTAGE-DIVIDER)



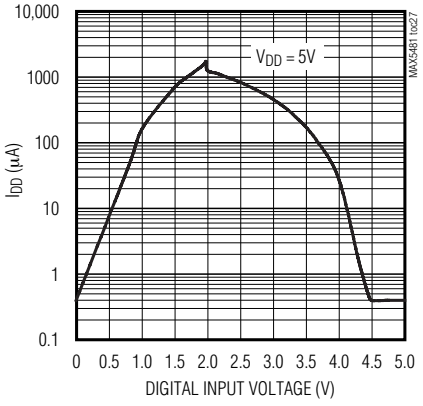
WIPER-TO-END RESISTANCE (R_{WL}) % CHANGE vs. TEMPERATURE (VARIABLE RESISTOR)



STANDBY SUPPLY CURRENT vs. TEMPERATURE



DIGITAL SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE

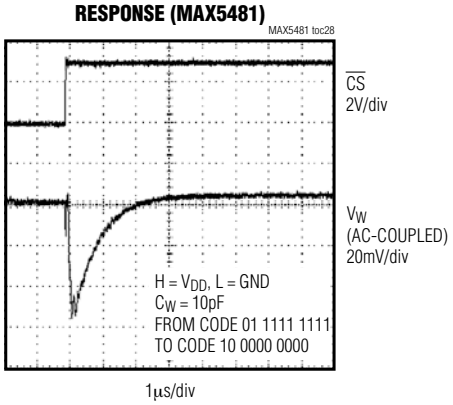


10-Bit, Nonvolatile, Linear-Taper Digital Potentiometers

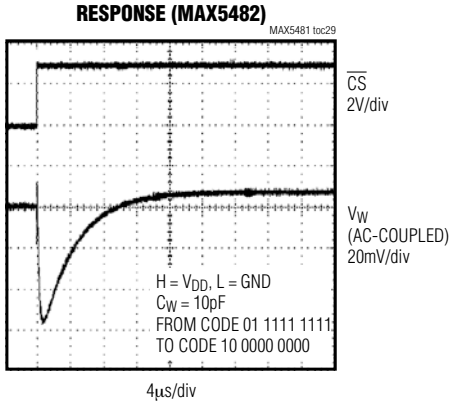
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

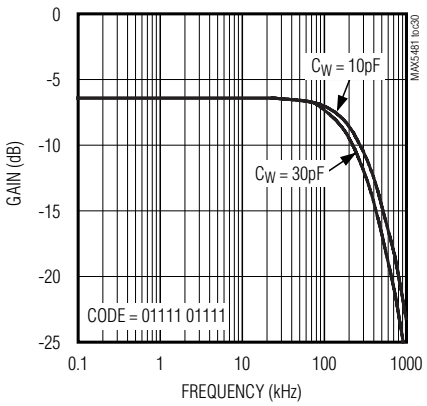
TAP-TO-TAP SWITCHING TRANSIENT RESPONSE (MAX5481)



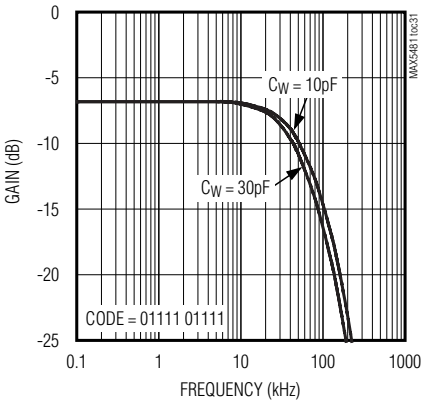
TAP-TO-TAP SWITCHING TRANSIENT RESPONSE (MAX5482)



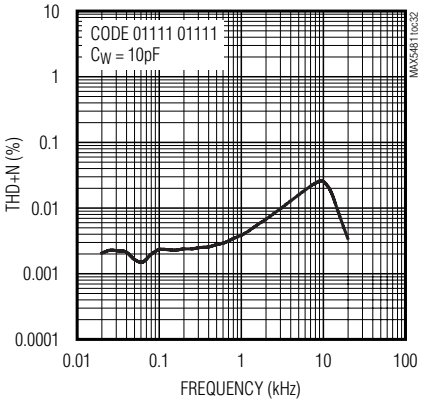
WIPER RESPONSE vs. FREQUENCY (MAX5481)



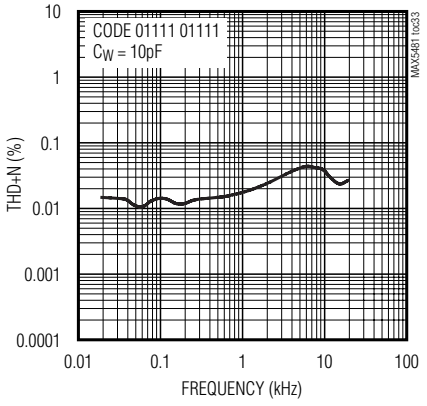
WIPER RESPONSE vs. FREQUENCY (MAX5482)



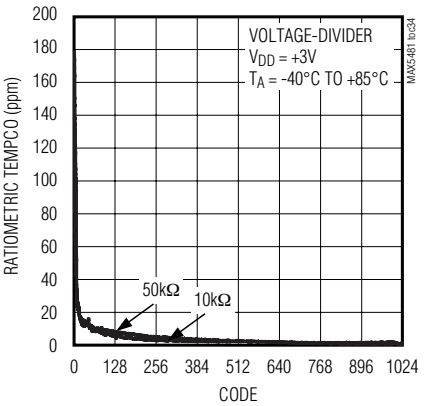
THD+N vs. FREQUENCY (MAX5481)



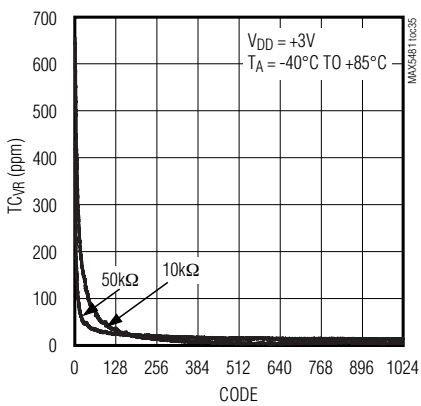
THD+N vs. FREQUENCY (MAX5482)



RATIOMETRIC TEMPERATURE COEFFICIENT vs. CODE



VARIABLE-RESISTOR TEMPERATURE COEFFICIENT vs. CODE



Pin Description

(MAX5481/MAX5482 Voltage-Dividers)

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	12	H	High Terminal
2	11	W	Wiper Terminal
3	10	L	Low Terminal
4–7, 15	7, 8, 9, 13	N.C.	No Connection. Not internally connected.
8, 16	14	V_{SS}	Negative Power-Supply Input. For single-supply operation, connect V_{SS} to GND. For dual-supply operation, -2.5V ≤ V_{SS} ≤ -0.2V as long as (V_{DD} - V_{SS}) ≤ +5.25V. Bypass V_{SS} to GND with a 0.1µF ceramic capacitor as close to the device as possible.
9	6	SPI/$\overline{UD}$	Interface-Mode Select. Select serial SPI interface when SPI/$\overline{UD}$ = 1. Select serial up/down interface when SPI/$\overline{UD}$ = 0.
10	5	DIN(U/$\overline{D}$)	Serial SPI Interface Data Input (SPI/$\overline{UD}$ = 1)
			Up/Down Control Input (SPI/$\overline{UD}$ = 0). With DIN(U/$\overline{D}$) low, a high-to-low SCLK($\overline{INC}$) transition decrements the wiper position. With DIN(U/$\overline{D}$) high, a high-to-low SCLK($\overline{INC}$) transition increments the wiper position.
11	4	SCLK($\overline{INC}$)	Serial SPI Interface Clock Input (SPI/$\overline{UD}$ = 1)
			Wiper-Increment Control Input (SPI/$\overline{UD}$ = 0). With $\overline{CS}$ low, the wiper position moves in the direction determined by the state of DIN(U/$\overline{D}$) on a high-to-low transition.
12	3	$\overline{CS}$	Active-Low Digital Input Chip Select
13	2	GND	Ground
14	1	V_{DD}	Positive Power-Supply Input (+2.7V ≤ V_{DD} ≤ +5.25V). Bypass V_{DD} to GND with a 0.1µF ceramic capacitor as close to the device as possible.
—	—	EP	Exposed Pad (TQFN Only). Externally connect EP to V_{SS} or leave unconnected.

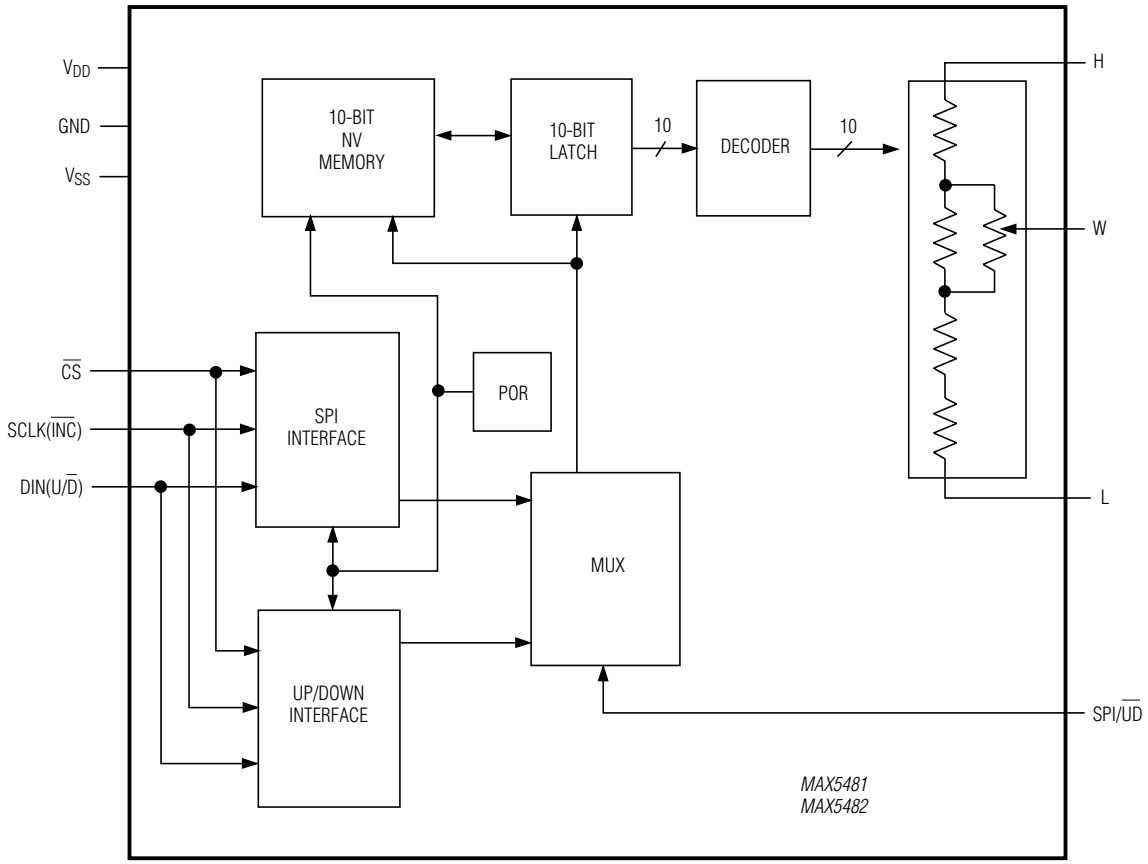
Pin Description (continued)

(MAX5483/MAX5484 Variable Resistors)

PIN		NAME	FUNCTION
TQFN	TSSOP		
4–7, 15	7, 8, 9, 13	N.C.	No Connection. Not internally connected.
1	12	D.N.C.	Do Not Connect. Leave unconnected for proper operation.
2	11	W	Wiper Terminal
3	10	L	Low Terminal
8, 16	14	V_{SS}	Negative Power-Supply Input. For single-supply operation, connect V_{SS} to GND. For dual-supply operation, -2.5V ≤ V_{SS} ≤ -0.2V as long as (V_{DD} - V_{SS}) ≤ 5.25V. Bypass V_{SS} to GND with a 0.1µF ceramic capacitor as close to the device as possible.
9	6	SPI/$\overline{UD}$	Interface-Mode Select. Select serial SPI interface when SPI/$\overline{UD}$ = 1. Select serial up/down interface when SPI/$\overline{UD}$ = 0.
10	5	DIN(U/$\overline{D}$)	Serial SPI Interface Data Input (SPI/$\overline{UD}$ = 1)
			Up/Down Control Input (SPI/$\overline{UD}$ = 0). With DIN(U/$\overline{D}$) low, a high-to-low SCLK($\overline{INC}$) transition decrements the wiper position. With DIN(U/$\overline{D}$) high, a high-to-low SCLK($\overline{INC}$) transition increments the wiper position.
11	4	SCLK($\overline{INC}$)	Serial SPI Interface Clock Input (SPI/$\overline{UD}$ = 1)
			Wiper Increment Control Input (SPI/$\overline{UD}$ = 0). With $\overline{CS}$ low, the wiper position moves in the direction determined by the state of DIN(U/$\overline{D}$) on a high-to-low transition.
12	3	$\overline{CS}$	Active-Low Digital Input Chip Select
13	2	GND	Ground
14	1	V_{DD}	Positive Power-Supply Input (+2.7V ≤ V_{DD} ≤ +5.25V). Bypass V_{DD} to GND with a 0.1µF ceramic capacitor as close to the device as possible.
—	—	EP	Exposed Pad (TQFN Only). Externally connect EP to V_{SS} or leave unconnected.

10-Bit, Nonvolatile, Linear-Taper Digital Potentiometers

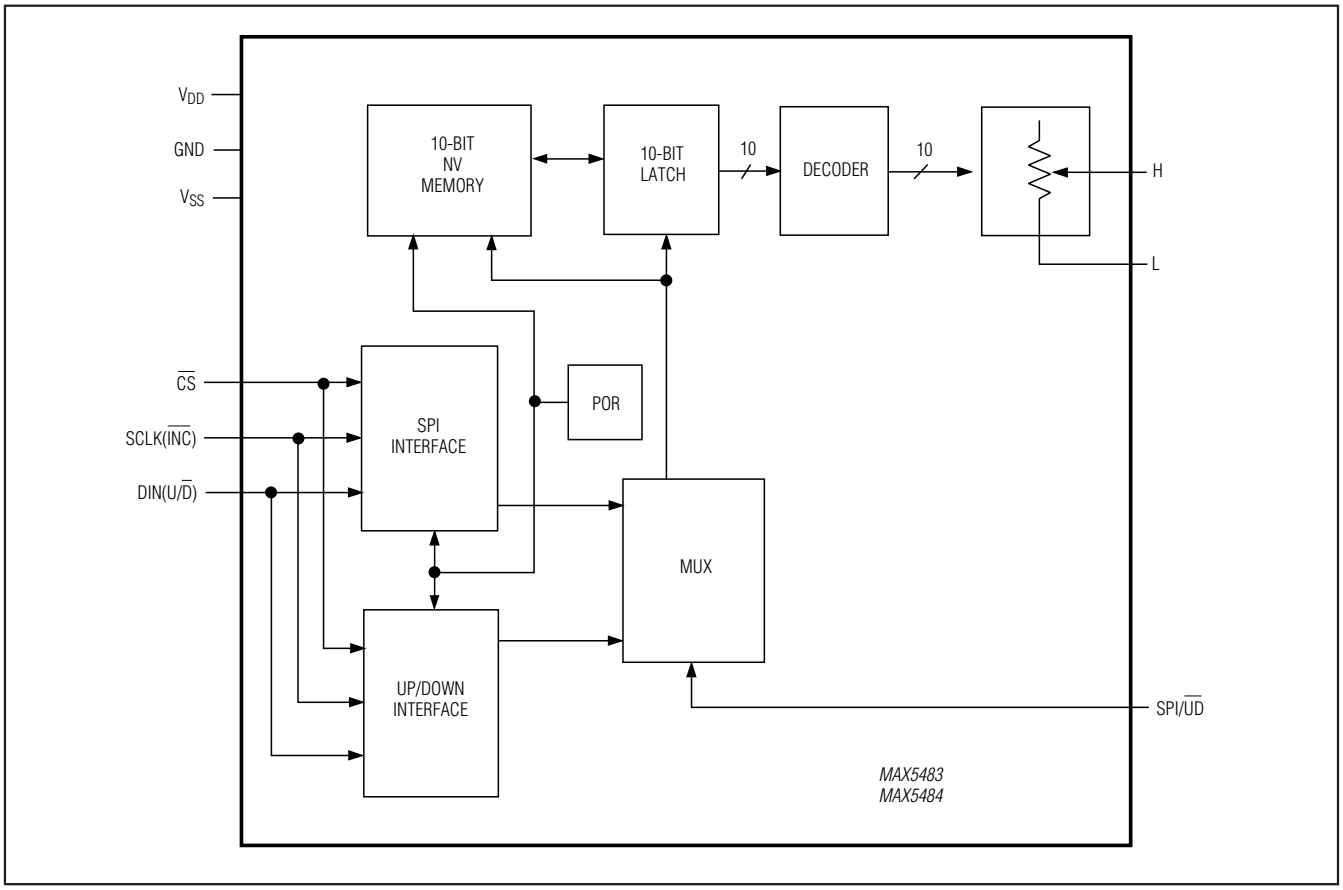
Functional Diagrams



NOTE: THE MAX5481/MAX5482 ARE NOT INTENDED FOR CURRENT TO FLOW THROUGH THE WIPER (SEE THE *MAX5481/MAX5482 PROGRAMMABLE VOLTAGE-DIVIDER* SECTION).

10-Bit, Nonvolatile, Linear-Taper Digital Potentiometers

Functional Diagrams (continued)



Detailed Description

The MAX5481/MAX5482 linear programmable voltage-dividers and the MAX5483/MAX5484 variable resistors feature 1024 tap points (10-bit resolution) (see the *Functional Diagrams*). These devices consist of multiple strings of equal resistor segments with a wiper contact that moves among the 1024 points through a pin-selectable 3-wire SPI-compatible serial interface or up/down interface. The MAX5481/MAX5483 provide a total end-to-end resistance of 10kΩ, and the MAX5482/MAX5484 have an end-to-end resistance of 50kΩ. The MAX5481/MAX5482 allow access to the high, low, and wiper terminals for a standard voltage-divider configuration.

MAX5481/MAX5482 Programmable Voltage-Dividers

The MAX5481/MAX5482 programmable voltage-dividers provide a weighted average of the voltage between the H and L inputs at the W output. Both devices feature 10-bit resolution and provide up to 1024 tap points between the H and L voltages. Ideally, the V_L voltage occurs at the wiper terminal (W) when all data bits are zero and the V_H voltage occurs at the wiper terminal when all data bits are one. The step size (1 LSB) voltage is equal to the voltage applied across terminals H and L divided by 2^{10}. Calculate the wiper voltage V_W as follows:

$$V_W(D) = D\left[\frac{V_{HL} - \left(|V_{FSE}| + |V_{ZSE}|\right)}{1023}\right] + V_L + |V_{ZSE}|$$

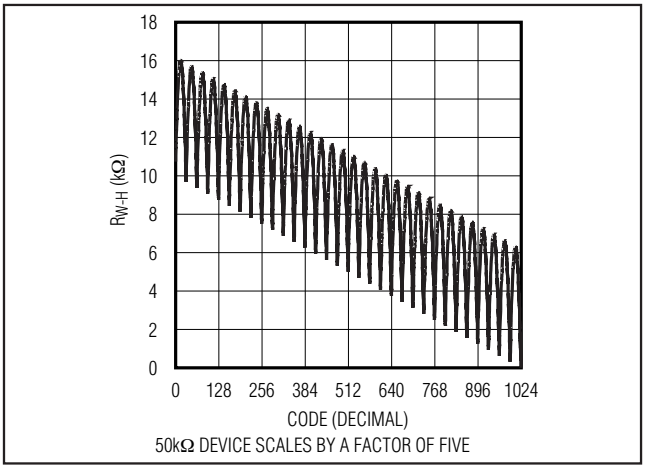


Figure 1. Resistance from W to H vs. Code (10kΩ Voltage-Divider)

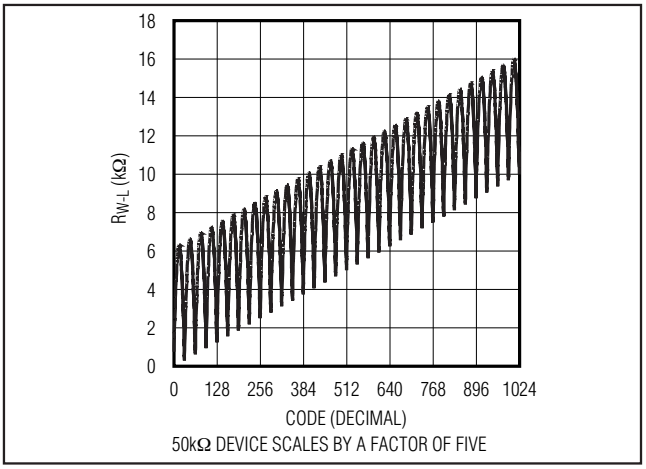


Figure 2. Resistance from W to L vs. Code (10kΩ Voltage-Divider)

where D is the decimal equivalent of the 10 data bits written (0 to 1023), V_{HL} is the voltage difference between the H and L terminals:

$$V_{FSE} = FSE\left[\frac{V_{HL}}{1024}\right], \text{and}$$

$$V_{ZSE} = ZSE\left[\frac{V_{HL}}{1024}\right]$$

The MAX5481 includes a total end-to-end resistance value of 10kΩ while the MAX5482 features an end-to-end resistance value of 50kΩ. **These devices are not intended to be used as a variable resistor**. Wiper current creates a nonlinear voltage drop in series with the wiper. To ensure temperature drift remains within specifications, do not pull current through the voltage-divider wiper. Connect the wiper to a high-impedance node. Figures 1 and 2 show the behavior of the MAX5481's resistance from W to H and from W to L. This does not apply to the variable-resistor devices

MAX5483/MAX5484 Variable Resistors

The MAX5483/MAX5484 provide a programmable resistance between W and L. The MAX5483 features a total end-to-end resistance value of 10kΩ, while the MAX5484 provides an end-to-end resistance value of 50kΩ. The programmable resolution of this resistance is equal to the nominal end-to-end resistance divided by 1024 (10-bit resolution). For example, each nominal segment resistance is 9.8Ω and 48.8Ω for the MAX5483 and the MAX5484, respectively.

Table 1. R_{WL} at Selected Codes

CODE (DECIMAL)	MAX5483 (10kΩ DEVICE)	MAX5484 (50kΩ DEVICE)
	R_{WL} (Ω)	R_{WL} (Ω)
0	70	110
1	80	160
512	5070	25,110
1023	10,070	50,110

The 10-bit data in the 10-bit latch register selects a wiper position from the 1024 possible positions, resulting in 1024 values for the resistance from W to L. Calculate the resistance from W to L (R_{WL}) by using the following formula:

$$R_{WL}(D) = \frac{D}{1023} \times R_{W-L} + R_Z$$

where D is decimal equivalent of the 10 data bits written, R_{W-L} is the nominal end-to-end resistance, and R_Z is the zero-scale error. Table 1 shows the values of R_{WL} at selected codes for the MAX5483/MAX5484.

Digital Interface

Configure the MAX5481–MAX5484 by a pin-selectable, 3-wire, SPI-compatible serial data interface or an up/down interface. Drive SPI/$\overline{UD}$ high to select the 3-wire SPI-compatible interface. Pull SPI/$\overline{UD}$ low to select the up/down interface.

Table 2. Command Decoding*

CLOCK EDGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	...	24
Bit Name	—	—	C1	C0	—	—	—	—	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	—	…	—
Write Wiper Register	0	0	0	0	0	0	0	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	…	X
Copy Wiper Register to NV Register	0	0	1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	…	—
Copy NV Register to Wiper Register	0	0	1	1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	…	—

**D9 is the MSB and D0 is the LSB.*
X = Don't care.

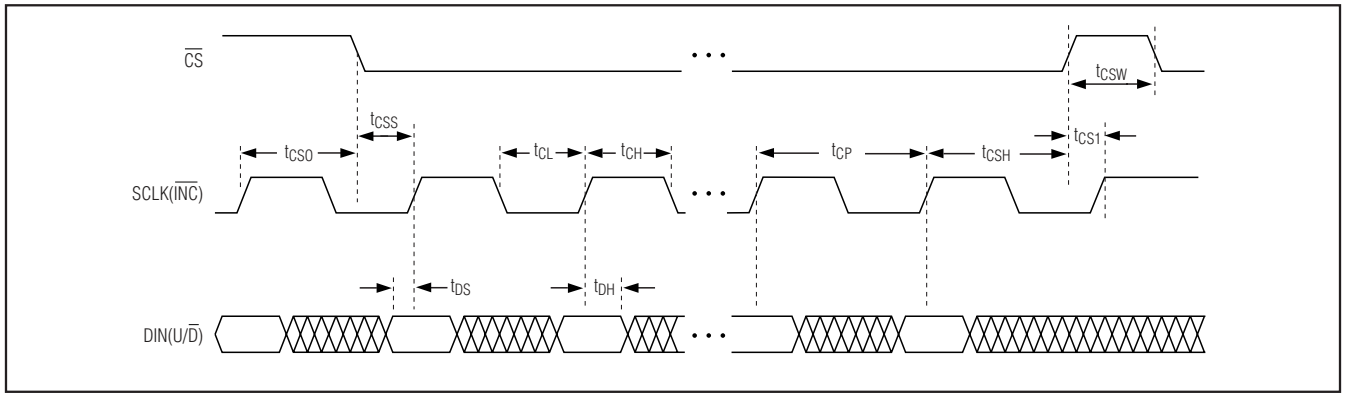


Figure 3. SPI-Compatible Serial-Interface Timing Diagram (SPI/UD = 1)

SPI-Compatible Serial Interface

Drive SPI/UD high to enable the 3-wire SPI-compatible serial interface (see Figure 3). This write-only interface contains three inputs: chip select (CS), data in (DIN(U/D)), and data clock (SCLK(INC)). Drive CS low to load the data at DIN(U/D) synchronously into the shift register on each SCLK(INC) rising edge.

The WRITE command (C1, C0 = 00) requires 24 clock cycles to transfer the command and data (Figure 4a). The COPY commands (C1, C0 = 10 or 11) use either eight clock cycles to transfer the command bits (Figure 4b) or 24 clock cycles with the last 16 data bits disregarded by the device.

After loading the data into the shift register, drive CS high to latch the data into the appropriate control register. Keep CS low during the entire serial data stream to avoid corruption of the data. Table 2 shows the command decoding.

Write Wiper Register

Data written to this register (C1, C0 = 00) controls the wiper position. The 10 data bits (D9–D0) indicate the position of the wiper. For example, if DIN(U/D) = 00 0000 0000, the wiper moves to the position closest to L. If DIN(U/D) = 11 1111 1111, the wiper moves closest to H.

This command writes data to the volatile random access memory (RAM), leaving the NV register unchanged. When the device powers up, the data stored in the NV register transfers to the wiper register, moving the wiper to the stored position. Figure 5 shows how to write data to the wiper register.

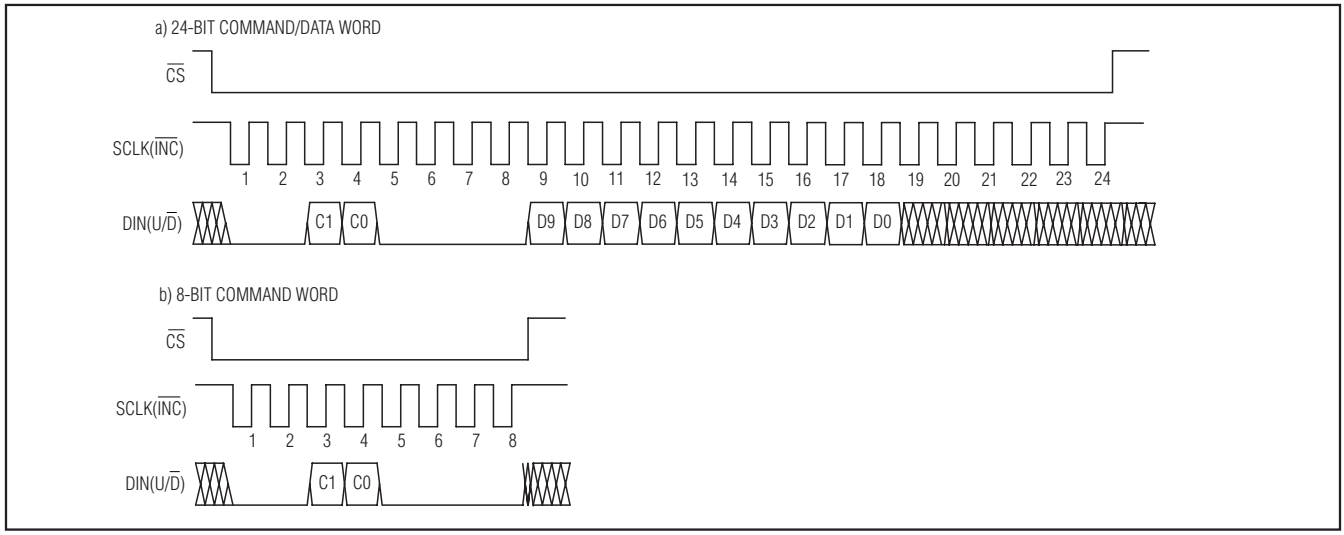


Figure 4. Serial SPI-Compatible Interface Format

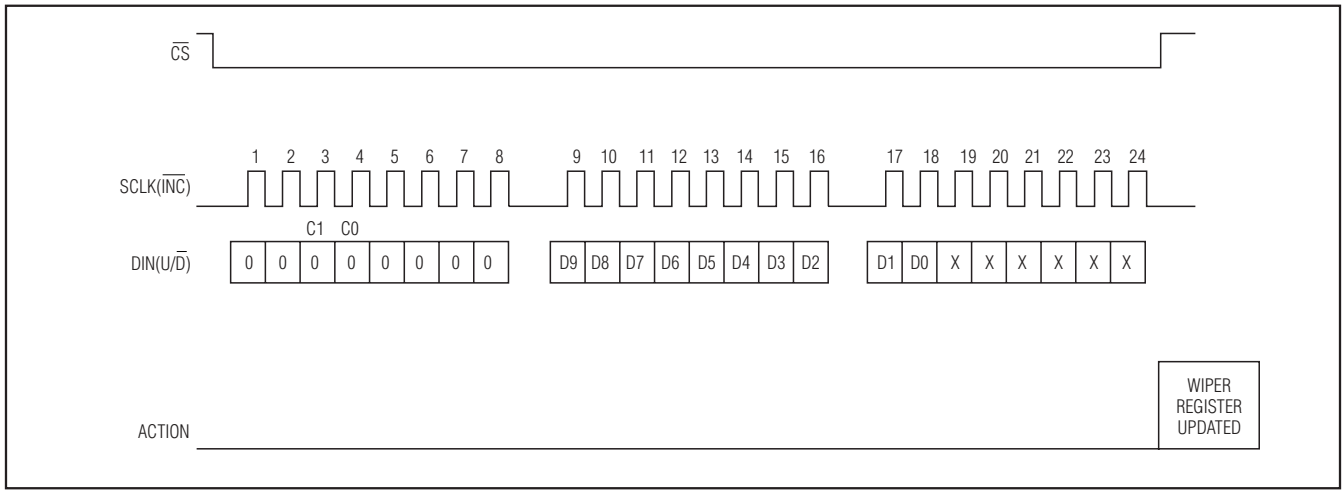


Figure 5. Write Wiper Register Operation

Table 3. Truth Table

$\overline{CS}$	DIN(U/$\overline{D}$)	SCLK($\overline{INC}$)	W
L	L	↓	Decrement
L	H	↓	Increment
L	X	↑	No Change
H	X	X	No Change
↓	X	X	No Change
↑	X	L	Position Not Stored
↑	X	H	Position Stored

↑ = *Low-to-high transition.*

↓ = *High-to-low transition.*

X = *Don't care.*

Copy Wiper Register to NV Register

The copy wiper register to NV register command (C1, C0 = 10) stores the current position of the wiper to the NV register for use at power-up. Figure 6 shows how to copy data from wiper register to NV register. The operation takes up to 12ms (max) after $\overline{CS}$ goes high to complete and no other operation should be performed until completion.

Copy NV Register to Wiper Register

The copy NV register to wiper register (C1, C0 = 11) restores the wiper position to the current value stored in the NV register. Figure 7 shows how to copy data from the NV register to the wiper register.

Digital Up/Down Interface

Figure 8 illustrates an up/down serial-interface timing diagram. In digital up/down interface mode (SPI/$\overline{UD}$ = 0), the logic inputs $\overline{CS}$, DIN(U/$\overline{D}$), and SCLK($\overline{INC}$) control the wiper position and store it in nonvolatile memory (see Table 3). The chip-select ($\overline{CS}$) input enables the serial interface when low and disables the interface when high. The position of the wiper is stored in the nonvolatile register when $\overline{CS}$ transitions from low to high while SCLK($\overline{INC}$) is high.

When the serial interface is active ($\overline{CS}$ low), a high-to-low (falling edge) transition on SCLK($\overline{INC}$) increments or decrements the internal 10-bit counter depending on the state of DIN(U/$\overline{D}$). If DIN(U/$\overline{D}$) is high, the wiper increments. If DIN(U/$\overline{D}$) is low, the wiper decrements.

The device stores the value of the wiper position in the nonvolatile memory when $\overline{CS}$ transitions from low to high while SCLK($\overline{INC}$) is high. The host system can disable the serial interface and deselect the device without storing the latest wiper position in the nonvolatile memory by keeping SCLK($\overline{INC}$) low while taking $\overline{CS}$ high.

Upon power-up, the MAX5481–MAX5484 load the value of nonvolatile memory into the wiper register, and set the wiper position to the value last stored.

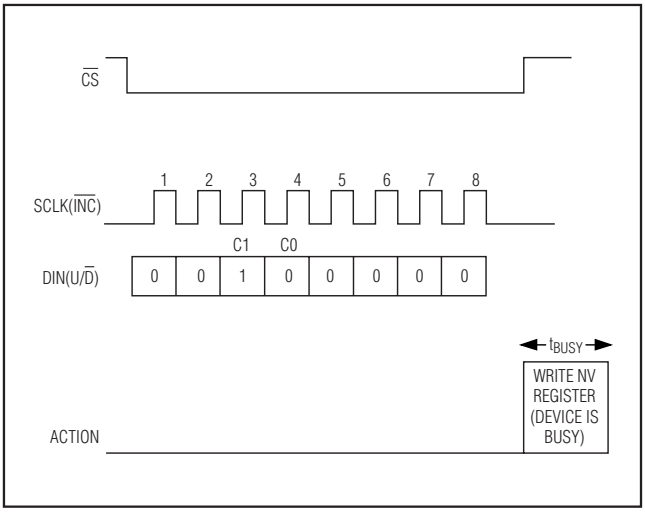


Figure 6. Copy Wiper Register to NV Register Operation

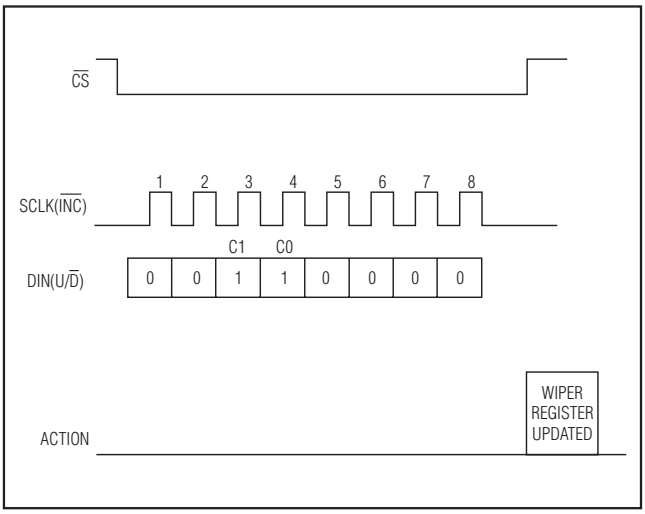


Figure 7. Copy NV Register to Wiper Register Operation

Standby Mode

The MAX5481–MAX5484 feature a low-power standby mode. When the device is not being programmed, it enters into standby mode and supply current drops to 0.5µA (typ).

Nonvolatile Memory

The internal EEPROM consists of a nonvolatile register that retains the last value stored prior to power-down. The nonvolatile register is programmed to midscale at the factory. The nonvolatile memory is guaranteed for 50 years of wiper data retention and up to 200,000 wiper write cycles.

Power-Up

Upon power-up, the MAX5481–MAX5484 load the data stored in the nonvolatile wiper register into the volatile wiper register, updating the wiper position with the data stored in the nonvolatile wiper register.

Applications Information

The MAX5481–MAX5484 are ideal for circuits requiring digitally controlled adjustable resistance, such as LCD contrast control (where voltage biasing adjusts the display contrast), or programmable filters with adjustable gain and/or cutoff frequency.

Positive LCD Bias Control

Figures 9 and 10 show an application where a voltage-divider or a variable resistor is used to make an adjustable, positive LCD-bias voltage. The op amp provides buffering and gain to the voltage-divider network made by the programmable voltage-divider (Figure 9) or to a fixed resistor and a variable resistor (see Figure 10).

Programmable Gain and Offset Adjustment

Figure 11 shows an application where a voltage-divider and a variable resistor are used to make a programmable gain and offset adjustment.

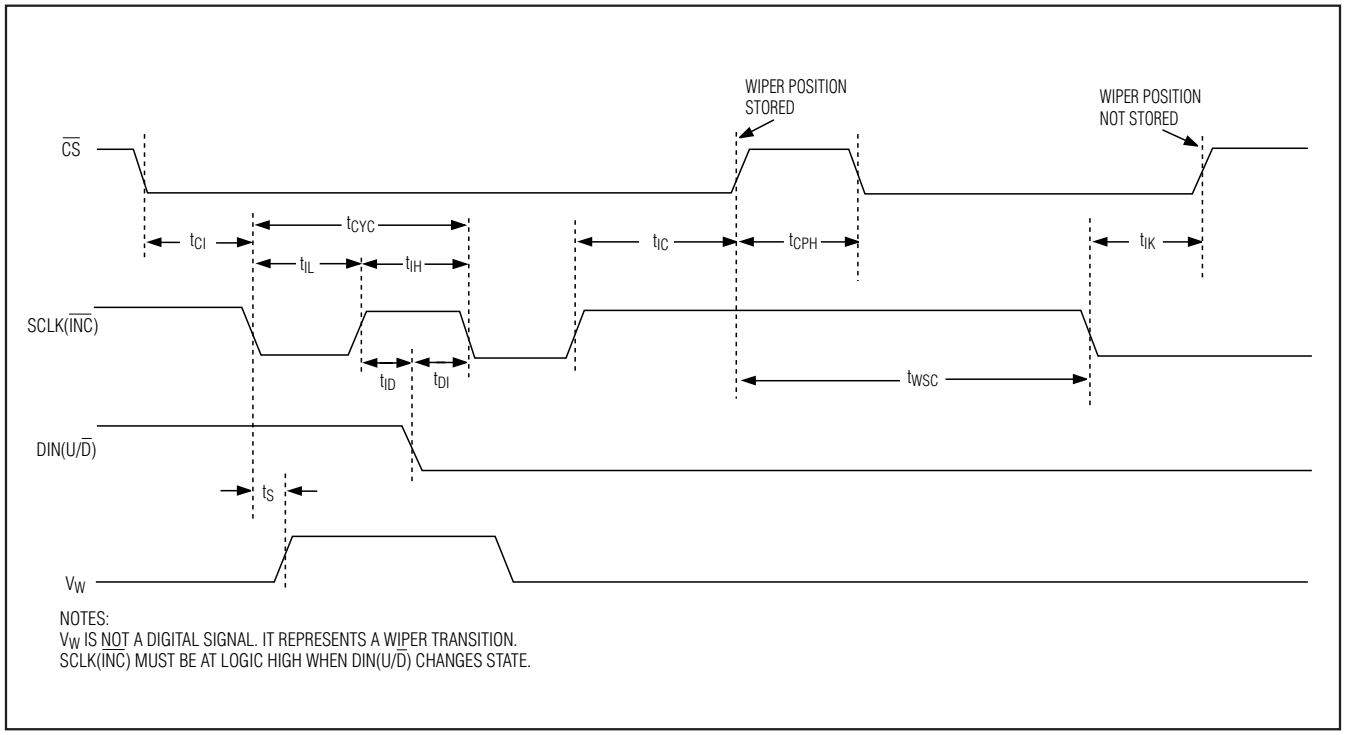


Figure 8. Up/Down Serial-Interface Timing Diagram (SPI/$\overline{UD}$ = 0)

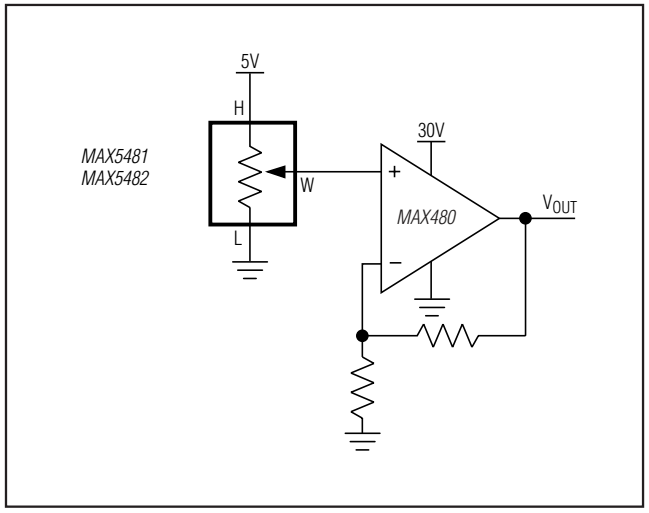


Figure 9. Positive LCD Bias Control Using a Voltage-Divider

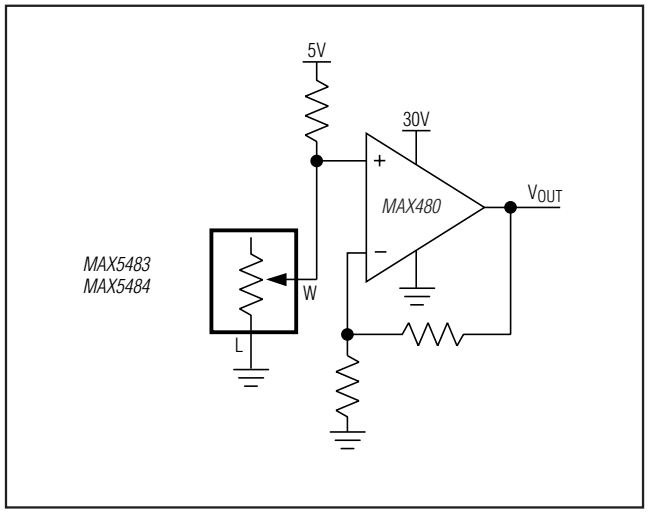


Figure 10. Positive LCD Bias Control Using a Variable Resistor

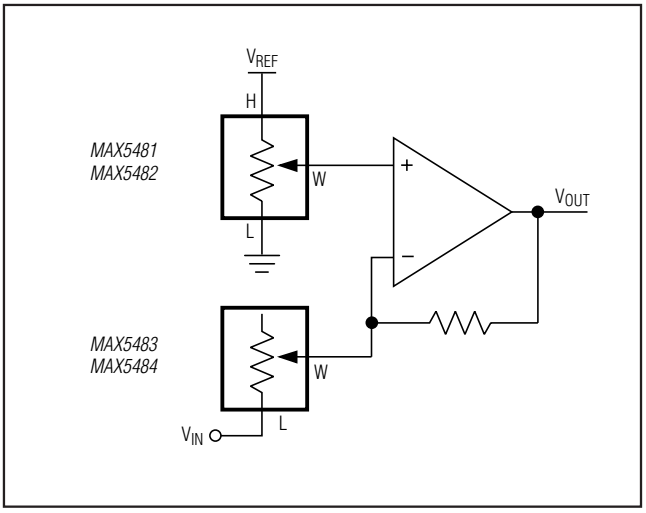


Figure 11. Programmable Gain/Offset Adjustment

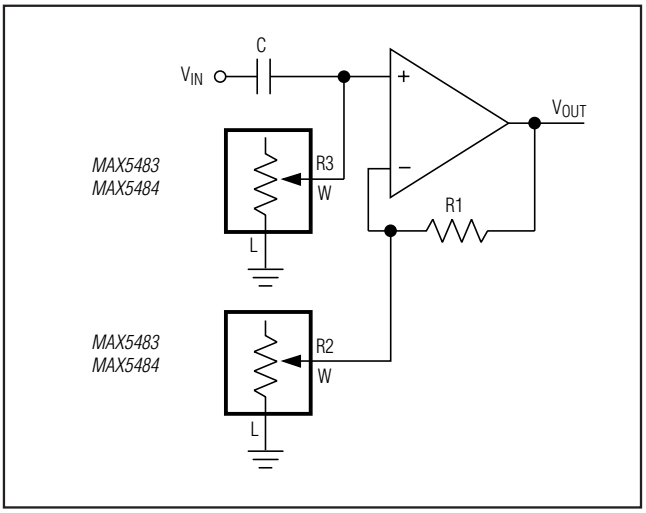


Figure 12. Programmable Filter

Programmable Filter

Figure 12 shows the configuration for a 1st-order programmable filter using two variable resistors. Adjust R2 for the gain and adjust R3 for the cutoff frequency. Use the following equations to estimate the gain (G) and the 3dB cutoff frequency (f_C):

$$G = 1 + \left(\frac{R1}{R2}\right)$$

$$f_C = \frac{1}{2\pi \times R3 \times C}$$

10-Bit, Nonvolatile, Linear-Taper Digital Potentiometers

Selector Guide

PART	CONFIGURATION	END-TO-END RESISTANCE (kΩ)
MAX5481ETE	Voltage-divider	10
MAX5481EUD	Voltage-divider	10
MAX5482ETE	Voltage-divider	50
MAX5482EUD	Voltage-divider	50
MAX5483ETE	Variable resistor	10
MAX5483EUD	Variable resistor	10
MAX5484ETE	Variable resistor	50
MAX5484EUD	Variable resistor	50

Ordering Information (continued)

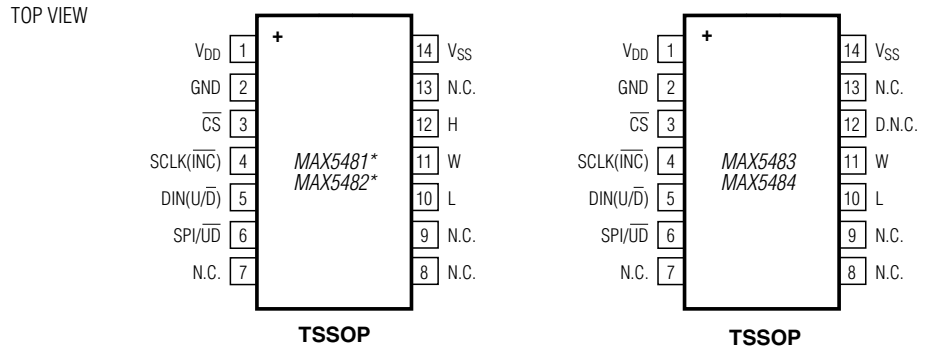
PART	PIN-PACKAGE	TOP MARK
MAX5482ETE+	16 TQFN-EP*	ACQ
MAX5482EUD+	14 TSSOP	—
MAX5483ETE+	16 TQFN-EP*	ACR
MAX5483EUD+	14 TSSOP	—
MAX5484ETE+	16 TQFN-EP*	ACS
MAX5484EUD+	14 TSSOP	—

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configurations (continued)



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633F+3	21-0136	90-0033
14 TSSOP	U14+1	21-0066	90-0113

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	12/07	Updated Table 3	16
4	4/10	Updated *Ordering Information*, *Absolute Maximum Ratings*, and Figure 8	1, 2, 17