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1 Description

The M93C46 (1 Kbit), M93C56 (2 Kbit), M93C66 (4 Kbit), M93C76 (8 Kbit) and M93C86 (16 Kbit) are Electrically Erasable PROgrammable Memory (EEPROM) devices accessed through the MICROWIRE bus protocol. The memory array can be configured either in bytes (x8b) or in words (x16b).

The M93Cx6-A125 devices operate within a voltage supply range from 1.8 V to 5.5 V

The M93Cx6-A125 devices are guaranteed over the -40 °C/+125 °C temperature range and are compliant with the Automotive standard AEC-Q100 Grade 1.

Table 2. Memory size versus organization

Device	Number of bits	Number of 8-bit bytes	Number of 16-bit words
M93C86	16384	2048	1024
M93C76	8192	1024	512
M93C66	4096	512	256
M93C56	2048	256	128
M93C46	1024	128	64

Figure 1. Logic diagram

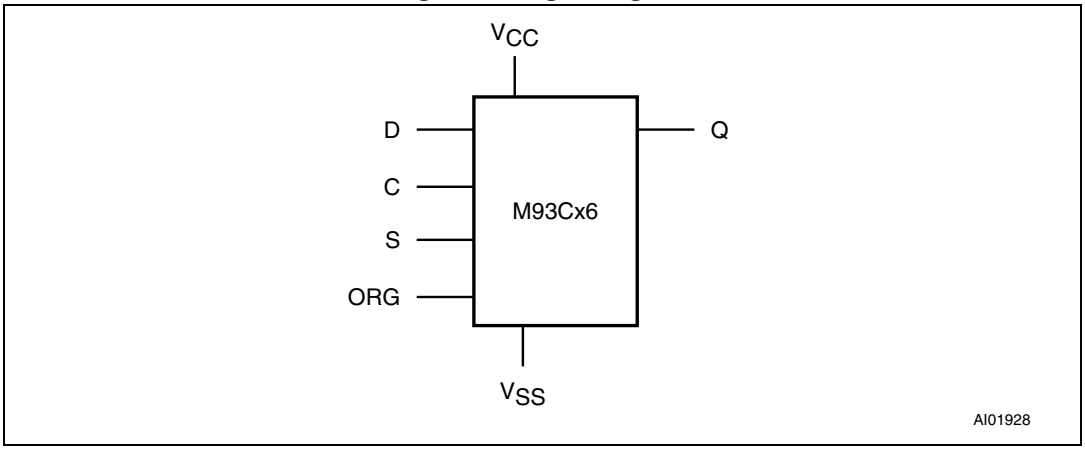


Table 3. Signal names

Signal name	Function	Direction
S	Chip Select	Input
D	Serial Data input	Input
Q	Serial Data output	Output
C	Serial Clock	Input
ORG	Organization Select	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

The M93Cx6-A125 is accessed by a set of instructions, as summarized in *Table 4*, and in more detail in *Table 5: Instruction set for the M93C46* to *Table 7: Instruction set for the M93C76 and M93C86*).

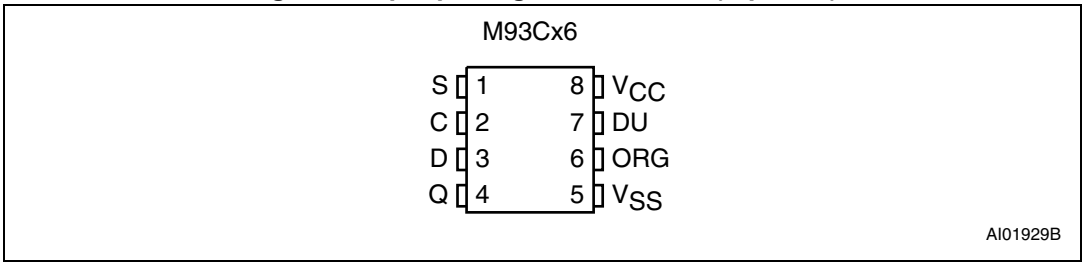
Table 4. Instruction set for the M93Cx6-A125

Instruction	Description	Data
READ	Read Data from Memory	Byte or Word
WRITE	Write Data to Memory	Byte or Word
WEN	Write Enable	-
WDS	Write Disable	-
ERASE	Erase Byte or Word	Byte or Word
ERAL	Erase All Memory	-
WRAL	Write All Memory with same Data	-

A Read Data from Memory (READ) instruction loads the address of the first byte or word to be read in an internal address register. The data at this address is then clocked out serially. The address register is automatically incremented after the data is output and, if Chip Select Input (S) is held High, the M93Cx6-A125 can output a sequential stream of data bytes or words. In this way, the memory can be read as a data stream from eight to 16384 bits long (in the case of the M93C86), or continuously (the address counter automatically rolls over to 00h when the highest address is reached).

Programming is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle) and does not require an Erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at a time into one of the byte or word locations of the M93Cx6-A125. After the start of the programming cycle, a Busy/Ready signal is available on Serial Data Output (Q) when Chip Select Input (S) is driven High. An internal Power-on Data Protection mechanism in the M93Cx6-A125 inhibits the device when the supply is too low.

Figure 2. 8-pin package connections (top view)



1. See *Section 12: Package mechanical data* for package dimensions, and how to identify pin-1.
2. DU = Don't Use. The DU (do not use) pin does not contribute to the normal operation of the device. It is reserved for use by STMicroelectronics during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}.

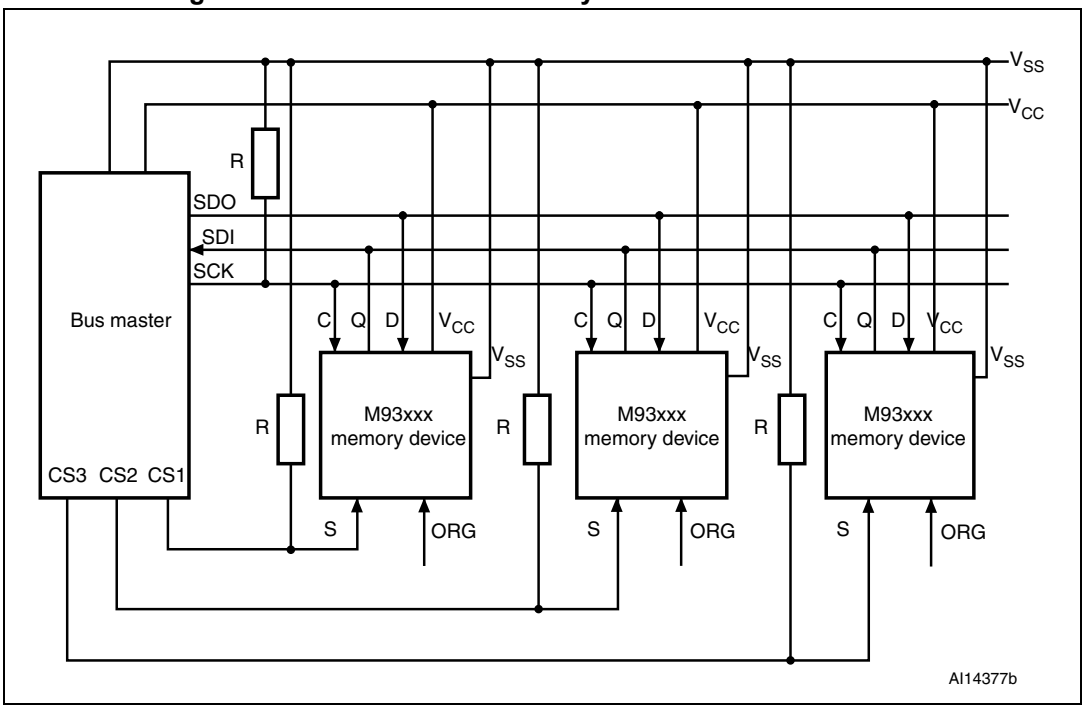
2 Connecting to the serial bus

Figure 3 shows an example of three memory devices connected to an MCU, on a serial bus. Only one device is selected at a time, so only one device drives the Serial Data output (Q) line at a time, the other devices are high impedance.

The pull-down resistor R (represented in *Figure 3*) ensures that no device is selected if the bus master leaves the S line in the high impedance state.

In applications where the bus master may be in a state where all inputs/outputs are high impedance at the same time (for example, if the bus master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the S line is pulled low): this ensures that C does not become high at the same time as S goes low, and so, that the t_{SLCH} requirement is met. The typical value of R is 100 kΩ

Figure 3. Bus master and memory devices on the serial bus



3 Operating features

3.1 Supply voltage (V_{CC})

3.1.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied. In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

3.1.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. During this time, the Chip Select (S) line is not allowed to float and should be driven to V_{SS}, it is therefore recommended to connect the S line to V_{SS} via a suitable pull-down resistor.

The V_{CC} rise time must not vary faster than 1 V/µs.

3.1.3 Power-up and device reset

In order to prevent inadvertent Write operations during power-up, a power on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the power on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in Operating conditions, in *Section 11: DC and AC parameters*).

When V_{CC} passes the POR threshold, the device is reset and is in the following state:

- Standby Power mode
- deselected (assuming that there is a pull-down resistor on the S line)

3.1.4 Power-down

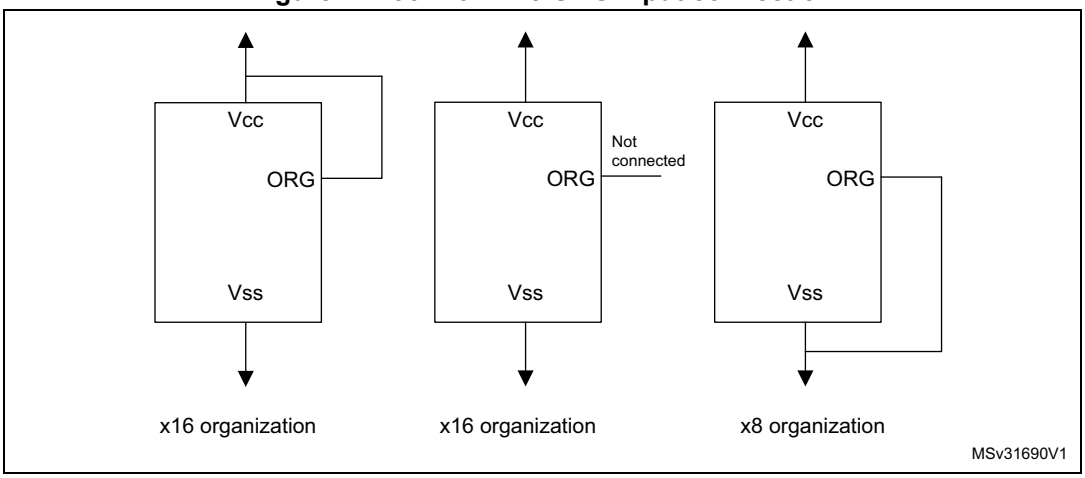
At power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops from the normal operating voltage to below the power on reset threshold voltage, the device stops responding to any instruction sent to it.

During power-down, the device must be deselected and in the Standby Power mode (that is, there should be no internal Write cycle in progress).

4 Memory organization

The M93Cx6-A125 memory is organized either as bytes (x8) or as words (x16). If Organization Select (ORG) is left unconnected (or connected to V_{CC}) the x16 organization is selected; when Organization Select (ORG) is connected to Ground (V_{SS}) the x8 organization is selected. When the M93Cx6-A125 is in Standby mode, Organization Select (ORG) should be set either to V_{SS} or V_{CC} to reach the device minimum power consumption (as any voltage between V_{SS} and V_{CC} applied to ORG input may increase the device Standby current).

Figure 4. M93Cx6-A125 ORG input connection



5 Instructions

The instruction set of the M93Cx6-A125 devices contains seven instructions, as summarized in *Table 5* to *Table 7*. Each instruction consists of the following parts, as shown in *Figure 5: READ, WRITE, WEN, WDS sequences*:

- Each instruction is preceded by a rising edge on Chip Select Input (S) with Serial Clock (C) being held low.
- A start bit, which is the first '1' read on Serial Data Input (D) during the rising edge of Serial Clock (C).
- Two op-code bits, read on Serial Data Input (D) during the rising edge of Serial Clock (C). (Some instructions also use the first two bits of the address to define the op-code).
- The address bits of the byte or word that is to be accessed. For the M93C46, the address is made up of 6 bits for the x16 organization or 7 bits for the x8 organization (see *Table 5*). For the M93C56 and M93C66, the address is made up of 8 bits for the x16 organization or 9 bits for the x8 organization (see *Table 6*). For the M93C76 and M93C86, the address is made up of 10 bits for the x16 organization or 11 bits for the x8 organization (see *Table 7*).

The M93Cx6-A125 devices are fabricated in CMOS technology and are therefore able to run as slow as 0 Hz (static input signals) or as fast as the maximum ratings specified in "AC characteristics" tables, in *Section 11: DC and AC parameters*.

Table 5. Instruction set for the M93C46

Instruction	Description	Start bit	Op-code	x8 origination (ORG = 0)			x16 origination (ORG = 1)		
				Address (1)	Data	Required clock cycles	Address (1)	Data	Required clock cycles
READ	Read Data from Memory	1	10	A6-A0	Q7-Q0	-	A5-A0	Q15-Q0	-
WRITE	Write Data to Memory	1	01	A6-A0	D7-D0	18	A5-A0	D15-D0	25
WEN	Write Enable	1	00	11X XXXX	-	10	11 XXXX	-	9
WDS	Write Disable	1	00	00X XXXX	-	10	00 XXXX	-	9
ERASE	Erase Byte or Word	1	11	A6-A0	-	10	A5-A0	-	9
ERAL	Erase All Memory	1	00	10X XXXX	-	10	10 XXXX	-	9
WRAL	Write All Memory with same Data	1	00	01X XXXX	D7-D0	18	01 XXXX	D15-D0	25

1. X = Don't Care bit.

Table 6. Instruction set for the M93C56 and M93C66

Instruction	Description	Start bit	Op-code	x8 origination (ORG = 0)			x16 origination (ORG = 1)		
				Address (1) (2)	Data	Required clock cycles	Address (1) (3)	Data	Required clock cycles
READ	Read Data from Memory	1	10	A8-A0	Q7-Q0	-	A7-A0	Q15-Q0	-
WRITE	Write Data to Memory	1	01	A8-A0	D7-D0	20	A7-A0	D15-D0	27
WEN	Write Enable	1	00	1 1XXX XXXX	-	12	11XX XXXX	-	11
WDS	Write Disable	1	00	0 0XXX XXXX	-	12	00XX XXXX	-	11
ERASE	Erase Byte or Word	1	11	A8-A0	-	12	A7-A0	-	11
ERAL	Erase All Memory	1	00	1 0XXX XXXX	-	12	10XX XXXX	-	11
WRAL	Write All Memory with same Data	1	00	0 1XXX XXXX	D7-D0	20	01XX XXXX	D15-D0	27

1. X = Don't Care bit.
2. Address bit A8 is not decoded by the M93C56.
3. Address bit A7 is not decoded by the M93C56.

Table 7. Instruction set for the M93C76 and M93C86

Instruction	Description	Start bit	Op-code	x8 Origination (ORG = 0)			x16 Origination (ORG = 1)		
				Address (1)(2)	Data	Required clock cycles	Address (1) (3)	Data	Required clock cycles
READ	Read Data from Memory	1	10	A10-A0	Q7-Q0	-	A9-A0	Q15-Q0	-
WRITE	Write Data to Memory	1	01	A10-A0	D7-D0	22	A9-A0	D15-D0	29
WEN	Write Enable	1	00	11X XXXX XXXX	-	14	11 XXXX XXXX	-	13
WDS	Write Disable	1	00	00X XXXX XXXX	-	14	00 XXXX XXXX	-	13
ERASE	Erase Byte or Word	1	11	A10-A0	-	14	A9-A0	-	13
ERAL	Erase All Memory	1	00	10X XXXX XXXX	-	14	10 XXXX XXXX	-	13
WRAL	Write All Memory with same Data	1	00	01X XXXX XXXX	D7-D0	22	01 XXXX XXXX	D15-D0	29

1. X = Don't Care bit.
2. Address bit A10 is not decoded by the M93C76.
3. Address bit A9 is not decoded by the M93C76.

5.1 Read Data from Memory

The Read Data from Memory (READ) instruction outputs data on Serial Data Output (Q). When the instruction is received, the op-code and address are decoded, and the data from the memory is transferred to an output shift register. A dummy 0 bit is output first, followed by the 8-bit byte or 16-bit word, with the most significant bit first. Output data changes are triggered by the rising edge of Serial Clock (C). The M93Cx6-A125 automatically increments the internal address register and clocks out the next byte (or word) as long as the Chip Select Input (S) is held High. In this case, the dummy 0 bit is *not* output between bytes (or words) and a continuous stream of data can be read (the address counter automatically rolls over to 00h when the highest address is reached).

5.2 Erase and Write data

5.2.1 Write Enable and Write Disable

The Write Enable (WEN) instruction enables the future execution of erase or write instructions, and the Write Disable (WDS) instruction disables it. When power is first applied, the M93Cx6-A125 initializes itself so that erase and write instructions are disabled. After a Write Enable (WEN) instruction has been executed, erasing and writing remains enabled until a Write Disable (WDS) instruction is executed, or until V_{CC} falls below the power-on reset threshold voltage. To protect the memory contents from accidental corruption, it is advisable to issue the Write Disable (WDS) instruction after every write cycle. The Read Data from Memory (READ) instruction is not affected by the Write Enable (WEN) or Write Disable (WDS) instructions.

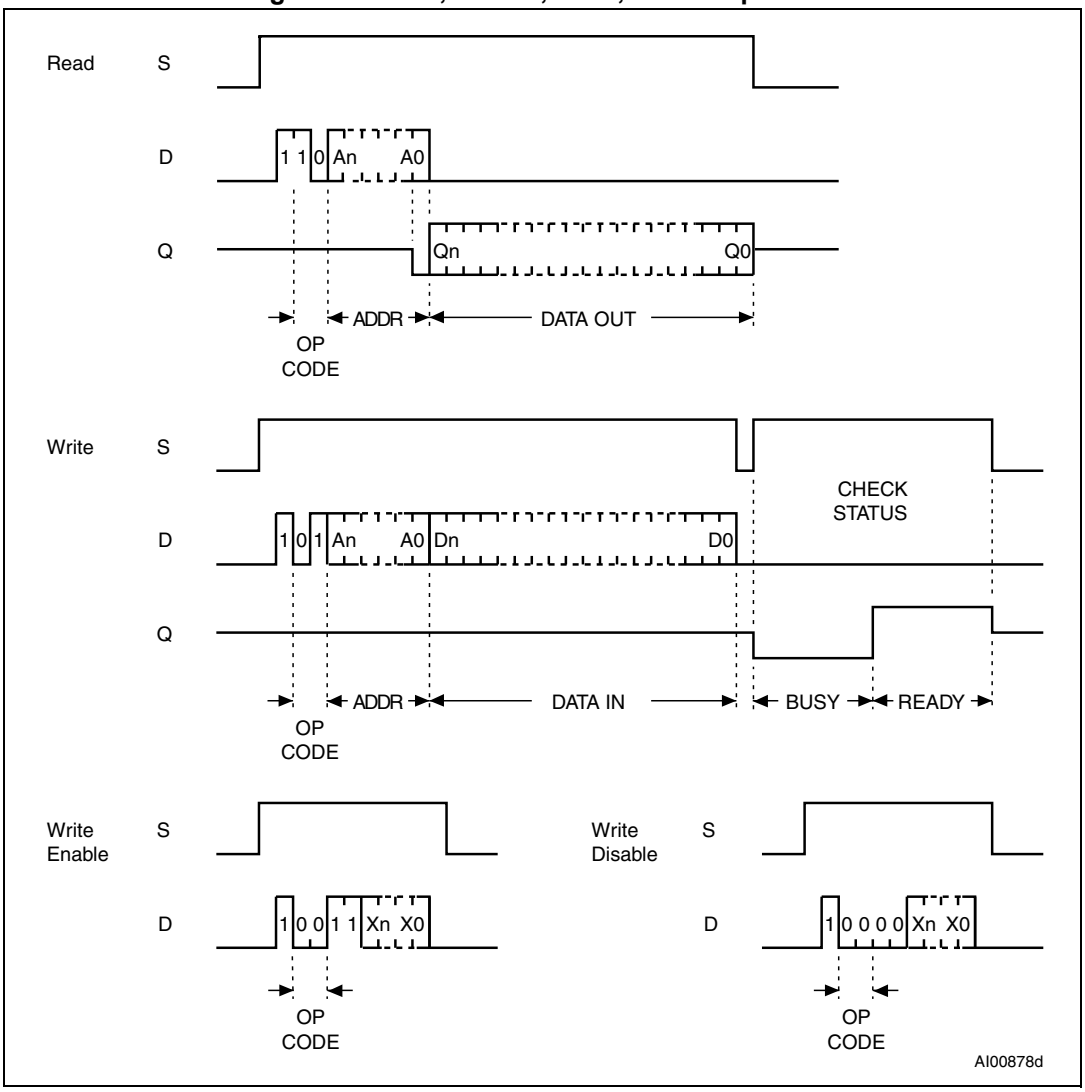
5.2.2 Write

For the Write Data to Memory (WRITE) instruction, 8 or 16 data bits follow the op-code and address bits. These form the byte or word that is to be written. As with the other bits, Serial Data Input (D) is sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, the Chip Select Input (S) must be taken low before the next rising edge of Serial Clock (C). If Chip Select Input (S) is brought low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed. The completion of the cycle can be detected by monitoring the READY/BUSY line, as described later in this document.

Once the Write cycle has been started, it is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle). The Write cycle is automatically preceded by an Erase cycle, so it is unnecessary to execute an explicit erase instruction before a Write Data to Memory (WRITE) instruction.

Figure 5. READ, WRITE, WEN, WDS sequences

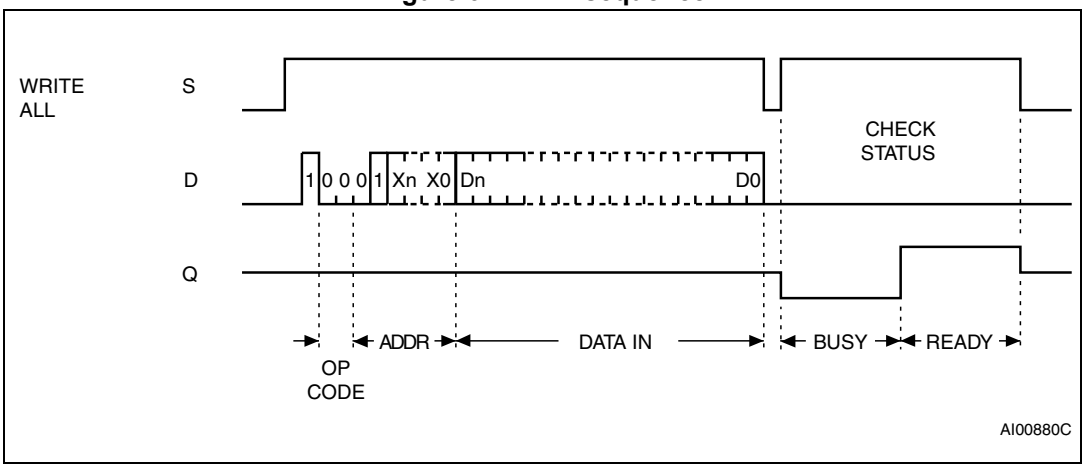


1. For the meanings of An, Xn, Qn and Dn, see *Table 5*, *Table 6* and *Table 7*.

5.2.3 Write All

As with the Erase All Memory (ERAL) instruction, the format of the Write All Memory with same Data (WRAL) instruction requires that a dummy address be provided. As with the Write Data to Memory (WRITE) instruction, the format of the Write All Memory with same Data (WRAL) instruction requires that an 8-bit data byte, or 16-bit data word, be provided. This value is written to all the addresses of the memory device. The completion of the cycle can be detected by monitoring the READY/$\overline{\text{BUSY}}$ line, as described next.

Figure 6. WRAL sequence



1. For the meanings of Xn and Dn, please see *Table 5*, *Table 6* and *Table 7*.

5.2.4 ECC (Error Correction Code) and Write cycling

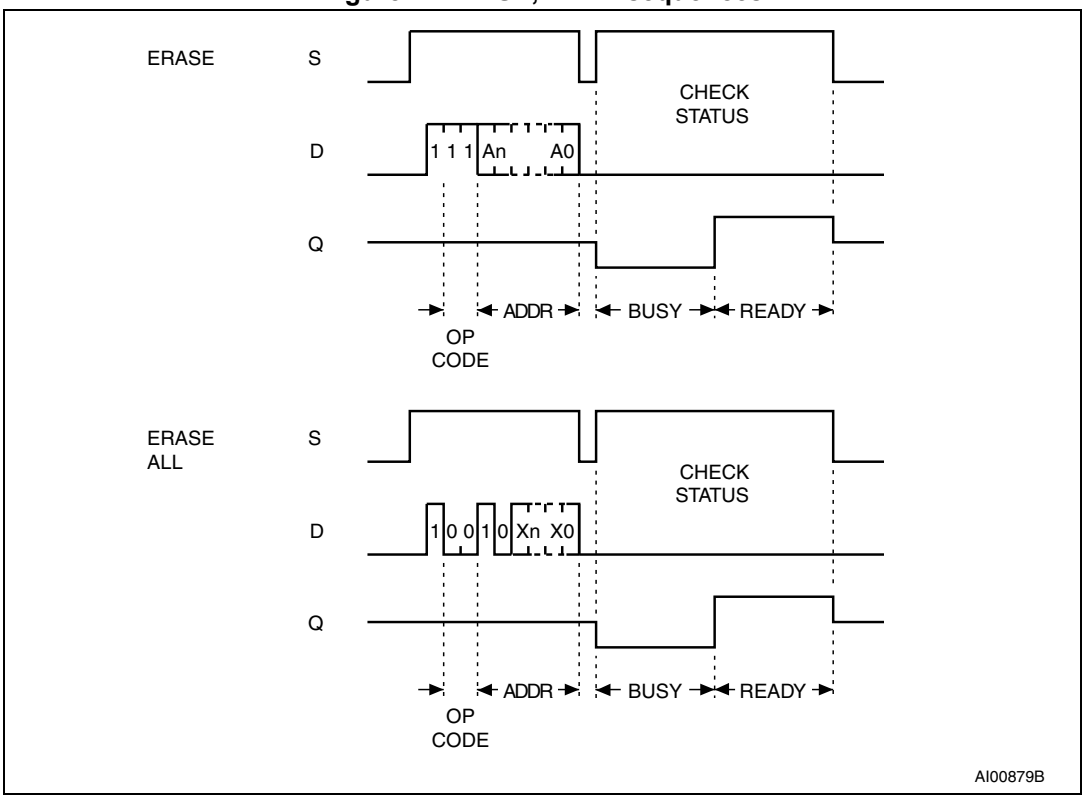
The devices identified with the Process letter “K” embed an Error Correction Code (ECC) internal logic function which is transparent for the Microwire communication protocol.

The ECC logic is implemented on each byte.

5.2.5 Erase Byte or Word

The Erase Byte or Word (ERASE) instruction sets the bits of the addressed memory byte (or word) to 1. Once the address has been correctly decoded, the falling edge of the Chip Select Input (S) starts the self-timed Erase cycle. The completion of the cycle can be detected by monitoring the READY/BUSY line, as described in *Section 6: READY/BUSY status*.

Figure 7. ERASE, ERAL sequences



1. For the meanings of An and Xn, please see *Table 5*, *Table 6* and *Table 7*.

5.2.6 Erase All

The Erase All Memory (ERAL) instruction erases the whole memory (all memory bits are set to 1). The format of the instruction requires that a dummy address be provided. The Erase cycle is conducted in the same way as the Erase instruction (ERASE). The completion of the cycle can be detected by monitoring the READY/BUSY line, as described in *Section 6: READY/BUSY status*.

6 READY/$\overline{\text{BUSY}}$ status

While the Write or Erase cycle is underway, for a WRITE, ERASE, WRAL or ERAL instruction, the Busy signal (Q=0) is returned whenever Chip Select input (S) is driven high. (Please note, though, that there is an initial delay, of t_{SLSH}, before this status information becomes available). In this state, the M93Cx6-A125 ignores any data on the bus. When the Write cycle is completed, and Chip Select Input (S) is driven high, the Ready signal (Q=1) indicates that the M93Cx6-A125 is ready to receive the next instruction. Serial Data Output (Q) remains set to 1 until the Chip Select Input (S) is brought low or until a new start bit is decoded.

7 Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

8 Common I/O operation

Serial Data Output (Q) and Serial Data Input (D) can be connected together, through a current limiting resistor, to form a common, single-wire data bus. Some precautions must be taken when operating the memory in this way, mostly to prevent a short circuit current from flowing when the last address bit (A0) clashes with the first data bit on Serial Data Output (Q). Please see the application note *AN394* for details.

9 Clock pulse counter

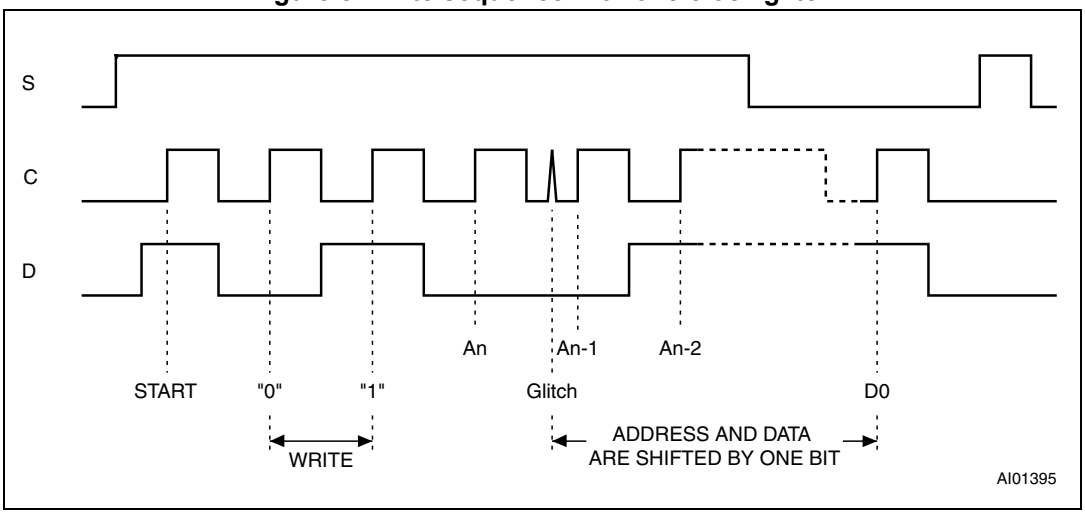
In a noisy environment, the number of pulses received on Serial Clock (C) may be greater than the number delivered by the master (the microcontroller). This can lead to a misalignment of the instruction of one or more bits (as shown in *Figure 8*) and may lead to the writing of erroneous data at an erroneous address.

To avoid this problem, the M93Cx6-A125 has an on-chip counter that counts the clock pulses from the start bit until the falling edge of the Chip Select Input (S). If the number of clock pulses received is not the number expected, the WRITE, ERASE, ERAL or WRAL instruction is aborted, and the contents of the memory are not modified.

The number of clock cycles expected for each instruction, and for each member of the M93Cx6-A125 family, are summarized in *Table 5: Instruction set for the M93C46* to *Table 7: Instruction set for the M93C76 and M93C86*. For example, a Write Data to Memory (WRITE) instruction on the M93C56 (or M93C66) expects 20 clock cycles (for the x8 organization) from the start bit to the falling edge of Chip Select Input (S). That is:

1 Start bit
+ 2 Op-code bits
+ 9 Address bits
+ 8 Data bits

Figure 8. Write sequence with one clock glitch



10 Maximum ratings

Stressing the device outside the ratings listed in the Absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_{OUT}	Output range (Q = V_{OH} or Hi-Z)	–0.50	V_{CC}+0.5	V
V_{IN}	Input range	–0.50	V_{CC}+1	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	-	4000	V

1. Compliant with JEDEC standard J-STD-020D (for small-body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).
2. Positive and negative pulses applied on pin pairs, according to the AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

11 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 9. Operating conditions (M93Cx6-A125)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	125	°C

Table 10. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
-	Input rise and fall times	-	50	ns
-	Input voltage levels	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input timing reference voltages	0.3 V_{CC} to 0.7 V_{CC}		V
-	Output timing reference voltages	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 9. AC testing input output waveforms

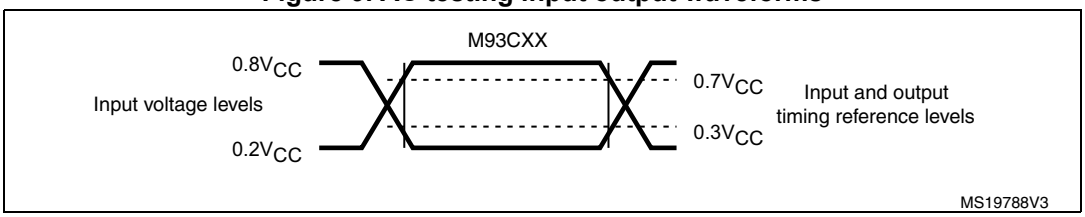


Table 11. Input and output capacitance

Symbol	Parameter	Test condition(1)	Min	Max	Unit
C_{OUT}	Output capacitance	V_{OUT} = 0V	-	8	pF
C_{IN}	Input capacitance	V_{IN} = 0V	-	6	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 1 MHz.

Table 12. Cycling performance by byte

Symbol	Parameter	Test condition	Min.	Max.	Unit
Ncycle	Write cycle endurance	TA ≤ 25 °C, 1.8 V < V_{CC} < 5.5 V	-	4,000,000	Write cycle(1)
		TA = 85 °C, 1.8 V < V_{CC} < 5.5 V	-	1,200,000	
		TA = 125 °C, 1.8 V < V_{CC} < 5.5 V	-	600,000	

1. A Write cycle is executed when either a Write, a Write All, an Erase or an Erase All instruction is decoded.

Table 13. DC characteristics

Symbol	Parameter	Test conditions (in addition to conditions specified in *Table 9*)	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}	-	2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}	-	2	
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open, f_C = 2 MHz	-	1	mA
		V_{CC} = 2.5 V, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open, f_C = 2 MHz	-	1	
		V_{CC} = 5.5 V, f_C = 2 MHz C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	1.5	
I_{CC0}(1)	Supply current (Write)	1.8 V ≤ V_{CC} < 5.5 V during t_W, $\overline{S} = V_{CC}$	-	1.5	mA
I_{CC1}	Supply current (Standby mode)	t° = 85 °C, V_{CC} = 1.8 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	1	µA
		t° = 85 °C, V_{CC} = 2.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	2	
		t° = 85 °C, V_{CC} = 5.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	3	
		t° = 125 °C, V_{CC} = 1.8 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	15	
		t° = 125 °C, V_{CC} = 2.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	15	
		t° = 125 °C, V_{CC} = 5.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	15	
V_{IL}	Input low voltage (D, C, S)	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} < 5.5 V	–0.45	0.3 V_{CC}	
V_{IH}	Input high voltage (D, C, S)	1.8 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+0.5	V
		2.5 V ≤ V_{CC} < 5.5 V	0.7 V_{CC}	V_{CC}+0.5	
V_{OL}	Output low voltage	V_{CC} = 1.8 V, I_{OL} = 1 mA	-	0.3	V
		V_{CC} ≥ 2.5 V, I_{OL} = 2.1 mA	-	0.4	
V_{OH}	Output high voltage	V_{CC} = 1.8 V, I_{OH} = 1 mA	0.8 V_{CC}	-	V
		V_{CC} ≥ 2.5 V, I_{OH} = -2.1 mA	0.8 V_{CC}	-	
V_{RES}	Internal reset threshold voltage	-	0.5	1.5	V

1. Average value during the Write cycle (t_W)

Table 14. AC characteristics

Test conditions specified in *Table 9* and *Table 10*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SK}	Clock frequency	D.C.	2	MHz
t_{SLCH}		Chip Select low to Clock high	50	-	ns
t_{SHCH}	t_{CSS}	Chip Select set-up time	50	-	ns
t_{SLSH}(1)	t_{CS}	Chip Select low to Chip Select high	200	-	ns
t_{CHCL}(2)	t_{SKH}	Clock high time	200	-	ns
t_{CLCH}(2)	t_{SKL}	Clock low time	200	-	ns
t_{DVCH}	t_{DIS}	Data in set-up time	50	-	ns
t_{CHDX}	t_{DIH}	Data in hold time	50	-	ns
t_{CLSH}	t_{SKS}	Clock set-up time (relative to S)	50	-	ns
t_{CLSL}	t_{CSH}	Chip Select hold time	0	-	ns
t_{SHQV}	t_{SV}	Chip Select to READY/$\overline{\text{BUSY}}$ status	-	200	ns
t_{SLQZ}(3)	t_{DF}	Chip Select low to output Hi-Z (V_{CC}>2.5 V)	-	100	ns
		Chip Select low to output Hi-Z (V_{CC}<2.5 V)	-	200	ns
t_{CHQL}	t_{PD0}	Delay to output low	-	200	ns
t_{CHQV}	t_{PD1}	Delay to output valid	-	200	ns
t_W	t_{WP}	Erase or Write cycle time	-	4	ms

1. Chip Select Input (S) must be brought low for a minimum of t_{SLSH} between consecutive instruction cycles.
2. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.
3. Value defined from characterization, not tested in production.

Figure 10. Synchronous timing (Start and op-code input)

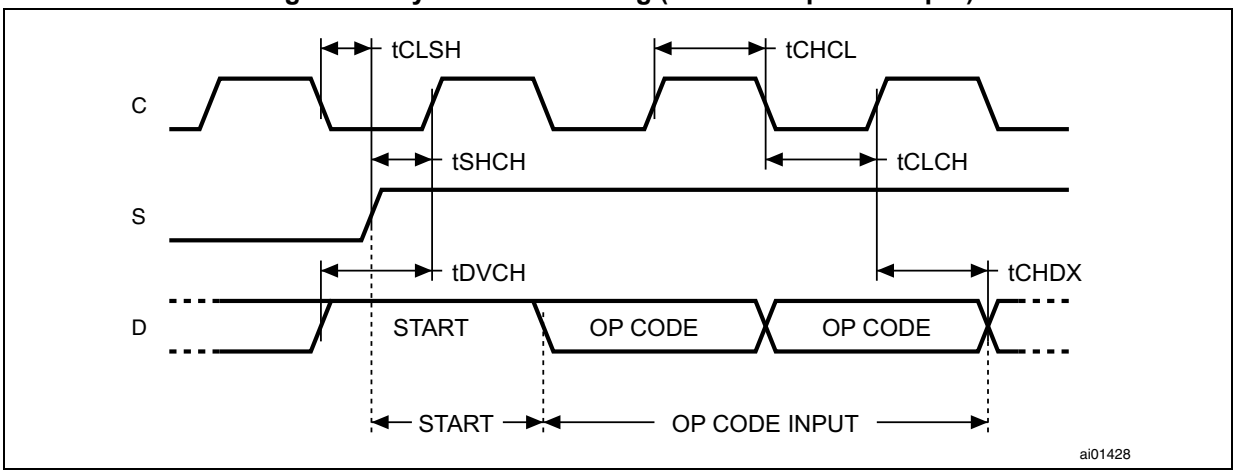


Figure 11. Synchronous timing (Read)

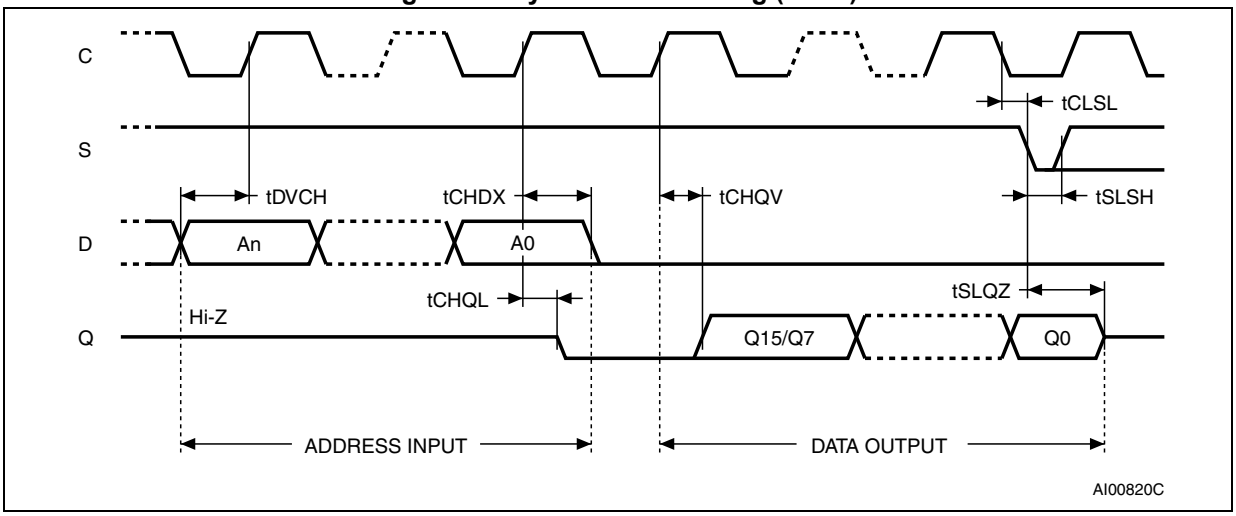
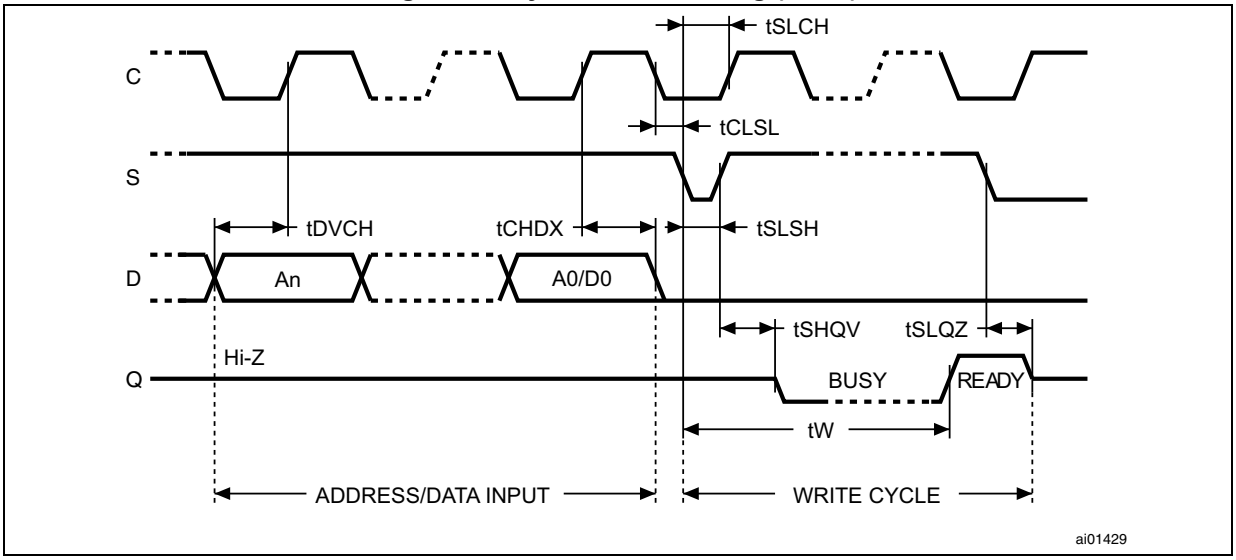


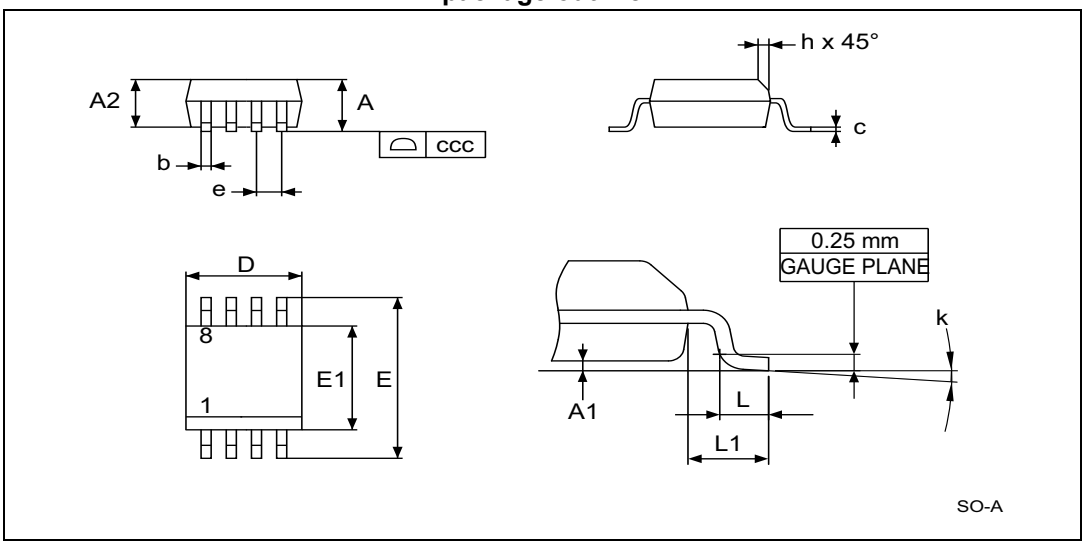
Figure 12. Synchronous timing (Write)



12 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 13. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package outline



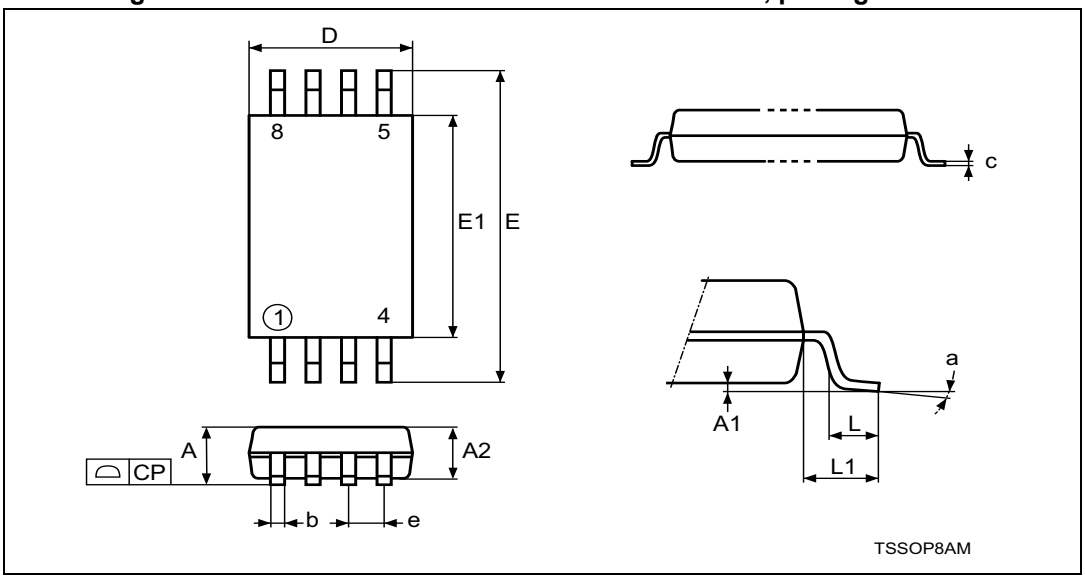
1. Drawing is not to scale.

Table 15. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	-	-	1.75	-	-	0.0689
A1	-	0.1	0.25	-	0.0039	0.0098
A2	-	1.25	-	-	0.0492	-
b	-	0.28	0.48	-	0.011	0.0189
c	-	0.17	0.23	-	0.0067	0.0091
ccc	-	-	0.1	-	-	0.0039
D	4.9	4.8	5	0.1929	0.189	0.1969
E	6	5.8	6.2	0.2362	0.2283	0.2441
E1	3.9	3.8	4	0.1535	0.1496	0.1575
e	1.27	-	-	0.05	-	-
h	-	0.25	0.5	-	0.0098	0.0197
k	-	0°	8°	-	0°	8°
L	-	0.4	1.27	-	0.0157	0.05
L1	1.04	-	-	0.0409	-	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 14. TSSOP8 – 8 lead thin shrink small outline, package outline



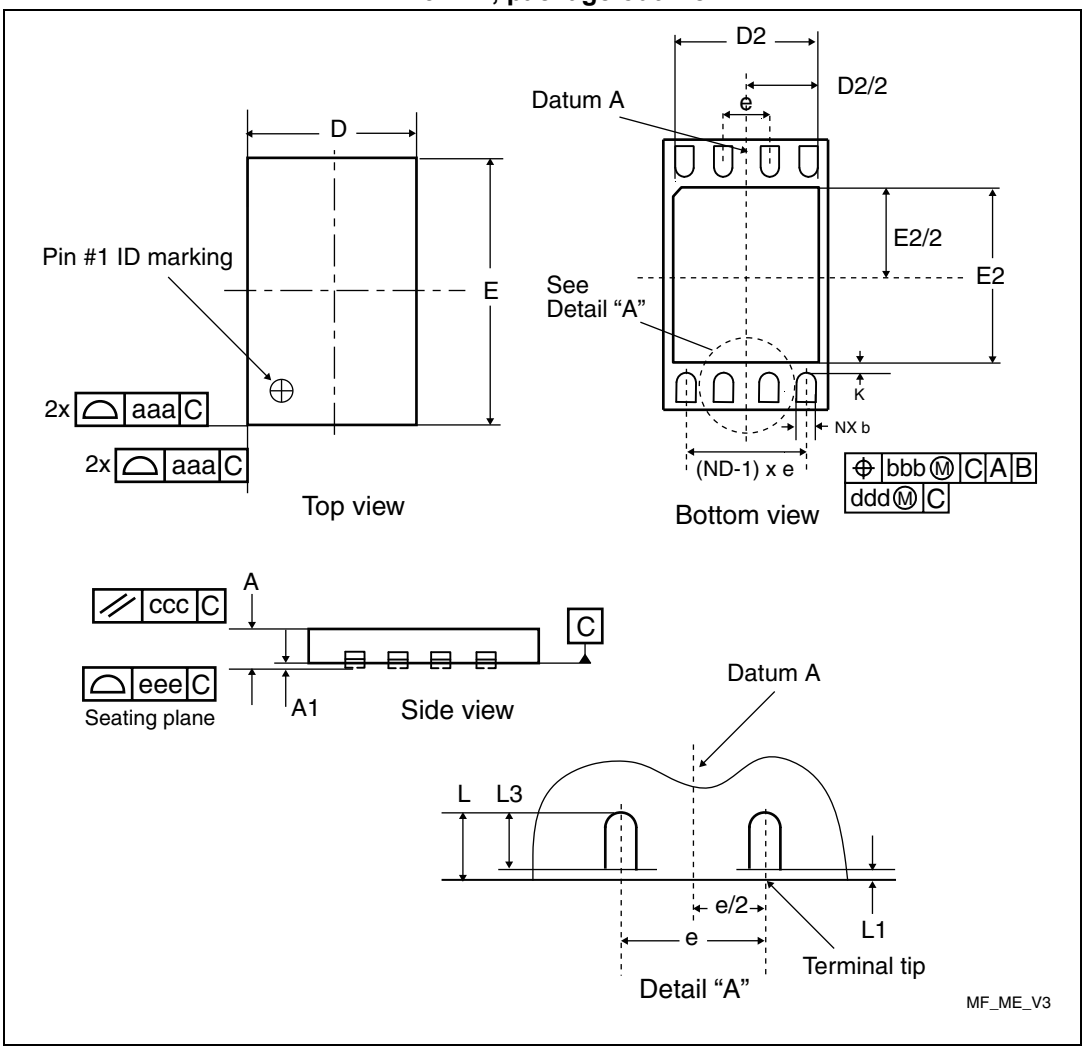
1. Drawing is not to scale.

Table 16. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	-	-	1.200	-	-	0.0472
A1	-	0.050	0.150	-	0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b	-	0.190	0.300	-	0.0075	0.0118
c	-	0.090	0.200	-	0.0035	0.0079
CP	-	-	0.100	-	-	0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000	-	-	0.0394	-	-
α	-	0°	8°	-	0°	8°
N	8			8		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 15. WFDFPN8 (MLP8) – 8-lead thin fine pitch dual flat package no lead 2 x 3 mm, package outline



1. Drawing is not to scale.

Table 17. WFDFPN8 (MLP8) – 8-lead thin fine pitch dual flat package no lead 2 x 3 mm, mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.750	0.700	0.800	0.0295	0.0276	0.0315
A1	0.045	0.025	0.065	0.0018	0.0010	0.0026
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.500			0.0197		
L1	-	-	0.150	-	-	0.0059
L3	-	0.300	-	-	0.0118	-
NX[2]	8					
ND[3]	4					
aaa	0.150			0.0059		
bbb	0.100			0.0039		
ccc	0.100			0.0039		
ddd	0.050			0.0020		
eee[4]	0.080			0.0031		
D2	-	1.050	1.450	-	0.0413	0.0571
E2	-	1.050	1.450	-	0.0413	0.0571
K	-	0.450	-	-	0.0177	-
L	-	0.300	0.500	-	0.0118	-

1. Values in inches are converted from mm and rounded to four decimal digits.
2. NX is the number of terminals.
3. ND is the number of terminals on “D” sides.
4. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

13 Part numbering

Table 18. Ordering information scheme

Example: M93C86 – R MN 3 T P /K

Device type

M93 = MICROWIRE serial EEPROM

Device function

86 = 16 Kbit (2048 x 8)

76 = 8 Kbit (1024 x 8)

66 = 4 Kbit (512 x 8)

56 = 2 Kbit (256 x 8)

46 = 1 Kbit (128 x 8)

Operating voltage

R = V_{CC} = 1.8 to 5.5 V

Package(1)

MN = SO8 (150 mils width)

DW = TSSOP8 (169 mils width)

MF = WFDFPN8 (2 x 3 mm)

Device grade

3 = Device tested with high reliability certified flow(2)
Automotive temperature range (–40 to 125 °C)

Packing

blank = standard packing

T = tape and reel packing

Plating technology

P = ECOPACK® (RoHS compliant)

Process

/K = Manufacturing technology code

1. All packages are ECOPACK2® (RoHS compliant and Halogen-free).
2. The high reliability certified flow (HRCF) is described in quality note QNEE9801. Please ask your nearest ST sales office for a copy.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

14 Revision history

Table 19. Document revision history

Date	Revision	Changes
15-Nov-2013	15	Removed Table 14 Cycling performance by byte
07-Aug-2013	1	Initial release
02-Dec-2013	2	Document status changed from “Preliminary data” to “Production data”. Updated: – *Features*: “data retention” bullet – *Table 9: Operating conditions (M93Cx6-A125)* – “T_{SLQZ}” row in *Table 14: AC characteristics* – Note (1) under *Table 8: Absolute maximum ratings* – *Table 13: DC characteristics* – *Figure 15: WFDFPN8 (MLP8) – 8-lead thin fine pitch dual flat package no lead 2 x 3 mm, package outline*. Renamed *Figure 11: Synchronous timing (Read)* and *Figure 12: Synchronous timing (Write)*.

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