

LV5232VH

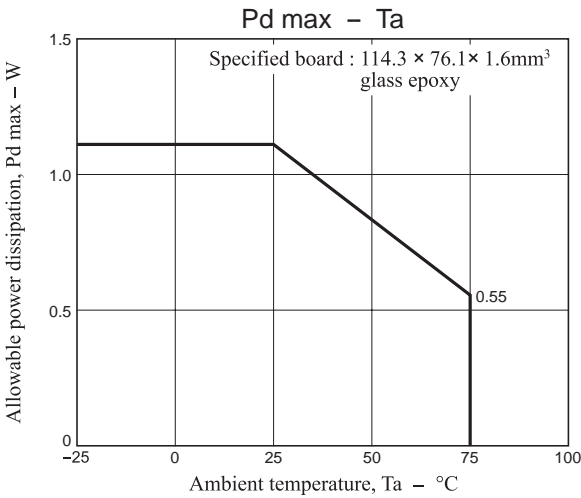
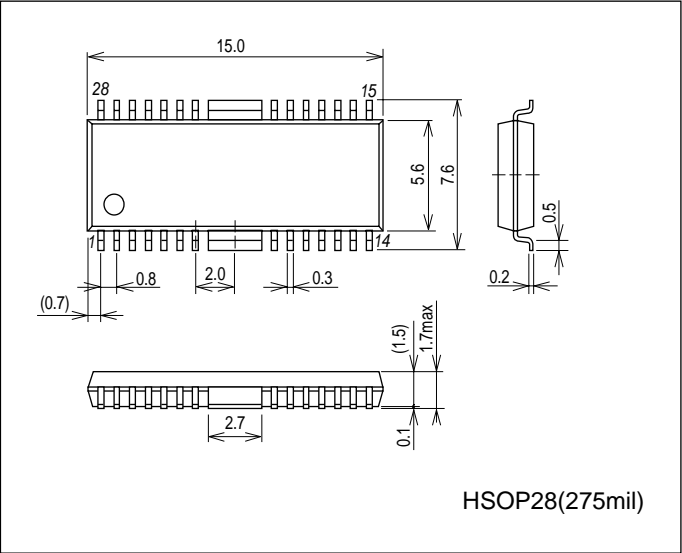
Electrical Characteristics at Ta = 25°C, VCC = 5.0V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|--------|---------------------------|-----------|------|-----------|------|
| | | | min | typ | max | |
| Quiescent current drain | ICC1 | LEDO driver off (standby) | | 30 | 40 | μA |
| LEDO output on resistance | Ron | IO = 30mA | | 5 | | Ω |
| OFF leak current | Ileak | VO = 42V | | 0 | 10 | μA |
| Driver output malfunction prevention voltage | Vt | | 2.58 | 2.70 | 2.82 | V |
| Control circuit block | | | | | | |
| H level 1 | VINH1 | Input H level | VCC × 0.8 | | | V |
| L level 1 | VINL1 | Input L level | 0 | | VCC × 0.2 | V |
| H level 2 | VOUTH1 | SOUT IO = -1mA | VCC - 0.3 | | | V |
| L level 2 | VOURL1 | SOUT IO = 1mA | 0 | | 0.3 | V |

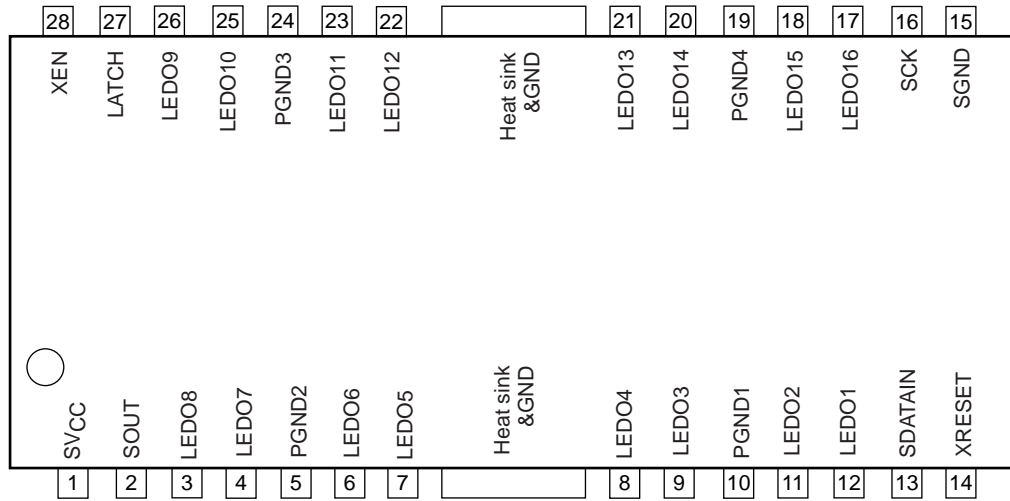
Package Dimensions

unit : mm (typ)

3222A



Pin Assignment

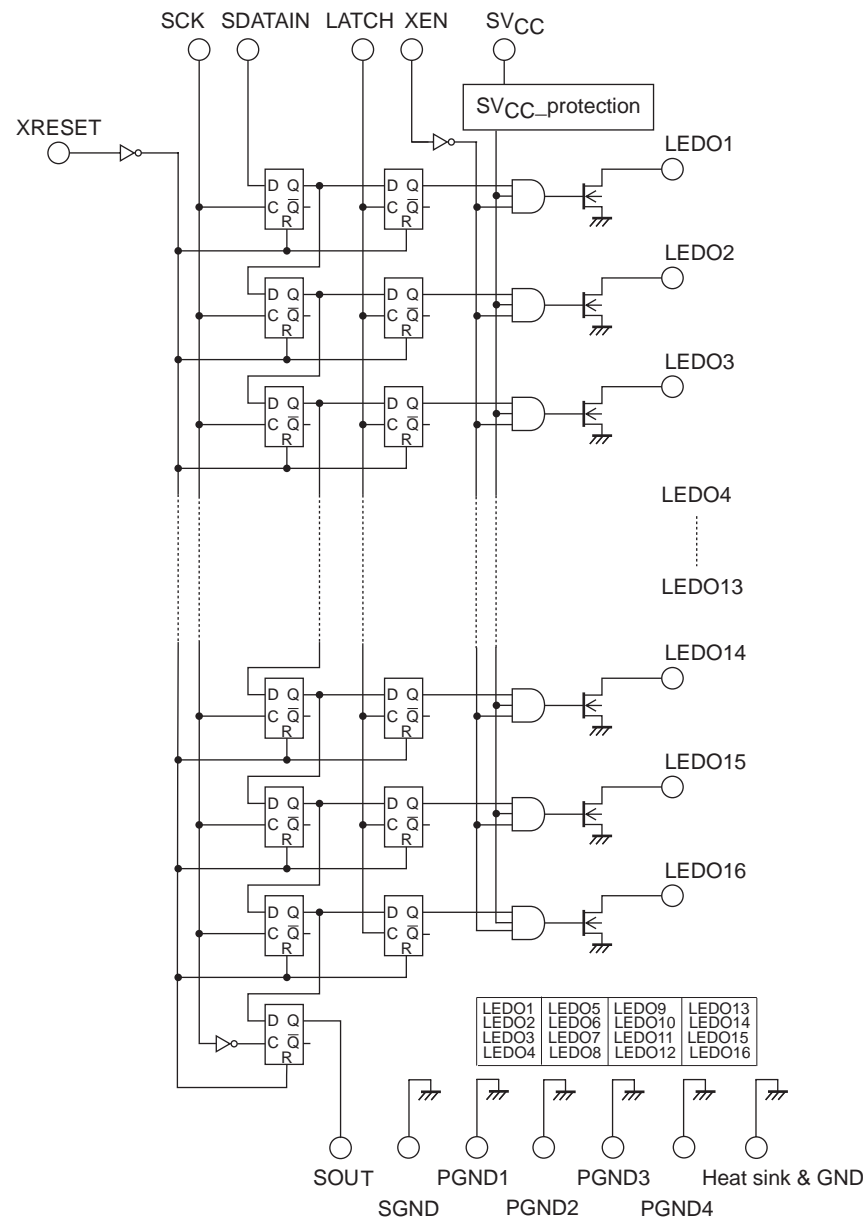


Top view

Pin Descriptions

| Pin No. | Pin name | I/O | Description |
|-----------|----------|-----|--|
| 1 | SVCC | | Power supply |
| 2 | SOUT | O | shift register output (final-stage shift register) |
| 3 | LEDO8 | O | LEDO8 Latch output (LEDO8 of shift register) |
| 4 | LEDO7 | O | LEDO7 Latch output (LEDO7 of shift register) |
| 5 | PGND2 | | GND |
| 6 | LEDO6 | O | LEDO6 Latch output (LEDO6 of shift register) |
| 7 | LEDO5 | O | LEDO5 Latch output (LEDO5 of shift register) |
| Heat sink | | | |
| 8 | LEDO4 | O | LEDO4 Latch output (LEDO4 of shift register) |
| 9 | LEDO3 | O | LEDO3 Latch output (LEDO3 of shift register) |
| 10 | PGND1 | | GND |
| 11 | LEDO2 | O | LEDO2 Latch output (LEDO2 of shift register) |
| 12 | LEDO1 | O | LEDO1 Latch output (LEDO1 of shift register) |
| 13 | SDATAIN | I | Serial Input |
| 14 | XRESET | I | Reset input (shift register and latch) |
| 15 | SGND | | GND |
| 16 | SCK | I | Clock input (for shift register) |
| 17 | LEDO16 | O | LEDO16 Latch output (LEDO16 of shift register) |
| 18 | LEDO15 | O | LEDO15 Latch output (LEDO15 of shift register) |
| 19 | PGND4 | | GND |
| 20 | LEDO14 | O | LEDO14 Latch output (LEDO14 of shift register) |
| 21 | LEDO13 | O | LEDO13 Latch output (LEDO13 of shift register) |
| Heat sink | | | |
| 22 | LEDO12 | O | LEDO12 Latch output (LEDO12 of shift register) |
| 23 | LEDO11 | O | LEDO11 Latch output (LEDO11 of shift register) |
| 24 | PGND3 | | GND |
| 25 | PGND10 | O | LEDO10 Latch output (LEDO10 of shift register) |
| 26 | PGND9 | O | LEDO9 Latch output (LEDO9 of shift register) |
| 27 | LATCH | I | Latch input When the latch input is held low, the LED0 output status is retained. When a high-level is input, the LED0 outputs change when the status of the shift register changes. |
| 28 | XEN | I | Enable inputs (LEDO1 to LEDO16) When a high-level is input, all the LED0 outputs are turned off. When a low-level is input, the shift register data is output to LED0. |

Block Diagram



LV5232VH

Pin Functions

| Pin No. | Pin Name | Pin function | Equivalent Circuit |
|--|---|---------------------------------|--|
| 13 16 | SDATAIN SCK | Pull-down input | |
| 14 27 28 | XRESET LATCH XEN | Pull-up input | |
| 2 | SOUT | SOUT output | |
| 3 4 6 7 8 9 11 12 17 18 20 21 22 23 25 26 | LEDO8 LEDO7 LEDO6 LEDO5 LEDO4 LEDO3 LEDO2 LEDO1 LEDO16 LEDO15 LEDO14 LEDO13 LEDO12 LEDO11 LEDO10 LEDO9 | LEDO outputs LEDO1 to LEDO16 | <p>LEDO1/LEDO2/LEDO3/LEDO4/ LEDO5/LEDO6/LEDO7/LEDO8/ LEDO9/LEDO10/LEDO11/LEDO12/ LEDO13/LEDO14/LEDO15/LEDO16</p> |

Function

The LV5232VH consists of 1) an 16-stage D-type flip-flop and 2) an 16-stage D-type flip-flop connected to the output of 1). When data is supplied to the serial data input (SDATAIN) and the clock pulse is supplied to the clock input (SCK), the serial data input signal is input to the internal shift register and the data already in the shift register shifted sequentially when the clock changes from low to high.

The serial output (SOUT) is used to connect multiple LV5232VH to expand the number of bits and is connected to the SDATAIN of the next stage. (Cascade connection supported.)

For parallel output, when the output control enable input (XEN) is low, the latch input (LATCH) changes from low to high and the clock pulse input changes from low to high, the serial data input signal is output to LEDO1, and the output is shifted sequentially. For parallel outputs (LEDO2 to LEDO16), the signals whose polarities inverted from those of the serial data input (SDATAIN) are output.

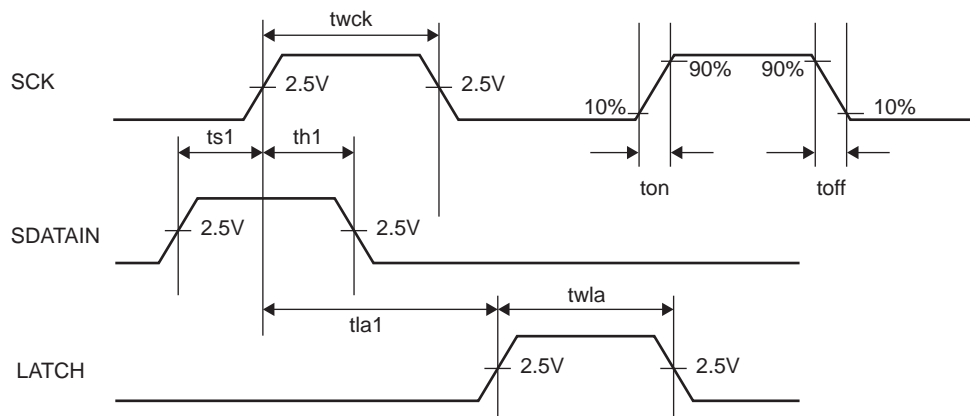
When the EN input is high, outputs LEDO1 through LEDO16 all turn off.

When the reset input is low, outputs LEDO1 through LEDO16 and SOUT outputs all turn off. The power must be turned on after checking that the reset input is low.

To prevent the malfunction, the output load protection circuit is built into. The output of LEDO1 to LEDO16 is compulsorily turned off when becoming below the voltage with a constant there is V_{CC} .

Timing conditions

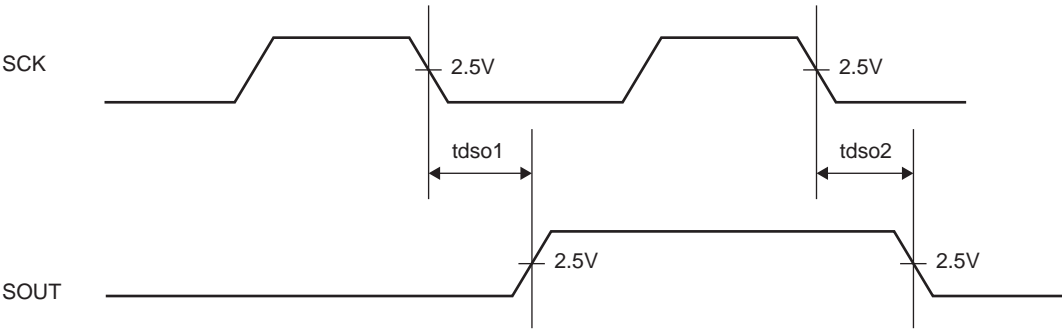
| Parameter | symbol | Conditions | min | typ | max | unit |
|--------------------|--------|--|-----|-----|-----|------|
| Clock frequency | fs1 | SCK Duty = 50% | | | 10 | MHz |
| Clock pulse width | twck | SCK | 50 | | | ns |
| Latch pulse width | twla | LATCH | 50 | | | ns |
| Data set up time | ts1 | SDATAIN setup time relative to the rise of SCK | 25 | | | ns |
| Data hold time | th1 | SDATAIN data hold time relative to the rise of SCK | 25 | | | ns |
| Clock latch time | tla1 | | 100 | | | ns |
| Input conditions 1 | ton | SCK and SDATAIN rise time | | | 100 | ns |
| Input conditions 2 | toff | SCL and SDATAIN fall time | | | 100 | ns |



LV5232VH

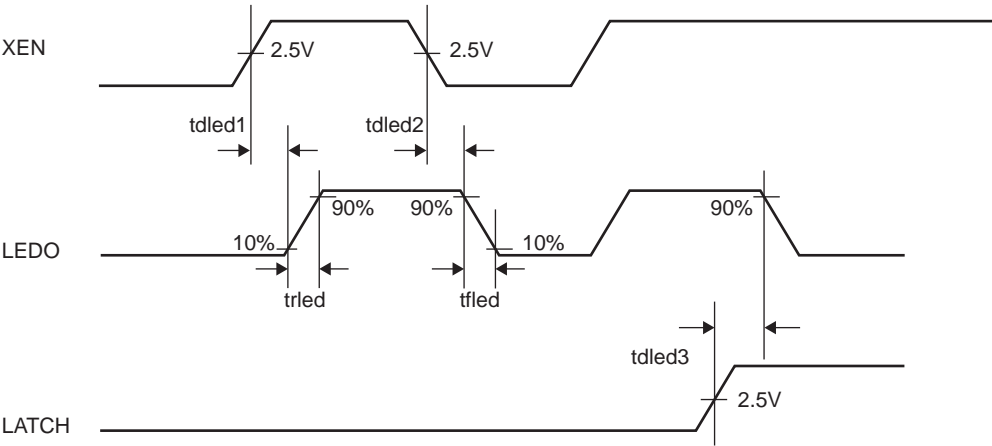
SOUT output timings

| Parameter | symbol | Conditions | min | typ | max | unit |
|-------------------|--------|---|-----|-----|-----|------|
| SOUT delay time 1 | tdso1 | The time from a SCK falling edge to SOUT rising edge | | | 50 | MHz |
| SOUT delay time 2 | tdso2 | The time from a SCK falling edge to SOUT falling edge | | | 50 | ns |

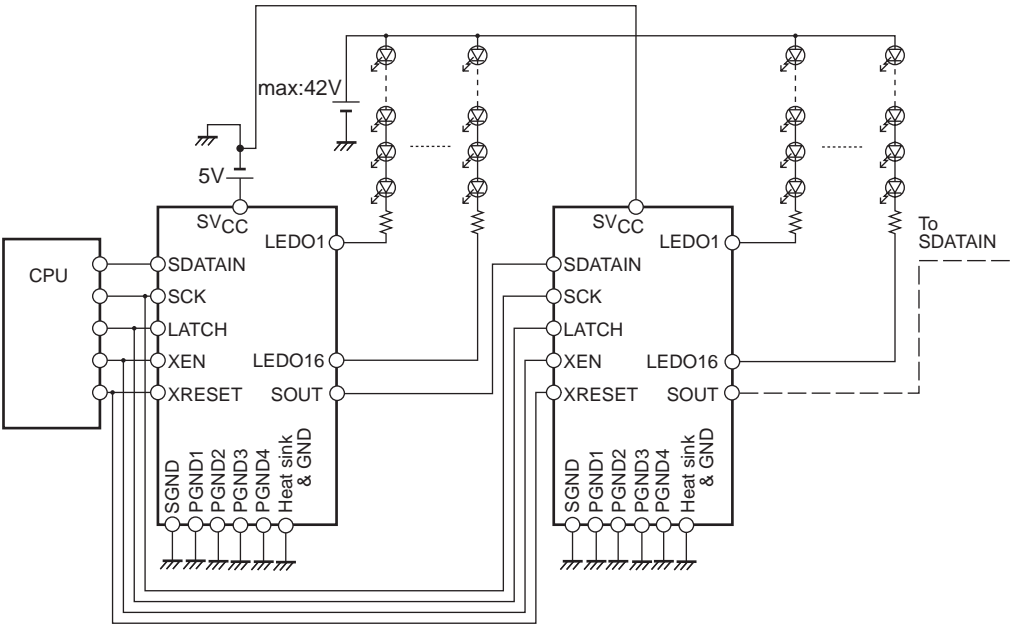


LEDO output timings

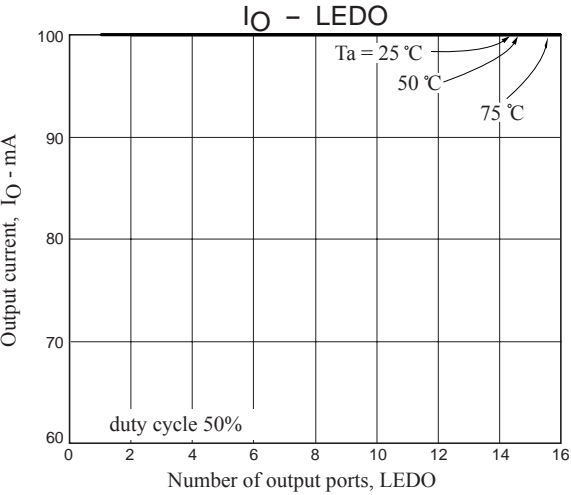
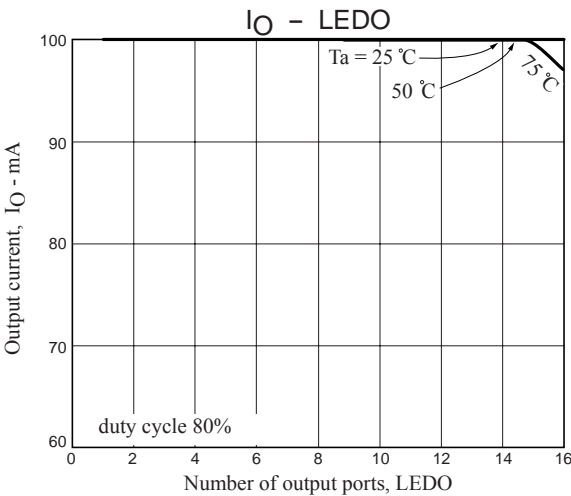
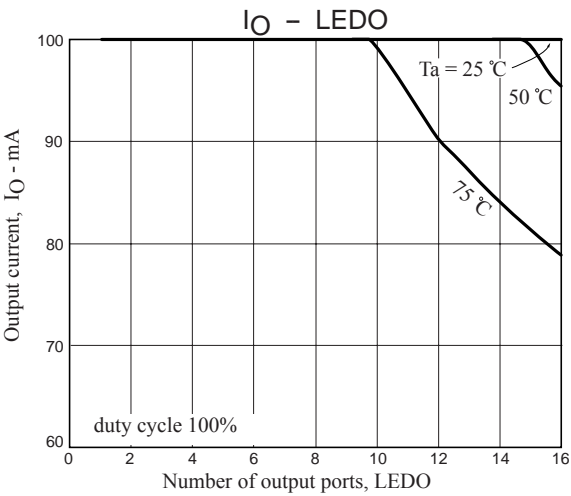
| Parameter | symbol | Conditions | min | typ | max | unit |
|-------------------|--------|---|-----|-----|-----|------|
| LEDO delay time 1 | tdled1 | The time from an XEN rising edge to LEDO rising edge $CL = 30pF, I_O = 100mA, V_O = 42V$ | | 100 | | ns |
| LEDO delay time 2 | tdled2 | The time from an XEN falling edge to LEDO falling edge $CL = 30pF, I_O = 100mA, V_O = 42V$ | | 100 | | ns |
| LEDO rise time | trled | LEDO rise time $CL = 30pF, I_O = 100mA, V_O = 42V$ | | 200 | | ns |
| LEDO fall time | tfled | LEDO fall time $CL = 30pF, I_O = 100mA, V_O = 42V$ | | 200 | | ns |
| LEDO delay time 3 | tdled3 | The time from a LATCH rising edge to LEDO falling edge $CL = 30pF, I_O = 100mA, V_O = 42V$ | | 200 | | ns |



Application Circuit Example



Temperature properties graph



ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|----------------|---|--------------------------|
| LV5232VH-TLM-H | HSOP28 (275mil) (Pb-Free / Halogen Free) | 2000 / Tape & Reel |
| LV5232VH-MPB-H | HSOP28 (275mil) (Pb-Free / Halogen Free) | 30 / Fan-Fold |

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