Notes: 1. Derate linearly 0.2 W/°C for T_C > +25 °C.

2. The following formula derives the maximum theoretical I_D limit. I_D is also limited by package and internal wires and may be limited due to pin diameter.

$$I_D = \sqrt{\frac{T_J\,(max) - T_C}{R_{\theta JC} \times R_{DS(on)} @ T_J\,(max)}}$$

3. I_{DM} = 4 x I_{D1} as calculated in note 1.

MECHANICAL and PACKAGING

- CASE: Ceramic LCC-18 with kovar gold plated lid.
- TERMINALS: Gold plating over nickel.
- MARKING: Manufacturer's ID, part number, date code, ESD symbol at Pin 1 location.
- TAPE & REEL option: Standard per EIA-481-D. Consult factory for quantities.
- See Package Dimensions on last page.

PART NOMENCLATURE

JAN 2N6796 U

Reliability Level
JAN = JAN Level
JANTX = JANTX Level
JANTXV = JANTXV Level
JANS = JANS level (2N6798)
Blank = Commercial

JEDEC type number
(see Electrical Characteristics table)

Surface Mount package

SYMBOLS & DEFINITIONS

Symbol	Definition
di/dt	Rate of change of diode current while in reverse-recovery mode, recorded as maximum value.
I_F	Forward current
R_G	Gate drive impedance
V_{DD}	Drain supply voltage
V_{DS}	Drain source voltage, dc
V_{GS}	Gate source voltage, dc

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage					
V_{GS} = 0 V, I_D = 1.0 mA	2N6796U	$V_{(BR)DSS}$	100		V
	2N6798U		200		
	2N6800U		400		
	2N6802U		500		
Gate-Source Voltage (Threshold)					
$V_{DS} \geq V_{GS}$, I_D = 0.25 mA		$V_{GS(th)1}$	2.0	4.0	V
$V_{DS} \geq V_{GS}$, I_D = 0.25 mA, T_J = +125°C		$V_{GS(th)2}$	1.0		
$V_{DS} \geq V_{GS}$, I_D = 0.25 mA, T_J = -55°C		$V_{GS(th)3}$		5.0	
Gate Current					
V_{GS} = ± 20 V, V_{DS} = 0 V		I_{GSS1}		±100	nA
V_{GS} = ± 20 V, V_{DS} = 0 V, T_J = +125°C		I_{GSS2}		±200	
Drain Current					
V_{GS} = 0 V, V_{DS} = 80 V	2N6796U	I_{DSS1}		25	µA
V_{GS} = 0 V, V_{DS} = 160 V	2N6798U				
V_{GS} = 0 V, V_{DS} = 320 V	2N6800U				
V_{GS} = 0 V, V_{DS} = 400 V	2N6802U				
Drain Current					
V_{GS} = 0 V, V_{DS} = 80 V, T_J = +125 °C	2N6796U	I_{DSS2}		0.25	mA
V_{GS} = 0 V, V_{DS} = 160 V, T_J = +125 °C	2N6798U				
V_{GS} = 0 V, V_{DS} = 320 V, T_J = +125 °C	2N6800U				
V_{GS} = 0 V, V_{DS} = 400 V, T_J = +125 °C	2N6802U				
Static Drain-Source On-State Resistance					
V_{GS} = 10 V, I_D = 5.0 A pulsed	2N6796U	$r_{DS(on)1}$		0.18	Ω
V_{GS} = 10 V, I_D = 3.5 A pulsed	2N6798U			0.40	
V_{GS} = 10 V, I_D = 2.0 A pulsed	2N6800U			1.00	
V_{GS} = 10 V, I_D = 1.5 A pulsed	2N6802U			1.50	
Static Drain-Source On-State Resistance					
V_{GS} = 10 V, I_D = 8.0 A pulsed	2N6796U	$r_{DS(on)2}$		0.195	Ω
V_{GS} = 10 V, I_D = 5.5 A pulsed	2N6798U			0.420	
V_{GS} = 10 V, I_D = 3.0 A pulsed	2N6800U			1.100	
V_{GS} = 10 V, I_D = 2.5 A pulsed	2N6802U			1.600	
Static Drain-Source On-State Resistance					
T_J = +125°C					
V_{GS} = 10 V, I_D = 5.0 A pulsed	2N6796U	$r_{DS(on)3}$		0.35	Ω
V_{GS} = 10 V, I_D = 3.5 A pulsed	2N6798U			0.75	
V_{GS} = 10 V, I_D = 2.0 A pulsed	2N6800U			2.40	
V_{GS} = 10 V, I_D = 1.5 A pulsed	2N6802U			3.50	
Diode Forward Voltage					
V_{GS} = 0 V, I_D = 8.0 A pulsed	2N6796U	V_{SD}		1.5	V
V_{GS} = 0 V, I_D = 5.5 A pulsed	2N6798U			1.4	
V_{GS} = 0 V, I_D = 3.0 A pulsed	2N6800U			1.4	
V_{GS} = 0 V, I_D = 2.5 A pulsed	2N6802U			1.4	

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted (continued)

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Gate Charge:					
On-State Gate Charge		$Q_{g(on)}$			nC
V_{GS} = 10 V, I_D = 8.0 A, V_{DS} = 50 V	2N6796U			28.51	
V_{GS} = 10 V, I_D = 5.5 A, V_{DS} = 50 V	2N6798U			42.07	
V_{GS} = 10 V, I_D = 3.0 A, V_{DS} = 50 V	2N6800U			34.75	
V_{GS} = 10 V, I_D = 2.5 A, V_{DS} = 50 V	2N6802U			33.00	
Gate to Source Charge		Q_{gs}			nC
V_{GS} = 10 V, I_D = 8.0 A, V_{DS} = 50 V	2N6796U			6.34	
V_{GS} = 10 V, I_D = 5.5 A, V_{DS} = 50 V	2N6798U			5.29	
V_{GS} = 10 V, I_D = 3.0 A, V_{DS} = 50 V	2N6800U			5.75	
V_{GS} = 10 V, I_D = 2.5 A, V_{DS} = 50 V	2N6802U			4.46	
Gate to Drain Charge		Q_{gd}			nC
V_{GS} = 10 V, I_D = 8.0 A, V_{DS} = 50 V	2N6796U			16.59	
V_{GS} = 10 V, I_D = 5.5 A, V_{DS} = 50 V	2N6798U			28.11	
V_{GS} = 10 V, I_D = 3.0 A, V_{DS} = 50 V	2N6800U			16.59	
V_{GS} = 10 V, I_D = 2.5 A, V_{DS} = 50 V	2N6802U			28.11	

SWITCHING CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Turn-on delay time		$t_{d(on)}$		30	ns
I_D = 8.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 30 V	2N6796U				
I_D = 5.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 77 V	2N6798U				
I_D = 3.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 176 V	2N6800U				
I_D = 2.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 225 V	2N6802U				
Rinse time		t_r			ns
I_D = 8.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 30 V	2N6796U			75	
I_D = 5.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 77 V	2N6798U			50	
I_D = 3.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 176 V	2N6800U			35	
I_D = 2.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 225 V	2N6802U			30	
Turn-off delay time		$t_{d(off)}$			ns
I_D = 8.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 30 V	2N6796U			40	
I_D = 5.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 77 V	2N6798U			50	
I_D = 3.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 176 V	2N6800U			55	
I_D = 2.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 225 V	2N6802U			55	
Fall time		t_f			ns
I_D = 8.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 30 V	2N6796U			45	
I_D = 5.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 77 V	2N6798U			40	
I_D = 3.0 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 176 V	2N6800U			35	
I_D = 2.5 A, V_{GS} = +10 V, R_G = 7.5 Ω, V_{DD} = 225 V	2N6802U			30	
Diode Reverse Recovery Time		t_{rr}			ns
di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 8.0 A	2N6796U			300	
di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 5.5 A	2N6798U			500	
di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 3.0 A	2N6800U			700	
di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 2.5 A	2N6802U			900	

GRAPHS

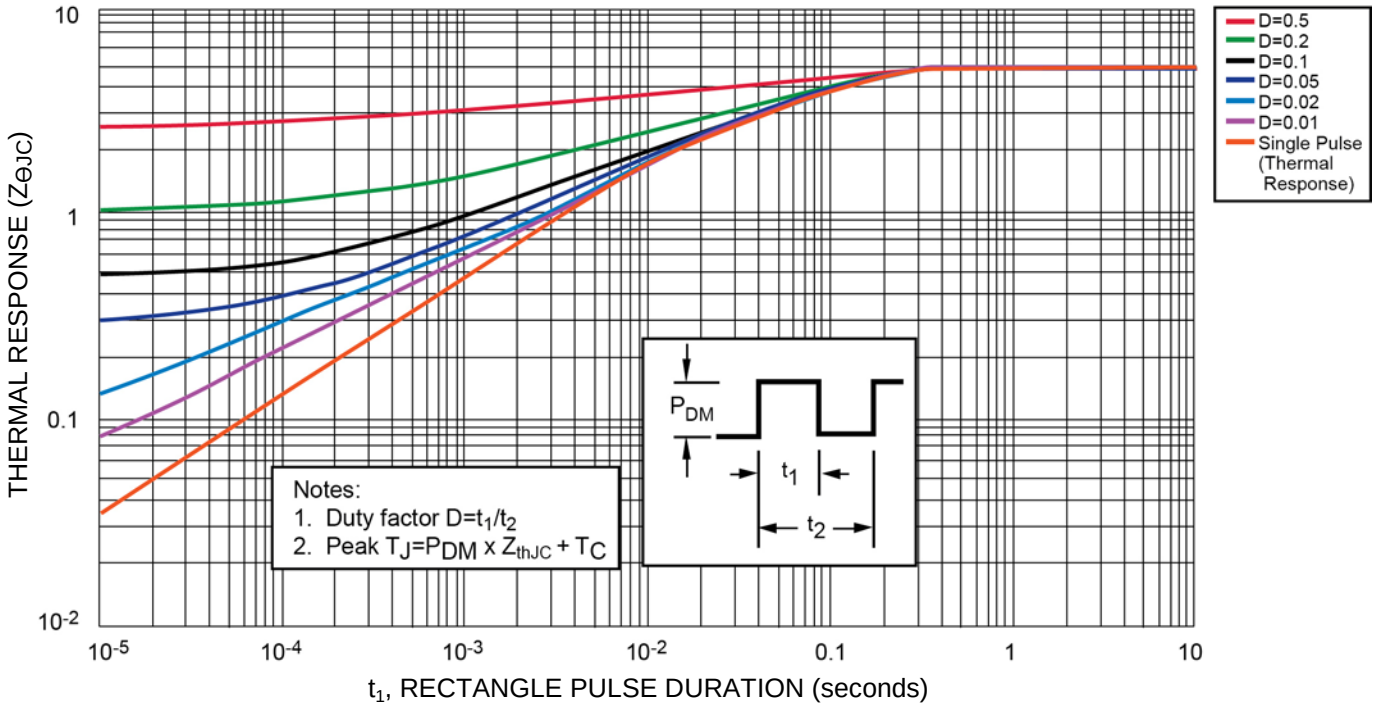
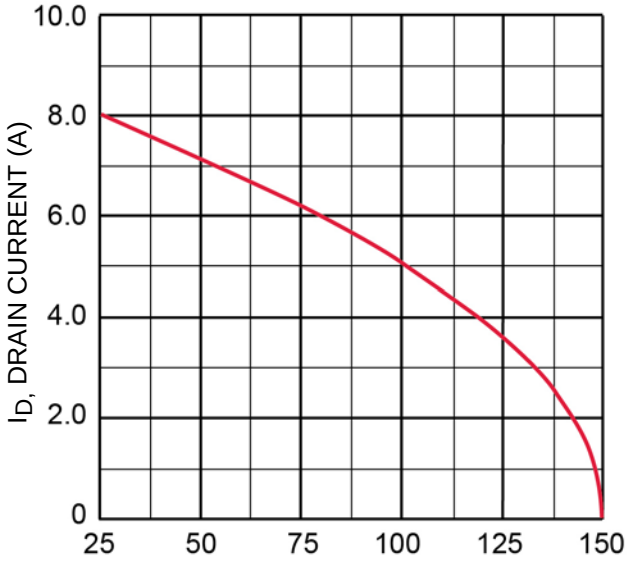


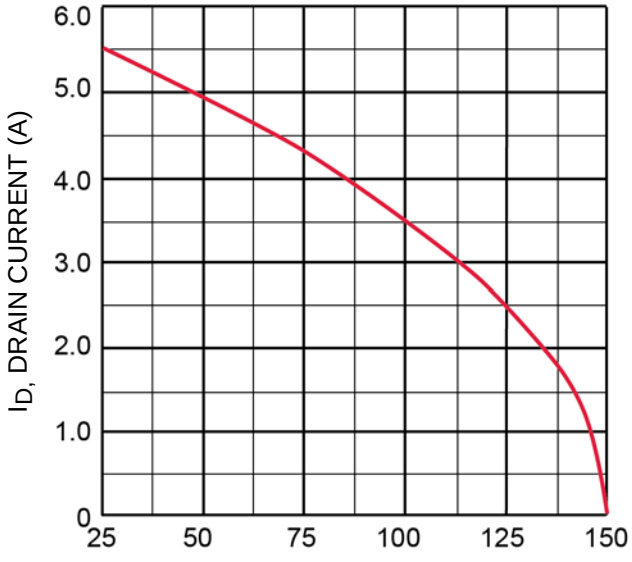
FIGURE 1 – Normalized Transient Thermal Impedance

GRAPHS (continued)

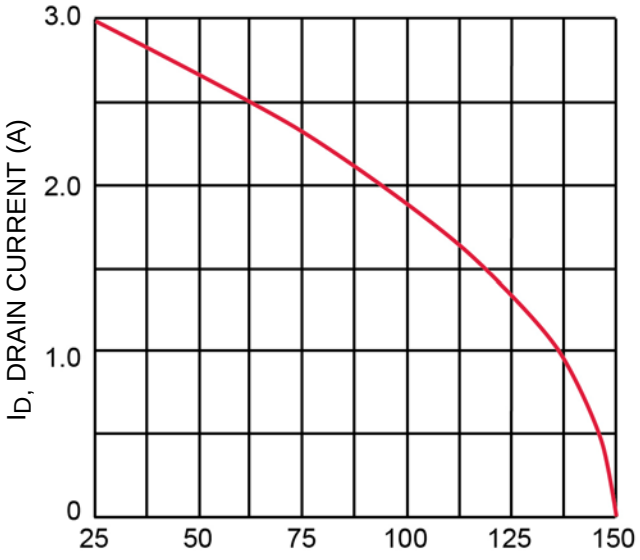
FIGURE 2 – Maximum Drain Current vs Case Temperature Graphs



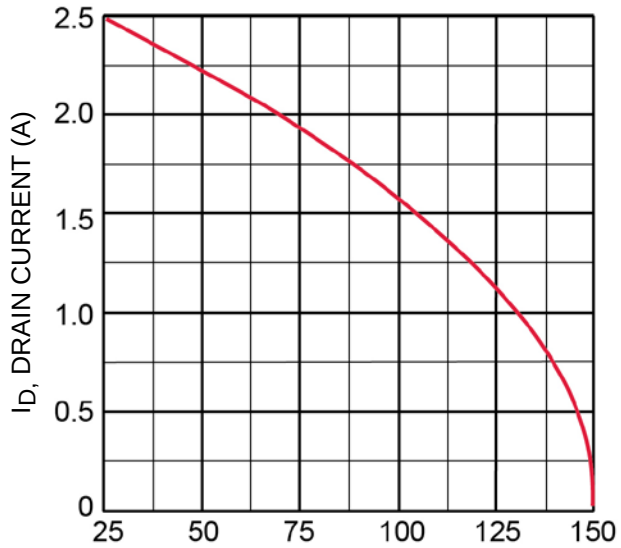
For 2N6796U



For 2N6798U



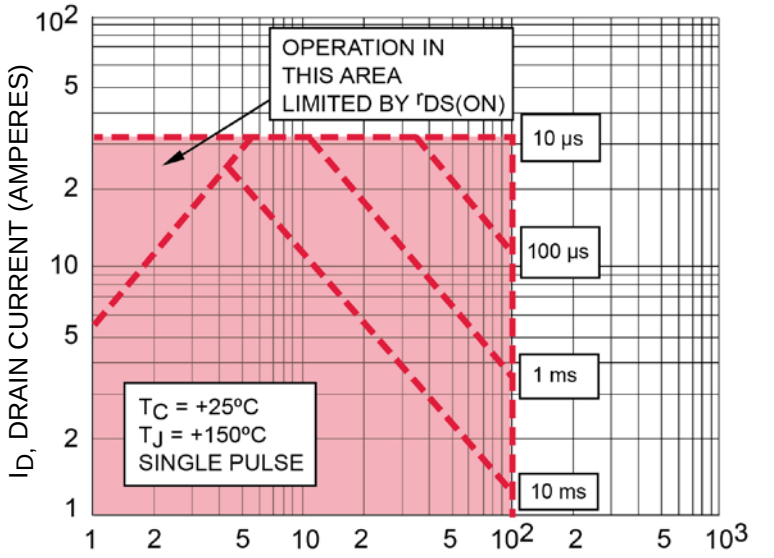
For 2N6800U

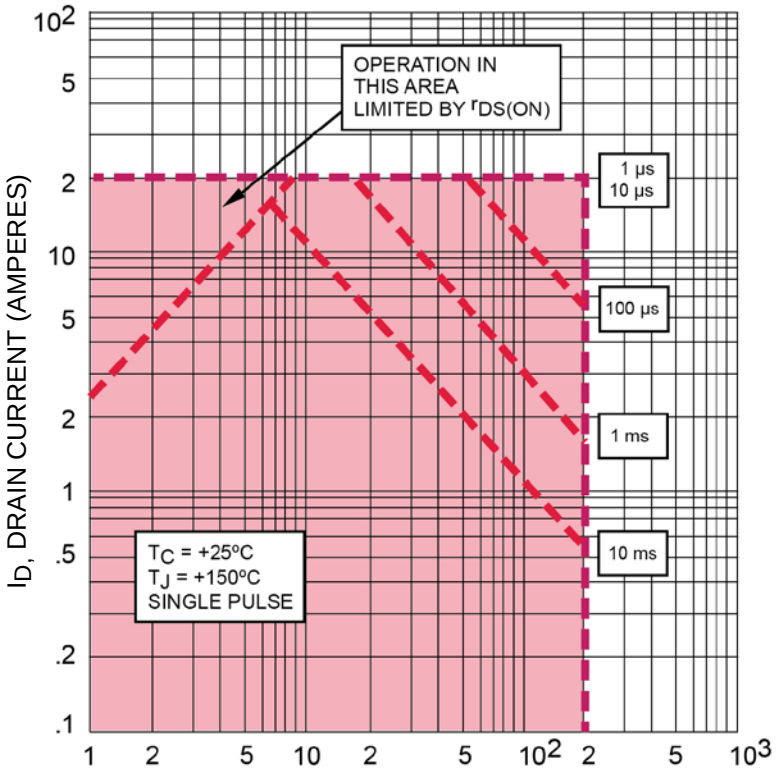


For 2N6802U

GRAPHS (continued)

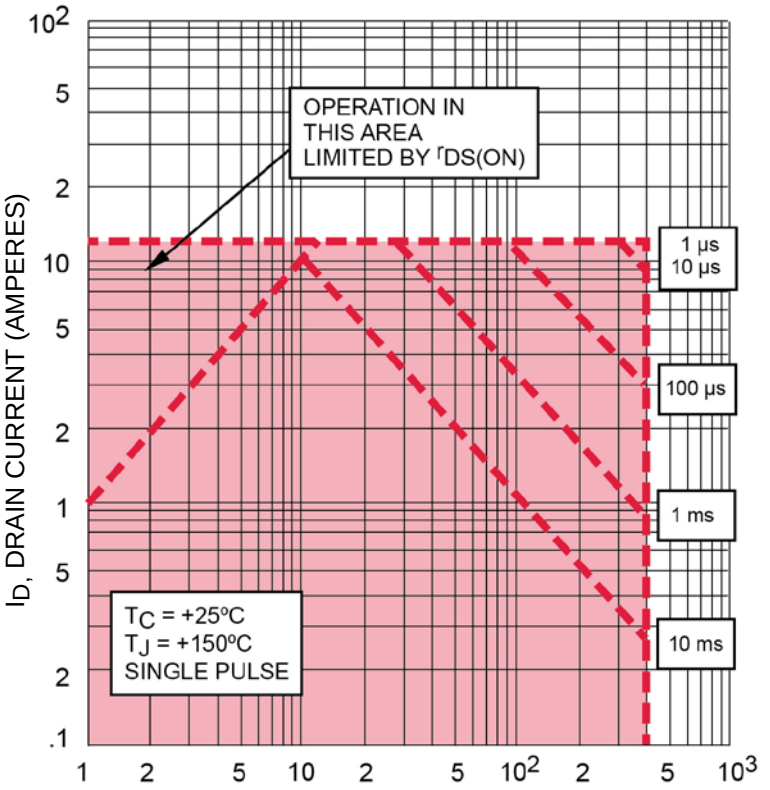
FIGURE 3 – Maximum Safe Operating Area

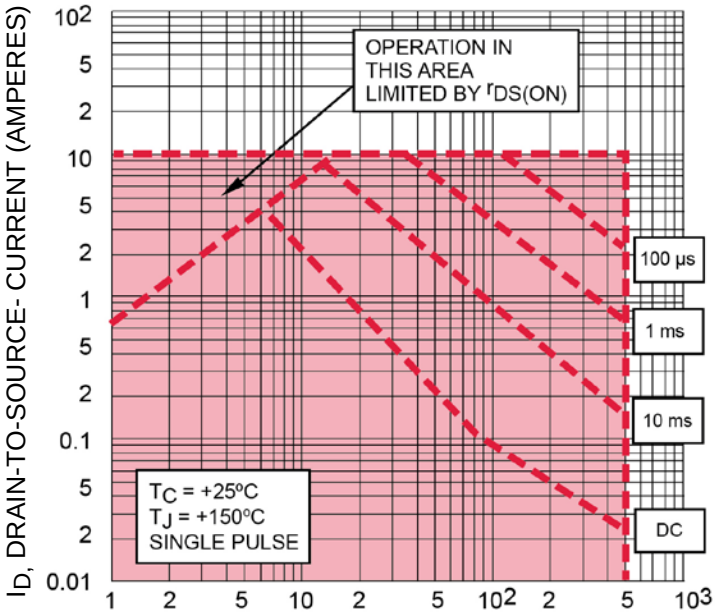




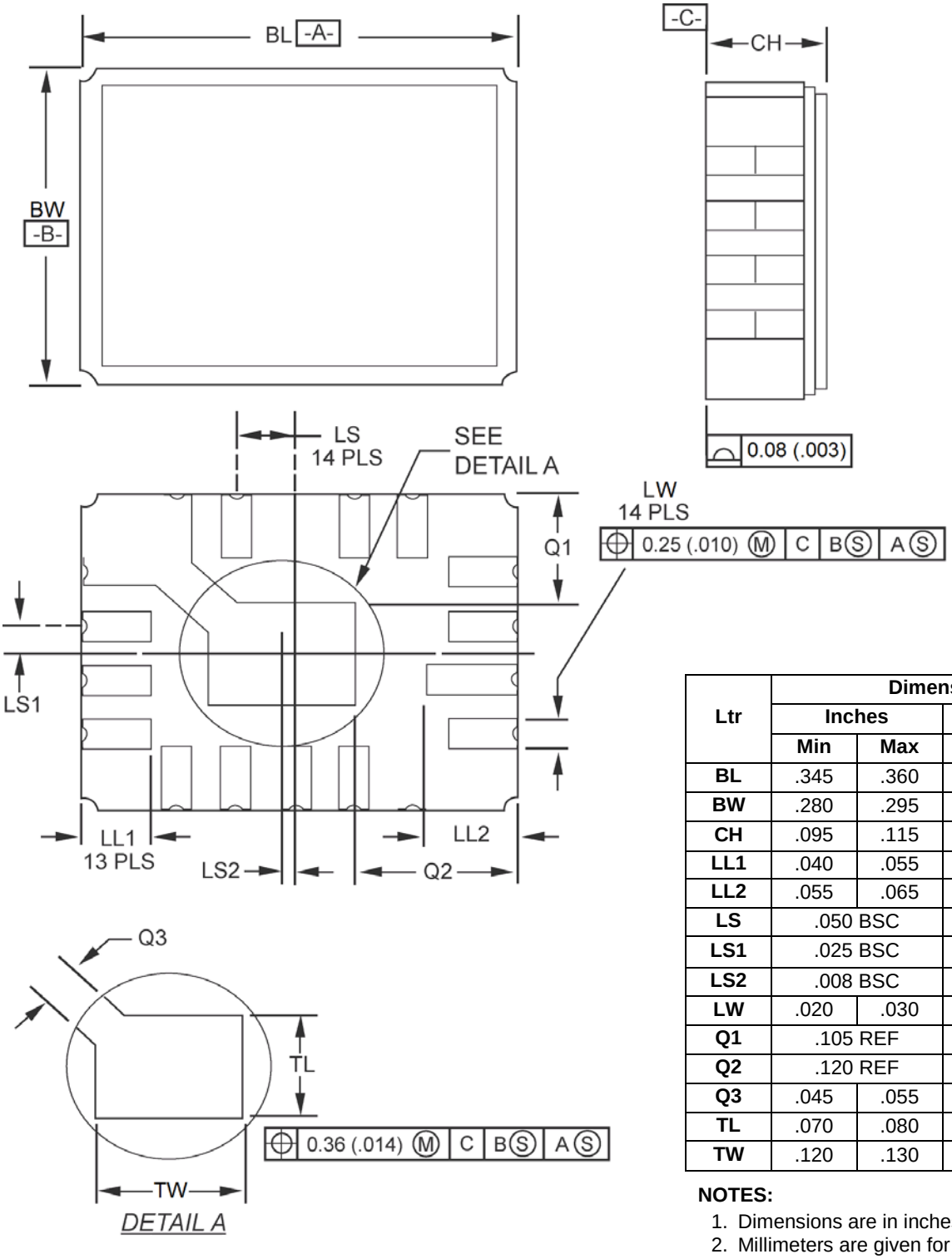
GRAPHS (continued)

FIGURE 3 – Maximum Safe Operating Area (continued)





PACKAGE DIMENSIONS

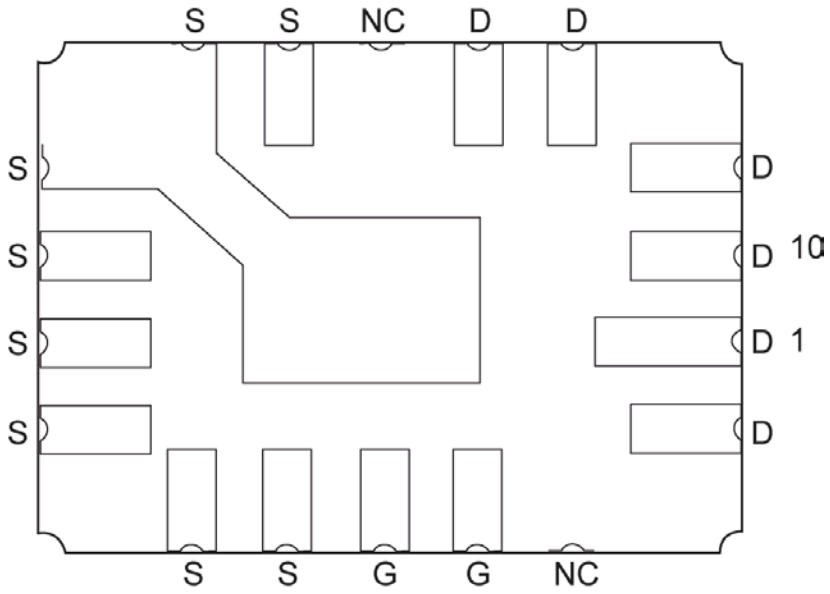


Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.345	.360	8.77	9.14
BW	.280	.295	7.12	7.49
CH	.095	.115	2.42	2.92
LL1	.040	.055	1.02	1.39
LL2	.055	.065	1.40	1.65
LS	.050 BSC		1.27 BSC	
LS1	.025 BSC		0.635 BSC	
LS2	.008 BSC		0.203 BSC	
LW	.020	.030	0.51	0.76
Q1	.105 REF		2.67 REF	
Q2	.120 REF		3.05 REF	
Q3	.045	.055	1.14	1.40
TL	.070	.080	1.78	2.03
TW	.120	.130	3.05	3.30

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.
4. Ceramic package only.

PAD LAYOUT



PAD ASSIGNMENTS