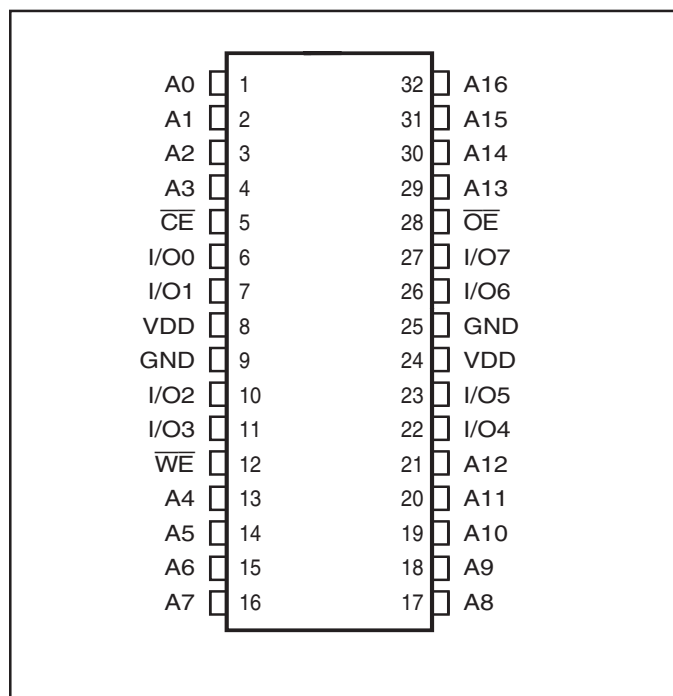


PIN CONFIGURATION

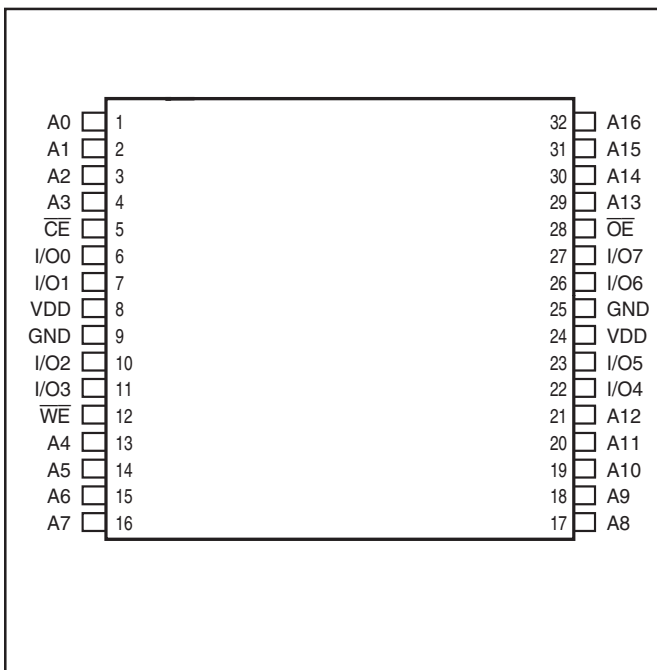
32-Pin SOJ



PIN CONFIGURATION

32-Pin TSOP (Type II) (T)

32-Pin STSOP (Type I) (H)

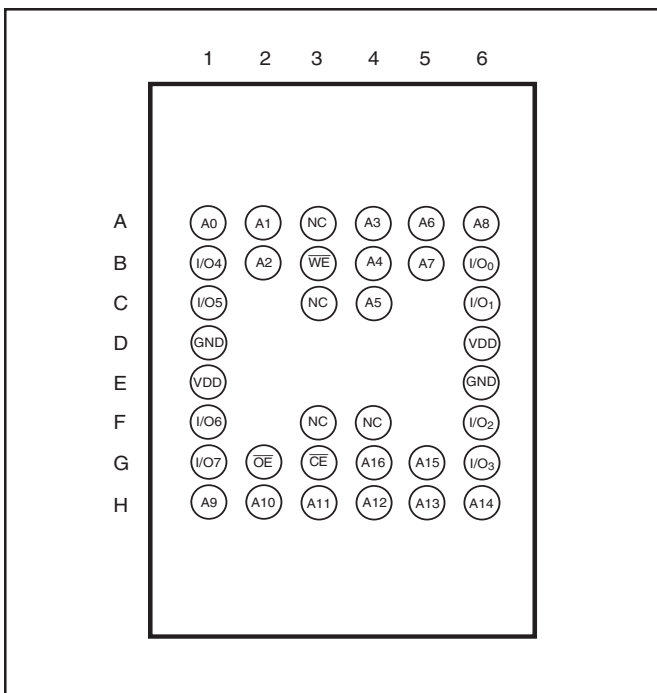


PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Data Inputs/Outputs
VDD	Power
GND	Ground

PIN CONFIGURATION

36-mini BGA (B) (8 mm x 10 mm)



TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V _{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I _{SB1} , I _{SB2}
Output Disabled	H	L	H	High-Z	I _{CC1} , I _{CC2}
Read	H	L	L	D _{OUT}	I _{CC1} , I _{CC2}
Write	L	L	X	D _{IN}	I _{CC1} , I _{CC2}

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to V _{DD} + 0.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
P _T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V _{DD}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	−40°C to +85°C	3.3V ± 0.15V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = −4.0 mA		2.4	—	V
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 8.0 mA		—	0.4	V
V _{IH}	Input HIGH Voltage			2.2	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage ⁽¹⁾			−0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	Com. Ind.	−1 −5	1 5	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled	Com. Ind.	−1 −5	1 5	μA

Note:

1. V_{IL} (min.) = −0.3V DC; V_{IL} (min.) = −2.0V AC (pulse width under V_{SS} < 5ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width over V_{DD} < 5ns). Not 100% tested.

IS63LV1024 POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 ns		-10 ns		-12 ns		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC1}	V _{DD} Operating Supply Current	V _{DD} = Max., $\overline{CE}$ = V _{IL} I _{OUT} = 0 mA, f = Max.	Com.	—	160	—	150	—	130	mA
			Ind.	—	170	—	160	—	140	
			typ. ⁽²⁾	—	105	—	95	—	75	
			Ind. (@ 15 ns)	—	—	—	—	—	90	
I _{SB}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = Max	Com.	—	55	—	45	—	40	mA
			Ind.	—	55	—	45	—	40	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	25	—	25	—	25	mA
			Ind.	—	30	—	30	—	30	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, V _{IN} $\geq$ V _{DD} - 0.2V, or V _{IN} $\leq$ 0.2V, f = 0	Com.	—	5	—	5	—	5	mA
			Ind.	—	10	—	10	—	10	
			typ. ⁽²⁾	—	0.5	—	0.5	—	0.5	
				—	—	—	—	—	—	

Notes:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.3V, T_A = 25°C. Not 100% tested.

IS63LV1024L POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 ns		-10 ns		-12 ns		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC1}	V _{DD} Operating Supply Current	V _{DD} = Max., $\overline{CE}$ = V _{IL} I _{OUT} = 0 mA, f = Max.	Com.	—	100	—	95	—	90	mA
			Ind.	—	110	—	105	—	100	
			typ. ⁽²⁾	—	75	—	70	—	65	
				—	—	—	—	—	—	
I _{SB}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = Max	Com.	—	35	—	30	—	25	mA
			Ind.	—	40	—	35	—	30	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	15	—	15	—	15	mA
			Ind.	—	20	—	20	—	20	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, V _{IN} $\geq$ V _{DD} - 0.2V, or V _{IN} $\leq$ 0.2V, f = 0	Com.	—	1	—	1	—	1	mA
			Ind.	—	1.5	—	1.5	—	1.5	
			typ. ⁽²⁾	—	0.05	—	0.05	—	0.05	
				—	—	—	—	—	—	

Notes:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.3V, T_A = 25°C. Not 100% tested.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{I/O}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-8 ns		-10 ns		-12 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	ns
t_{OHA}	Output Hold Time	2	—	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	—	12	ns
t_{DOE}	$\overline{OE}$ Access Time	—	4	—	5	—	6	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	0	4	0	5	0	6	ns
$t_{LZCE}^{(2)}$	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	ns
$t_{HZCE}^{(2)}$	$\overline{CE}$ to High-Z Output	0	4	0	5	0	6	ns
t_{PU}	$\overline{CE}$ to Power Up Time	0	—	0	—	0	—	ns
t_{PD}	$\overline{CE}$ to Power Down Time	—	8	—	10	—	12	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V loading specified in Figure 1.
2. Tested with the loading specified in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

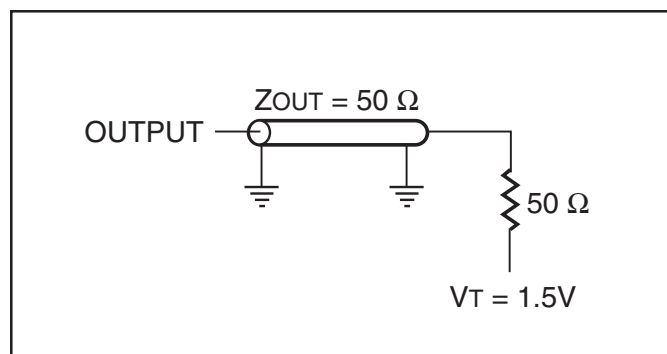


Figure 1

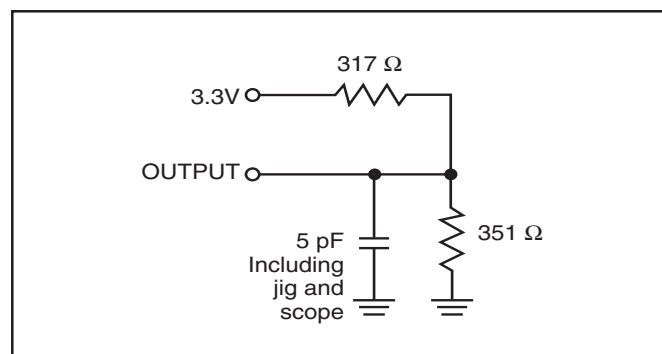
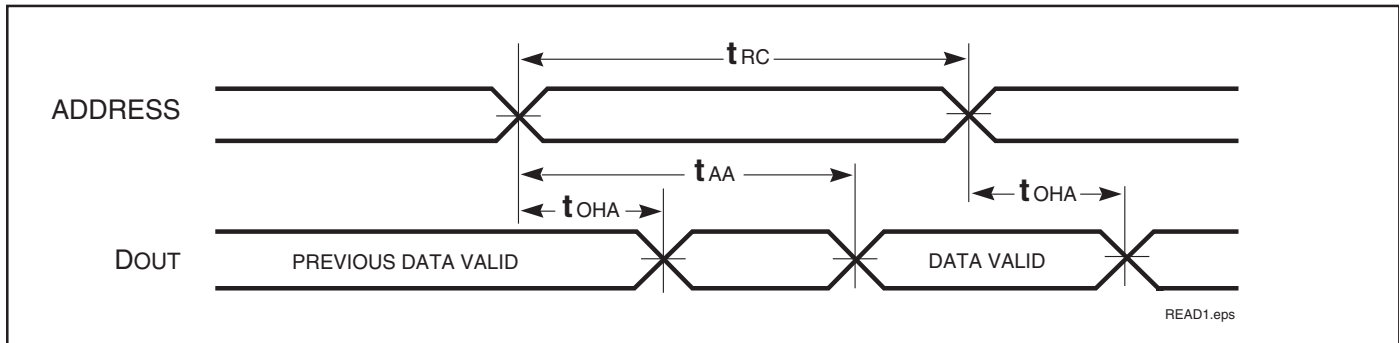


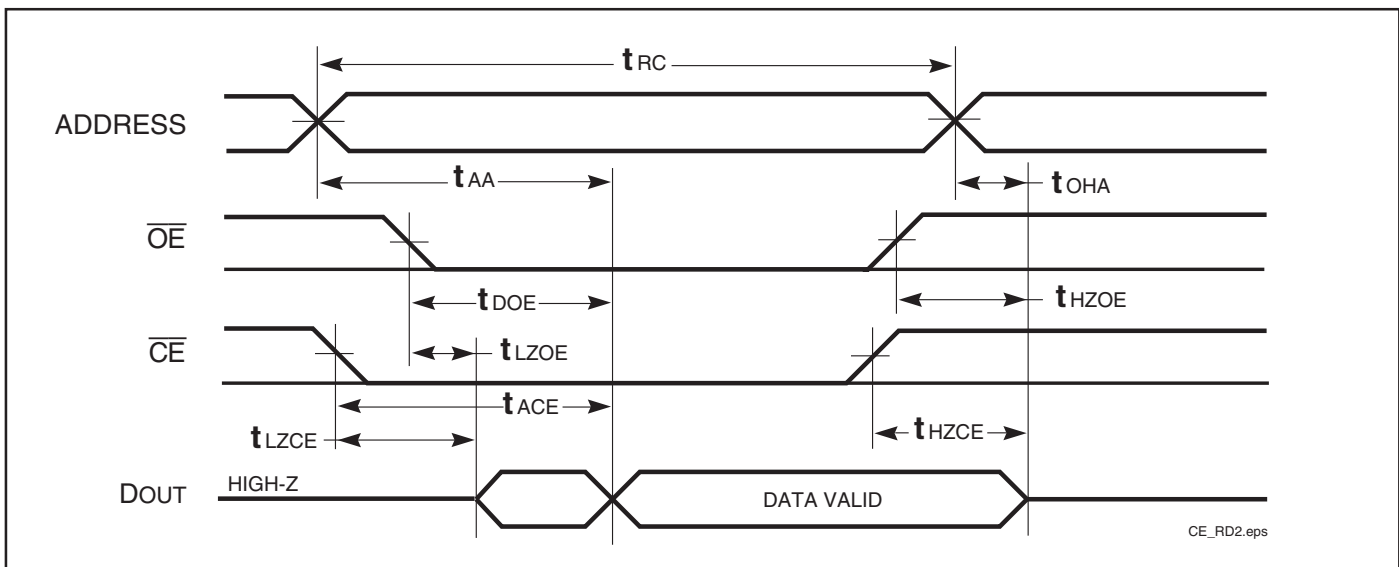
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)



READ CYCLE NO. 2^(1,3)



Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL} .
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

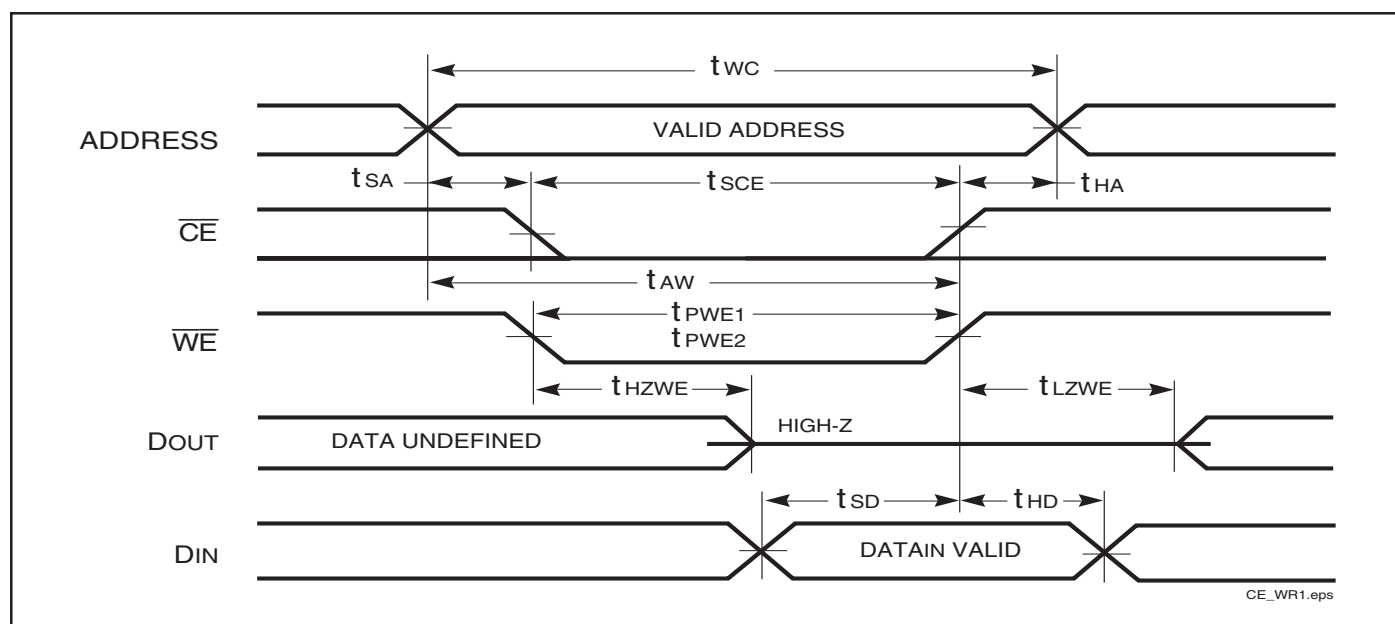
Symbol	Parameter	-8 ns		-10 ns		-12 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t _{SCE}	$\overline{CE}$ to Write End	7	—	7	—	8	—	ns
t _{AW}	Address Setup Time to Write End	8	—	8	—	8	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	ns
t _{PWE₁} ⁽¹⁾	$\overline{WE}$ Pulse Width ($\overline{OE}$ High)	7	—	7	—	8	—	ns
t _{PWE₂} ⁽²⁾	$\overline{WE}$ Pulse Width ($\overline{OE}$ Low)	8	—	10	—	12	—	ns
t _{SD}	Data Setup to Write End	5	—	5	—	6	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t _{HZWE} ⁽²⁾	$\overline{WE}$ LOW to High-Z Output	—	4	—	5	—	6	ns
t _{LZWE} ⁽²⁾	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	3	—	ns

Notes:

1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

AC WAVEFORMS

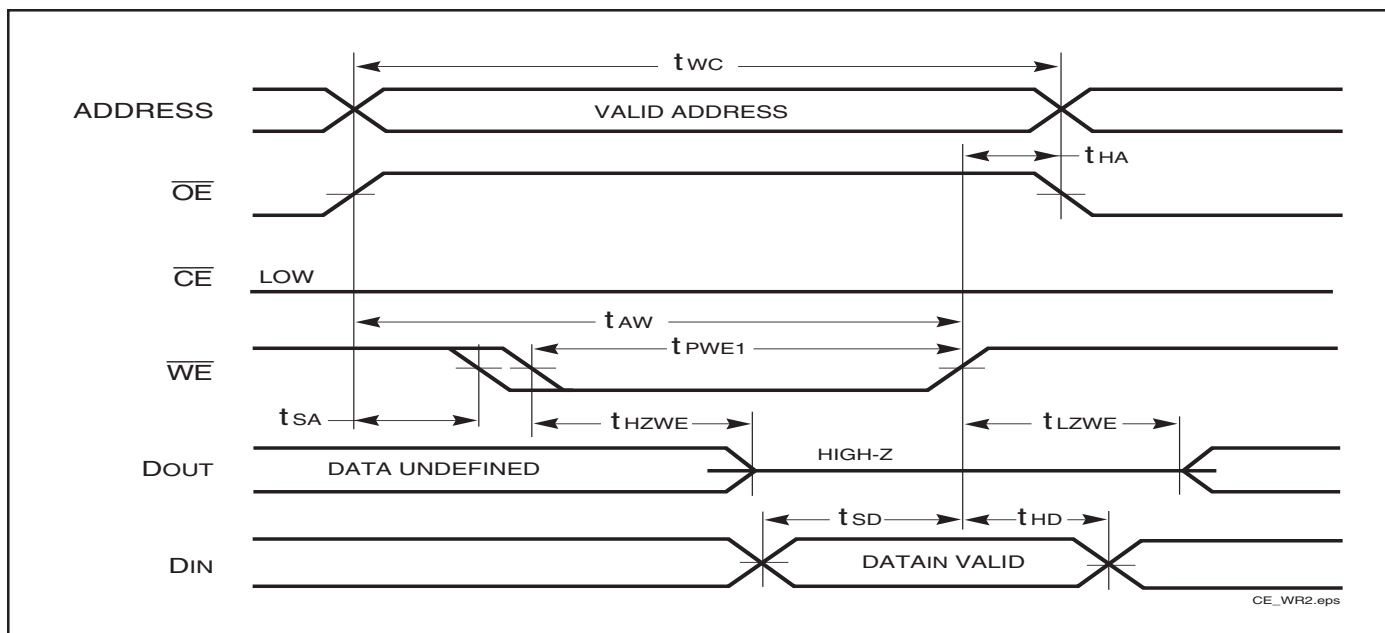
WRITE CYCLE NO. 1^(1,2) ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)



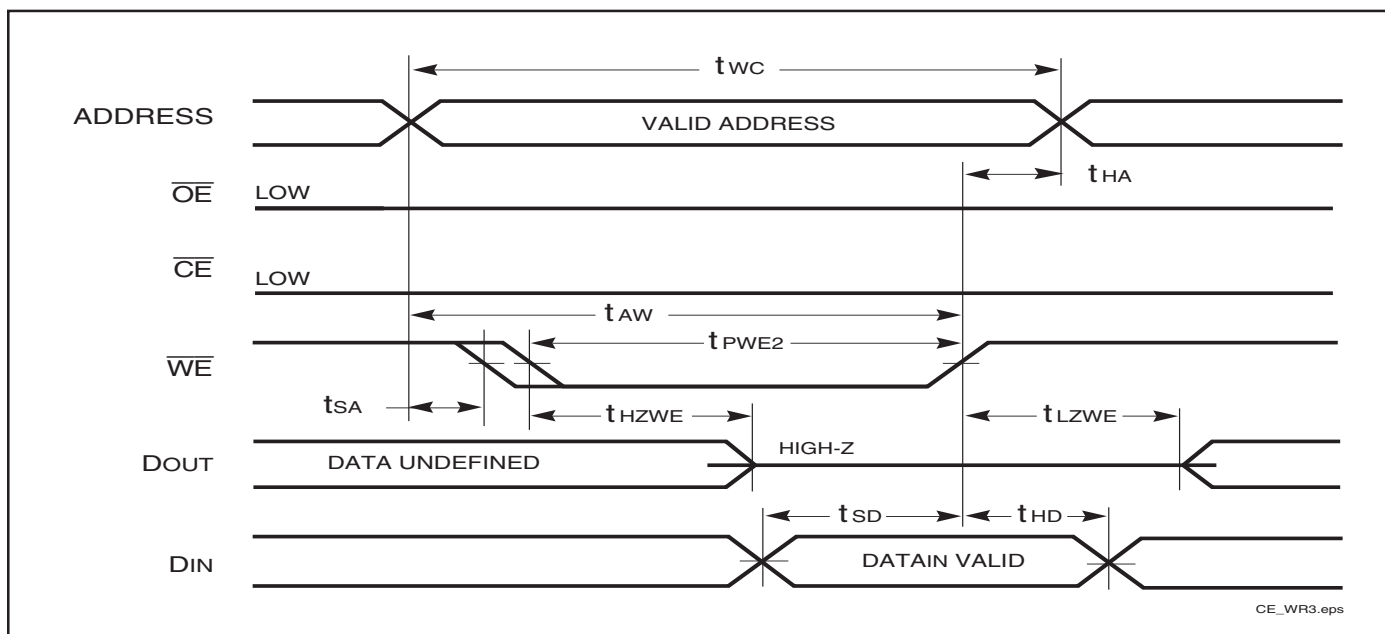
CE_WR1.eps

AC WAVEFORMS

WRITE CYCLE NO. 2⁽¹⁾ ($\overline{WE}$ Controlled, $\overline{OE}$ = HIGH during Write Cycle)



($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



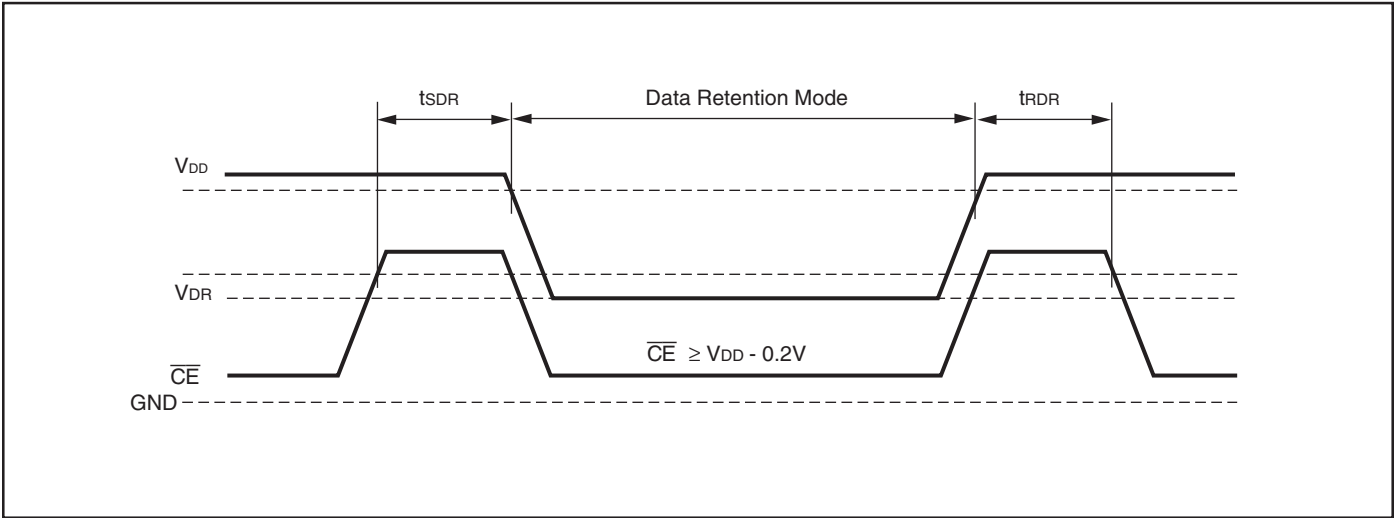
Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.

Symbol	Parameter	Test Condition	Options	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I _{DR}	Data Retention Current	V _{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	IS63LV1024 IS63LV1024L	—	0.5 0.05	10 1.5	mA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform		t _{RC}	—	—	ns

Note 1: Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

($\overline{CE}$ Controlled)



Speed (ns)	Order Part No.	Package
8	IS63LV1024-8K	400-mil Plastic SOJ
	IS63LV1024-8KL	400-mil Plastic SOJ, Lead-free
10	IS63LV1024-10T	TSOP (Type II)
	IS63LV1024-10J	300-mil Plastic SOJ
	IS63LV1024-10K	400-mil Plastic SOJ
12	IS63LV1024-12T	TSOP (Type II)
	IS63LV1024-12J	300-mil Plastic SOJ
	IS63LV1024-12JL	300-mil Plastic SOJ, Lead-free
	IS63LV1024-12KL	400-mil Plastic SOJ, Lead-free

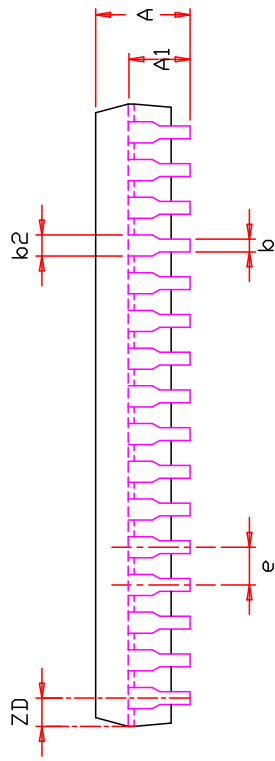
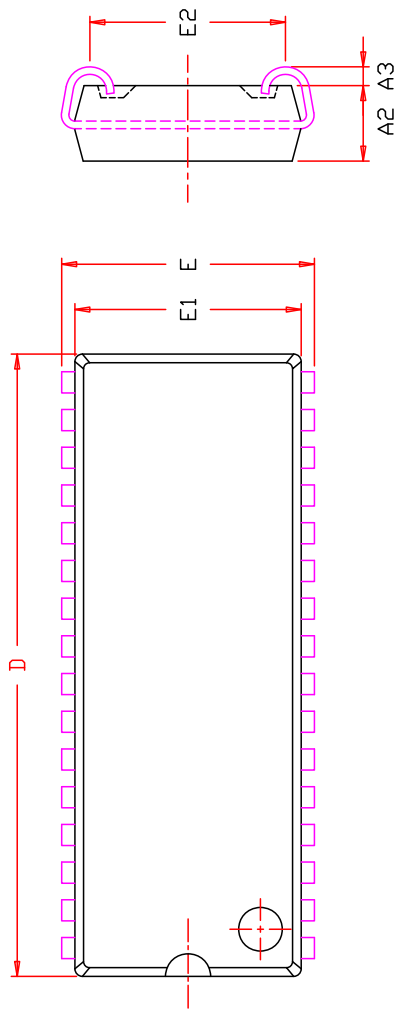
Speed (ns)	Order Part No.	Package
8	IS63LV1024-8KI	400-mil Plastic SOJ
10	IS63LV1024-10KI	400-mil Plastic SOJ
12	IS63LV1024-12TI	TSOP (Type II)

Speed (ns)	Order Part No.	Package
8	IS63LV1024L-8T	TSOP (Type II)
	IS63LV1024L-8TL	TSOP (Type II), Lead-free
	IS63LV1024L-8B	mBGA (8mmx10mm)
10	IS63LV1024L-10T	TSOP (Type II)
	IS63LV1024L-10TL	TSOP (Type II), Lead-free
	IS63LV1024L-10HL	sTSOP (Type I) (8mm x13.4mm), Lead-free
12	IS63LV1024L-12T	TSOP (Type II)
	IS63LV1024L-12TL	TSOP (Type II), Lead-free
	IS63LV1024L-12H	sTSOP (Type I) (8mm x13.4mm)
	IS63LV1024L-12J	300-mil Plastic SOJ
	IS63LV1024L-12JL	300-mil Plastic SOJ, Lead-free
	IS63LV1024L-12B	mBGA (8mmx10mm)

Speed (ns)	Order Part No.	Package
8	IS63LV1024L-8TI	TSOP (Type II)
	IS63LV1024L-8JI	300-mil Plastic SOJ
	IS63LV1024L-8KI	400-mil Plastic SOJ
	IS63LV1024L-8BI	mBGA (8mmx10mm)
10	IS63LV1024L-10HI	sTSOP (Type I) (8mm x13.4mm)
	IS63LV1024L-10JLI	300-mil Plastic SOJ, Lead-free
	IS63LV1024L-10KLI	400-mil Plastic SOJ, Lead-free
	IS63LV1024L-10TLI	TSOP (Type II), Lead-free
12	IS63LV1024L-12BI	mBGA (8mmx10mm)
	IS63LV1024L-12BLI	mBGA (8mmx10mm), Lead-free
	IS63LV1024L-12TI	TSOP (Type II)
	IS63LV1024L-12TLI	TSOP (Type II), Lead-free

Speed (ns)	Top Mark	Order Part No.	Package
8	IS63LV1024L-10KLI	U788B-8KLI	400-mil Plastic SOJ, Lead-free
	IS63LV1024L-10TLI	U788A-8TLI	TSOP (Type II), Lead-free

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.05		3.76	0.120		0.148
A1	2.08		2.41	0.082		0.095
A2	2.41	2.54	2.67	0.095	0.100	0.105
A3	0.64		1.09	0.025		0.043
b	0.41		0.51	0.016		0.020
b2	0.66		0.81	0.026		0.032
D	20.82		21.09	0.820		0.830
E	8.38	8.51	8.64	0.330	0.335	0.340
E1	7.49	7.62	7.75	0.295	0.300	0.305
E2	6.48		6.99	0.255		0.275
e	1.27 BSC.			0.050 BSC.		
ZD	0.95 REF.			0.037 REF.		

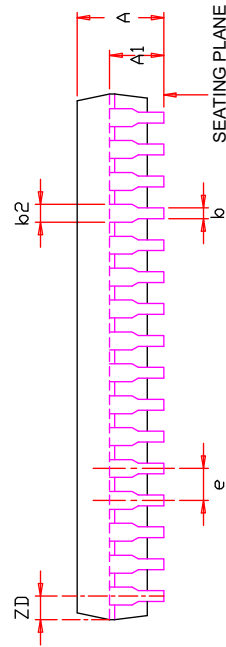
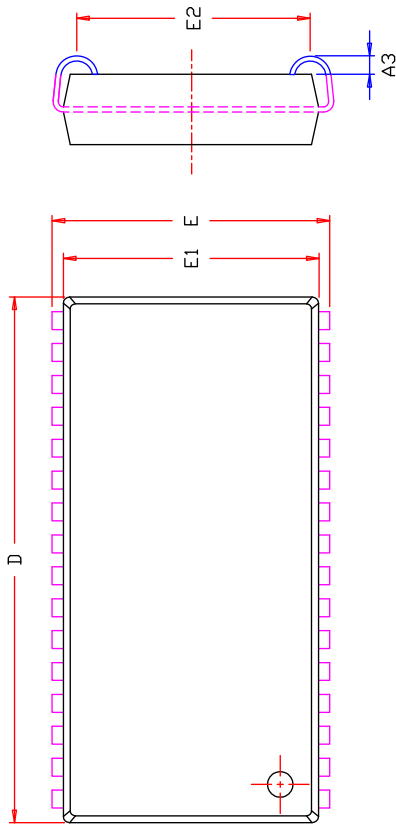


NOTE :

- 1. CONTROLLING DIMENSION : MM
- 2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

ISSI	TITLE	32L 300mil SOJ Package Outline	REV.	C	DATE	08/14/2009

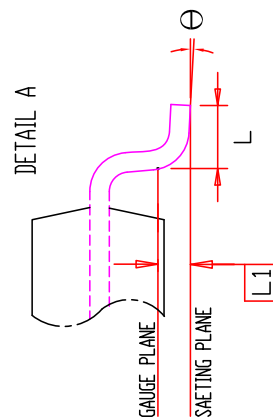
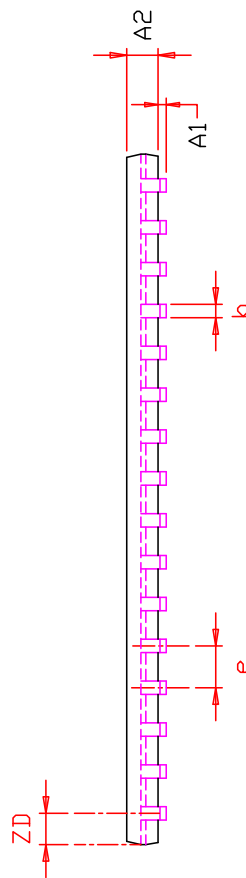
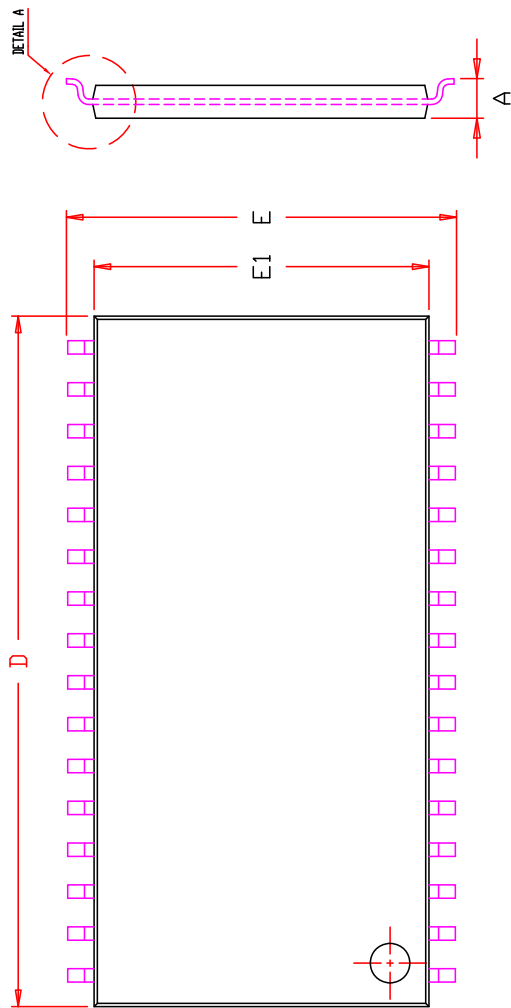
SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	NOM.	MAX.	MIN. NOM. MAX.
A	3.25		3.76	0.128 0.148
A1	2.08		0.082	
A3	0.635		0.025	
b	0.38		0.51	0.015 0.020
b2	0.66	0.71	0.81	0.026 0.028 0.032
D	20.82	20.95	21.08	0.820 0.825 0.830
E	11.05	11.18	11.30	0.435 0.440 0.445
E1	10.03	10.16	10.29	0.395 0.400 0.405
E2	9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC	
ZD	0.95 REF		0.037 REF	



NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027.

ISSI	TITLE	32L 400mil SOJ Package Outline	REV.	E	DATE	12/19/2007
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NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.52	0.012		0.020
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	1.27	BSC.		0.050	BSC.	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25	BSC.		0.010	BSC.	
ZD	0.95	REF.		0.037	REF.	
Θ	0		8°	0		8°



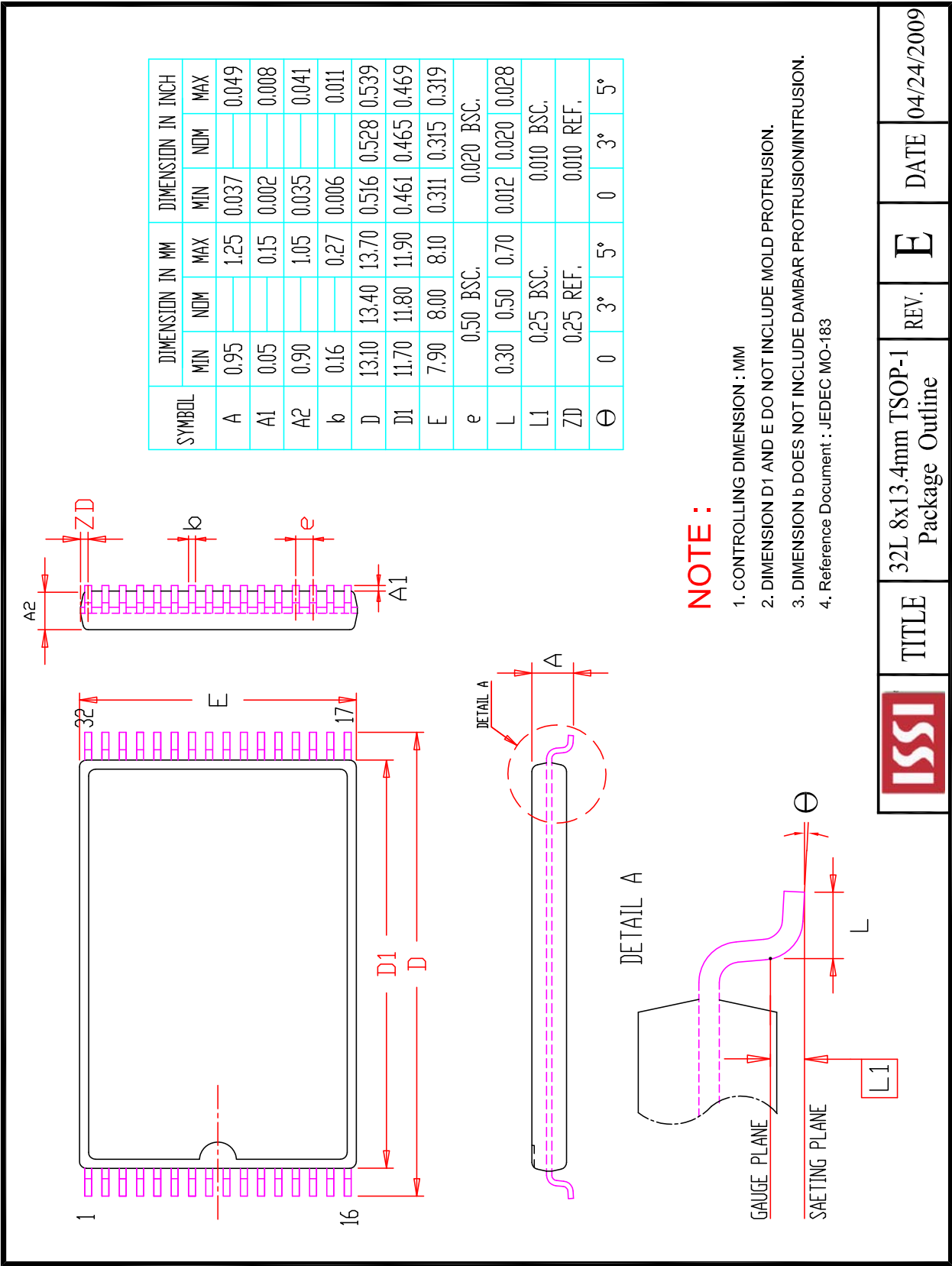
32L 400mil TSOP-2
Package Outline

TITLE

REV. E

DATE

06/23/2009



ISSI	TITLE	32L 8x13.4mm TSOP-1 Package Outline	REV.	E	DATE	04/24/2009
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