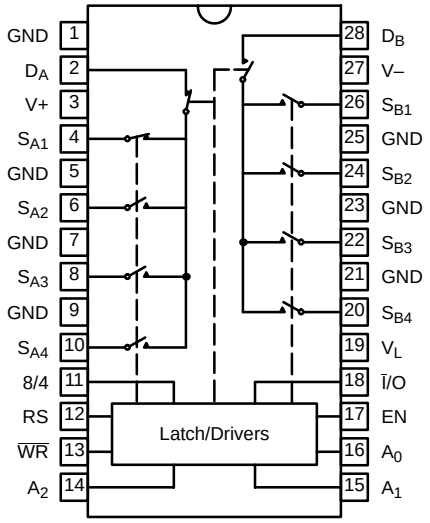
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG538ADJ

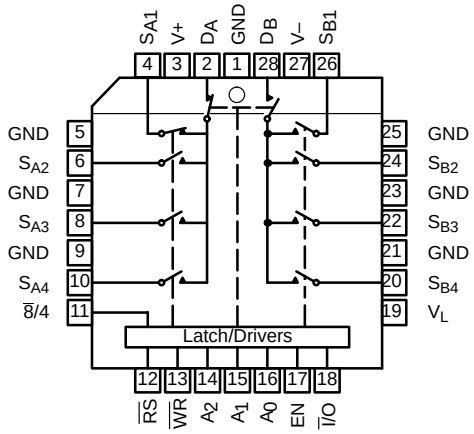
Dual-In-Line



Top View

DG538ADN

PLCC



Top View

TRUTH TABLE — DG534A								
$\overline{I}$/O	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	$\overline{4}$/2[a]	On Switch	
X	X	X	X	⌐	1	1	Maintains previous state	
X	X	X	X	X	0	X	None (latches cleared)	
X	X	X	0	0	1	X	None	Latches Transparent
0	0	0	1	0	1	0	S_{A1}	D_A and D_B may be connected externally
0	0	1	1	0	1	0	S_{A2}	
0	1	0	1	0	1	0	S_{B1}	
0	1	1	1	0	1	0	S_{B2}	
0	X	0	1	0	1	1	S_{A1} and S_{B1}	
0	X	1	1	0	1	1	S_{A2} and S_{B2}	
1	Note b			1	1	Note c		

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

TRUTH TABLE — DG538A									
$\overline{I}$/O	A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	$\overline{8}$/4[a]	On Switch	
X	X	X	X	X	⌐‾	1	1	Maintains previous state	
X	X	X	X	X	X	0	X	None (latches cleared)	
X	X	X	X	0	0	1	X	None	Latches Transparent
0	0	0	0	1	0	1	0	S_{A1}	D_A and D_B should be connected externally
0	0	0	1	1	0	1	0	S_{A2}	
0	0	1	0	1	0	1	0	S_{A3}	
0	0	1	1	1	0	1	0	S_{A4}	
0	1	0	0	1	0	1	0	S_{B1}	
0	1	0	1	1	0	1	0	S_{B2}	
0	1	1	0	1	0	1	0	S_{B3}	
0	1	1	1	1	0	1	0	S_{B4}	
0	X	0	0	1	0	1	1	S_{A1} and S_{B1}	
0	X	0	1	1	0	1	1	S_{A2} and S_{B2}	
0	X	1	0	1	0	1	1	S_{A3} and S_{B3}	
0	X	1	1	1	0	1	1	S_{A4} and S_{B4}	
1	Note b				1	1	Note c		

Logic “0” = $V_{AL} \leq 0.8$ V
Logic “1” = $V_{AH} \geq 2$ V
X = Don’t Care

Notes:
a. Connect D_A and D_B together externally for single-ended operation.
b. With $\overline{I}$/O high, A_n and EN pins become outputs and reflect latch contents. See timing diagrams for more detail.
c. $\overline{8}$/4 can be either “1” or “0” but should not change during these operations.

ORDERING INFORMATION		
Temperature Range	**Package**	**Part Number**
DG534A		
–40 to 85°C	20-Pin Plastic DIP	DG534ADJ
	20-Pin PLCC	DG534ADN
–55 to 125°C	20-Pin Sidebraze	DG534AAP/883, 5962-906021MRC
DG538A		
–40 to 85°C	28-Pin Plastic DIP	DG538ADJ
	28-Pin PLCC	DG538ADN
–55 to 125°C	28-Pin Sidebraze	DG538AAP/883, 5962-8976001MXA

ABSOLUTE MAXIMUM RATINGS

V+ to GND ..... –0.3 V to +21 V
V+ to V– ..... –0.3 V to +21 V
V– to GND ..... –10 V to +0.3 V
V_L ..... 0 V to (V+) + 0.3 V
Digital Inputs ..... (V–) –0.3 V to (V_L) + 0.3 V
or 20 mA, whichever occurs first
V_S, V_D ..... (V–) –0.3 V to (V–) + 14 V
or 20 mA, whichever occurs first
Current (any terminal) Continuous ..... 20 mA
Current(S or D) Pulsed l ms 10% Duty ..... 40 mA

Storage Temperature (A Suffix) ..... –65 to 150°C
(D Suffix) ..... –65 to 125°C

Power Dissipation (Package)[a]
Plastic DIP[b] ..... 625 mW
PLCC[c] ..... 450 mW
Sidebraze[d] ..... 1200 mW

Notes:
a. All leads soldered or welded to PC board.
b. Derate 8.3 mW/°C above 75°C.
c. Derate 6 mW/°C above 75°C.
d. Derate 16 mW/°C above 75°C.

SPECIFICATIONS[a]

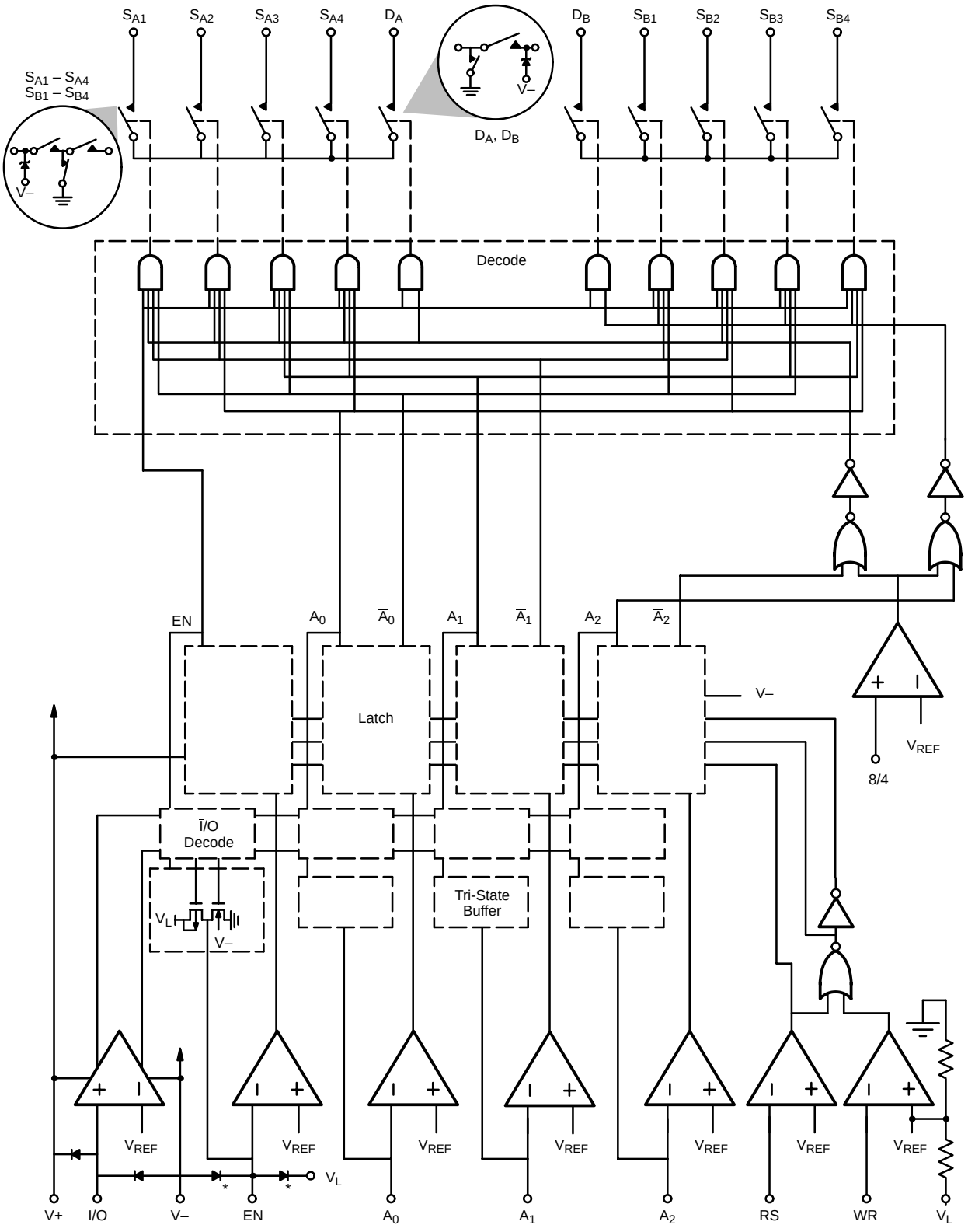
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –3 V, V_L = 5 V $\overline{WR}$ = 0.8 V, $\overline{RS}$, EN= 2 V		Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[g]	V_{ANALOG}	V– = –5 V		Full		–5	8	–5	8	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_S = 0 V V_{AIL} = 0.8 V, V_{AIH} = 2 V Sequence Each Switch On		Room Full	45		90 120		90 120	Ω
Resistance Match Between Channels	$\Delta r_{DS(on)}$			Room			9		9	
Source Off Leakage Current	$I_{S(off)}$	V_S = 8 V, V_D = 0 V, EN = 0.8 V		Room Full	0.05	–5 –50	5 50	–5 –50	5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 0 V, V_D = 8 V, EN = 0.8 V		Room Full	0.1	–20 –500	20 500	–20 –100	20 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 8 V		Room Full	0.1	–20 –1000	20 1000	–20 –200	20 200	
Digital Control										
Input Voltage High	V_{AIH}			Full		2		2		V
Input Voltage Low	V_{AIL}			Full			0.8		0.8	
Address Input Current	I_{AI}	V_{AI} = 0 V, or 2 V or 5 V		Room Full	–0.1	–1 –10	1 10	–1 –10	1 10	µA
Address Output Current	I_{AO}	V_{AO} = 2.7 V		Room	–21		–2.5		–2.5	mA
		V_{AO} = 0.4 V		Room	3.5	2.5		2.5		
Dynamic Characteristics										
On State Input Capacitance[g]	$C_{S(on)}$	See Figure 11	PLCC	Room	28		40		40	pF
			DIP	Room	31		45		45	
Off State Input Capacitance[g]	$C_{S(off)}$	See Figure 12	PLCC	Room	3		5		4	
			DIP	Room	4				5	
Off State Output Capacitance[g]	$C_{D(off)}$		PLCC	Room	6		10		8	
			DIP	Room	8				10	
Transition Time	t_{TRANS}	See Figure 4		Room Full	160		300 500		300 500	ns
Break-Before-Make Interval	t_{OPEN}			Room Full	80	50 25		50 25		
EN, $\overline{WR}$ Turn On Time	t_{ON}	See Figure 2 and 3		Room Full	150		300 500		300 500	
EN, Turn Off Time	t_{OFF}	See Figure 2		Room Full	105		175 300		175 300	
Charge Injection	Qi	See Figure 5		Room	–70					pC

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –3 V, V_L = 5 V $\overline{WR}$ = 0.8 V, $\overline{RS}$, EN= 2 V		Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)										
Chip Disabled Crosstalk[f]	$X_{TALK(CD)}$	R_L = 75 Ω, f = 5 MHz EN = 0.8 V See Figure 8	PLCC	Room	–75					dB
			DIP	Room	–65					
Adjacent Input Crosstalk[f]	$X_{TALK(AI)}$	R_{IN} = 10 Ω R_L = 10 kΩ f = 5 MHz SeeFigure 9	PLCC	Room	–97					
			DIP	Room	–87					
		R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz See Figure 7	PLCC	Room	–80					
			DIP	Room	–70					
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω R_L = 10 kΩ f = 5 MHz See Figure 7	PLCC	Room	–77					
			DIP	Room	–72					
		R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz See Figure 7	PLCC	Room	–77					
			DIP	Room	–72					
Differential Crosstalk	$X_{TALK(DIFF)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz, See Figure 10		Room	–84					
		R_{IN} = R_L = 75 Ω f = 5 MHz, See Figure 10		Room	–84					
Bandwidth	BW	R_L = 50 Ω, See Figure 6		Room	500					MHz
Power Supplies										
Positive Supply Current	I+	Any One Channel Selected with Address Inputs at GND or 5 V		Room Full	0.6		2 5		2 5	mA
Negative Supply Current	I–			Room Full	0.6	–1.8 –2		–1.8 –2		
Functional Check of Maximum Operating Supply Voltage Range	V+ to V–	Functional Test Only		Full		10	21	10	21	V
	V– to GND			Full		–5.5	0	–5.5	0	
	V+ to GND			Full		10	21	10	21	
Logic Supply Current	I_L			Full	150		500		500	µA
Timing										
Reset to Write	t_{RW}	See Figure 1		Room Full	–22	50		50		ns
$\overline{WR}$, $\overline{RS}$ Minimum Pulse Width	t_{MPW}			Room Full	60	200		200		
A_0, A_1, EN Data Valid to Strobe	t_{DW}			Room Full	20	100		100		
A_0, A_1, EN Data Valid after Strobe	t_{WD}			Room Full	–20	50		50		
Address Bus Tri-State[e]	t_{AZ}			Room	25					
Address Bus Output	t_{AO}			Room	95					
Address Bus Input	t_{AI}			Room	110					

Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Defined by system bus requirements.
f. Each individual pin shown as GND must be grounded.
g. Guaranteed by design, not subject to production test.

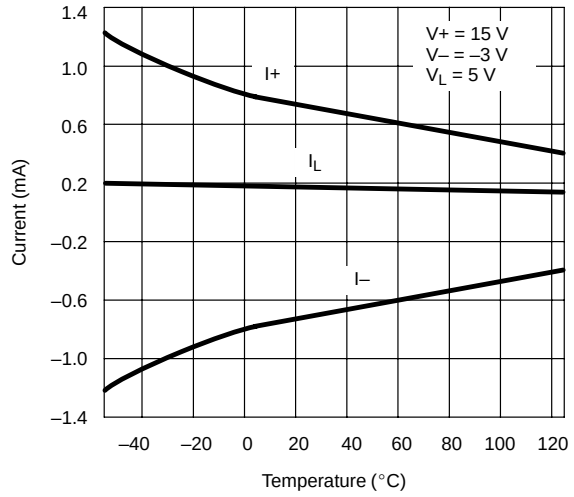
CONTROL CIRCUITRY



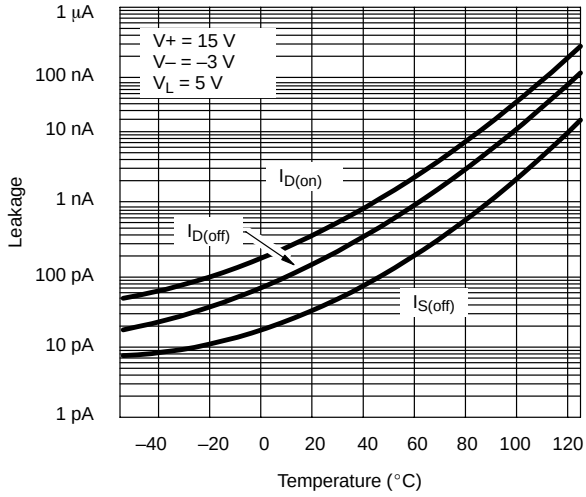
*Typical all Readback (A_X, EN) pins

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

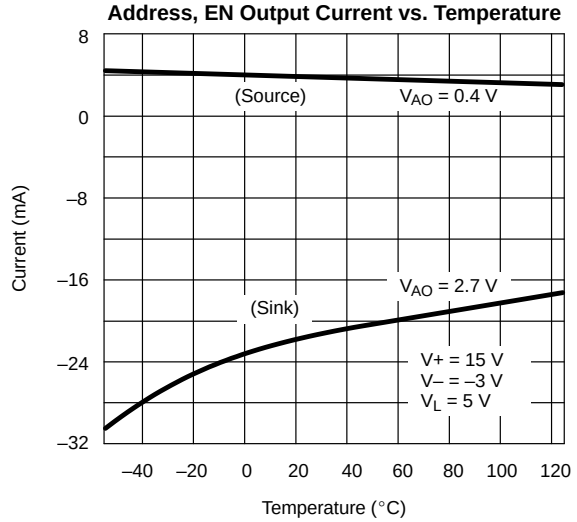
Supply Currents vs. Temperature



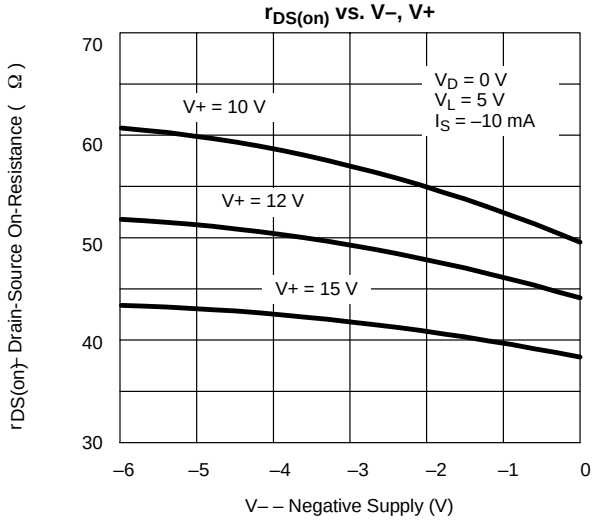
Leakage vs. Temperature



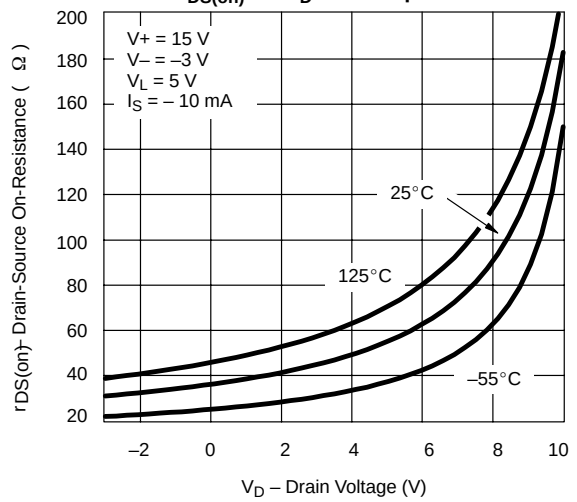
Address, EN Output Current vs. Temperature



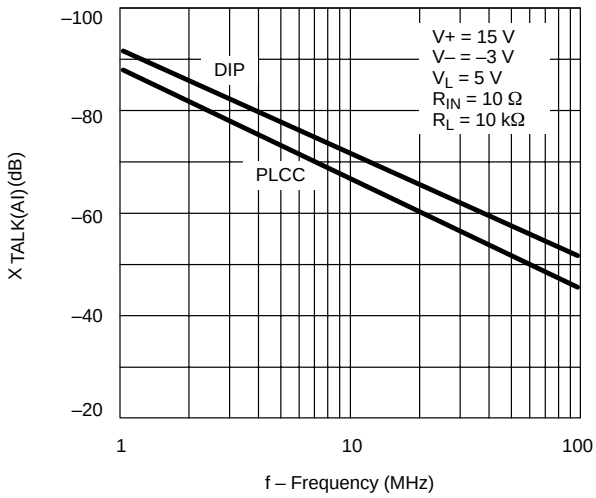
$r_{DS(on)}$ vs. V–, V+



$r_{DS(on)}$ vs. V_D and Temperature

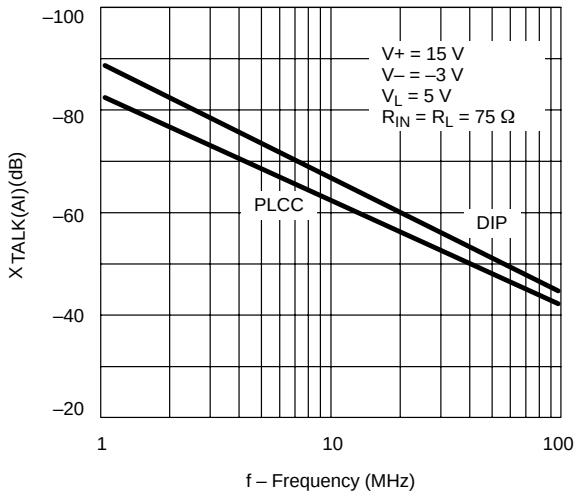


Adjacent Input Crosstalk vs. Frequency

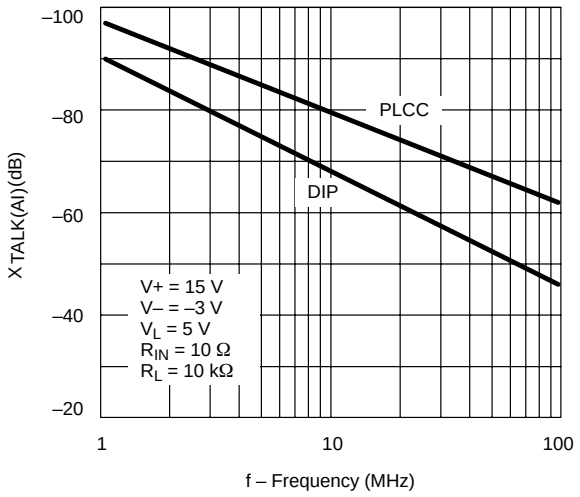


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

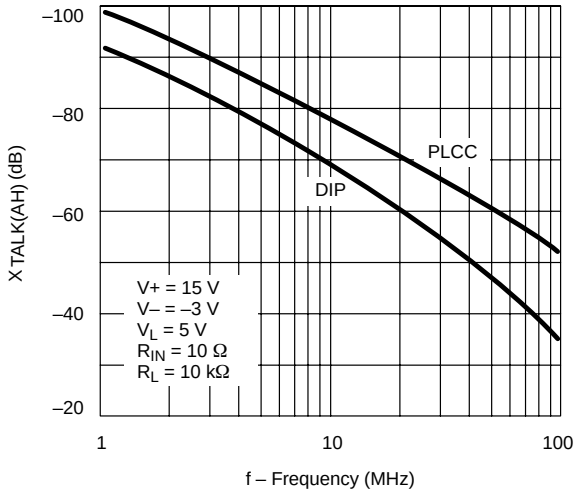
Adjacent Input Crosstalk vs. Frequency



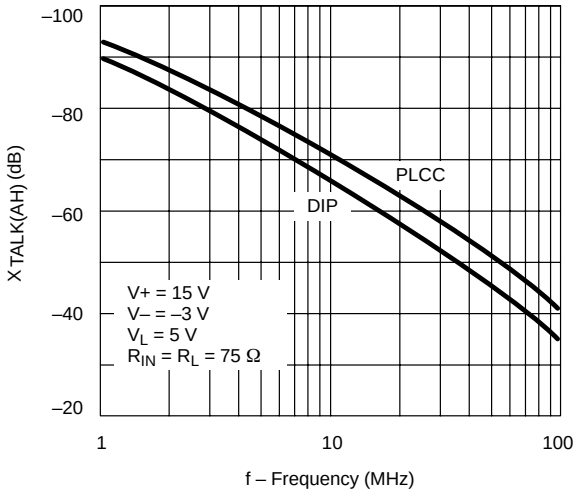
Adjacent Input Crosstalk vs. Frequency



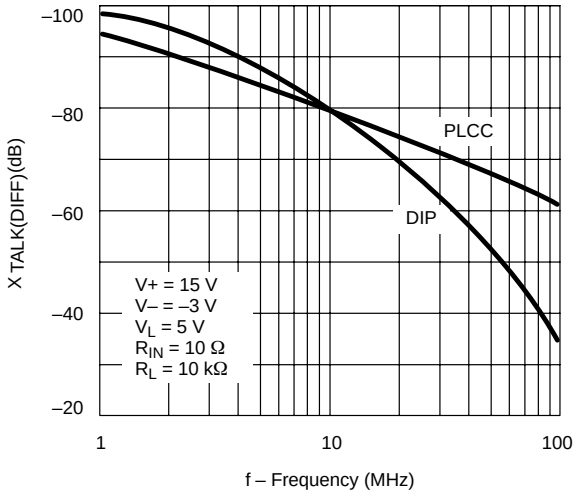
All Hostile Crosstalk vs. Frequency



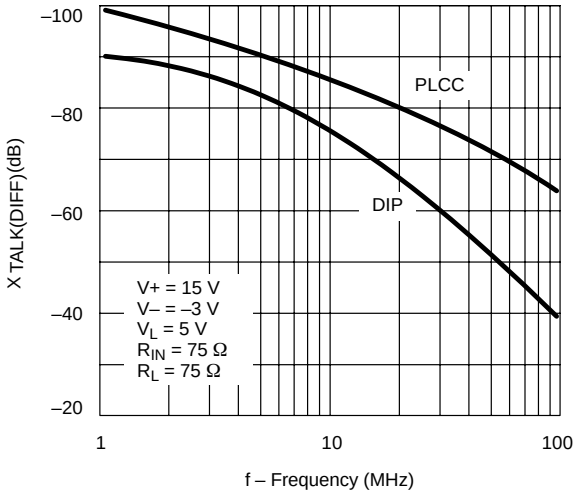
All Hostile Crosstalk vs. Frequency



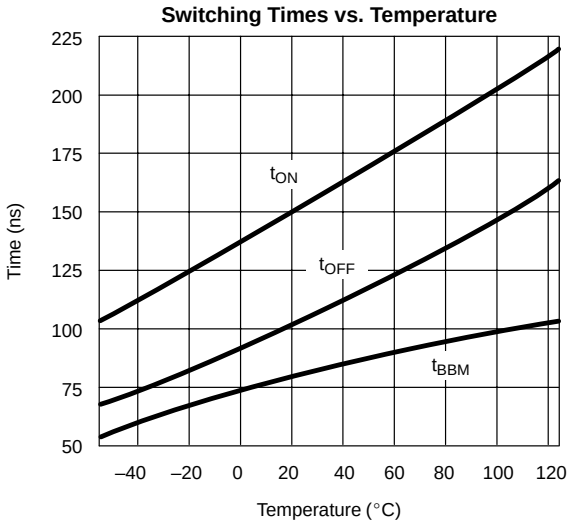
Differential Crosstalk vs. Frequency

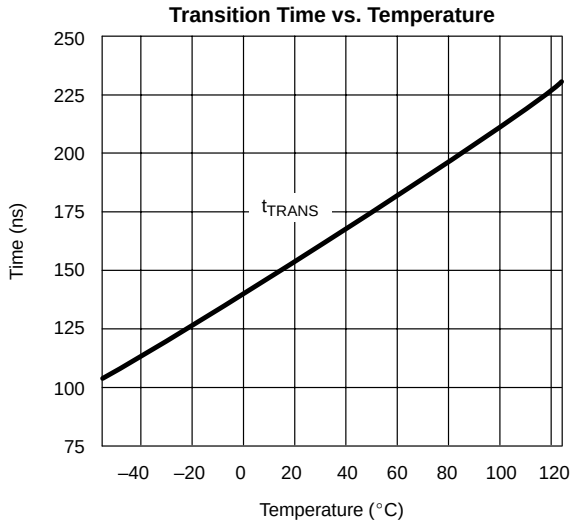


Differential Crosstalk vs. Frequency

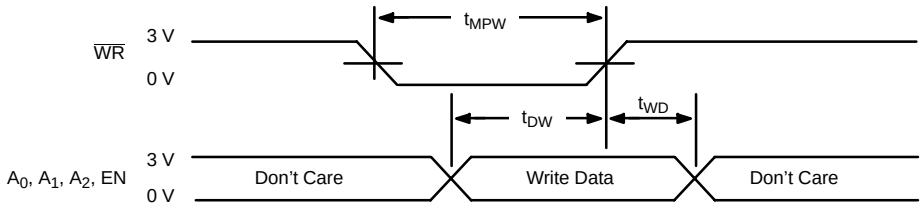


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

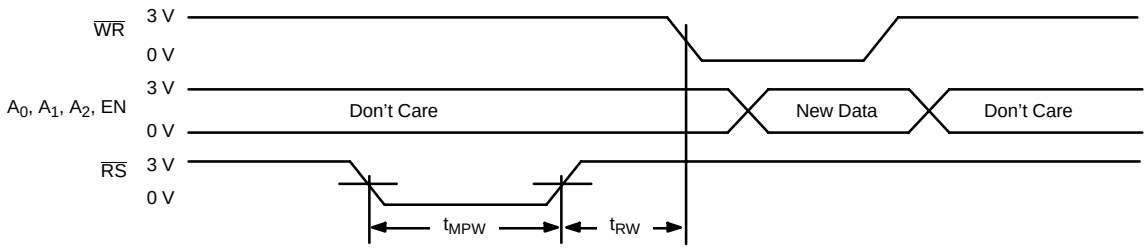




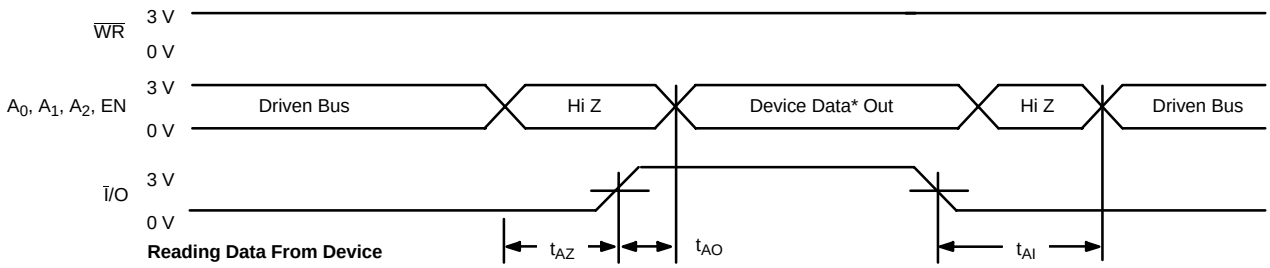
OUTPUT TIMING REQUIREMENTS



Writing Data to Device



Delay Time Required after Reset before Write



Reading Data From Device

FIGURE 1.

TEST CIRCUITS

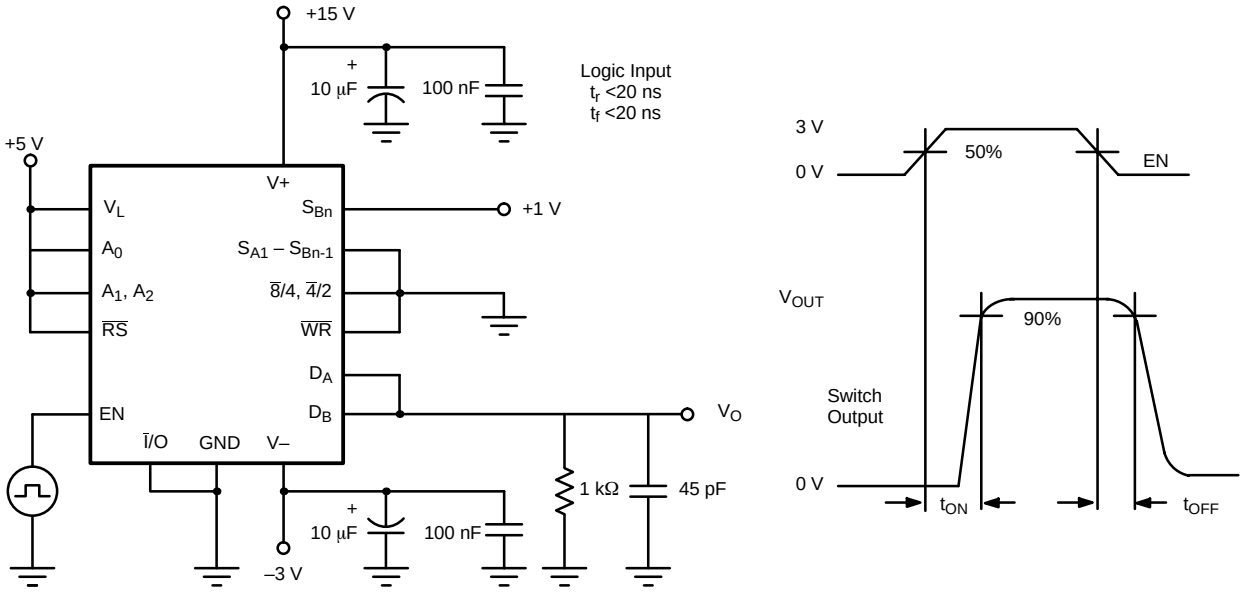


FIGURE 2. EN, CS, $\overline{CS}$, Turn On/Off Time

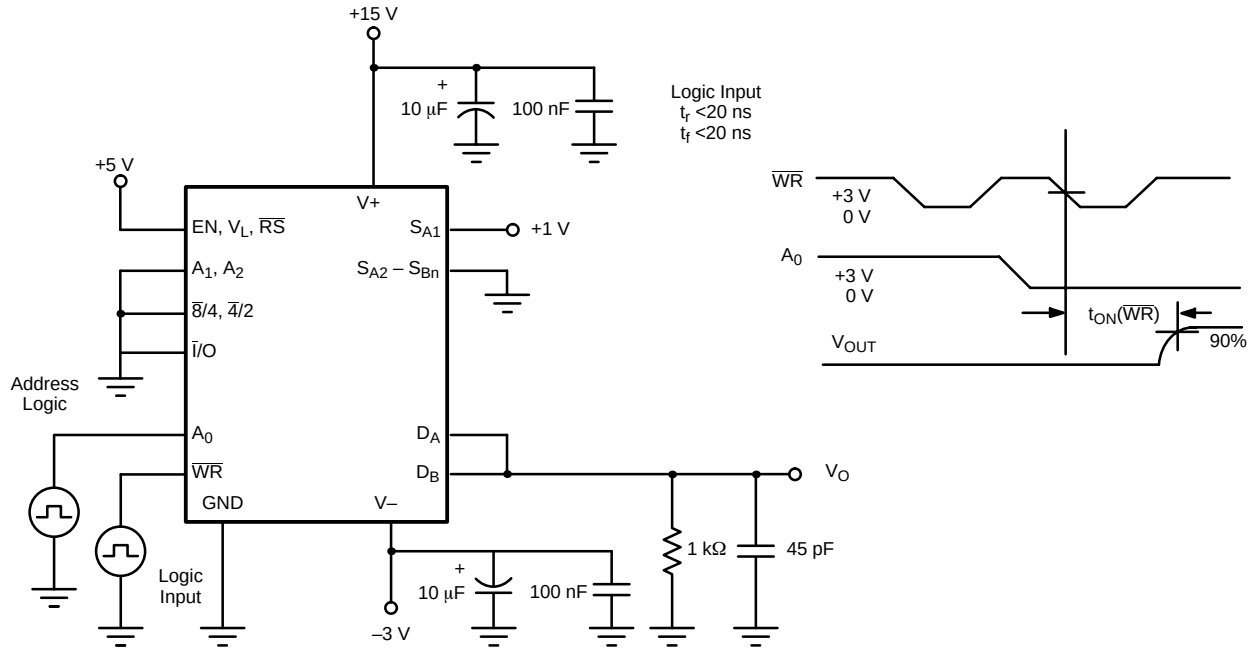


FIGURE 3. $\overline{WR}$, Turn On Time

TEST CIRCUITS

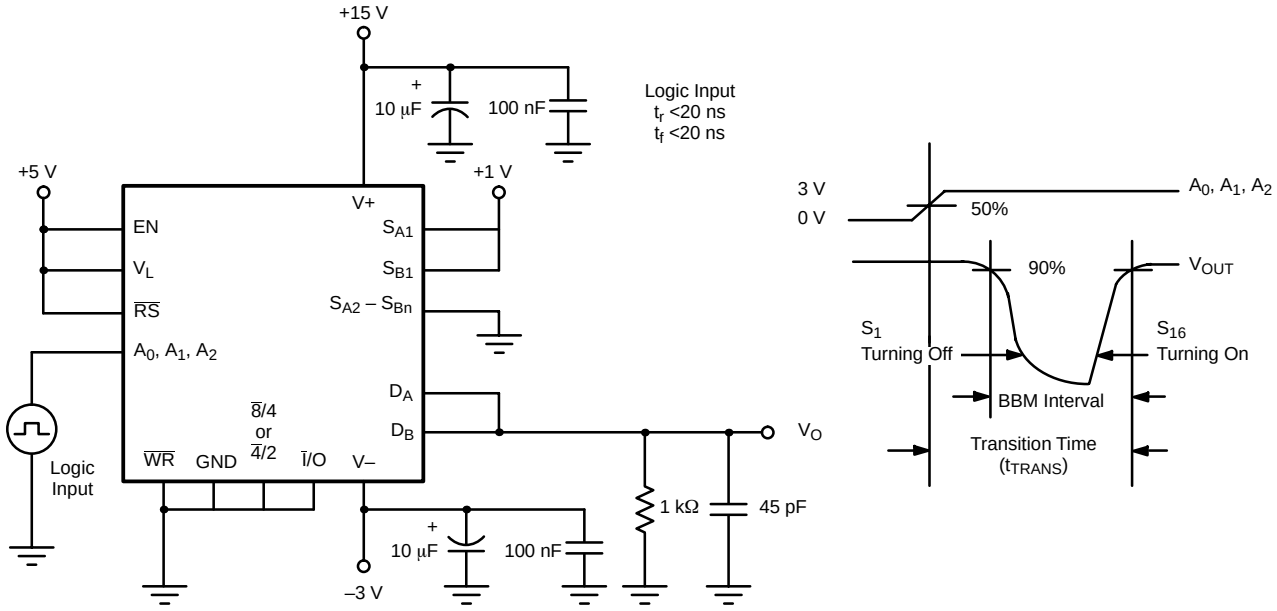


FIGURE 4. Transition Time and Break-Before-Make Interval

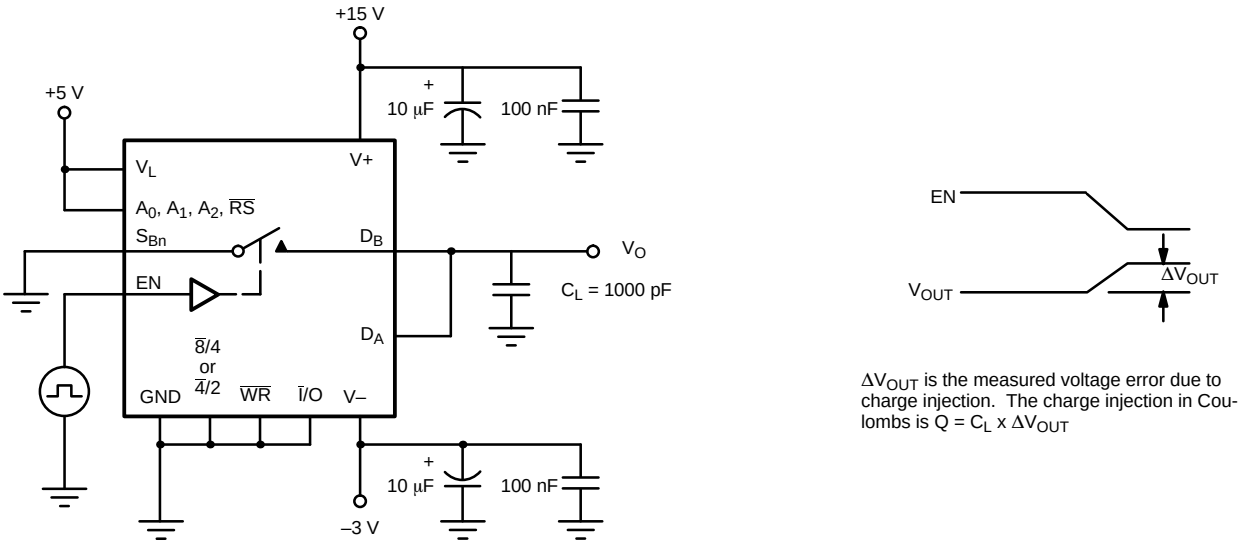


FIGURE 5. Charge Injection

TEST CIRCUITS

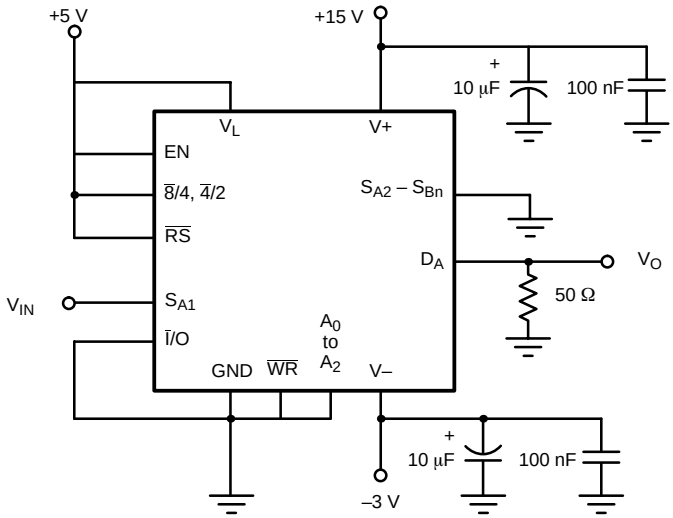


FIGURE 6. Bandwidth

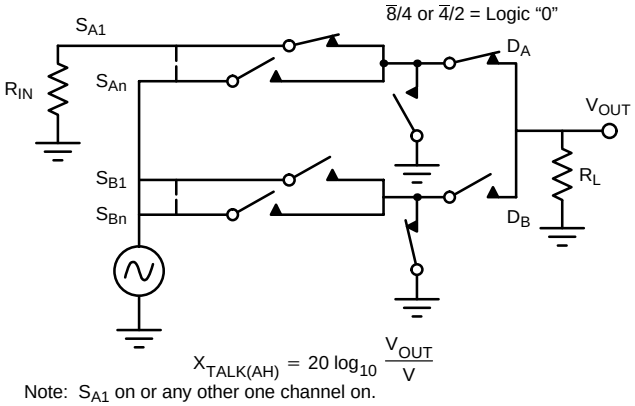


FIGURE 7. All Hostile Crosstalk

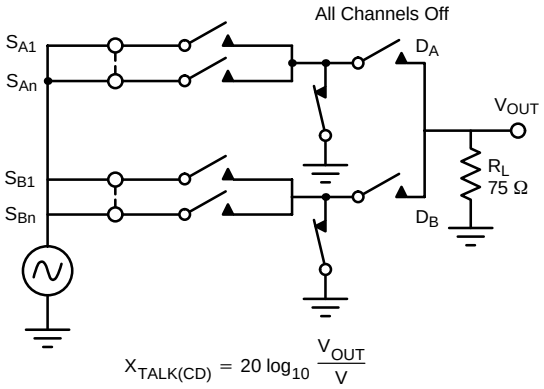


FIGURE 8. Chip Disabled Crosstalk

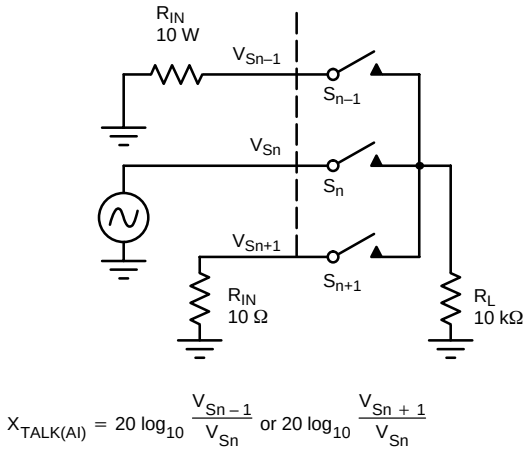


FIGURE 9. Adjacent Input Crosstalk

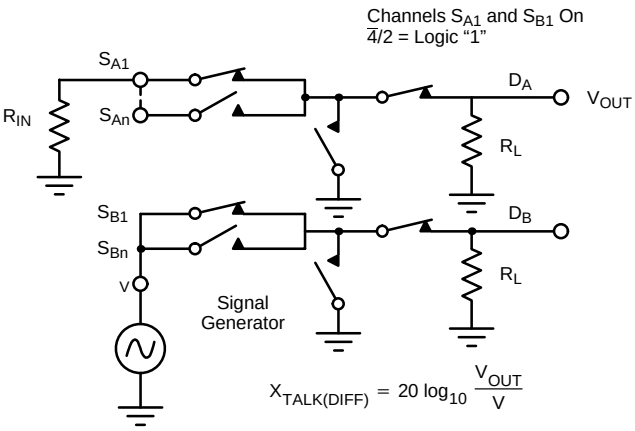


FIGURE 10. Differential Crosstalk

TEST CIRCUITS

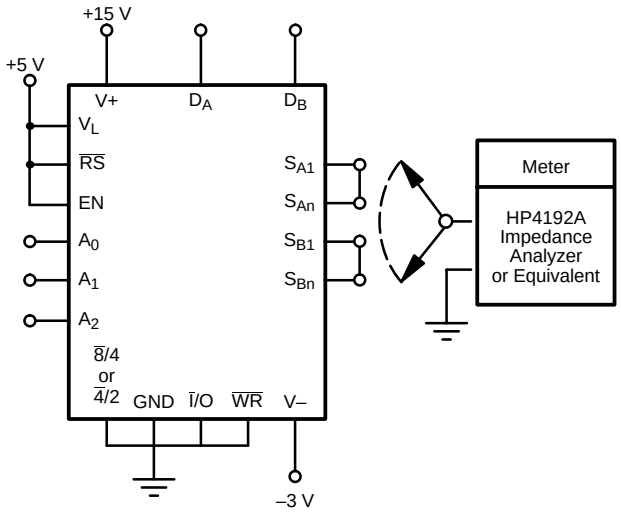


FIGURE 11. On State Input Capacitance

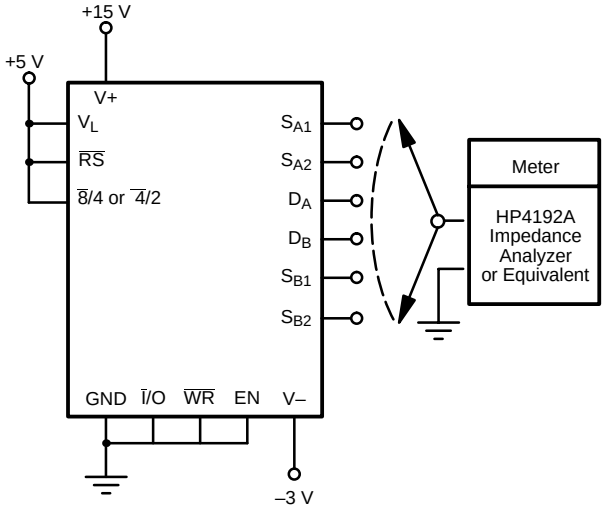
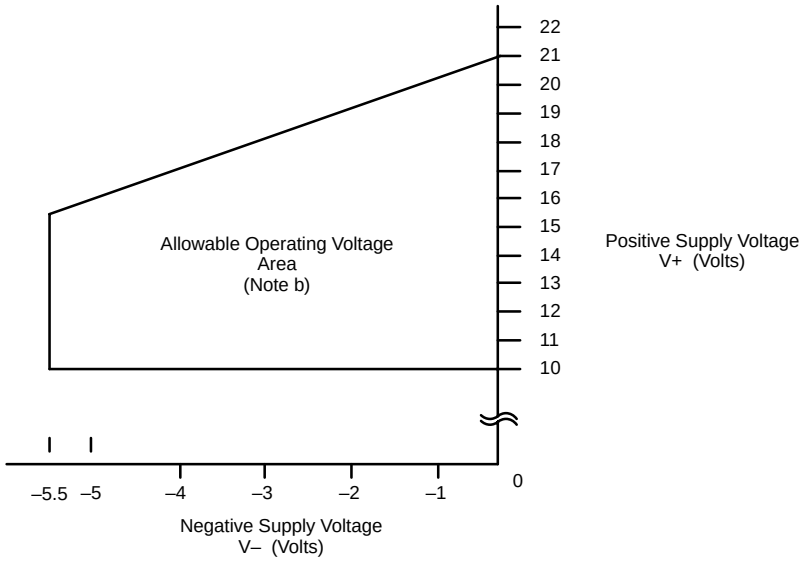


FIGURE 12. Off State Input/Output Capacitance

OPERATING VOLTAGE RANGE



Notes:
a. Both V+ and V– must have decoupling capacitors mounted as close as possible to the device pins. Typical decoupling capacitors would be 10-µF tantalum bead in parallel with 100-nF ceramic disc.
b. Production tested with V+ = 15 V and V– = –3 V.
a. For V_L = 5 V ±10%, 0.8- or 2-V TTL compatibility is maintained over the entire operating voltage range.

FIGURE 13.

PIN DESCRIPTION

Symbol	Pin Number		Description
	DG534ADJ	DG538A	
D_A	2	2	Analog Output/Input
V+	3	3	Positive Supply Voltage
S_{A1}	4	4	Analog Input/Output
S_{A2}	6	6	Analog Input/Output
S_{A3}	–	8	Analog Input/Output
S_{A4}	–	10	Analog Input/Output
$\overline{4}$/2	7	–	4 x 1 or 2 x 2 Select
$\overline{8}$/4	–	11	8 x 1 or 4 x 2 Select
$\overline{RS}$	8	12	Reset
$\overline{WR}$	9	13	Write command that latches A, EN
A_0, A_1, A_2	11, 10, –	16, 15, 14	Binary address inputs that determine which channel(s) is/are connected to the output(s)
EN	12	17	Enable. Input/Output, if EN = 0, all channels are open
$\overline{I}$/O	13	18	Input/Output control. Used to write to or read from the address latches
V_L	14	19	Logic Supply Voltage, usually +5 V
S_{B4}	–	20	Analog Input/Output
S_{B3}	–	22	Analog Input/Output
S_{B2}	15	24	Analog Input/Output
S_{B1}	17	26	Analog Input/Output
V–	18	27	Negative Supply Voltage
D_B	19	28	Analog Output/Input
GND	1, 5, 16	1, 5, 7, 9, 21, 23, 25	Analog and Digital Grounds. All grounds should be connected externally to optimize dynamic performance

APPLICATIONS

Device Description

The DG534A/538A D/CMOS wideband multiplexers offer single-ended or differential functions. A $\overline{8}$/4 or $\overline{4}$/2 logic input pin selects the single-ended or differential mode.

To meet the high dynamic performance demands of video, high definition TV, digital data routing (in excess of 100 Mbps), etc., the DG534A/538A are fabricated with DMOS transistors configured in ‘T’ arrangements with second level ‘L’ configurations (see Functional Block Diagram).

Use of DMOS technology yields devices with very low capacitance and low $r_{DS(on)}$. This directly relates to improved high frequency signal handling and higher switching speeds, while maintaining low insertion loss figures. The ‘T’ and ‘L’ switch configurations further improve dynamic performance by greatly reducing crosstalk and output node capacitances.

The DG534A/DG538A are improved pin-compatible replacements for the non-A versions. Improvements include: higher current readback drivers, readback of the EN bit, latchup protection

Frequency Response

A single multiplexer on-channel exhibits both resistance [$r_{DS(on)}$] and capacitance [$C_{S(on)}$]. This RC combination causes a frequency dependent attenuation of the analog signal. The –3-dB bandwidth of the DG534A/538A is typically 500 MHz (into 50 Ω). This figure of 500 MHz illustrates that the switch-channel cannot be represented by a simple RC combination. The on capacitance of the channel is distributed along the on-resistance, and hence becomes a more complex multi-stage network of R’s and C’s making up the total $r_{DS(on)}$ and $C_{S(on)}$.

APPLICATIONS (CONT'D)

Power Supplies and Decoupling

A useful feature of the DG534A/538A is its power supply flexibility. It can be operated from unipolar supplies (V– connected to 0 V) if required. Allowable operating voltage ranges are shown in Figure 13.

Note that the analog signal must not go below V– by more than 0.3 V (see absolute maximum ratings). However, the addition of a V– pin has a number of advantages:

a. It allows flexibility in analog signal handling, i.e. with V– = –5 V and V+ = 15 V, up to ±5 V ac signals can be accepted.

b. The value of on capacitance ($C_{S(on)}$) may be reduced by increasing the reverse bias across the internal FET body to source junction. V+ has no effect on $C_{S(on)}$.

   It is useful to note that tests indicate that optimum video differential phase and gain occur when V– is –3 V.

c. V– eliminates the need to bias an ac analog signal using potential dividers and large decoupling capacitors.

It is established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG534/538 is adversely affected by poor decoupling of power supply pins. Also, since the substrate of the device is connected to the negative supply, proper decoupling of this pin is essential.

Rules:

a. Decoupling capacitors should be incorporated on all power supply pins (V+, V–, V_L).

b. They should be mounted as close as possible to the device pins.

c. Capacitors should have good frequency characteristics - tantalum bead and/or ceramic disc types are suitable. Recommended decoupling capacitors are 1- to 10-µF tantalum bead, in parallel with 100-nF ceramic or polyester.

d. Additional high frequency protection may be provided by 51-Ω carbon film resistors connected in series with the power supply pins (see Figure 14).

Board Layout

PCB layout rules for good high frequency performance must also be observed to achieve the performance boasted by the DG534A/538A. Some tips for minimizing stray effects are:

a. Use extensive ground planes on double sided PCB separating adjacent signal paths. Multilayer PCB is even better.

b. Keep signal paths as short as practically possible with all channel paths of near equal length.

c. Use strip-line layout techniques.

Improvements in performance can be obtained by using PLCC parts instead of DIPs. The stray effects of the quad PLCC package are lower than those of the dual-in-line packages. Sockets for the PLCC packages usually increase crosstalk.

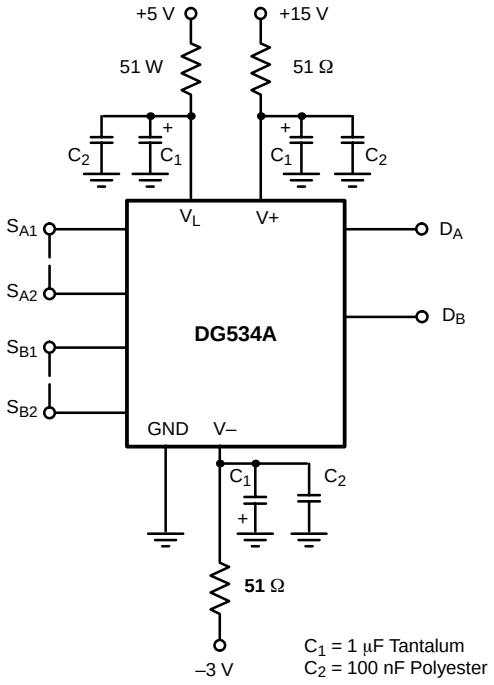


FIGURE 14. DG534A Power Supply Decoupling

Interfacing

Logic interfacing is easily accomplished. Comprehensive addressing and control functions are incorporated in the design.

The V_L pin permits interface to various logic types. The device is primarily designed to be TTL or CMOS logic compatible with +5 V applied to V_L. The actual logic threshold can be raised simply by increasing V_L.

APPLICATIONS (CONT'D)

A typical switching threshold versus V_L is shown in Figure 15.

These devices feature an address readback (Tally) facility, whereby the last address written to the device may be output to the system. This allows improved status monitoring and hand shaking without additional external components.

This function is controlled by the $\overline{I}$/O pin, which directly addresses the tri-state buffers connected to the EN and address pins. EN and address pins can be assigned to accept data (when $\overline{I}$/O = 0; $\overline{WR}$ = 0; $\overline{RS}$ = 1), or output data (when $\overline{I}$/O = 1; $\overline{WR}$ = 1; $\overline{RS}$ = 1), or to reflect a high impedance and latched state (when $\overline{I}$/O = 0; $\overline{WR}$ = 1; $\overline{RS}$ = 1).

When $\overline{I}$/O is high, the address output can sink or source current. Note that V_L is the logic high output condition. This point must be respected if V_L is varied for input logic threshold shifting.

Further control pins facilitate easy microprocessor interface. On chip address, data latches are activated by $\overline{WR}$, which serves as a strobe type function eliminating the need for peripheral latch or memory I/O port devices. Also, for ease of interface, a direct reset function ($\overline{RS}$) allows all latches to be cleared and switches opened. Reset should be used during power up, etc., to avoid spurious switch action. See Figure 16.

Channel address data can only be entered during $\overline{WR}$ low, when the address latches are transparent and $\overline{I}$/O is low. Similarly, address readback is only operational when $\overline{WR}$ and $\overline{I}$/O are high.

The Siliconix CLC410 Video amplifier is recommended as an output buffer to reduce insertion loss and to drive coaxial cables. For low power video routing applications or for unity gain input buffers CLC111/CLC114 are recommended.

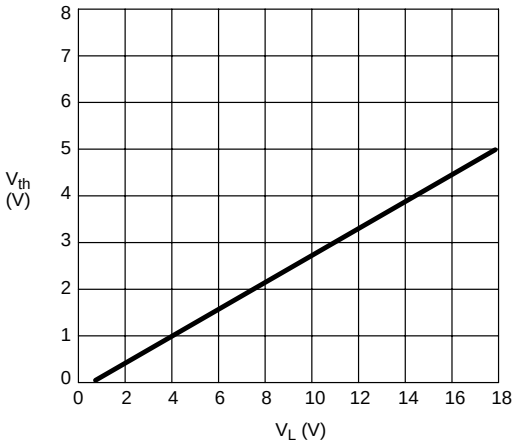


FIGURE 15. Switching Threshold Voltage vs. V_L

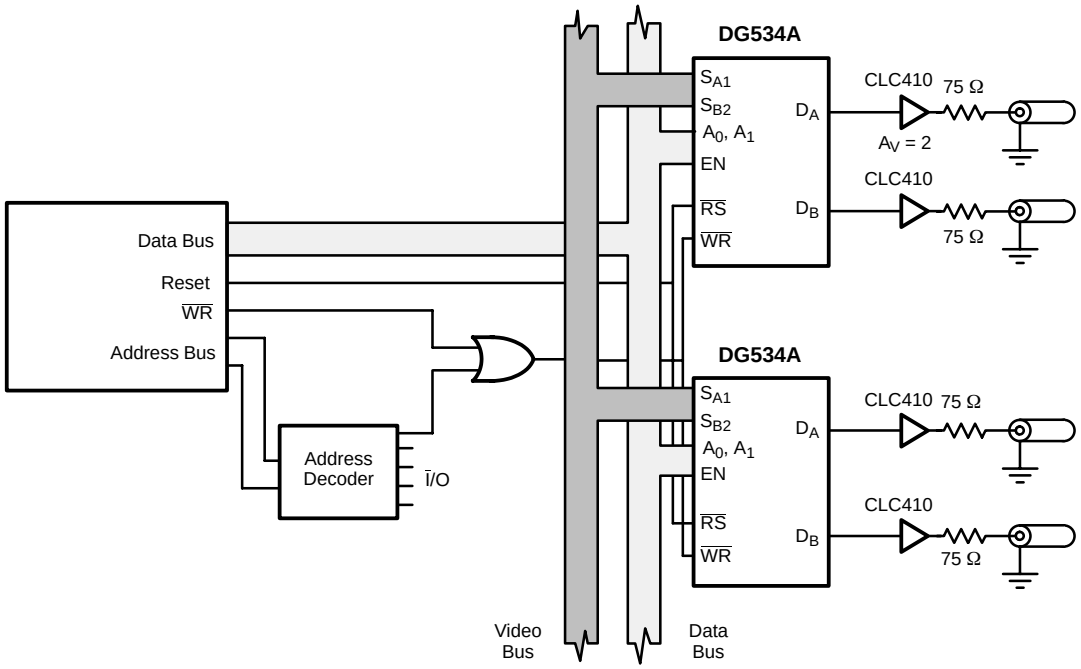


FIGURE 16. DG534A in a Video Matrix

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