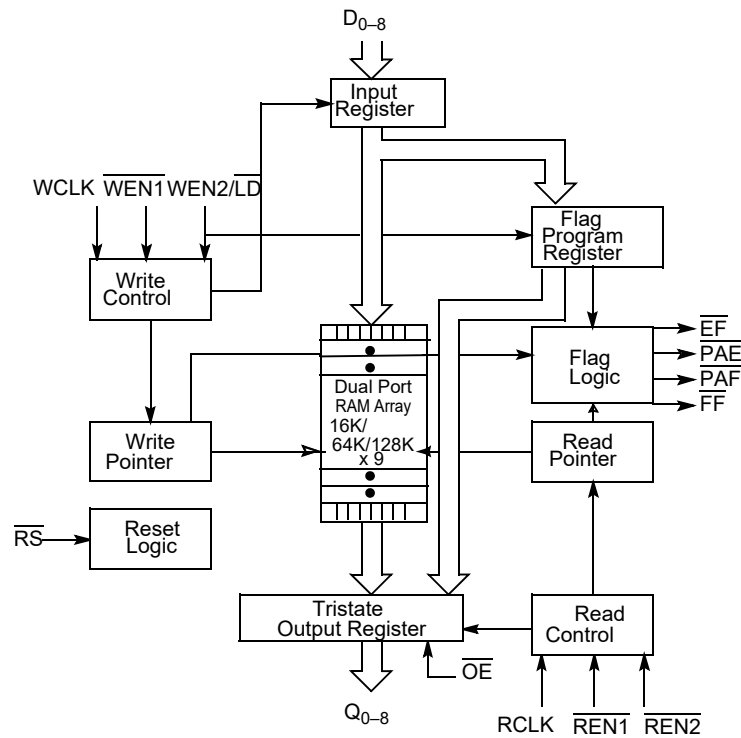


## Logic Block Diagram

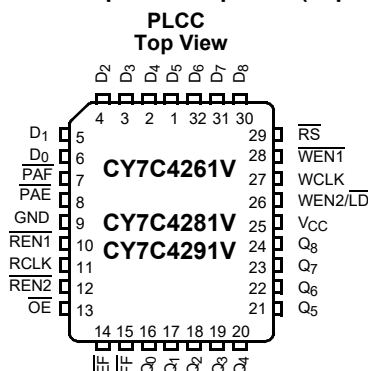


## Contents

<b>Pin Configuration .....</b>	<b>4</b>	<b>Switching Characteristics .....</b>	<b>10</b>
<b>Pin Definitions .....</b>	<b>4</b>	<b>Switching Waveforms .....</b>	<b>11</b>
<b>Architecture .....</b>	<b>5</b>	<b>Ordering Information .....</b>	<b>18</b>
<b>Resetting the FIFO .....</b>	<b>5</b>	Ordering Code Definitions .....	18
<b>FIFO Operation .....</b>	<b>5</b>	<b>Package Diagram .....</b>	<b>19</b>
<b>Programming .....</b>	<b>5</b>	<b>Acronyms .....</b>	<b>20</b>
Programmable Flag (PAE, PAF) Operation .....	6	<b>Document Conventions .....</b>	<b>20</b>
<b>Width-Expansion Configuration .....</b>	<b>7</b>	Units of Measure .....	20
<b>Flag Operation .....</b>	<b>7</b>	<b>Document History Page .....</b>	<b>21</b>
Full Flag .....	7	<b>Sales, Solutions, and Legal Information .....</b>	<b>23</b>
Empty Flag .....	7	Worldwide Sales and Design Support .....	23
<b>Maximum Ratings .....</b>	<b>8</b>	Products .....	23
<b>Operating Range .....</b>	<b>8</b>	PSoC® Solutions .....	23
<b>Electrical Characteristics .....</b>	<b>8</b>	Cypress Developer Community .....	23
<b>Capacitance .....</b>	<b>8</b>	Technical Support .....	23
<b>AC Test Loads and Waveforms .....</b>	<b>9</b>		

## Pin Configuration

Figure 1. 32-pin PLCC pinout (Top View)



## Pin Definitions

Pin No.	Signal Name	Description	I/O	Description
1–6, 30–32	D <sub>0–8</sub>	Data inputs	I	Data inputs for 9-bit bus.
16–24	Q <sub>0–8</sub>	Data outputs	O	Data outputs for 9-bit bus.
28	WEN1	Write enable 1	I	The only write enable when device is configured to have programmable flags. Data is written on a LOW-to-HIGH transition of WCLK when WEN1 is asserted and FF is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when WEN1 is LOW and WEN2/LD and FF are HIGH.
26	WEN2/LD Dual mode pin	Write enable 2 Load	I	If HIGH at reset, this pin operates as a second write enable. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. WEN1 must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the FF is LOW. If the FIFO is configured to have programmable flags, WEN2/LD is held LOW to write or read the programmable flag offsets.
10, 12	REN1, REN2	Read enable inputs	I	Enables the device for Read operation. Both REN1 and REN2 must be asserted to allow a read operation.
27	WCLK	Write clock	I	The rising edge clocks data into the FIFO when WEN1 is LOW and WEN2/LD is HIGH and the FIFO is not full. When LD is asserted, WCLK writes data into the programmable flag-offset register.
11	RCLK	Read clock	I	The rising edge clocks data out of the FIFO when REN1 and REN2 are LOW and the FIFO are not Empty. When WEN2/LD is LOW, RCLK reads data out of the programmable flag-offset register.
14	EF	Empty flag	O	When EF is LOW, the FIFO is empty. EF is synchronized to RCLK.
15	FF	Full flag	O	When FF is LOW, the FIFO is full. FF is synchronized to WCLK.
8	PAE	Programmable almost empty	O	When PAE is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO. PAE is synchronized to RCLK.
7	PAF	Programmable almost full	O	When PAF is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. PAF is synchronized to WCLK.
29	RS	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
13	OE	Output enable	I	When OE is LOW, the FIFO's data outputs drive the bus to which they are connected. If OE is HIGH, the FIFO's outputs are in High Z (high-impedance) state.

## Architecture

The CY7C4261/81/91V consists of an array of 16K, 64K, or 128K words of nine bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, REN1, REN2, WEN1, WEN2, RS), and flags (EF, PAE, PAF, FF).

## Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ( $\overline{RS}$ ) cycle. This causes the FIFO to enter the Empty condition signified by  $\overline{EF}$  being LOW. All data outputs ( $Q_{0-8}$ ) go LOW  $t_{RSF}$  after the rising edge of  $\overline{RS}$ . In order for the FIFO to reset to its default state, the user must not read or write while  $\overline{RS}$  is LOW. All flags are guaranteed to be valid  $t_{RSF}$  after  $\overline{RS}$  is taken LOW.

## FIFO Operation

When the  $\overline{WEN1}$  signal is active LOW,  $\overline{WEN2}$  is active HIGH, and FF is active HIGH, data present on the  $D_{0-8}$  pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the  $\overline{REN1}$  and  $\overline{REN2}$  signals are active LOW and EF is active HIGH, data in the FIFO memory will be presented on the  $Q_{0-8}$  outputs. New data will be presented on each rising edge of RCLK while  $\overline{REN1}$  and  $\overline{REN2}$  are active.  $\overline{REN1}$  and  $\overline{REN2}$  must set up  $t_{ENS}$  before RCLK for it to be a valid read function.  $\overline{WEN1}$  and  $\overline{WEN2}$  must occur  $t_{ENS}$  before WCLK for it to be a valid write function.

An output enable ( $\overline{OE}$ ) pin is provided to three-state the  $Q_{0-8}$  outputs when  $\overline{OE}$  is asserted. When  $\overline{OE}$  is enabled (LOW), data in the output register will be available to the  $Q_{0-8}$  outputs after  $t_{OE}$ . If devices are cascaded, the  $\overline{OE}$  function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its  $Q_{0-8}$  outputs even after additional reads occur.

**Write Enable 1 ( $\overline{WEN1}$ ).** If the FIFO is configured for programmable flags, Write Enable 1 ( $\overline{WEN1}$ ) is the only write enable control pin. In this configuration, when Write Enable 1 ( $\overline{WEN1}$ ) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

**Write Enable 2/Load ( $\overline{WEN2/LD}$ ).** This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows for depth expansion. If Write Enable 2/Load ( $\overline{WEN2/LD}$ ) is set active HIGH at Reset ( $\overline{RS} = \text{LOW}$ ), this pin operates as a second write enable pin.

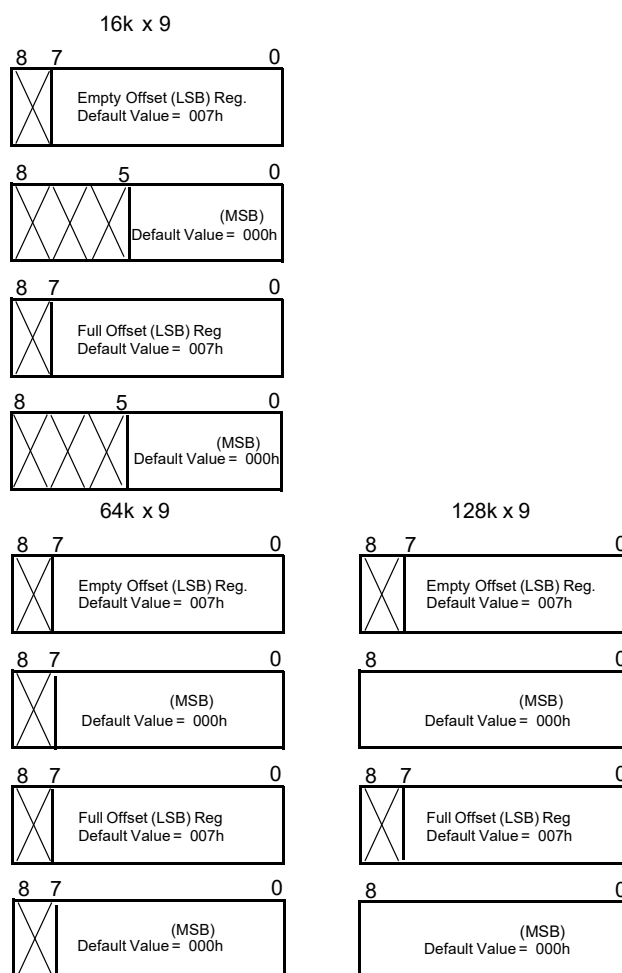
If the FIFO is configured to have two write enables, when Write Enable ( $\overline{WEN1}$ ) is LOW and Write Enable 2/Load ( $\overline{WEN2/LD}$ ) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

## Programming

When  $\overline{WEN2/LD}$  is held LOW during Reset, this pin is the load ( $\overline{LD}$ ) enable for flag offset programming. In this configuration,  $\overline{WEN2/LD}$  can be used to access the four 9-bit offset registers contained in the CY7C4261/81/91V for writing or reading data to these registers.

When the device is configured for programmable flags and both  $\overline{WEN2/LD}$  and  $\overline{WEN1}$  are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when  $\overline{WEN2/LD}$  and  $\overline{WEN1}$  are LOW. The fifth LOW-to-HIGH transition of WCLK while  $\overline{WEN2/LD}$  and  $\overline{WEN1}$  are LOW writes data to the empty LSB register again. Figure 2 shows the registers sizes and default values for the various device types.

**Figure 2. Offset Register Location and Default Values**



It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the  $\overline{WEN2/LD}$  input HIGH, the FIFO is returned to normal read



and write operation. The next time  $\overline{\text{WEN2/LD}}$  is brought LOW, a write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when  $\overline{\text{WEN2/LD}}$  is LOW and both  $\overline{\text{REN1}}$  and  $\overline{\text{REN2}}$  are LOW. LOW-to-HIGH transitions of RCLK read register contents to the data outputs. Writes and reads should not be performed simultaneously on the offset registers.



### Programmable Flag ( $\overline{\text{PAE}}$ , $\overline{\text{PAF}}$ ) Operation

Whether the flag offset registers are programmed as described in Table 1 or the default values are used, the programmable almost-empty flag ( $\overline{\text{PAE}}$ ) and programmable almost-full flag ( $\overline{\text{PAF}}$ ) states are determined by their corresponding offset registers and the difference between the read and write pointers.

**Table 1. Writing the Offset Registers** <sup>[1]</sup>

$\overline{\text{LD}}$	$\overline{\text{WEN}}$	WCLK	Selection
0	0		Empty offset (LSB) Empty offset (MSB) Full offset (LSB) Full offset (MSB)
0	1		No operation

**Table 1. Writing the Offset Registers (continued)** <sup>[1]</sup>

$\overline{\text{LD}}$	$\overline{\text{WEN}}$	WCLK	Selection
1	0		Write into FIFO
1	1		No operation

The number formed by the empty offset least significant bit register and empty offset most significant bit register is referred to as  $n$  and determines the operation of  $\overline{\text{PAE}}$ .  $\overline{\text{PAE}}$  is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains  $n$  or fewer unread words.  $\overline{\text{PAE}}$  is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains  $(n+1)$  or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as  $m$  and determines the operation of  $\overline{\text{PAF}}$ .  $\overline{\text{PAF}}$  is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4261V ( $16k - m$ ), CY7C4281V ( $64k - m$ ) and CY7C4291V ( $128k - m$ ).  $\overline{\text{PAF}}$  is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than  $m$ .

**Table 2. Status Flags**

Number of Words in FIFO			$\overline{\text{FF}}$	$\overline{\text{PAF}}$	$\overline{\text{PAE}}$	$\overline{\text{EF}}$
CY7C4261V	CY7C4281V	CY7C4291V				
0	0	0	H	H	L	L
1 to $n^{[2]}$	1 to $n^{[2]}$	1 to $n^{[2]}$	H	H	L	H
$(n + 1)$ to $(16384 - (m + 1))$	$(n + 1)$ to $(65536 - (m + 1))$	$(n + 1)$ to $(131072 - (m + 1))$	H	H	H	H
$(16384 - m)^{[3]}$ to 16383	$(65536 - m)^{[3]}$ to 65535	$(131072 - m)^{[3]}$ to 131071	H	L	H	H
16384	65536	131072	L	L	H	H

#### Notes

- The same selection sequence applies to reading from the registers.  $\overline{\text{REN1}}$  and  $\overline{\text{REN2}}$  are enabled and a read is performed on the LOW-to-HIGH transition of RCLK.
- $n$  = Empty Offset ( $n = 7$  default value).
- $m$  = Full Offset ( $m = 7$  default value).

## Width-Expansion Configuration

Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags ( $\overline{EF}$  and  $\overline{FF}$ ). The partial status flags ( $\overline{PAE}$  and  $\overline{PAF}$ ) can be detected from any one device. [Figure 3](#) demonstrates a 18-bit word width by using two CY7C42x1Vs. Any word width can be attained by adding additional CY7C42x1Vs.

When the CY7C42x1V is in a Width-Expansion Configuration, the Read Enable ( $\overline{REN2}$ ) control input can be grounded (see [Figure 3](#)). In this configuration, the Write Enable 2/Load ( $\overline{WEN2/LD}$ ) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

## Flag Operation

The CY7C4261/81/91V devices provide five flag pins to indicate the condition of the FIFO contents. Empty, Full,  $\overline{PAE}$ , and  $\overline{PAF}$  are synchronous.

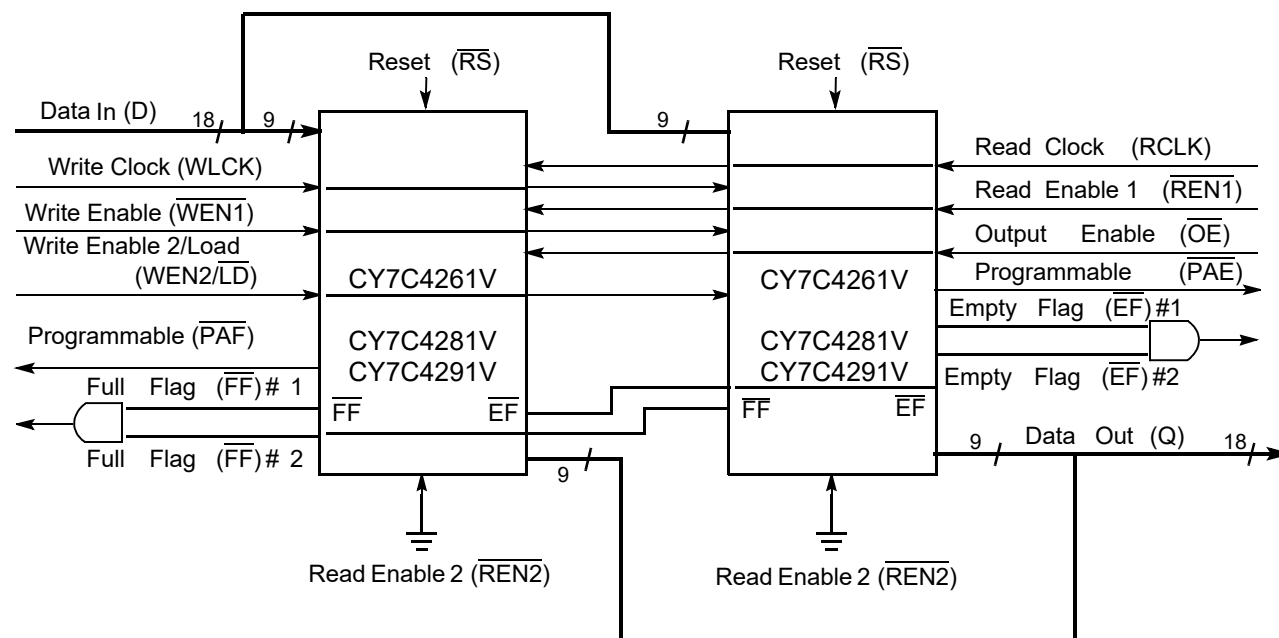
### Full Flag

The Full Flag ( $\overline{FF}$ ) will go LOW when the device is full. Write operations are inhibited whenever  $\overline{FF}$  is LOW regardless of the state of  $\overline{WEN1}$  and  $\overline{WEN2/LD}$ .  $\overline{FF}$  is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

### Empty Flag

The Empty Flag ( $\overline{EF}$ ) will go LOW when the device is empty. Read operations are inhibited whenever  $\overline{EF}$  is LOW, regardless of the state of  $\overline{REN1}$  and  $\overline{REN2}$ .  $\overline{EF}$  is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

**Figure 3. Block Diagram of 16K/64K/128K × 9 Low-Voltage Deep Sync FIFO Memory used in a Width-Expansion Configuration**



## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature

with power applied ..... -55 °C to +125 °C

Supply voltage to ground potential ..... -0.5 V to +3.6 V

DC voltage applied to outputs

in High-Z state ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage ..... -0.5 V to  $V_{CC} + 0.5$  V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage

(per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}^{[4]}$
Commercial	0 °C to +70 °C	3.3 V ± 300 mV

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	7C4261/81V-10		7C4261/91V-15		Unit
			Min	Max	Min	Max	
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Min.},$ $I_{OH} = -1.0$ mA	2.4	—	2.4	—	V
		$V_{CC} = 3.0$ V, $I_{OH} = -2.0$ mA					
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Min.},$ $I_{OL} = 4.0$ mA	—	0.4	—	0.4	V
		$V_{CC} = 3.0$ V, $I_{OL} = 8.0$ mA					
$V_{IH}$	Input HIGH voltage	—	2.0	$V_{CC}$	2.0	$V_{CC}$	V
$V_{IL}$	Input LOW voltage	—	-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input leakage current	$V_{CC} = \text{Max.}$	-10	+10	-10	+10	μA
$I_{OZL}$ $I_{OZH}$	Output OFF, High Z current	$\overline{OE} \geq V_{IH},$ $V_{SS} < V_O < V_{CC}$	-10	+10	-10	+10	μA
$I_{CC1}^{[5]}$	Active power supply current	— Commercial	—	25	—	25	mA
$I_{SB}^{[6]}$	Average standby current	— Commercial	—	4	—	4	mA

## Capacitance

Parameter <sup>[7]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25$ °C, $f = 1$ MHz,	5	pF
$C_{OUT}$	Output capacitance	$V_{CC} = 3.3$ V	7	pF

### Notes

4.  $V_{CC}$  Range for commercial -10 ns is 3.3 V ± 150 mV.

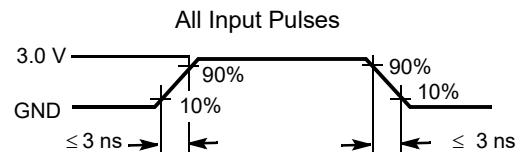
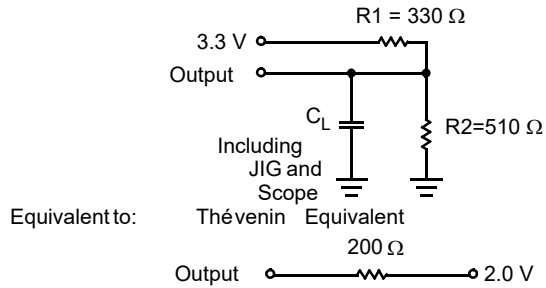
5. Input signals switch from 0 V to 3 V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency of 20 MHz, while data inputs switch at 10 MHz. Outputs are unloaded.

6. All inputs =  $V_{CC} - 0.2$  V, except WCLK and RCLK (which are at frequency = 0 MHz). All outputs are unloaded.

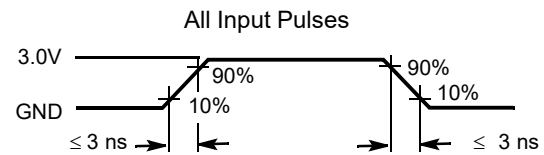
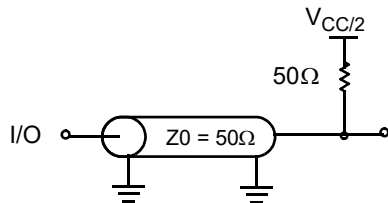
7. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms

**Figure 4. AC Test Loads and Waveforms (-15) [8, 9]**



**Figure 5. AC Test Loads and Waveforms (-10)**



### Notes

8.  $C_L = 30 \text{ pF}$  for all AC parameters except for  $t_{OHZ}$ .
9.  $C_L = 5 \text{ pF}$  for  $t_{OHZ}$ .



## Switching Characteristics

Over the Operating Range

Parameter	Description	7C4261/81V-10		7C4261/91V-15		Unit
		Min	Max	Min	Max	
$t_S$	Clock cycle frequency	–	100	–	66.7	MHz
$t_A$	Data access time	2	8	2	10	ns
$t_{CLK}$	Clock cycle time	10	–	15	–	ns
$t_{CLKH}$	Clock HIGH time	4.5	–	6	–	ns
$t_{CLKL}$	Clock LOW time	4.5	–	6	–	ns
$t_{DS}$	Data set-up time	3.5	–	4	–	ns
$t_{DH}$	Data hold time	0	–	0	–	ns
$t_{ENS}$	Enable set-up time	3.5	–	4	–	ns
$t_{ENH}$	Enable hold time	0	–	0	–	ns
$t_{RS}$	Reset pulse width <sup>[10]</sup>	10	–	15	–	ns
$t_{RSS}$	Reset set-up time	8	–	10	–	ns
$t_{RSR}$	Reset recovery time	8	–	10	–	ns
$t_{RSF}$	Reset to flag and output time	–	10	–	15	ns
$t_{OLZ}$	Output enable to output in low Z <sup>[10]</sup>	0	–	0	–	ns
$t_{OE}$	Output enable to output valid	3	7	3	10	ns
$t_{OHZ}$	Output enable to output in high Z <sup>[11]</sup>	3	7	3	8	ns
$t_{WFF}$	Write clock to full flag	–	8	–	10	ns
$t_{REF}$	Read clock to empty flag	–	8	–	10	ns
$t_{PAF}$	Clock to programmable almost-full flag	–	8	–	10	ns
$t_{PAE}$	Clock to programmable almost-full flag	–	8	–	10	ns
$t_{SKEW1}$	Skew time between read clock and write clock for empty flag and full flag	5	–	6	–	ns
$t_{SKEW2}$	Skew time between read clock and write clock for almost-empty flag and almost-full flag	10	–	15	–	ns

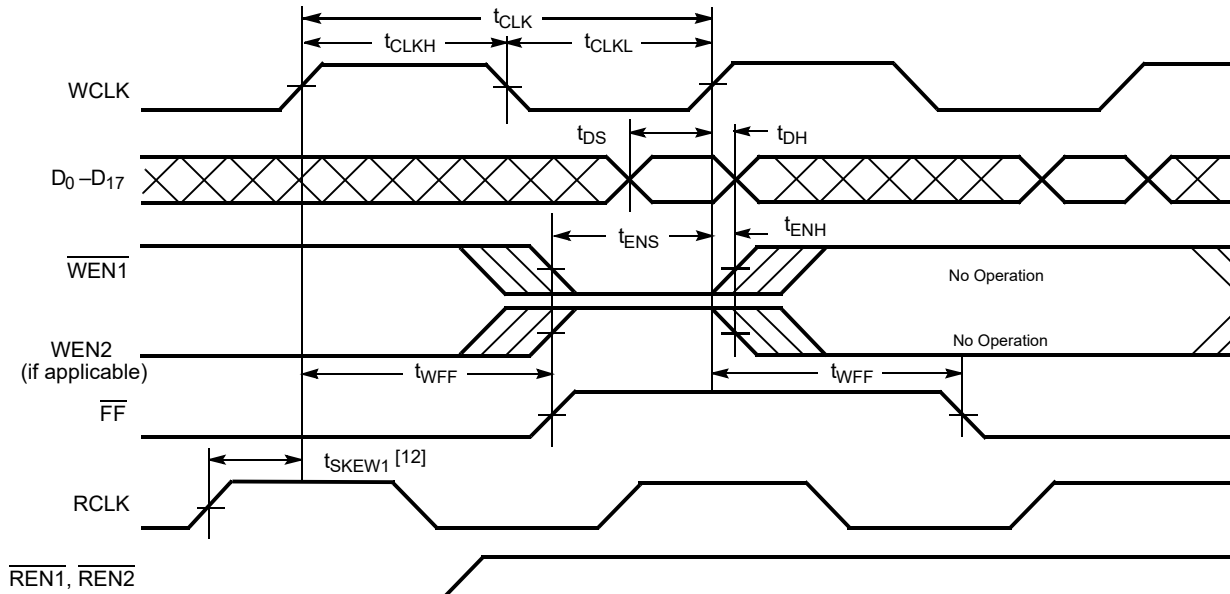
### Notes

10. Pulse widths less than minimum values are not allowed.

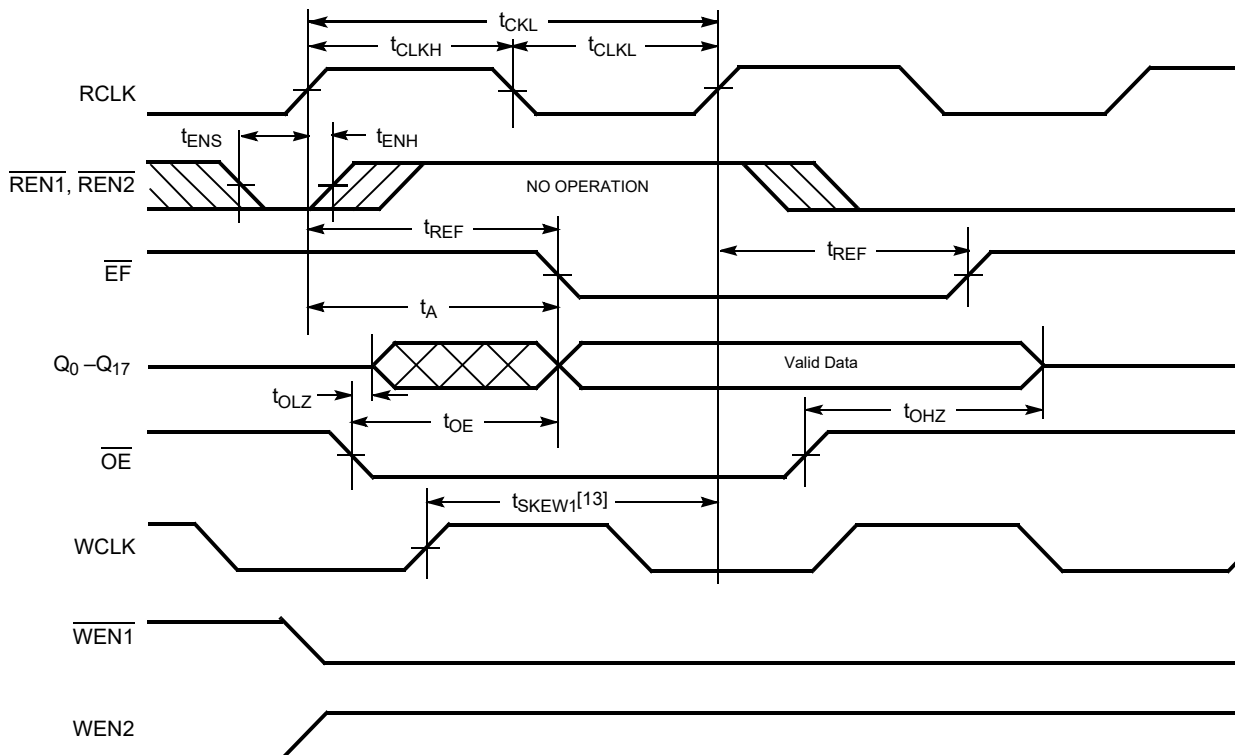
11. Values guaranteed by design, not currently tested.

## Switching Waveforms

**Figure 6. Write Cycle Timing**



**Figure 7. Read Cycle Timing**

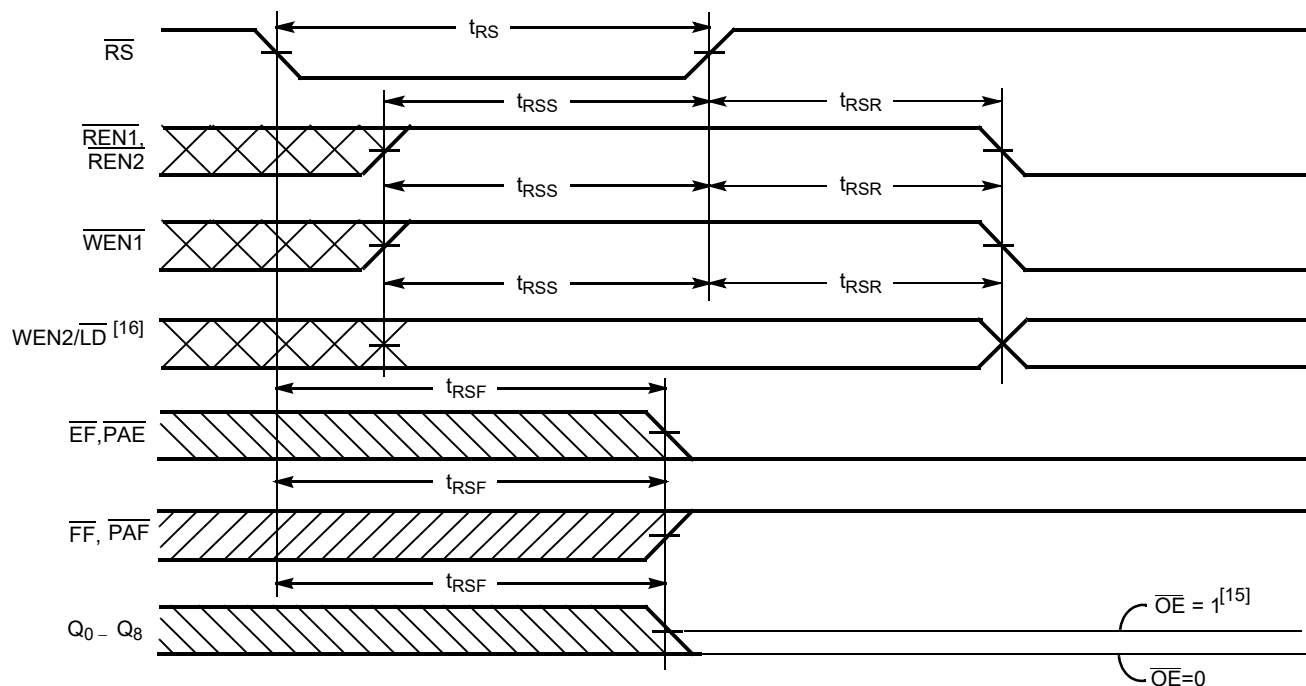


### Notes

12.  $t_{SKEW1}$  is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that  $\overline{FF}$  will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than  $t_{SKEW1}$ , then  $\overline{FF}$  may not change state until the next WCLK rising edge.
13.  $t_{SKEW1}$  is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that  $\overline{EF}$  will go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than  $t_{SKEW1}$ , then  $\overline{EF}$  may not change state until the next RCLK rising edge.

## Switching Waveforms (continued)

Figure 8. Reset Timing <sup>[14]</sup>



### Notes

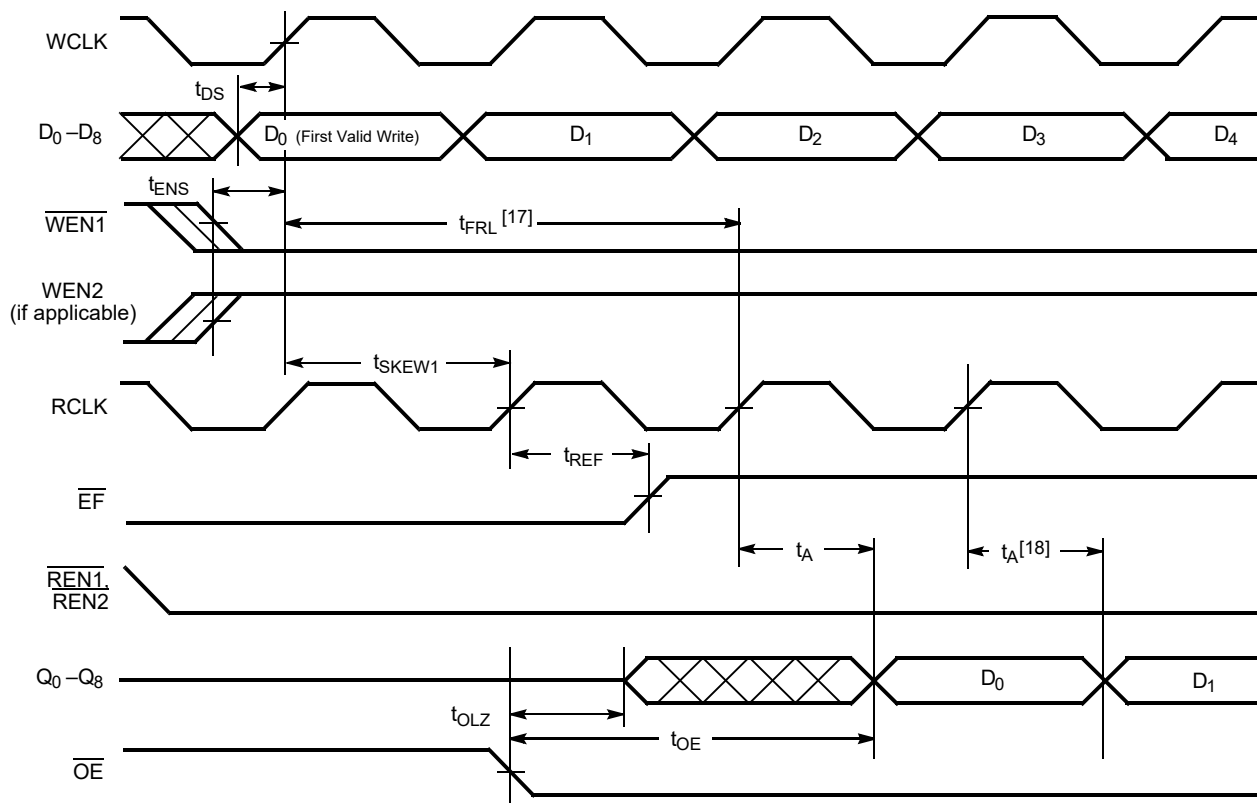
14. The clocks (RCLK, WCLK) can be free-running during reset.

15. After reset, the outputs will be LOW if  $\overline{OE} = 0$  and three-state if  $\overline{OE} = 1$ .

16. Holding  $\overline{WEN2/LD}$  HIGH during reset will make the pin act as a second enable pin. Holding  $\overline{WEN2/LD}$  LOW during reset will make the pin act as a load enable for the programmable flag offset registers.

## Switching Waveforms (continued)

Figure 9. First Data Word Latency after Reset with Read and Write

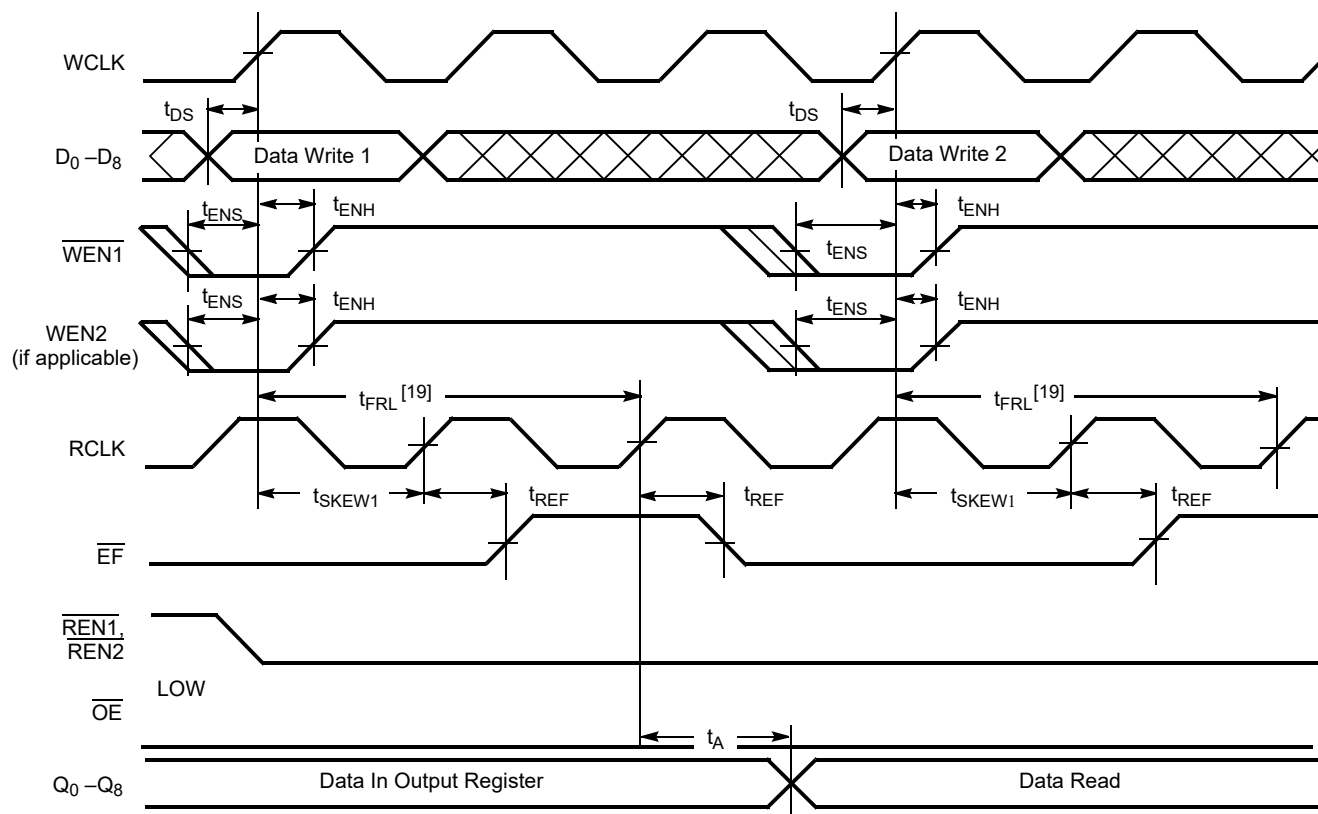


### Notes

17. When  $t_{SKEW1} \geq$  minimum specification,  $t_{FRL}$  (maximum) =  $t_{CLK} + t_{SKEW2}$ . When  $t_{SKEW1} <$  minimum specification,  $t_{FRL}$  (maximum) = either  $2 \cdot t_{CLK} + t_{SKEW1}$  or  $t_{CLK} + t_{SKEW1}$ . The Latency Timing applies only at the Empty Boundary ( $\overline{EF} = \text{LOW}$ ).
18. The first word is available the cycle after  $\overline{EF}$  goes HIGH, always.

## Switching Waveforms (continued)

Figure 10. Empty Flag Timing

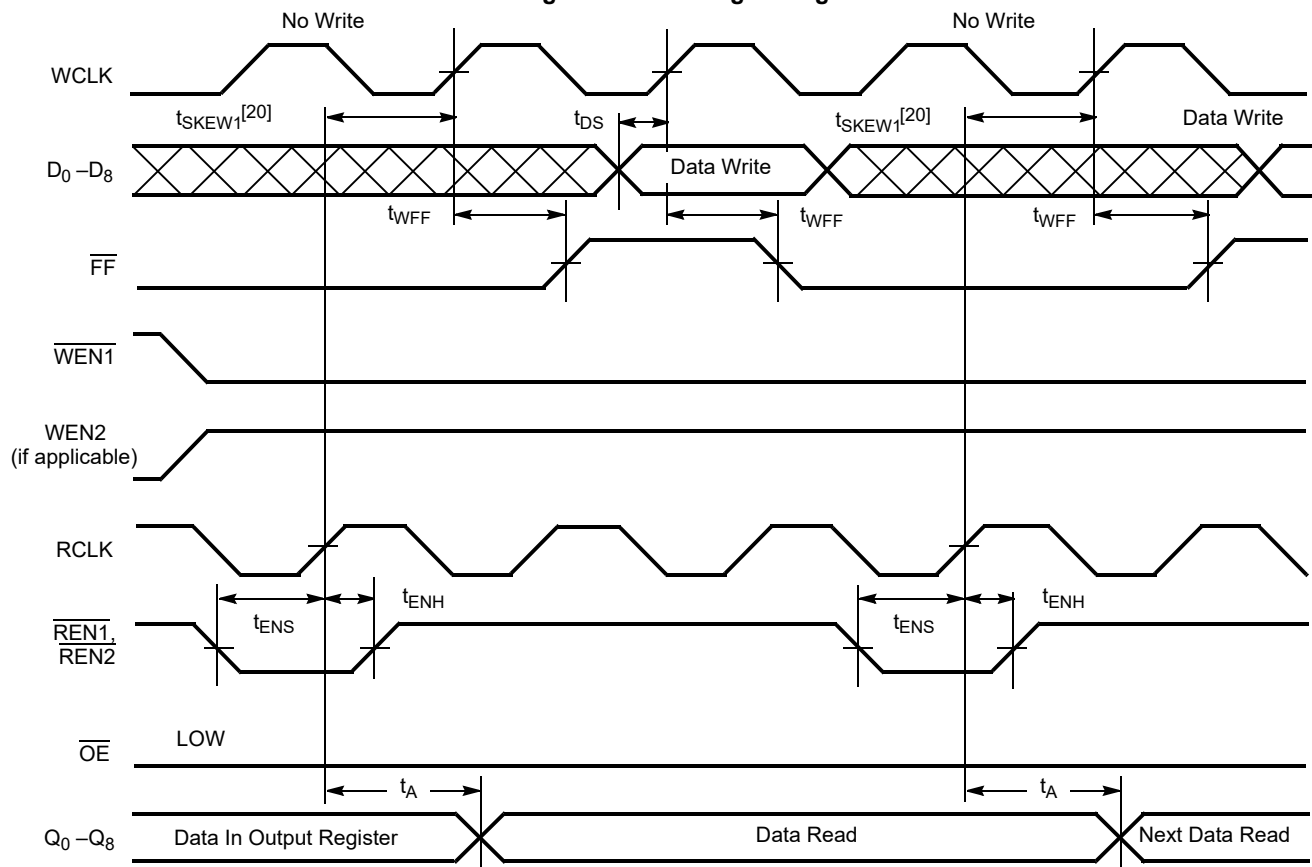


### Note

19. When  $t_{SKEW1} \geq$  minimum specification,  $t_{FRL}$  (maximum) =  $t_{CLK} + t_{SKEW2}$ . When  $t_{SKEW1} <$  minimum specification,  $t_{FRL}$  (maximum) = either  $2 \cdot t_{CLK} + t_{SKEW1}$  or  $t_{CLK} + t_{SKEW1}$ . The Latency Timing applies only at the Empty Boundary (EF = LOW).

## Switching Waveforms (continued)

Figure 11. Full Flag Timing

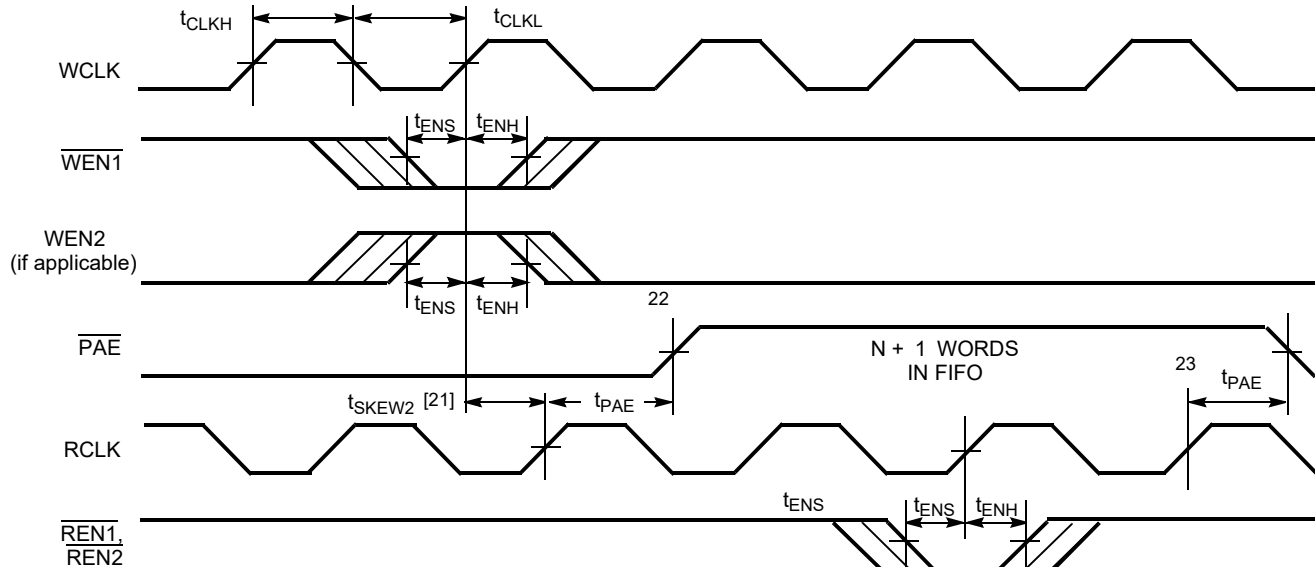


### Note

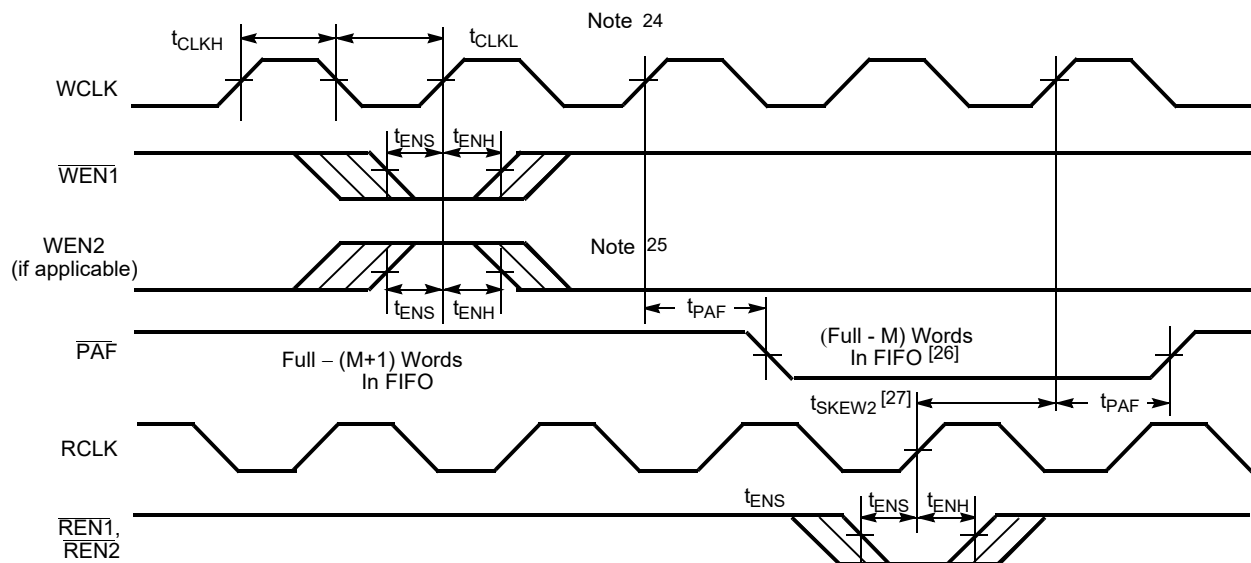
20.  $t_{SKEW1}$  is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that  $\overline{FF}$  will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than  $t_{SKEW1}$ , then  $\overline{FF}$  may not change state until the next WCLK rising edge.

## Switching Waveforms (continued)

**Figure 12. Programmable Almost Empty Flag Timing**



**Figure 13. Programmable Almost Full Flag Timing**



### Notes

21.  $t_{SKEW2}$  is the minimum time between a rising WCLK and a rising RCLK edge for  $\overline{PAE}$  to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than  $t_{SKEW2}$ , then  $\overline{PAE}$  may not change state until the next RCLK.
22.  $\overline{PAE}$  offset = n.
23. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when  $\overline{PAE}$  goes LOW.
24. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words of the FIFO when  $\overline{PAF}$  goes LOW.
25.  $\overline{PAF}$  offset = m.
26. 16K - m words for CY7C4261V, 64K - m words for CY7C4281V, and 128K - m words for CY4291V.
27.  $t_{SKEW2}$  is the minimum time between a rising RCLK edge and a rising WCLK edge for  $\overline{PAF}$  to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than  $t_{SKEW2}$ , then  $\overline{PAF}$  may not change state until the next WCLK.

## Switching Waveforms (continued)

Figure 14. Write Programmable Registers

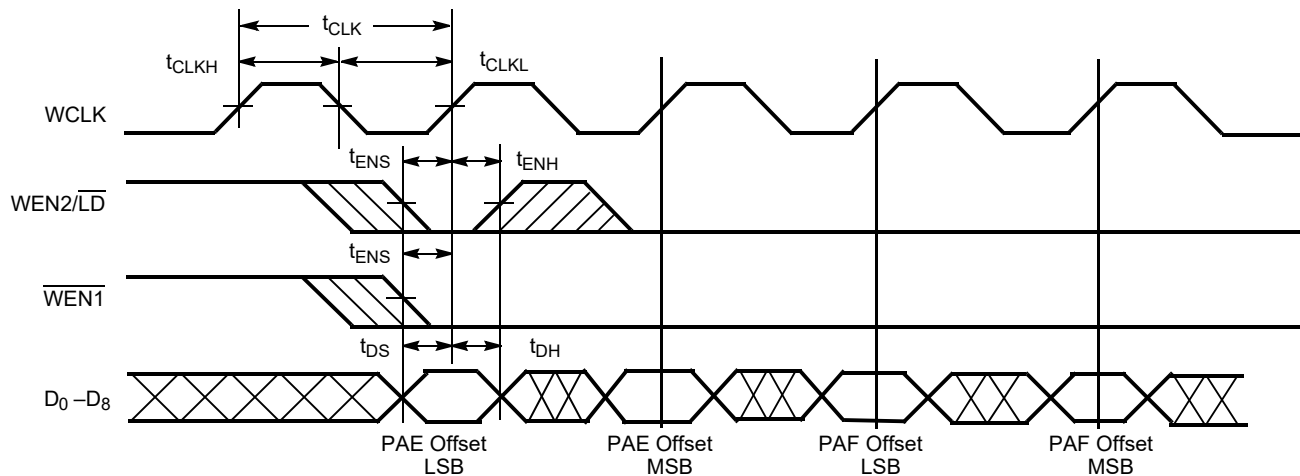
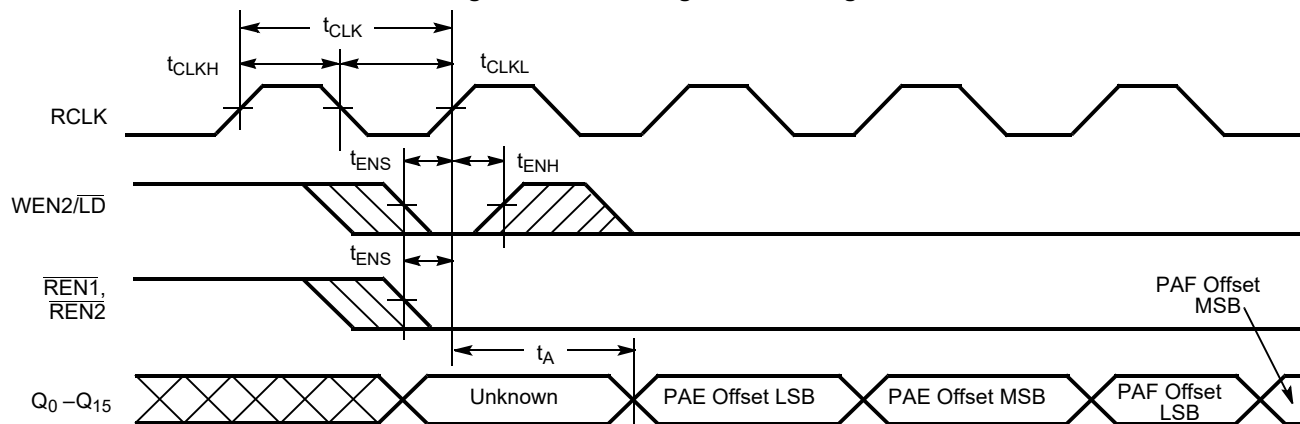


Figure 15. Read Programmable Registers

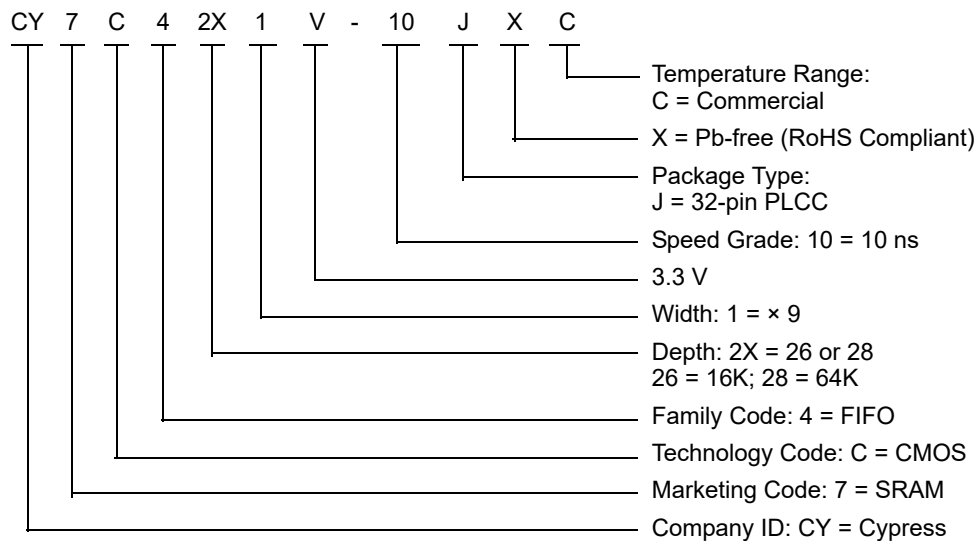




## Ordering Information

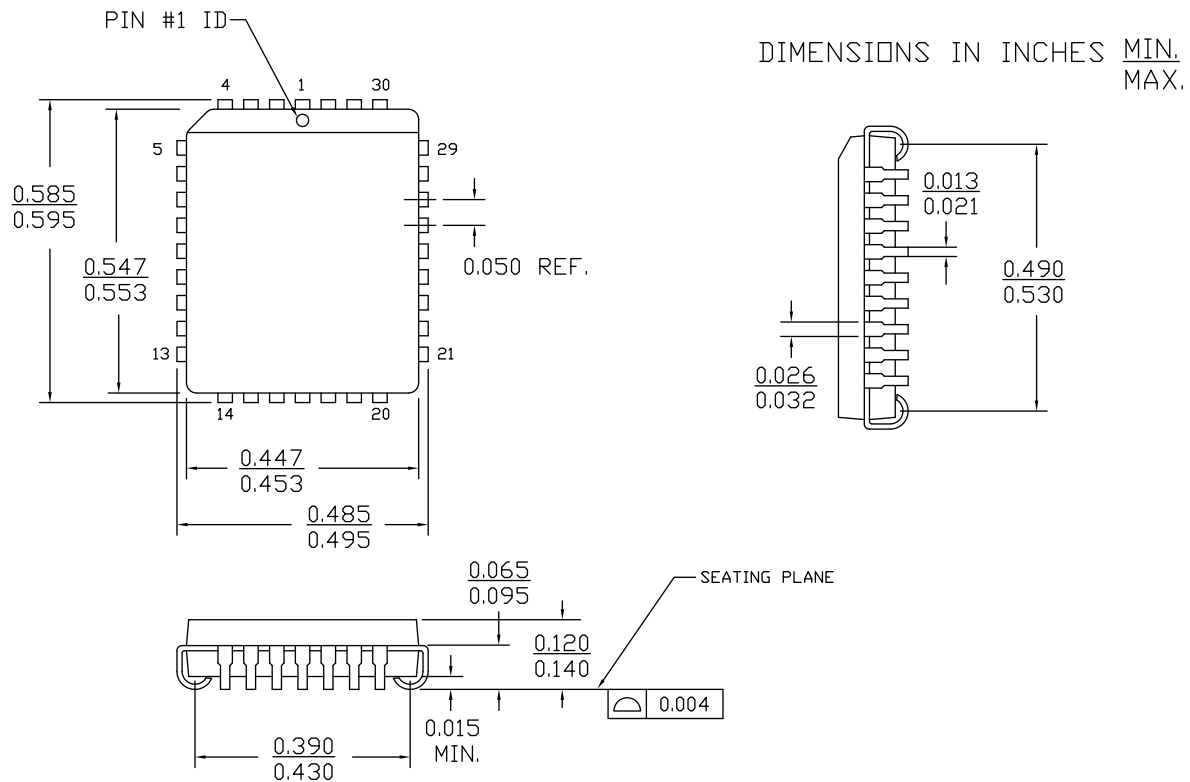
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
<b>16K × 9 Low-Voltage Deep Sync FIFO</b>				
10	CY7C4261V-10JXC	J65	32-pin Pb-free plastic leaded chip carrier	Commercial

## Ordering Code Definitions



## Package Diagram

Figure 16. 32-pin PLCC (0.453 × 0.553 Inches) J65 Package Outline, 51-85002



51-85002 \*E

## Acronyms

**Table 3. Acronyms**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

**Table 4. Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
μA	microampere
mA	milliampere
ns	nanosecond
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C4261V/CY7C4281V/CY7C4291V, 16K/64K/128K × 9 Low-Voltage Deep Sync™ FIFOs Document Number: 38-06013				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	106474	SZV	09/15/2001	Changed Spec number from 38-00656 to 38-06013.
*A	127858	FSG	09/04/2003	Updated <a href="#">Switching Waveforms</a> : Replaced $t_{\text{SKEW}2}$ with $t_{\text{SKEW}1}$ in <a href="#">Figure 10</a> . Fixed typos in <a href="#">Figure 10</a> , <a href="#">Figure 11</a> , <a href="#">Figure 12</a> , <a href="#">Figure 13</a> .
*B	386127	ESH	08/04/2005	Added Pb-free logo to top of front page. Updated <a href="#">Ordering Information</a> : Updated part numbers.
*C	2896378	RAME	03/19/2010	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Package Diagram</a> : spec 51-85002 – Changed revision from *B to *C.
*D	2906525	RAME	04/07/2010	Updated <a href="#">Ordering Information</a> : Updated part numbers.
*E	3069396	ADMU	10/22/2010	Updated <a href="#">Programming</a> : Updated <a href="#">Programmable Flag (PAE, PAF) Operation</a> : Replaced PAF with PAE in “PAF is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words”. Replaced $\overline{\text{PAE}}$ with $\overline{\text{PAF}}$ in “PAE is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4261 (16K-m) and CY7C4271 (32K-m)”. Updated <a href="#">Ordering Information</a> : No change in part numbers. Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms and Units of Measure</a> . Updated to new template.
*F	3210221	ADMU	03/25/2011	Updated <a href="#">Ordering Information</a> : Updated part numbers.
*G	3325014	ADMU	07/22/2011	Removed -25 speed bin related information in all instances across the document. Updated <a href="#">Package Diagram</a> : spec 51-85002 – Changed revision from *C to *D.
*H	3847934	ADMU	12/20/2012	Updated <a href="#">Ordering Information</a> : Updated part numbers.
*I	4486851	ADMU	08/28/2014	Removed CY7C4271V related information in all instances across the document. Removed Industrial Temperature Range related information in all instances across the document. Updated <a href="#">Selection Guide</a> : Removed CY7C4291V related information in 10 ns speed bin column. Updated <a href="#">Electrical Characteristics</a> : Removed CY7C4291V related information in 10 ns speed bin column. Updated <a href="#">Switching Characteristics</a> : Removed CY7C4291V related information in 10 ns speed bin column. Updated to new template.
*J	4581652	ADMU	11/26/2014	Updated <a href="#">Functional Description</a> : Added “For a complete list of related documentation, <a href="#">click here</a> .” at the end.

**Document History Page (continued)**

Document Title: CY7C4261V/CY7C4281V/CY7C4291V, 16K/64K/128K × 9 Low-Voltage Deep Sync™ FIFOs Document Number: 38-06013				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
*K	5437523	VINI	09/15/2016	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Package Diagram</a> : spec 51-85002 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*L	6015470	VINI	01/05/2018	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated to new template.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

Arm® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Internet of Things	<a href="http://cypress.com/iot">cypress.com/iot</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
Microcontrollers	<a href="http://cypress.com/mcu">cypress.com/mcu</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Power Management ICs	<a href="http://cypress.com/pmic">cypress.com/pmic</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless Connectivity	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

### Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation, 2001-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.