

CY62137EV30 MoBL[®]

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Pin Configurations

Figure 1. 48-ball VFBGA (Top View) $^{[1, 2]}$

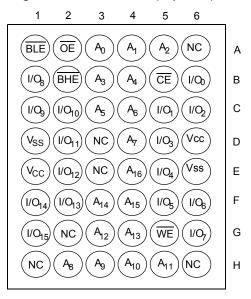


Figure 2. 44-pin TSOP II (Top View) [1]

	O 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18	44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27	A5 A6 AZOBE BLO15 I/O14 I/O13 I2 VCC11 I/O9 VCC A8
I/O ₆ ⊑ I <u>/O7</u> ⊑	15 16 17	30 29 28	I/O ₈

Product Portfolio

Product V _{CC} Range (V)							Power Di	ssipation		
		_C Range	(V)	Speed	Operating I _{CC} (mA)		– Standby I _{SB2} (μA)			
Froduct				(ns)	f = 1 MHz f = f _{max}					
	Min	Тур ^[3]	Мах		Тур ^[3]	Мах	Тур ^[3]	Мах	Тур ^[3]	Мах
CY62137EV30-45LL	2.2 V	3.0 V	3.6 V	45 ns	2	2.5	15	20	1	7

Notes

1. NC pins are not connected on the die. 2. Pins D3, H1, G2, H6 and H3 in the 48-ball VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb and 64 Mb respectively. 3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25$ °C.



Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	–65 °C to + 150 °C
Ambient temperature with power applied	–55 °C to + 125 °C
Supply voltage to ground potential ^[4, 5]	–0.3 V to (V _{CC(MAX)} + 0.3 V)
DC voltage applied to outputs in High Z state ^[4, 5]	–0.3 V to (V _{CC(MAX)} + 0.3 V)

DC input voltage ^[4, 5]	.–0.3 V to (V _{CC(MAX)} + 0.3 V)
Output current into outputs (LO	W)20 mA
Static discharge voltage (per MIL-STD-883, Method 301	5) > 2001 V
Latch up current	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V cc ^[6]
CY62137EV30-45LL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Deverseter	Decerintien	Test Com	Test Conditions 45 ns				11
Parameter	Description	lest Con	aitions	Min	Тур [7]	Max	Unit
V _{OH}	Output HIGH voltage	I _{OH} = -0.1 mA	V _{CC} = 2.20 V	2.0	_	_	V
		I _{OH} = -1.0 mA	V _{CC} = 2.70 V	2.4	_	_	V
V _{OL}	Output LOW voltage	I _{OL} = 0.1 mA	V _{CC} = 2.20 V	-	_	0.4	V
		I _{OL} = 2.1 mA	V _{CC} = 2.70 V	-	-	0.4	V
V _{IH}	Input HIGH voltage	V _{CC} = 2.2 V to 2.7	V	1.8	-	V _{CC} +0.3	V
		V _{CC} = 2.7 V to 3.6	V	2.2	_	V _{CC} + 0.3	V
VIL	Input LOW voltage	V _{CC} = 2.2 V to 2.7 V		-0.3	_	0.6	V
		V _{CC} = 2.7 V to 3.6 V		-0.3	_	0.8	V
I _{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$		–1	_	+1	μA
I _{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, Output disabled		–1	_	+1	μA
I _{CC}	V _{CC} Operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$	-	15	20	mA
		f = 1 MHz	I _{OUT} = 0 mA CMOS levels	-	2.0	2.5	
I _{SB1} ^[8]	Automatic CE power-down current — CMOS inputs	$\label{eq:constraint} \hline \hline \hline \hline CE \ge V_{CC} - 0.2 \ V \\ (BHE and BLE) \ge V \\ V_{IN} \ge V_{CC} - 0.2 \ V, \\ f = f_{max} (address a \\ f = 0 \ (OE and WE) \\ V_{CC} = 3.60 \ V \\ \hline \hline$	V _{CC} – 0.2 V, V _{IN} <u>≤</u> 0.2 V, nd data only),	_	1	7	μA
I _{SB2} ^[8]	Automatic CE power-down current — CMOS inputs		V _{CC} – 0.2 V,	-	1	7	μΑ

Notes

Notes
4. V_{IL(min.)} = -2.0 V for pulse durations less than 20 ns.
5. V_{IL(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a 100 μs ramp time from 0 to Vcc(min) and 200 μs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.
8. Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

Document Number: 38-05443 Rev. *H



Capacitance

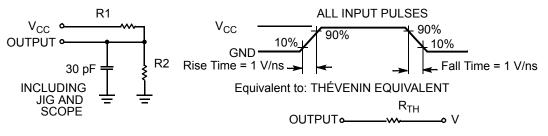
Parameter ^[9]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	$T_A = 25 \degree C$, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[9]	Description	Test Conditions	48-ball BGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	77	°C/W
Θ ^{JC}	Thermal resistance (junction to case)		10	13	°C/W

AC Test Loads and Waveforms





Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

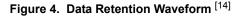


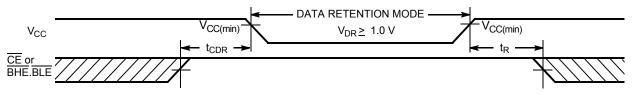
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[10]	Max	Unit
V _{DR}	V _{CC} for data retention		1	-	-	V
I _{CCDR} ^[11]	Data retention current	$\label{eq:constraint} \begin{array}{l} V_{CC} = 1 \text{ V}, \\ \overline{CE} \geq V_{CC} - 0.2 \text{ V or} \\ (\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}, \\ V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V} \end{array}$	-	0.8	3	μΑ
t _{CDR} ^[12]	Chip deselect to data retention time		0	-	_	ns
t _R ^[13]	Operation recovery time		45	-	-	ns

Data Retention Waveform





Notes

- 10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25$ °C. 11. Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ specification. Other inputs can be left floating.

- 12. Tested initially and after any design or process changes that may affect these parameters. 13. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} \ge 100 µs or stable at V_{CC(min.)} \ge 100 µs. 14. BHE.BLE is the AND of both BHE and BLE. The chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.



Switching Characteristics

Over the Operating Range

Parameter [15, 16]	Description	45	45 ns		
Parameter [10, 10]	Description	Min	Мах	Unit	
Read Cycle				-	
t _{RC}	Read cycle time	45	_	ns	
t _{AA}	Address to data valid	-	45	ns	
t _{OHA}	Data hold from address change	10	-	ns	
t _{ACE}	CE LOW to data valid	-	45	ns	
t _{DOE}	OE LOW to data valid	-	22	ns	
t _{LZOE}	OE LOW to Low Z ^[17]	5	-	ns	
t _{HZOE}	OE HIGH to High Z ^[17, 18]	_	18	ns	
t _{LZCE}	CE LOW to Low Z ^[17]	10	-	ns	
t _{HZCE}	CE HIGH to High Z ^[17, 18]	-	18	ns	
t _{PU}	CE LOW to power-up	0	-	ns	
t _{PD}	CE HIGH to power-down	-	45	ns	
t _{DBE}	BLE/BHE LOW to data valid	-	45	ns	
t _{LZBE}	BLE/BHE LOW to Low Z ^[17]	5	-	ns	
t _{HZBE}	BLE/BHE HIGH to High Z ^[17, 18]	-	18	ns	
Write Cycle ^{[19, 20}]		•		
t _{WC}	Write cycle time	45	_	ns	
t _{SCE}	CE LOW to write end	35	-	ns	
t _{AW}	Address setup to write end	35	-	ns	
t _{HA}	Address hold from write end	0	-	ns	
t _{SA}	Address setup to write start	0	_	ns	
t _{PWE}	WE pulse width	35	-	ns	
t _{BW}	BLE/BHE LOW to write end	35	-	ns	
t _{SD}	Data setup to write end	25	-	ns	
t _{HD}	Data hold from write end	0	-	ns	
t _{HZWE}	WE LOW to High Z ^[17, 18]				
t _{LZWE}	WE HIGH to Low Z ^[17]	10	-	ns	

Notes

19. Test conditions for all parameters other than in-state parameters asoline signal transition time of sits (1V/iis) of less, timing reference levels of V_{CC(typ})/2, input pulse levels of 0 to V_{CC(typ}), and output loading of the specified I_{OL}/I_{OH} as shown in Figure 3 on page 5.
16. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
27. Attemptions temperature and writers and writers are no longer applicable. They are available for download the step temption to the step temption.

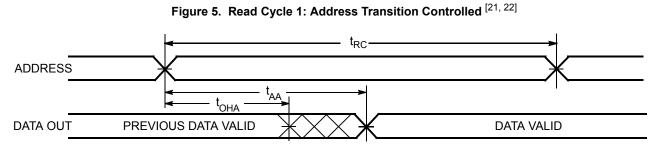
17. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZDE} is less than t_{LZDE}, and t_{HZWE} is less than t_{LZWE} for any given device

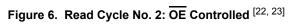
18. t_{HZOE}, t_{HZCE}, t_{HZEE}, and t_{HZWE} transitions are measured when the <u>outputs</u> enter <u>a high</u> impedance state.
19. The internal write time of the memory is defined by the overlap of WE, CE = V_{IL}. BHE and BLE = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INAC<u>TIVE</u>. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
20. The minimum pulse width for write cycle 3 (WE controlled, OE LOW) should be equal to the sum of tsp and tHzWE.

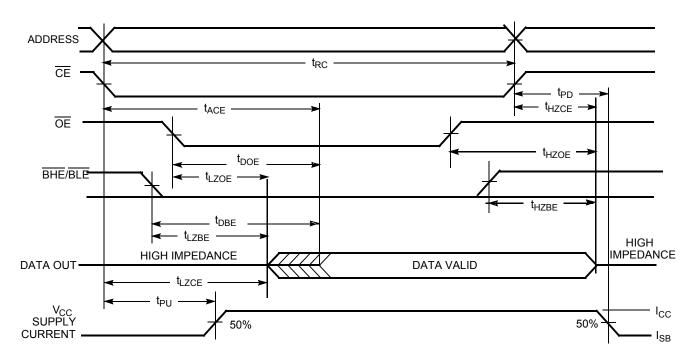
^{15.} Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of V_{CC(typ)}/2, input pulse



Switching Waveforms







Notes

21. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} and $\overline{BLE} = V_{IL}$. 22. WE is HIGH for read cycle. 23. Address valid prior to or coincident with \overline{CE} and \overline{BHE} , \overline{BLE} transition LOW.



Switching Waveforms (continued)

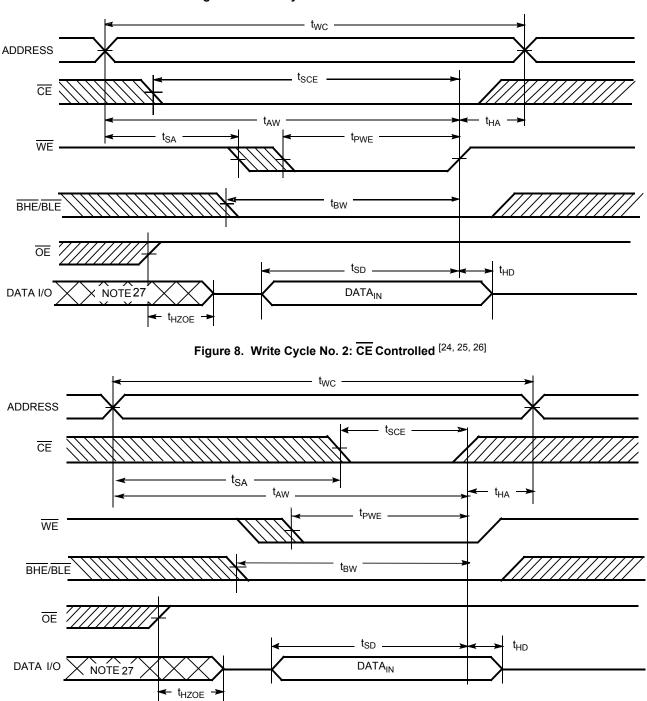


Figure 7. Write Cycle No. 1: WE Controlled ^[24, 25, 26]

Notes

- 24. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write
- 25. Data I/O is high impedance if $\overline{OE} = V_{IH.}$ 26. If \overline{CE} goes HIGH simultaneously with WE = V_{IH} , the output remains in a high impedance state.
- 27. During this period, the I/Os are in output state and input signals should not be applied.



Switching Waveforms (continued)

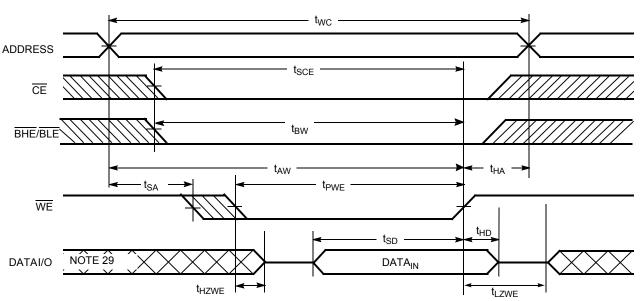
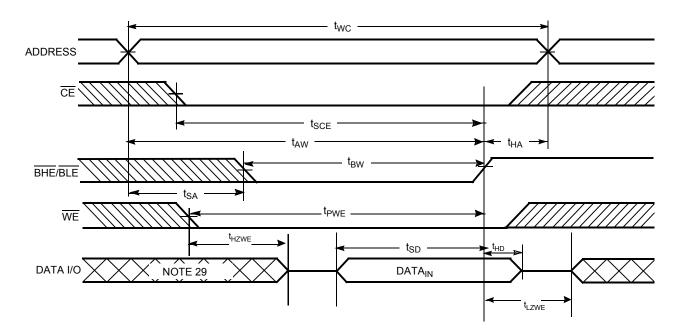


Figure 9. Write Cycle No. 3: WE Controlled, OE LOW [28]

Figure 10. Write Cycle No. 4: BHE/BLE Controlled, OE LOW [28]



Notes_____28. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state. 29. During this period, the I/Os are in output state and input signals should not be applied.





Truth Table

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
Н	Х	Х	X ^[30]	X ^[30]	High Z	Deselect/power-down	Standby (I _{SB})
X ^[30]	Х	Х	Н	Н	High Z	Deselect/power-down	Standby (I _{SB})
L	Н	L	L	L	Data out (I/O _O –I/O ₁₅)	Read	Active (I _{CC})
L	Н	L	Н	L	Data out (I/O _O –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Read	Active (I _{CC})
L	Н	L	L	Н	Data out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Read	Active (I _{CC})
L	Н	Н	L	L	High Z	Output disabled	Active (I _{CC})
L	Н	Н	Н	L	High Z	Output disabled	Active (I _{CC})
L	Н	Н	L	Н	High Z	Output disabled	Active (I _{CC})
L	L	Х	L	L	Data in (I/O _O –I/O ₁₅)	Write	Active (I _{CC})
L	L	Х	Н	L	Data in (I/O _O –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Write	Active (I _{CC})
L	L	Х	L	Н	Data in (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Write	Active (I _{CC})

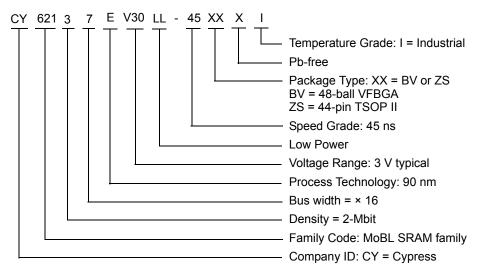
Note 30. Chip enable (\overline{CE}) and Byte enables (\overline{BHE} / \overline{BLE}) must be at fixed CMOS levels (not floating). Intermediate voltage levels on these pins is not permitted.



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62137EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
45	CY62137EV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

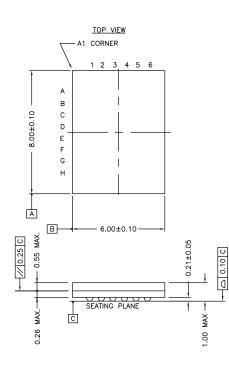
Ordering Code Definitions

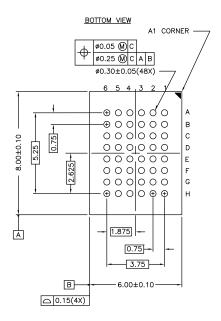




Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150





NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H



Package Diagrams (continued)

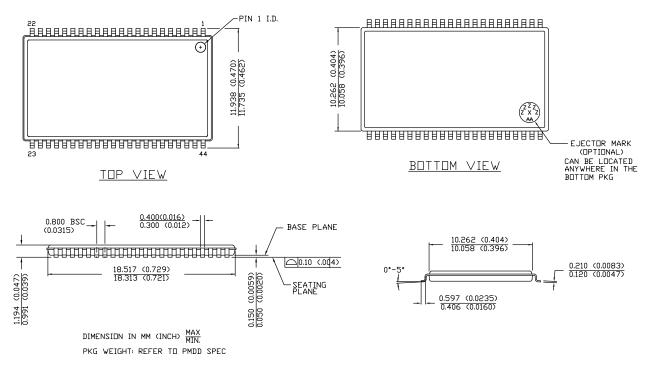


Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087

51-85087 *E





Acronyms

Acronym	Description			
BLE	byte low enable			
BHE	byte high enable			
CE	chip enable			
CMOS	complementary metal oxide semiconductor			
I/O	input/output			
OE	output enable			
SRAM	static random access memory			
TSOP	thin small outline package			
VFBGA	very fine-pitch ball gird array			
WE	write enable			

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μS	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
%	percent
pF	picofarad
Ω	ohm
V	volt
W	watt





Document History Page

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	203720	AJU	See ECN	New data sheet
*A	234196	AJU	See ECN	Changed I _{CC} MAX at f=1MHz from 1.7 mA to 2.0 mA Changed I _{CC} TYP from 12 mA (35 ns speed bin) and 10 mA (45 ns speed bin to 15 mA and 12 mA respectively Changed I _{CC} MAX from 20 mA (35 ns speed bin) and 15 mA (45 ns speed bin to 25 mA and 20 mA respectively Changed I _{SB1} and I _{SB2} TYP from 0.6 μ A to 0.7 μ A Changed I _{SB1} and I _{SB2} MAX from 1.5 μ A to 2.5 μ A Changed I _{CCDR} from 1 μ A to 2 μ A Fixed typos on TSOP II pinout: Pin 18-22: address lines Pin 23: NC Added Pb-free information
*B	427817	NXR	See ECN	Converted from Advanced Information to Final. Removed 35 ns Speed Bin Removed "L" version Changed ball E3 from DNU to NC. Removed the redundant footnote on DNU. Moved Product Portfolio from Page # 3 to Page #2. Changed I _{CC} (Max) value from 2 mA to 2.5 mA and I _{CC} (Typ) value from 1.5 mA to 2 mA at f=1 MHz Changed I _{CC} (Typ) value from 12 mA to 15 mA at f = f _{max} =1/t _{RC} Changed I _{SB1} and I _{SB2} Typ. values from 0.7 μ A to 1 μ A and Max. values fror 2.5 μ A to 7 μ A. Changed V _{CC} stabilization time in footnote #7 from 100 μ s to 200 μ s Changed V _{CC} stabilization time in footnote #7 from 100 μ s to 200 μ s Changed V _{CC} from 1.5V to 1V on Page# 4. Changed I _{CCDR} from 2 μ A to 3 μ A. Added I _{CCDR} from 2 μ A to 3 μ A. Added I _{CCDR} from 6 ns to 5 ns Changed t _{LZEE} from 6 ns to 5 ns Changed t _{LZEE} from 3 ns to 5 ns Changed t _{LZCE} , t _{HZEE} and t _{LZWE} from 15 ns to 18 ns Changed t _{SD} from 20 ns to 35 ns Changed t _{SD} from 20 ns to 25 ns Updated the Ordering Information table and replaced the Package Name column with Package Diagram.
*C	2604685	VKN / PYRS	11/12/08	Added footnote 8 related to I _{SB2} and I _{CCDR} Added footnote 13 related to AC timing parameters
*D	3143896	RAME	01/17/2011	Added Acronyms and Units of Measure table Added Ordering Code Definitions Added TOC Converted all tablenote to footnotes Updated Package Diagrams 51-85150 from *D to *F
*E	3283711	AJU	06/15/2011	Removed the Note "For best practice recommendations, refer to the Cypres application note "SRAM System Design Guidelines" on http://www.cypress.com." and its reference in Functional Description. Updated in new template.



Document History Page (continued)

	Document Title: CY62137EV30 MoBL [®] , 2-Mbit (128 K × 16) Static RAM Document Number: 38-05443				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change	
*F	3806123	TAVA	11/08/2012	Updated Data Retention Waveform (Updated Figure 4 (Changed " $V_{DR} \ge 1.5 V$ " to " $V_{DR} \ge 1.0 V$ ")). Updated Package Diagrams (spec 51-85150 (Changed revision from *F to *H), spec 51-85087 (Changed revision from *C to *E)).	
*G	4101224	VINI	08/21/2013	Updated Switching Characteristics: Updated Note 16. Updated in new template. Completing Sunset Review.	
*H	4574264	VINI	11/19/2014	Added related documenation hyperlink in page 1. Added note references 4 and 5 to Supply voltage to ground potential in Maximum Ratings. Added note 20 in Switching Characteristics. Provided note reference to Write Cycle in the Switching Characteristics table.	



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